Functional Safety Information

ISO1211 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for ISO1211 (8-D) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

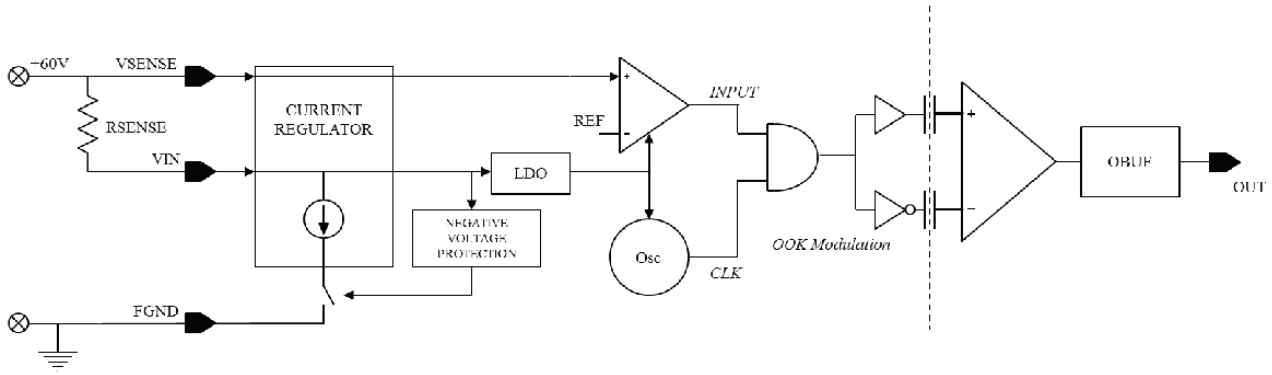

Figure 1-1. Functional Block Diagram

ISO1211 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 8-D (Narrow Body SOIC) Package

This section provides functional safety failure in time (FIT) rates for the 8-D package of ISO1211 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	17
Die FIT rate	9
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 450mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55 °C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ISO1211 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT state undetermined	38
OUT stuck to default state	34
OUT not in voltage or timing specification	17
OUT stuck high	4
OUT stuck low	4
OUT stuck to non-default state	3

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ISO1211 (8-D package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Note

When pin short-to-ground cases are discussed, only the same side ground shorts are considered.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

4.1 8-D (narrow-body SOIC) Package

Figure 4-1 shows the ISO1211 pin diagram for the 8-D package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ISO1211 data sheet.

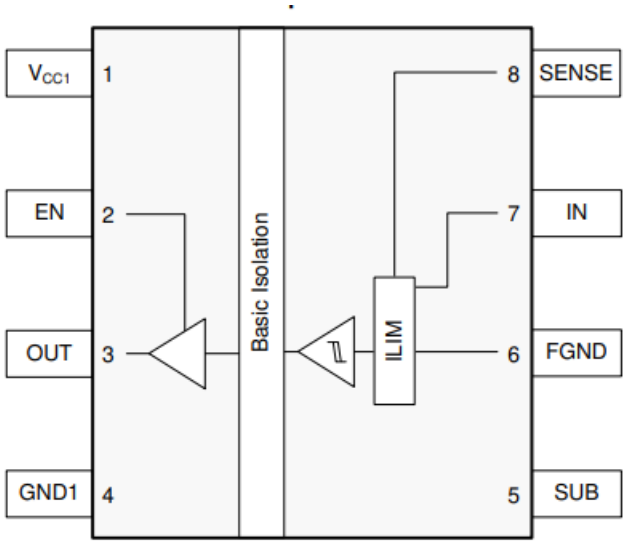

Figure 4-1. Pin Diagram (8-D) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V_{CC1}	1	No power to the device on the logic side. Verify that the *absolute maximum ratings* for all pins of the device are met; otherwise, device damage is plausible. OUT state undetermined.	A
EN	2	Disables the output buffer for OUT. OUT is in a high impedance state.	B
OUT	3	OUT stuck low. Device damage is plausible if IN and SENSE cause OUT to stay high for an extended period of time.	A
GND1	4	GND1 shorted to GND1. Normal operation.	D
SUB	5	Substrate shorted to FGND. A negative potential in the IN and SENSE pins can cause permanent damage.	A
FGND	6	FGND shorted to FGND. Normal Operation	D
IN	7	IN shorted to FGND and device damage is plausible	A
SENSE	8	SENSE shorted to FGND and device damage is plausible	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V_{CC1}	1	Device is not powered up. If EN is high, then current can flow through ESD to V_{CC1}, which can cause potential damage.	A
EN	2	Control on OUT output buffer is lost but field side data from IN and SENSE to OUT channels continues normally.	B
OUT	3	State of OUT undetermined. Field side data from IN and SENSE to OUT is lost.	B
GND1	4	No return ground pin.	B
SUB	5	Substrate opened as expected. Normal operation.	D
FGND	6	No return ground for field side.	B
IN	7	No device damage but there is loss of critical functionality.	B
SENSE	8	No device damage but there is loss of critical functionality.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effects	Failure Effect Class
V_{CC1}	1	EN	Externally, the V_{CC1} supply and EN driver output is shorted when V_{CC1} and EN is supplied and the logic high level and OUT is enabled and functions as expected. This function is dependent on the V_{CC1} and EN pin level results of the device. If V_{CC1} and EN is not supplied and low then OUT is not enabled and the output is off.	B
EN	2	OUT	Device damage is plausible.	A
OUT	3	GND1	OUT stuck low. Data communication from IN and SENSE to OUT is lost. Device damage is plausible if IN and SENSE cause OUT to stay high for an extended period of time.	A
GND1	4	OUT	OUT stuck low. Data communication from IN and SENSE to OUT is lost. Device damage is plausible if IN and SENSE cause OUT to stay high for an extended period of time.	A
SUB	5	FGND	Substrate shorted to FGND. Device damage is plausible.	A
FGND	6	IN	FGND shorted to IN and device damage is plausible.	A
IN	7	SENSE	IN shorted to SENSE and device damage is plausible.	A
SENSE	8	IN	IN shorted to SENSE and device damage is plausible.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V_{CC1}	1	No effect. Normal operation.	D
EN	2	Functionality to disable the output buffer OUT is lost. OUT behaves as expected.	B
OUT	3	OUT stuck high. Data communication from IN and SENSE to OUT is lost. Device damage is plausible if IN and SENSE cause OUT to be low.	A
GND1	4	This causes high current to flow in the device and device damage is plausible.	A
SUB	5	Substrate shorted to V_{CC1} and device damage is plausible.	A
FGND	6	Field side ground shorted to V_{CC1}. Causes high current to flow in the device and device damage is plausible.	A
IN	7	IN shorted to V_{CC1} and device damage is plausible.	A
SENSE	8	SENSE shorted to V_{CC1} and device damage is plausible.	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265