Functional Safety Information

TPS74801-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS74801-Q1 (VQFN and VSON packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

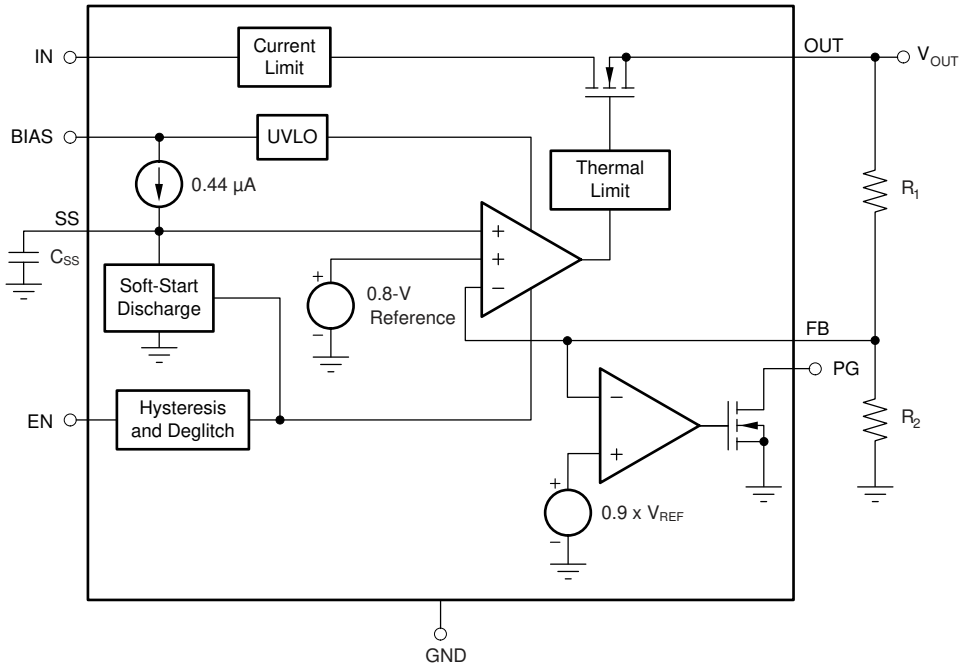

Figure 1-1. Functional Block Diagram

The TPS74801-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VQFN Package

This section provides functional safety failure in time (FIT) rates for the VQFN package of the TPS74801-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	21
Die FIT rate	5
Package FIT rate	16

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1000 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VSON Package

This section provides functional safety failure in time (FIT) rates for the VSON package of the TPS74801-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	5
Package FIT rate	4

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1000 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS74801-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT no output (GND)	35
OUT high (following input)	10
OUT not in specification voltage or timing	45
PG false trip, fails to trip	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS74801-Q1 (VQFN and VSON packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pullup resistor on $\overline{CS}$ to VDD
- RC filter on every analog input, AINx.

  Series resistors are sized to limit the input currents into the analog inputs to <10 mA in all circumstances (for example, in case the device is unpowered and the input signal is applied).
- The device is the only slave on the SPI bus.

4.1 VQFN Package

Figure 4-1 shows the TPS74801-Q1 pin diagram for the VQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS74801-Q1 data sheet.

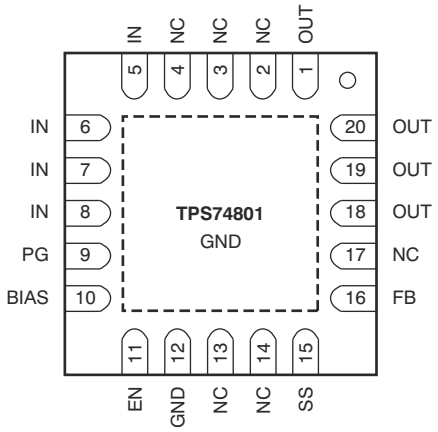

Figure 4-1. Pin Diagram (VQFN) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Device hits current limit state. If the power dissipation is significant, the device hits thermal shutdown state, and could continue to cycle between the two states. Continuously running the device above rated current degrades device reliability.	A
NC	2	No impact. Normal operation with improved thermal performance.	D
NC	3	No impact. Normal operation with improved thermal performance.	D
NC	4	No impact. Normal operation with improved thermal performance.	D
IN	5	Device does not turn on. No damage to device.	B
IN	6	Device does not turn on. No damage to device.	B
IN	7	Device does not turn on. No damage to device.	B
IN	8	Device does not turn on. No damage to device.	B
PG	9	No damage to device. PG functionality does not work. No impact on remaining functionality.	B
BIAS	10	No damage to device. Because band gap and control circuits do not power up, output voltage is not regulated and remains low at 0 V.	B
EN	11	Device does not turn on. No damage to device.	B
GND	12	No impact. Normal operation.	D
NC	13	No impact. Normal operation with improved thermal performance.	D
NC	14	No impact. Normal operation with improved thermal performance.	D
SS	15	Quiescent current increases. Device output remains at 0 V. No damage to device.	B
FB	16	Loss of functionality, device does not regulate. Output voltage tracks input voltage and equals V_{IN} minus the dropout. No damage to device.	B
NC	17	No impact. Normal operation with improved thermal performance.	D
OUT	18	Same as pin 1.	B/A
OUT	19	Same as pin 1.	B/A
OUT	20	Same as pin 1.	B/A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	No impact. Normal operation. Load still connected to remaining OUT pins (18, 19, and 20). There is a small risk that the bond wires connecting to the remaining OUT pins may fuse under heavily loaded conditions.	D/A
NC	2	No impact. Normal operation.	D
NC	3	No impact. Normal operation.	D
NC	4	No impact. Normal operation.	D
IN	5	Normal operation. Power supply still connected to remaining IN pins (6, 7, and 8), however there is a small risk that the bond wires connecting to the remaining IN pins may fuse under heavily loaded conditions.	D/A
IN	6	Same as pin 5.	D/A
IN	7	Same as pin 5.	D/A
IN	8	Same as pin 5.	D/A
PG	9	No damage to device. PG functionality does not work. No impact on remaining functionality.	B
BIAS	10	No damage to device. Because band gap and control circuits do not power up, output voltage is not regulated and remains low at 0 V.	B
EN	11	Because the voltage floats to an indeterminate state, the device can disable.	B
GND	12	With the reference pin floating, the voltages at the remaining pins are floating as well and the device is not functional. There is a risk of violating absolute maximum ratings.	B/A
NC	13	No impact. Normal operation.	D
NC	14	No impact. Normal operation.	D
SS	15	No impact. Normal operation. Start-up time defaults to 200 µs, approximately.	D
FB	16	Loss of functionality. Output pin voltage is not regulated and remains in an indeterminate state.	B
NC	17	No impact. Normal operation.	D
OUT	18	Same as pin 1.	D/A
OUT	19	Same as pin 1.	D/A
OUT	20	Same as pin 1.	D/A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	NC	No impact. Normal operation.	D
NC	2	NC	No impact. Normal operation.	D
NC	3	NC	No impact. Normal operation.	D
NC	4	IN	No impact. Normal operation.	D
IN	5	IN	No impact. Normal operation.	D
IN	6	IN	No impact. Normal operation.	D
IN	7	IN	No impact. Normal operation.	D
IN	8	PG	Very high risk of damage to PG pin and device, resulting from excess current drawn when PG open drain becomes low impedance.	A
PG	9	BIAS	Very high risk of damage to PG pin and device, resulting excess current drawn when PG open drain becomes low impedance.	A
BIAS	10	EN	Device remains ON regardless of enable signal value.	B
EN	11	GND	Device remains OFF regardless of enable signal value.	B
GND	12	NC	No impact. Normal operation.	D
NC	13	NC	No impact. Normal operation.	D
NC	14	SS	No impact. Normal operation.	D
SS	15	FB	The error amplifier output rails to either one of its supplies, and the LDO output is either at 0 V or tracks V_{IN} and equals V_{IN} – dropout.	B
FB	16	NC	No impact. Normal operation.	D
NC	17	OUT	No impact. Normal operation.	D
OUT	18	OUT	No impact. Normal operation.	D
OUT	19	OUT	No impact. Normal operation.	D
OUT	20	OUT	No impact. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Device is not functional, output voltage is not regulated and equals V_{IN}.	B
NC	2	No impact. Normal operation.	D
NC	3	No impact. Normal operation.	D
NC	4	No impact. Normal operation.	D
IN	5	No impact. Normal operation.	D
IN	6	No impact. Normal operation.	D
IN	7	No impact. Normal operation.	D
IN	8	No impact. Normal operation.	D
PG	9	Very high risk of damage to PG pin and device, resulting from excess current drawn when PG open drain becomes low impedance.	A
BIAS	10	Can be certain of normal operation only if sufficient dropout ($V_{IN} \geq V_{OUT} + V_{DO}$, where $V_{DO} = I_{OUT} \times (1.6 / 1.5)$) and V_{IN} ($V_{IN} \geq 2.7$ V) are provided. Device does not turn on for lower values of V_{IN}, and V_{OUT} remains at 0 V.	B/D
EN	11	Device remains ON regardless of enable signal value.	B
GND	12	Device does not turn on.	B
NC	13	No impact. Normal operation.	D
NC	14	No impact. Normal operation.	D
SS	15	LDO output pin voltage is not regulated and tracks V_{IN}. V_{OUT} equals V_{IN} – dropout.	B
FB	16	LDO output pin voltage is not regulated and equals V_{IN} (under no-load conditions).	B
NC	17	No impact. Normal operation.	D
OUT	18	Same as pin 1.	A
OUT	19	Same as pin 1.	A
OUT	20	Same as pin 1.	A

4.2 VSON Package

Figure 4-2 shows the TPS74801-Q1 pin diagram for the VSON package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS74801-Q1 data sheet.

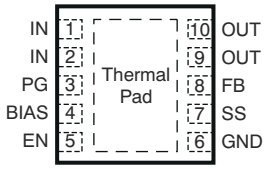

Figure 4-2. Pin Diagram (VSON Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	Device does not turn on. No damage to device.	B
IN	2	Device does not turn on. No damage to device.	B
PG	3	No damage to device. PG functionality does not work. No impact on remaining functionality.	B
BIAS	4	No damage to device. Because band gap and control circuits do not power up, output voltage is not regulated and remains low at 0 V.	B
EN	5	Device does not turn on. No damage to device.	B
GND	6	No Impact. Normal operation.	D
SS	7	Quiescent current increases. Device output remains at 0 V. No damage to device.	B
FB	8	Loss of functionality, device does not regulate. Output voltage tracks input voltage and equals V_{IN} minus the dropout. No damage to device.	B
OUT	9	Device hits current limit state. If the power dissipation is significant, the device hits thermal shutdown state, and may continue to cycle between the two states. Continuously running the device above rated current degrades device reliability.	A
OUT	10	Same as pin 9.	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	Normal operation. Power supply still connected to remaining IN pin (2), however there is a small risk that the bond wire connecting to the remaining IN pin may fuse under heavily loaded conditions.	D/A
IN	2	Same as pin 1.	D/A
PG	3	No damage to device. PG functionality does not work. No impact on remaining functionality.	B
BIAS	4	No damage to device. Because band gap and control circuits do not power up, output voltage is not regulated and remains low at 0 V.	B
EN	5	Because the voltage floats to an indeterminate value, the device can disable.	B
GND	6	With the reference pin floating, the voltages at the remaining pins are floating as well and the device is not functional. There is a risk of violating the absolute maximum ratings.	B/A
SS	7	No impact. Normal operation. Start-up time defaults to 200 µs, approximately.	D
FB	8	Loss of functionality. Output pin voltage is not regulated and remains in an indeterminate state.	B
OUT	9	No impact. Normal operation. Load still connected to remaining OUT pin (10). There is a small risk that the bond wire connecting to the remaining OUT pin may fuse under heavily loaded conditions.	D/A
OUT	10	Same as pin 9.	D/A

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	IN	No impact. Normal operation.	D
IN	2	PG	Very high risk of damage to PG pin and device, resulting from excess current drawn when PG open drain becomes low impedance.	A
PG	3	BIAS	Very high risk of damage to PG pin and device, resulting from excess current drawn when PG open drain becomes low impedance.	A
BIAS	4	EN	Device remains ON regardless of enable signal value.	B
EN	5	GND	Device remains OFF regardless of enable signal value.	B
GND	6	SS	Quiescent current increases. Device output remains at 0 V. No damage to device.	B
SS	7	FB	The error amplifier output rails to either one of its supplies, and the LDO output is either at 0 V or tracks V_{IN} and equals V_{IN} – dropout.	B
FB	8	OUT	V_{OUT} is set to V_{FB} = 0.8 V.	B
OUT	9	OUT	No impact. Normal operation.	D
OUT	10	IN	Output voltage is not regulated and equals V_{IN}.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No impact. Normal operation.	D
IN	2	No impact. Normal operation.	D
PG	3	Very high risk of damage to PG pin and device, resulting from excess current drawn when PG open drain becomes low impedance.	A
BIAS	4	Can be certain of normal operation only if sufficient dropout ($V_{IN} \geq V_{OUT} + V_{DO}$, where $V_{DO} = I_{OUT} \times (1.6 / 1.5)$) and V_{IN} ($V_{IN} \geq 2.7$ V) are provided. Device does not turn on for lower values of V_{IN}, and V_{OUT} remains at 0 V.	B
EN	5	Device remains ON regardless of enable signal value.	B
GND	6	Device does not turn on.	B
SS	7	LDO output pin voltage is not regulated and tracks V_{IN}. V_{OUT} equals V_{IN} – dropout.	B
FB	8	LDO output pin voltage is not regulated and equals V_{IN} (under no-load conditions).	B
OUT	9	Device is not functional, output voltage is not regulated and equals V_{IN}.	B
OUT	10	Same as pin 9.	B

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