Functional Safety Information

TLIN2024A-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TLIN2024A-Q1 which is a quad-channel interconnect network (LIN) transceiver in 24-pin RGY (VQFN) package to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

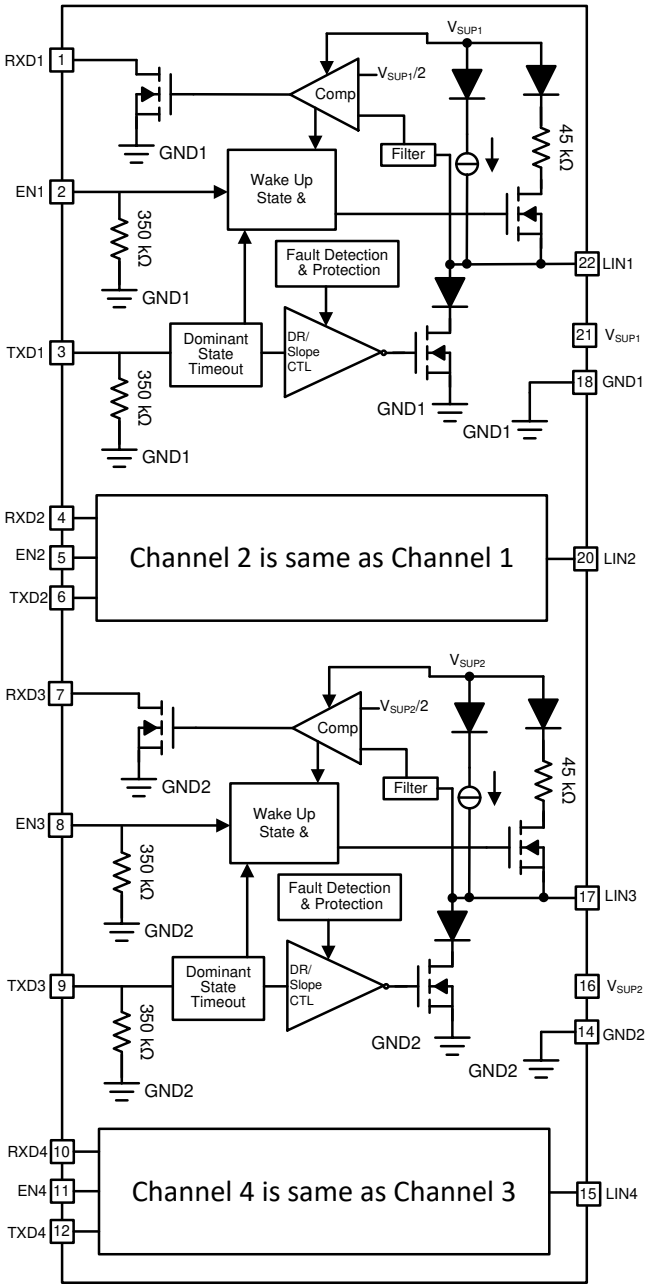

Figure 1-1. Functional Block Diagram

TLIN2024A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TLIN2024A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) (RGY)
Total Component FIT Rate	14
Die FIT Rate	4
Package FIT Rate	10

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 422 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLIN2024A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Transmitter fail	66%
Receiver fail	3%
Logic I/O or state control fail	13%
Global power management fail	18%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLIN2024A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the device pin diagram. For a detailed description of the device pins, please refer to the *Pin Configuration and Functions* section in the TLIN2024A-Q1 data sheet.

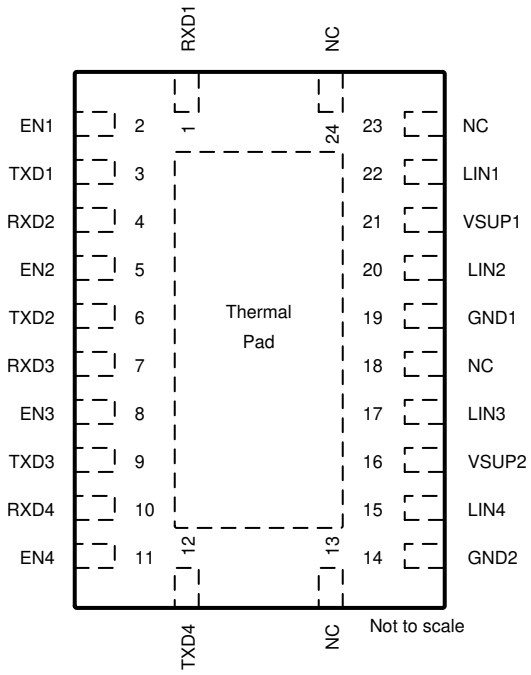

Figure 4-1. RGY Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All conditions within the recommended operating conditions specified in datasheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RXD1	1	RXD1 biased dominant, no communication from LIN1 bus to MCU possible.	B
EN1	2	LIN1 channel may only operate in standby mode after power on. If short on EN1 occurs in normal mode, LIN1 channel would be forced to enter sleep mode and could disable LIN communication	B
TXD1	3	TXD1 biased dominant, no communication from MCU to LIN1 bus possible.	B
RXD2	4	RXD2 biased dominant, no communication from LIN2 bus to MCU possible.	B
EN2	5	LIN2 channel may only operate in standby mode after power on. If short on EN2 occurs in normal mode, LIN2 channel would be forced to enter sleep mode and could disable LIN communication.	B
TXD2	6	TXD2 biased dominant, no communication from MCU to LIN2 bus possible.	B
RXD3	7	RXD3 biased dominant, no communication from LIN3 bus to MCU possible.	B
EN3	8	LIN3 channel may only operate in standby mode after power on. If short on EN3 occurs in normal mode, LIN3 channel would be forced to enter sleep mode and could disable LIN communication.	B
TXD3	9	TXD3 biased dominant, no communication from MCU to LIN3 bus possible.	B
RXD4	10	RXD4 biased dominant, no communication from LIN4 bus to MCU possible.	B
EN4	11	LIN4 channel may only operate in standby mode after power on. If short on EN4 occurs in normal mode, LIN4 channel would be forced to enter sleep mode and could disable LIN communication.	B
TXD4	12	TXD4 biased dominant, no communication from MCU to LIN4 bus possible.	B
NC	13	No impact to performance.	D
GND2	14	None	D
LIN4	15	LIN4 biased dominant, no LIN communication possible.	B
VSUP2	16	Channels 3 and 4 unpowered and will not function.	B
LIN3	17	LIN3 biased dominant, no LIN communication possible.	B
NC	18	No impact to performance.	D
GND1	19	None	D
LIN2	20	LIN2 biased dominant, no LIN communication possible.	B
VSUP1	21	Channels 1 and 2 unpowered and will not function.	B
LIN1	22	LIN1 biased dominant, no LIN communication possible.	B
NC	23	No impact to performance.	D
NC	24	No impact to performance.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RXD1	1	No communication from LIN1 bus to MCU possible.	B
EN1	2	Biased low due to internal pull-down so LIN1 in standby mode.	B
TXD1	3	No communication from MCU to LIN1 bus possible.	B
RXD2	4	No communication from LIN2 bus to MCU possible.	B
EN2	5	Biased low due to internal pull-down so LIN2 in standby mode.	B
TXD2	6	No communication from MCU to LIN2 bus possible.	B
RXD3	7	No communication from LIN3 bus to MCU possible.	B
EN3	8	Biased low due to internal pull-down so LIN3 in standby mode.	B
TXD3	9	No communication from MCU to LIN3 bus possible.	B
RXD4	10	No communication from LIN4 bus to MCU possible.	B
EN4	11	Biased low due to internal pull-down so LIN4 in standby mode.	B
TXD4	12	No communication from MCU to LIN4 bus possible.	B
NC	13	No impact to performance.	D
GND2	14	Channels 3 and 4 are unpowered and will not function.	B
LIN4	15	No LIN4 communication possible.	B
VSUP2	16	Channels 3 and 4 are unpowered and will not function.	B
LIN3	17	No LIN3 communication possible.	B
NC	18	No impact to performance.	D
GND1	19	Chanels 1 and 2 are unpowered and will not function.	B
LIN2	20	No LIN2 communication possible.	B
VSUP1	21	Channels 1 and 2 are unpowered and will not function.	B
LIN1	22	No LIN1 communication possible.	B
NC	23	No impact to performance.	D
NC	24	No impact to performance.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
RXD1	1	EN1	LIN1 will go into sleep mode when a dominant bit is received on the LIN1 bus, disabling communication.	B
EN1	2	TXD1	With TXD toggling, LIN1 channel will transition between normal and sleep mode, corrupting communication.	B
TXD1	3	RXD2	Communication on TXD1 will corrupt the received data from LIN2 to RXD2.	B
RXD2	4	EN2	With data toggling on RXD2 via LIN2 bus, EN2 toggles and causes LIN2 channel to transition between normal and sleep modes.	B
EN2	5	TXD2	With TXD toggling, LIN2 channel will transition between normal and sleep mode, corrupting communication.	B
TXD2	6	RXD3	Communication on TXD2 will corrupt the received data from LIN3 to RXD3.	B
RXD3	7	EN3	With data toggling on RXD3 via LIN3 bus, EN3 toggles and causes LIN3 channel to transition between normal and sleep modes.	B
EN3	8	TXD3	With TXD toggling, LIN3 channel will transition between normal and sleep mode, corrupting communication.	B
TXD3	9	RXD4	Communication on TXD3 will corrupt the received data from LIN4 to RXD4.	B
RXD4	10	EN4	With data toggling on RXD4 via LIN4 bus, EN4 toggles and causes LIN4 channel to transition between normal and sleep modes.	B
EN4	11	TXD4	With TXD toggling, LIN4 channel will transition between normal and sleep mode, corrupting communication.	B
TXD4	12	NC	No impact to performance.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
NC	13	GND2	No impact to performance.	D
GND2	14	LIN4	LIN4 biased dominant, no LIN4 communication possible.	B
LIN4	15	$V_{SUP}2$	LIN4 biased recessive, no LIN4 communication possible.	B
VSUP2	16	LIN3	LIN3 biased dominant, no LIN3 communication possible.	B
LIN3	17	NC	No impact to performance.	D
NC	18	GND1	No impact to performance.	D
GND1	19	LIN2	LIN2 biased dominant, no LIN2 communication possible.	B
LIN2	20	$V_{SUP}1$	LIN2 biased recessive, no LIN2 communication possible.	B
VSUP1	21	LIN1	LIN1 biased dominant, no LIN1 communication possible.	B
LIN1	22	NC	No impact to performance.	D
NC	23	NC	No impact to performance.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{SUP} supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RXD1	1	Absolute maximum voltage violation, transceiver may be damaged	A
EN1	2	Absolute maximum voltage violation, transceiver may be damaged	A
TXD1	3	Absolute maximum voltage violation, transceiver may be damaged	A
RXD2	4	Absolute maximum voltage violation, transceiver may be damaged	A
EN2	5	Absolute maximum voltage violation, transceiver may be damaged	A
TXD2	6	Absolute maximum voltage violation, transceiver may be damaged	A
RXD3	7	Absolute maximum voltage violation, transceiver may be damaged	A
EN3	8	Absolute maximum voltage violation, transceiver may be damaged	A
TXD3	9	Absolute maximum voltage violation, transceiver may be damaged	A
RXD4	10	Absolute maximum voltage violation, transceiver may be damaged	A
EN4	11	Absolute maximum voltage violation, transceiver may be damaged	A
TXD4	12	Absolute maximum voltage violation, transceiver may be damaged	A
NC	13	No impact to performance	D
GND2	14	Device is unpowered and will not funtion	B
LIN4	15	LIN4 biased recessive, no LIN4 communication possible	B
VSUP2	16	None	D
LIN3	17	LIN3 biased recessive, no LIN3 communication possible	B
NC	18	No impact to performance	D
GND1	19	Device is unpowered and will not funtion	B
LIN2	20	LIN2 biased recessive, no LIN2 communication possible	B
VSUP1	21	None	D
LIN1	22	LIN1 biased recessive, no LIN1 communication possible	B
NC	23	No impact to performance	D
NC	24	No impact to performance	D

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265