*Functional Safety Information*

# *TLV759P*
# *Functional Safety FIT Rate, FMD and Pin FMA*

## Table of Contents



## Trademarks

# 1 Overview

This document contains information for TLV759P (DRV package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

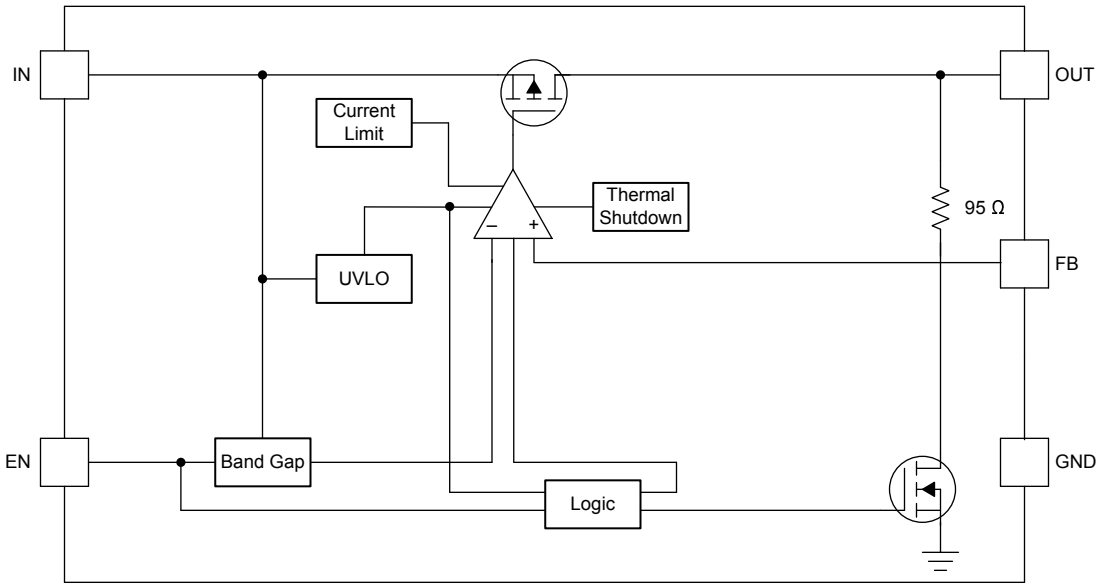


**Figure 1-1. TLV759P Functional Block Diagram**

TLV759P was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TLV759P based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Package | DRV |
| Total Component FIT Rate | 5 |
| Die FIT Rate | 3 |
| Package FIT Rate | 2 |

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 250 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog / mixed | 25 FIT | 55°C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLV759P in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| VOUT High (Following VIN) | 20.83% |
| VOUT Not in Specification or Removed from Load | 8.33% |
| VOUT Low (No Output) | 33.33% |
| No Failures | 29.17% |
| Output always enabled | 4.17% |
| Possible FB pin damage | 4.17% |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLV759P. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-3)
- Pin open-circuited (see Table 4-4)
- Pin short-circuited to an adjacent pin (seeTable 4-5)
- Pin short-circuited to supply (see Table 4-6)

Table 4-3 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

Figure 4-1 shows the TLV759P pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLV759P data sheet.

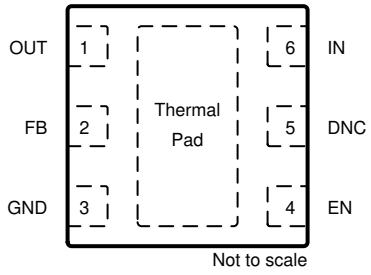


**Figure 4-1. Pin Diagram for the TLV759P DRV Package [6 Pin Adjustable WSON]**

**Table 4-2. Pin Functions**

| Pin | | I/O | DESCRIPTION |
|---|---|---|---|
| Name | No. | | |
| OUT | 1 | OUTPUT | Regulated Output |
| FB | 2 | - | Input to the Control Loop Error Amplifier |
| GND | 3 | - | Ground |
| EN | 4 | INPUT | Drive Greater Than VEN(HIGH) to Turn On the Regulator. Drive Less Than VEN(LOW) to Put Regulator in Shutdown Mode |
| DNC | 5 | - | Do Not Connect |
| IN | 6 | INPUT | Inpur Supply |
| Thermal Pad | Pad | - | Connect the thermal pad Ground for Improved Thermal Performance |

**Table 4-3. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin | | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| Name | No. | | |
| OUT | 1 | Output voltage will be near/at ground - Device will enter current limit. It may cycle in and out of thermal shutdown depending on power dissipation | B |
| FB | 2 | Device will stop regulating. VOUT becomes equal to VIN minus dropout because the pass FET is driven on as hard as possible | B |
| GND | 3 | - | D |
| EN | 4 | Device will turn off | B |
| DNC | 5 | - | D |
| IN | 6 | No Output Voltage. Input Supply can be 0V | B |

**Table 4-4. Pin FMA for Device Pins Open-Circuited**

| Pin | | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| Name | No. | | |
| OUT | 1 | Output voltage is disconnected from load | B |
| FB | 2 | Error amplifier input is left floating, output voltage will not equal to set voltage and will drift up to VIN minus a dropout voltage | B |
| GND | 3 | Device may disable | B |
| EN | 4 | Device may disable | B |
| DNC | 5 | - | D |
| IN | 6 | No output voltage | B |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin | | Shorted To | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|---|
| Name | No. | | | | |
| OUT | 1 | FB | 2 | VOUT will be set to VFB = 0.55 Vdc | B |
| FB | 2 | GND | 3 | Device will stop regulating. VOUT becomes equal to VIN minus dropout because the pass FET is driven on as hard as possible | B |
| GND | 3 | EN | 4 | Output is forced OFF, VOUT is 0.0V | B |
| EN | 4 | DNC | 5 | - | D |
| DNC | 5 | IN | 6 | - | D |
| IN | 6 | OUT | 1 | Device will stop regulating. VOUT becomes equal to VIN | B |

**Table 4-6. Pin FMA for Device Pins Short-Circuited to supply**

| Pin | | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| Name | No. | | |
| OUT | 1 | Device will stop regulating. VOUT becomes equal to VIN | B |
| FB | 2 | FB pin will be damaged if VIN is higher than 2V | A |
| GND | 3 | Input supply will be driven to GND. No Output Voltage | B |
| EN | 4 | Output is enabled regardless of external control logic on the enable pin | B |
| DNC | 5 | - | D |
| IN | 6 | No Effect | D |

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