Application Report

Optimizing Design of Smart Thermostats with Logic and Translation Use Cases

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ABSTRACT

Smart thermostats integrate numerous subsystems in a very small space. Though the thermostats differ in style and features, they share similar digital interfacing challenges, such as driving solid-state relays to route the incoming 24 V AC power to the appropriate HVAC systems. All of the use cases shown in the *Block Diagram* and *Logic and Translation Use Cases* sections of this document are commonly seen in smart thermostat designs.

Logic gates, voltage translators, and other logic devices are utilized for many purposes throughout modern electronic systems. This document provides example solutions for common design challenges that can be solved using logic and translation. Not all of the solutions here appear in every system, however all solutions shown are commonly used and effective.

There are dozens of logic families available from Texas Instruments, and it can be difficult to select the right one for the application. Smart thermostats vary in features, but the key design parameters remain the same making it easier to identify an appropriate family for this application. Refer to *Section 4* in this document for help finding the right logic family for the use case.

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Trademarks

1 Block Diagram

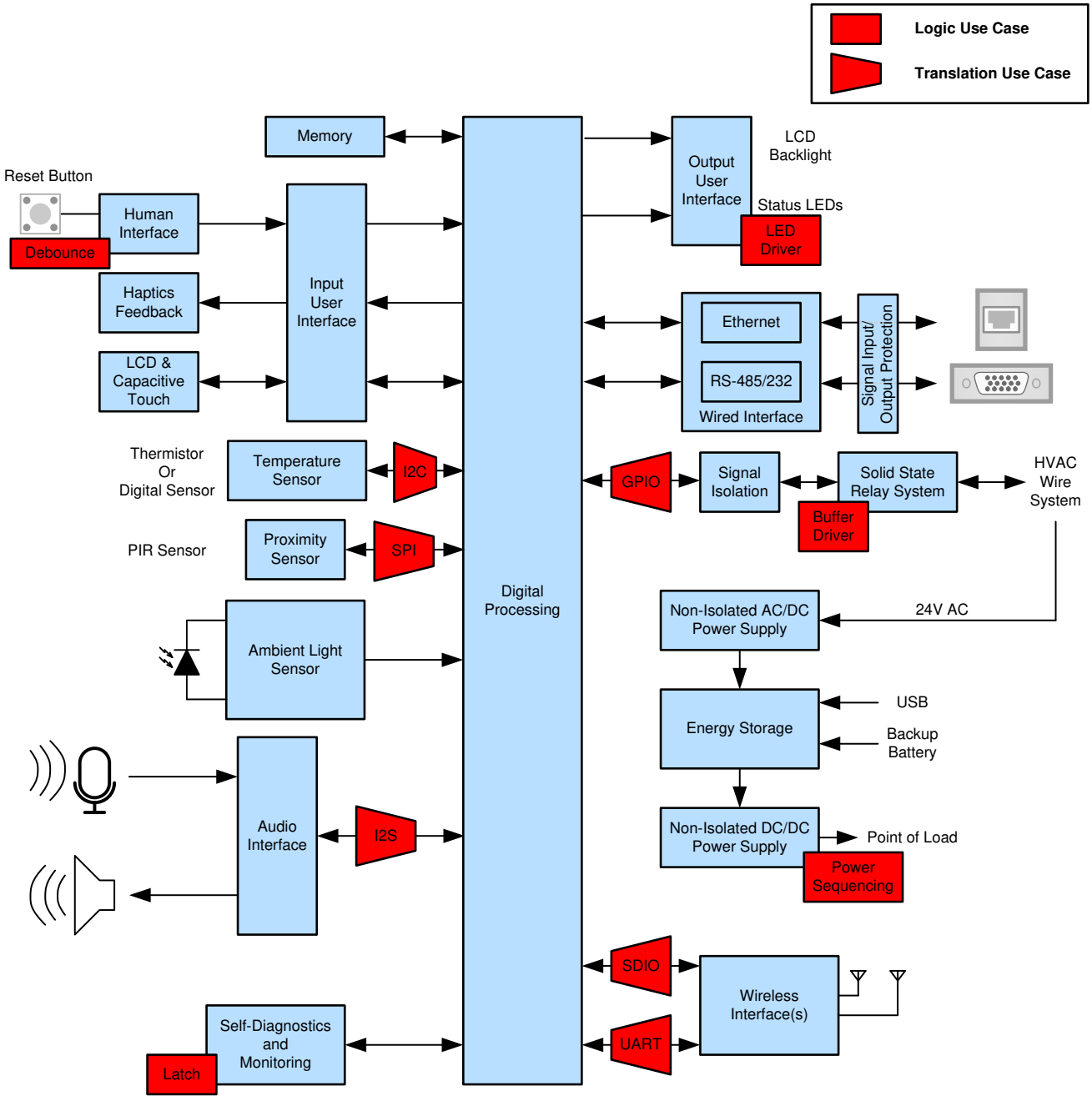

Figure 1-1. Simplified Block Diagram for Smart Thermostats

For the purpose of this report, a simplified smart thermostat system block diagram is used to illustrate the logic and translation use cases. See *Smart Thermostats* for a more complete view of the interactive online End Equipment Reference Diagram.

2 Optimizing Communication with Wireless Interfaces

It is extremely common for smart thermostats to utilize wireless interfaces such as Wi-Fi™, ZigBee™, or Bluetooth™ to connect to a local network. In many designs, the simplest method to achieve this is to utilize pre-built and pre-approved modules. These modules often have limited voltage operation ranges, and to support their usage, voltage-level shifters are typically required between the extremely low power processor, often operating as low as 1.2 V, and the wireless module, commonly operating at 3.3 V.

The most common communication protocols used between the processor and wireless interface are SDIO and UART. Each is addressed specifically in the following sections.

2.1 SDIO Voltage Translation

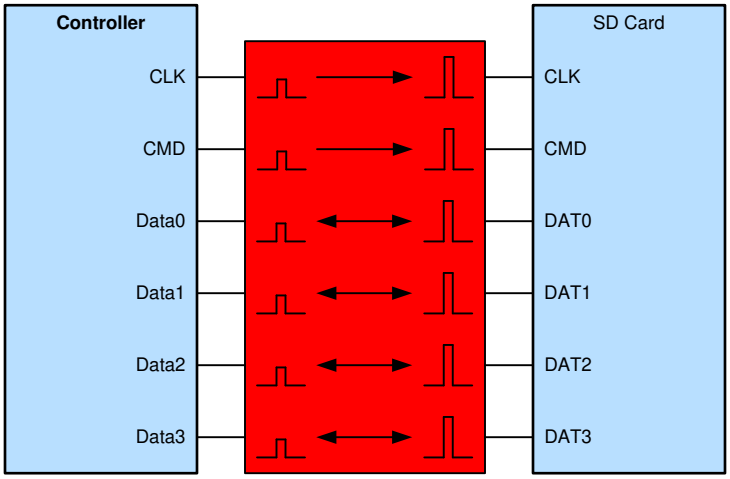

Figure 2-1. Using Voltage Translation with an SD Card Communication Bus

- Enable communication when devices have mismatched logic voltage levels.
- Improve data rates over discrete translation solutions.
- Protect controller while SD Card is not connected.
- See *online parametric search tool* to find the right voltage level translator.

2.2 SPI Voltage Translation

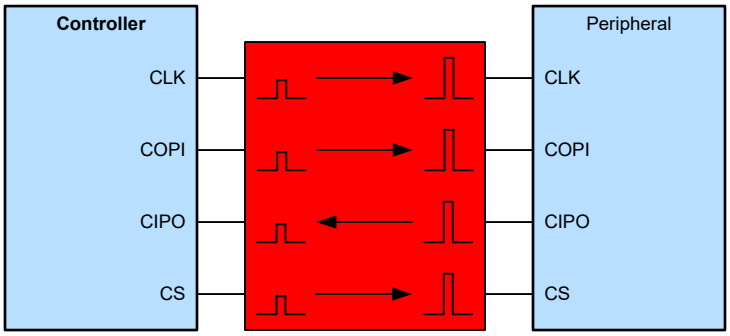

Figure 2-2. Using Voltage Translation with a SPI-Communication Bus

- Enable communication when devices have mismatched logic voltage levels.
- Prevent damage to devices that cannot support higher voltage inputs.
- Improve data rates over discrete translation solutions.
- Provide protection from disconnected peripherals.
- See *online parametric search tool* to find the right voltage level translator.

3 Logic and Translation Use Cases

3.1 Logic Use Cases

3.1.1 Drive Indicator LEDs

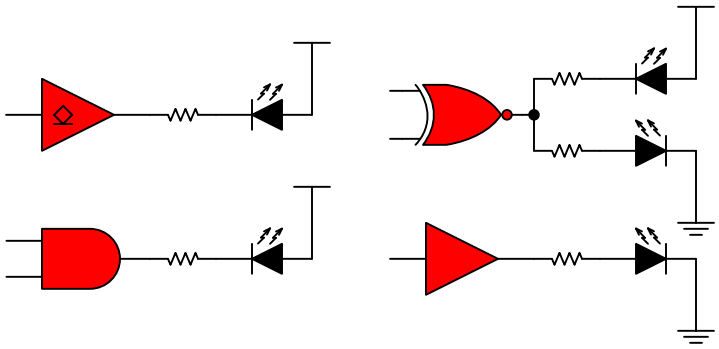

Figure 3-1. Using Logic as Indicator LED Driver Application Examples

- Add system indicators without controller interaction required.
- Most logic gates can drive low-current indicator LEDs (1 mA to 25 mA).
- Logic functions add configurability.
- Disable indicator LEDs as desired.

3.1.2 Power Sequencing: Combine Power-Good Signals

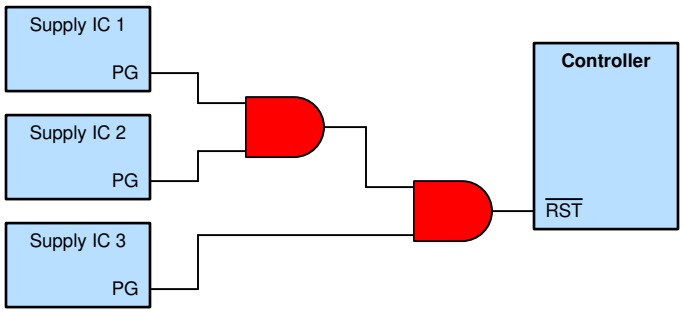

Figure 3-2. Using Logic to Combine Multiple Power-Good Signals

- Combine power good signals to drive an active low reset.
- Add power indicator LEDs without software or system controller interaction.
- See *Combining Power Good Signals.* for more about this use case in the Logic Minute video.
- See *online parametric search tool.* to find the right AND gate.

3.1.3 Debounce Switches and Buttons

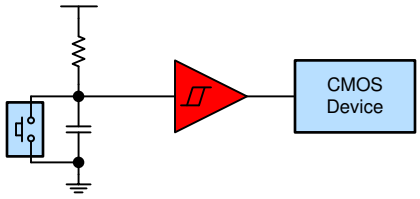

Figure 3-3. Using Logic to Prevent Multiple Triggers of a CMOS Input Due to Switch Bounce

- Prevents multiple triggers of CMOS inputs due to switch bounce.
- Works when the system controller is asleep.
- Works without a system controller.
- Reduces controller code complexity; no software debounce is required.
- See *Debounce a Switch* Logic Minute video for more information about this use case.
- See *online parametric search tool* to find the right Schmitt-trigger buffer.

3.1.4 Latching Alarm Circuit with Reset

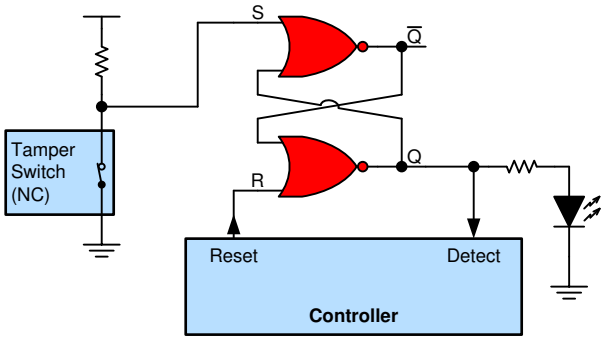

Figure 3-4. Using Logic to Monitor a Normally Closed (NC) Tamper Switch

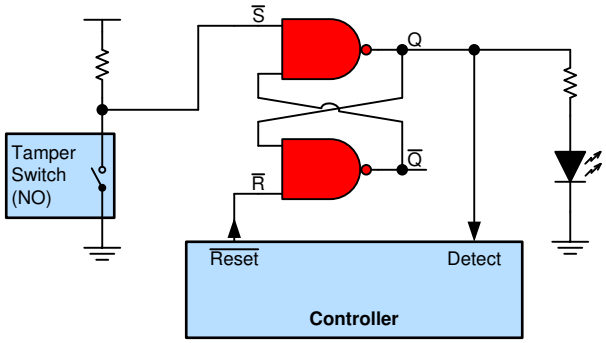

Figure 3-5. Using Logic to Monitor a Normally Open (NO) Tamper Switch

- Flags any tampering.
- Extremely low power.
- Works while the controller sleeps.
- Can be used without a controller.
- See *Using an S-R Latch in Alarm Circuitry* Logic Minute video for more information about this use case.
- See *online parametric search tool* to find the right NOR or NAND gate.

3.1.5 Buffer and Driver: Condition Digital Signals

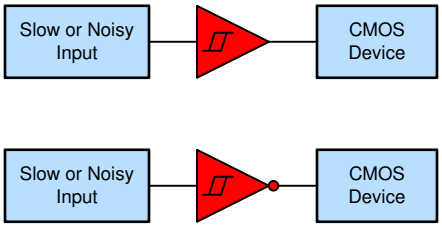

Figure 3-6. Using Schmitt-Trigger Drivers to Remove Noise or Slow Edges from Digital Signals

- Removes moderate noise from digital signals.
- Prevents multiple switching events for CMOS inputs.
- Speeds up slow input edges to meet input transition rate requirements.
- See *Eliminate Slow or Noisy Input Signals* Logic Minute video for more information about this use case.
- See *online parametric search tool.* to find the right Schmitt-trigger buffer or inverter.

3.2 Voltage Translation Use Cases

3.2.1 SPI Communication

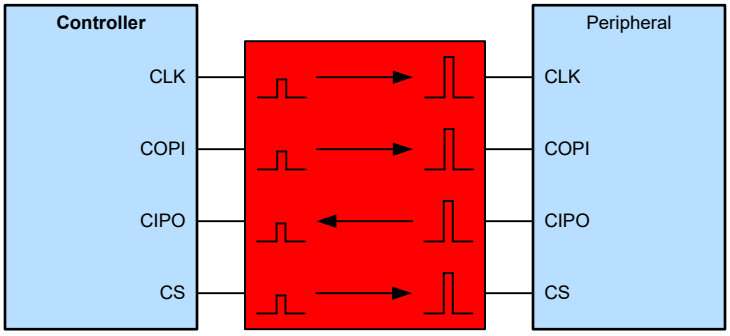

Figure 3-7. Using Voltage Translation with a SPI-Communication Bus

- Enable communication when devices have mismatched logic voltage levels.
- Prevent damage to devices that cannot support higher voltage inputs.
- Improve data rates over discrete translation solutions.
- Provide protection from disconnected peripherals.
- See *online parametric search tool* to find the right voltage level translator.

3.2.2 GPIO Communication

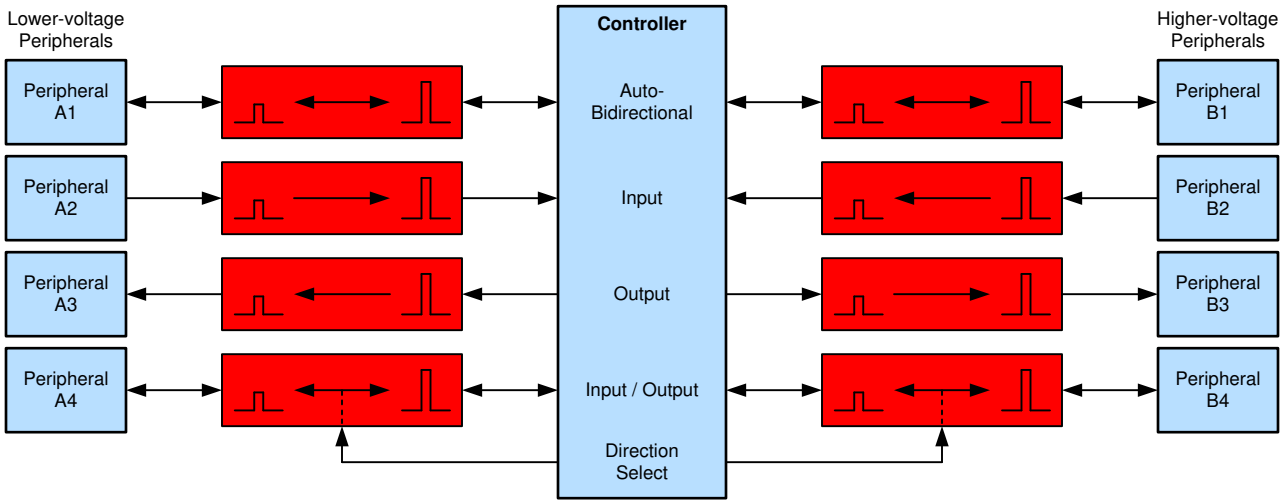

Figure 3-8. Using Voltage Translation with GPIO Communications

- Enable communication when devices have mismatched logic voltage levels.
- Prevent damage to devices that cannot support higher voltage inputs.
- Improve data rates over discrete translation solutions.
- Provides protection from disconnected peripherals.
- See *online parametric search tool* to find the right voltage level translator.

3.2.3 I²C Communication

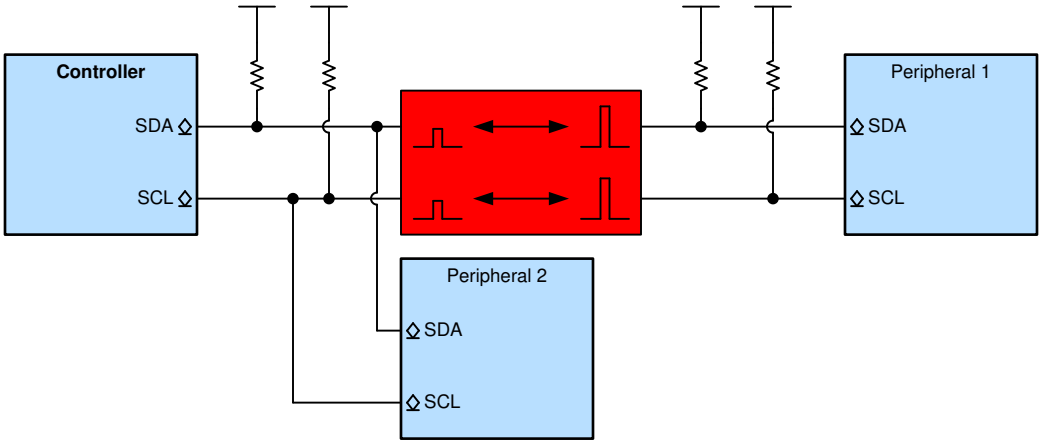

Figure 3-9. Using Voltage Translation with an I² Communication Bus

- Enable communication when devices have mismatched logic voltage levels.
- Prevent damage to devices that cannot support higher voltage inputs.
- Improve data rates over discrete translation solutions.
- See *online parametric search tool* to find the right voltage level translator.

3.2.4 I2S Communication

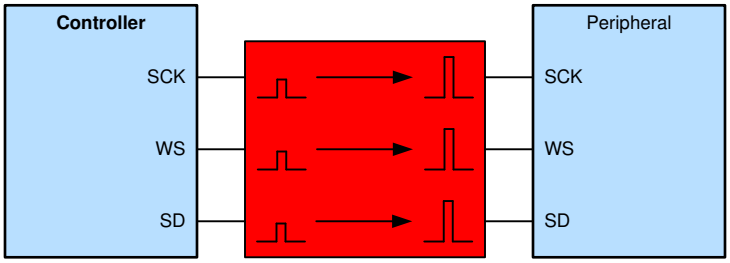

Figure 3-10. Using Voltage Translation with an I2S Communication Bus

- Enable communication when devices have mismatched logic voltage levels.
- Prevent damage to devices that cannot support higher voltage inputs.
- Improve data rates over discrete translation solutions.
- Protect controller while peripheral is not connected.
- See *online parametric search tool* to find the right voltage level translator.

4 Recommended Logic and Translation Families for Smart Thermostats

4.1 AUP: Advanced Ultra-Low-Power CMOS Logic and Translation

Key Features: SN74**AUPxG**xxxx

- Low static- and dynamic-power consumption.
- Wide V_{CC} operating range: 0.8 V to 3.6 V.
- Input hysteresis allows for slow input transition rate.
- Best in class for speed-power optimization.
- I_{off} spec for partial power down support.
- Packaging Options:
  - DSBGA
  - SC70
  - SM8
  - SON
  - SOT-23
  - SOT
  - UQFN
  - US8
  - X2SON

Key Features: SN74**AUPxT**xxxx

- Low static- and dynamic-power consumption.
- 1.65 V to 3.6 V translation range.
- Best in class for speed-power optimization.
- I_{off} spec for partial power down support.

See *online parametric search tool* to find the right AUP family logic and voltage level translation devices.

4.2 AXC: Advanced eXtremely Low-Voltage CMOS Translation

Key Features

- Up and Down Translation Across 0.65 V to 3.6 V.
- Designed with glitch suppression circuitry to improve power sequencing performance.
- Maximum Quiescent Current (I_{CCA} + I_{CCB}) as low as 6 µA (85°C Maximum) and 14 µA (125°C Maximum).
- Up to 500-Mbps support when translating from 1.8 V to 3.3 V.
- V_{CC} Isolation Feature – If either V_{CC} input is below 100 mV, all I/Os outputs are disabled and become high impedance.
- I_{off} supports partial-power-down mode operation.
- Operating Temperature: –40°C to +125°C.
- Packaging Options:
  - SC70
  - SM8
  - SON
  - SOT-23
  - SOT
  - UQFN
  - US8
  - X2SON

See *online parametric search tool* to find the right AXC family voltage level translation devices.

4.3 LVC: Low-Voltage CMOS Logic and Translation

Key Features: SN74**LVC**xxxx

- Huge portfolio of logic functions.
- LVC: 4+ channels per package.
- Over-voltage tolerant inputs allow unidirectional down-translation with any function.
- High-drive outputs (up to 32 mA).
- Up to 250-Mbps operation.
- I_{off} supports partial-power-down mode operation.
- Packaging Options:
  - SOIC
  - TSSOP
  - VQFN
  - SOP
  - SSOP

Key Features: SN74**LVCxG**xxxx

- Put one, two, or three channels of any logic function right where they are needed.
- Configurable gates available ('57, '58, '97, '98, '99 functions).
- Over-voltage tolerant inputs allow unidirectional down-translation with any gate or buffer.
- High-drive outputs (up to 32 mA).
- Up to 250-Mbps operation.
- I_{off} supports partial-power-down mode operation.
- Packaging Options:
  - SOT-23
  - SC70
  - X2SON
  - SOT-5X3
  - SON
  - DSBGA

Key Features: SN74**LVCxT**xxxx

- LVCxT: Up and Down Translation Across 1.65 V to 5.5 V.
- 1, 2, 8, or 16 channels per device.
- High-drive outputs (up to 32 mA).
- Up to 250-Mbps operation.
- I_{off} supports partial-power-down mode operation.

Find the right LVC family logic and voltage level translation devices through the *online parametric search tool*.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2019) to Revision A (April 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	2
• Updated the *Using Voltage Translation with a SPI-communication Bus* figure for inclusive SPI terms	6

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