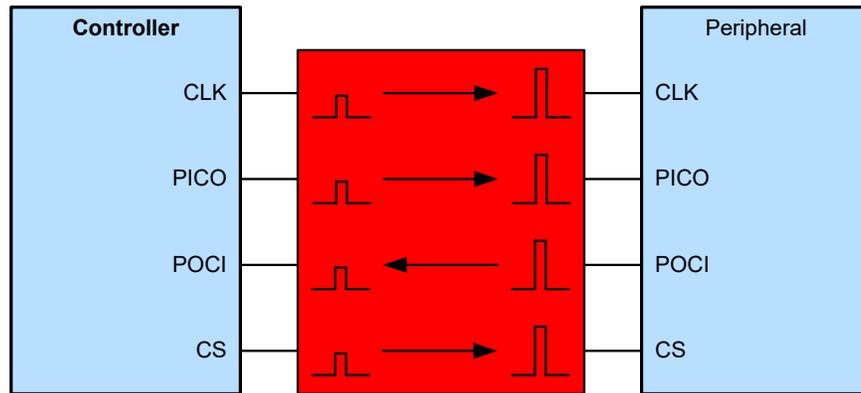


Translate Voltages for SPI



Example SPI Voltage Translation Block Diagram

See more about this use case in the *Logic Minute* video [Voltage Translation for SPI](#).

Design Considerations

- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- [\[FAQ\] What are the power sequencing requirements for the translation device?](#)
- [\[FAQ\] What should be done with unused I/O pins of the level translator devices?](#)
- Need additional assistance? Ask our engineers a question on the [TI E2E™ Logic Support Forum](#)

Recommended Parts

Part Number	AEC-Q100	Voltage Translation Range	Features
TXU0304		1.1 V–5.5 V	Schmitt-trigger inputs Integrated pulldown resistors V_{CC} Isolation and V_{CC} Disconnect
TXU0304-Q1	✓		
SN74AXC4T774		0.65 V–3.6 V	Direction controlled Glitch-free power supply sequencing V_{CC} Isolation
SN74AXC4T774-Q1	✓		

For more devices, browse through the [online parametric tool](#) where you can sort by desired voltage, channel numbers, and other features.

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