SN3257-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for SN3257-Q1 (TSSOP-16 and SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

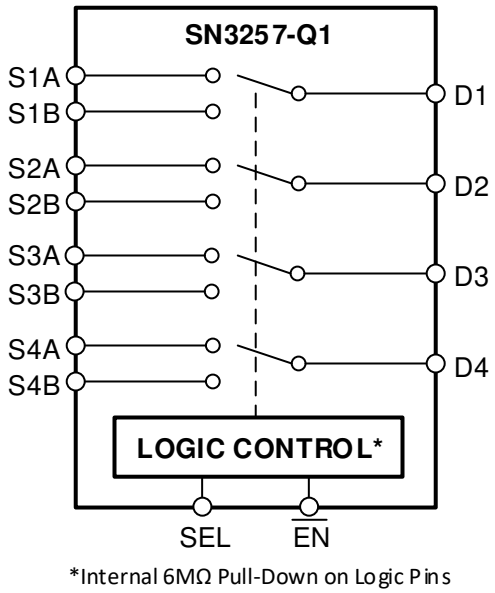

Figure 1. Functional Block Diagram

SN3257-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TSSOP-16 and SOT-23 package of SN3257-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)	
	TSSOP-16	SOT-23
Total Component FIT Rate	13	9
Die FIT Rate	4	4
Package FIT Rate	9	5

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation:100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, Analog, Mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN3257-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Switch channel stuck on	20%
Switch channel stuck off	20%
Switch functional - high resistance	25%
Switch out of specification voltage or leakage	25%
Pin to Pin short any two pins	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN3257-Q1 (TSSOP-16 and SOT-23 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)
- Pin short-circuited to VDD (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 TSSOP-16 and SOT-23 Package

Figure 2 and Figure 3 shows the SN3257-Q1 pin diagram for the TSSOP-16 and SOT-23 package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the SN3257-Q1 datasheet.

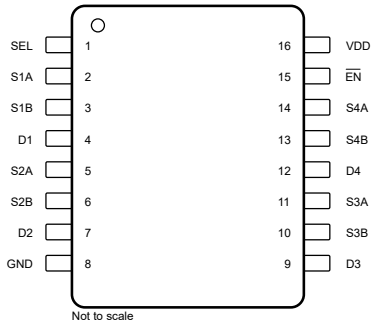

Figure 2. Pin Diagram (TSSOP-16 Package)

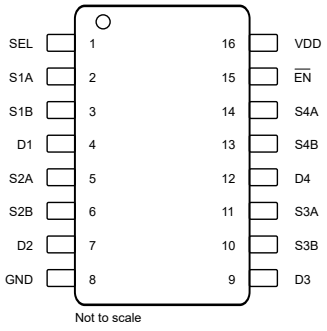

Figure 3. Pin Diagram (SOT-23 Package)

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SEL	1	SEL stuck low. Cannot control switch states	B
S1A	2	Corruption of signal passed onto the D1 pin. If there is no limiting resistor in the switch path device damage possible	A
S1B	3	Corruption of signal passed onto the D1 pin. If there is no limiting resistor in the switch path device damage possible	A
D1	4	Corruption of signal passed onto the S1A/S1B pins. If there is no limiting resistor in the switch path device damage possible	A
S2A	5	Corruption of signal passed onto the D2 pin. If there is no limiting resistor in the switch path device damage possible	A
S2B	6	Corruption of signal passed onto the D2 pin. If there is no limiting resistor in the switch path device damage possible	A
D2	7	Corruption of signal passed onto the S2A/S2B pins. If there is no limiting resistor in the switch path device damage possible	A
GND	8	No effect, normal operation	D
D3	9	Corruption of signal passed onto the S3A/S3B pins. If there is no limiting resistor in the switch path device damage possible	A
S3B	10	Corruption of signal passed onto the D3 pin. If there is no limiting resistor in the switch path device damage possible	A
S3A	11	Corruption of signal passed onto the D3 pin. If there is no limiting resistor in the switch path device damage possible	A
D4	12	Corruption of signal passed onto the S4A/S4B pins. If there is no limiting resistor in the switch path device damage possible	A
S4B	13	Corruption of signal passed onto the D4 pin. If there is no limiting resistor in the switch path device damage possible	A
S4A	14	Corruption of signal passed onto the D4 pin. If there is no limiting resistor in the switch path device damage possible	A
/EN	15	/EN Stuck low. Can no longer disable device	B
VDD	16	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SEL	1	Loss of control of SEL pin. Cannot control switch. Will default to all A switches on	B
S1A	2	Corruption of signal passed onto the D1 pin.	B
S1B	3	Corruption of signal passed onto the D1 pin.	B
D1	4	Corruption of signal passed onto the S1A/S1B pins.	B
S2A	5	Corruption of signal passed onto the D2 pin.	B
S2B	6	Corruption of signal passed onto the D2 pin.	B
D2	7	Corruption of signal passed onto the S2A/S2B pins.	B
GND	8	No effect, normal operation	B
D3	9	Corruption of signal passed onto the S3A/S3B pins.	B
S3B	10	Corruption of signal passed onto the D3 pin.	B
S3A	11	Corruption of signal passed onto the D3 pin.	B
D4	12	Corruption of signal passed onto the S4A/S4B pins.	B
S4B	13	Corruption of signal passed onto the D4 pin.	B
S4A	14	Corruption of signal passed onto the D4 pin.	B
/EN	15	Loss of control of /EN pin. Cannot disable switch. Will default to switches enabled	B
VDD	16	Device unpowered. Device not functional.	B

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effect(s)	Failure Effect Class
SEL	1	S1A	Corruption of signal passed onto the D1 pin. Switch state will be undefined	B
S1A	2	S1B	Corruption of signal passed onto the D1 pin.	B
S1B	3	D1	Corruption of signal passed onto the D1 pin.	B
D1	4	S2A	Corruption of signal passed onto the S1A/S1B & D2 pins.	B
S2A	5	S2B	Corruption of signal passed onto the D2 pin.	B
S2B	6	D2	Corruption of signal passed onto the D2 pin.	B
D2	7	GND	Corruption of signal passed onto the S2A/S2B pins. If there is no limiting resistor in the switch path device damage possible	A
GND	8	D3	Not considered, Corner pin.	D
D3	9	S3B	Corruption of signal passed onto the S3A/S3B & D3 pins.	A
S3B	10	S3A	Corruption of signal passed onto the D3 pin.	A
S3A	11	D4	Corruption of signal passed onto the S3A & D3/D4 pins.	A
D4	12	S4B	Corruption of signal passed onto the D4 pin.	A
S4B	13	S4A	Corruption of signal passed onto the D4 pin.	A
S4A	14	/EN	Corruption of signal passed onto the D4 pin. Switch state will be undefined	A
/EN	15	VDD	/EN Stuck high. Can no longer enable the device	B
VDD	16	SEL	Not considered, Corner pin.	D

Table 8. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SEL	1	SEL stuck high. Cannot control switch states	B
S1A	2	Corruption of signal passed onto the D1 pin. If there is no limiting resistor in the switch path device damage possible	A
S1B	3	Corruption of signal passed onto the D1 pin. If there is no limiting resistor in the switch path device damage possible	A
D1	4	Corruption of signal passed onto the S1A/S1B pins. If there is no limiting resistor in the switch path device damage possible	A
S2A	5	Corruption of signal passed onto the D2 pin. If there is no limiting resistor in the switch path device damage possible	A
S2B	6	Corruption of signal passed onto the D2 pin. If there is no limiting resistor in the switch path device damage possible	A
D2	7	Corruption of signal passed onto the S2A/S2B pins. If there is no limiting resistor in the switch path device damage possible	A
GND	8	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
D3	9	Corruption of signal passed onto the S3A/S3B pins. If there is no limiting resistor in the switch path device damage possible	A
S3B	10	Corruption of signal passed onto the D3 pin. If there is no limiting resistor in the switch path device damage possible	A
S3A	11	Corruption of signal passed onto the D3 pin. If there is no limiting resistor in the switch path device damage possible	A
D4	12	Corruption of signal passed onto the S4A/S4B pins. If there is no limiting resistor in the switch path device damage possible	A
S4B	13	Corruption of signal passed onto the D4 pin. If there is no limiting resistor in the switch path device damage possible	A
S4A	14	Corruption of signal passed onto the D4 pin. If there is no limiting resistor in the switch path device damage possible	A
/EN	15	/EN Stuck high. Can no longer enable the device	B
VDD	16	No effect, normal operation	D

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