Usage of I²C™ for CDCE(L)949, CDCE(L)937, CDCE(L)925, CDCE(L)913

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ABSTRACT

This document presents a method to smoothly change frequency by I²C™ protocol on Texas Instruments CDCE(L)949, CDCE(L)937, CDCE(L)925, CDCE(L)913 Clock Synthesizers, thus avoiding unnecessary intermediate frequencies. It also includes a code example to generate the I²C protocol for the CDCE(L)9xx with the TMS320C645x.

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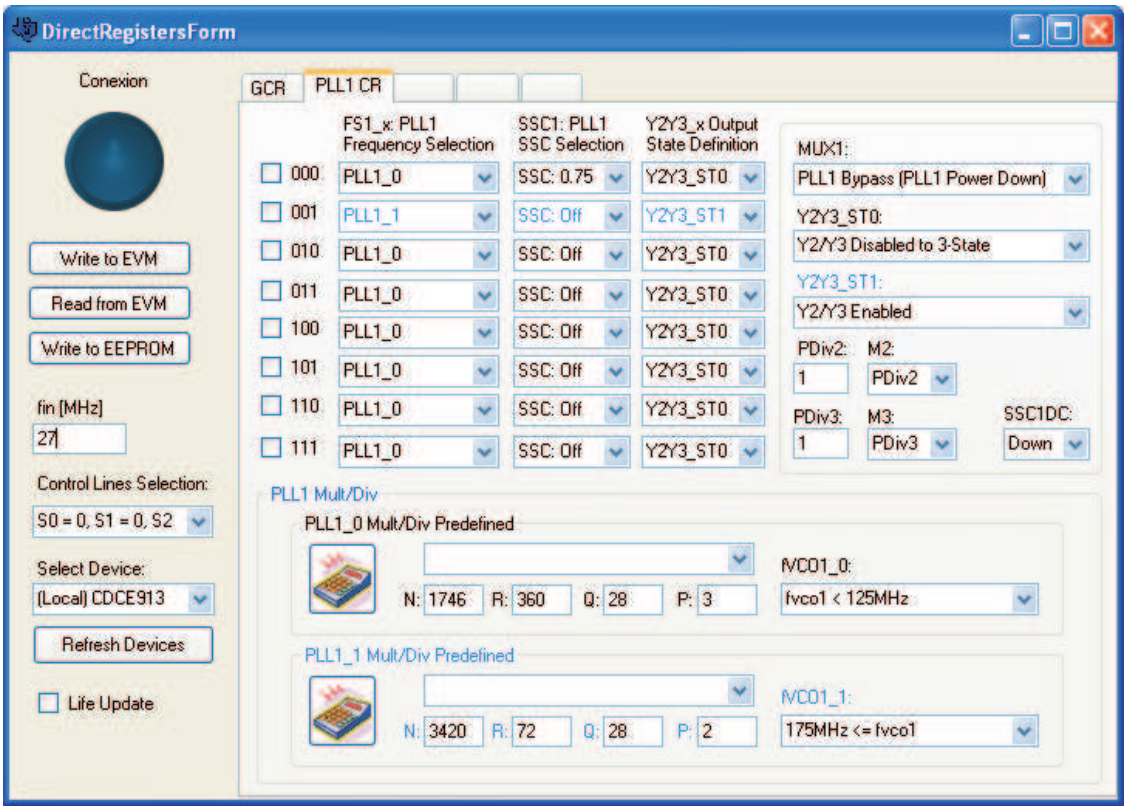
1 Active Setup

The configuration registers simultaneously store many setups (device's configuration), but only one of them is set active by control lines S2, S1, and S0.



NOTE: All the possible setups for PLL1 are displayed.

Figure 1. Screenshot of TI ClockPro Programming Software

Leaving S1 and S2 unconnected while I²C™ mode is enabled (bit 6 from register 2h is set to 0), S1 and S2 are internally understood to be 0, and S0 is the only control line that acts as such. If S0 is left disconnected, then S0 is set to 1 because of the internal pullup (500 kΩ).

For example, in Figure 1 the active setup is highlighted in blue when S0 is set to 1 (by leaving it floating or by voltage level), and the I²C mode is active (S2 and S1 are set internally to 0). In this active setup, FS1_x PLL1 is pointing to PLL1_1 settings (N = 3420, R = 72, Q = 28 and P = 2) to be loaded in PLL1; also, the spread-spectrum clocking (SSC) is off in PLL1 and Y2Y3x Output State Definition enables Y2 and Y3 as stated in Y2Y3_ST1. By setting S0 to 0, the active setup changes as FS1 transfers the PLL1_0 settings to PLL1. This also sets the spread of PLL1 to 0.75% downspread and "Disable to 3 state," the output status of Y2 and Y3, as the Y2Y3x Output State Definition is pointing to Y2Y3_ST0.

When not in I²C mode (control selection lines mode), the bit 6 from register 2h is set to 1. The control lines S1 and S2 are then set to work as such (therefore no longer understood as I²C lines), and the rest of the setups can be accessed. Then, when S0, S1, and S2 are left disconnected, because of the pullup resistor, the setup selected is S2 = 1, S1 = 1, and S0 = 1. All eight combinations are possible in this mode; therefore, many setups are selectable.

2 How to Update/Change PLL Settings With I²C on CDCE(L)949, CDCE(L)937, CDCE(L)925, and CDCE(L)913

The FS byte in the configuration register selects what PLLsetup register is active for its correspondent PLL. Each PLL has an FS byte associated, and each of the bits of FS byte is related to a S0, S1, and S2 combination. Table 1 shows the configuration registers byte addresses related to PLL1.

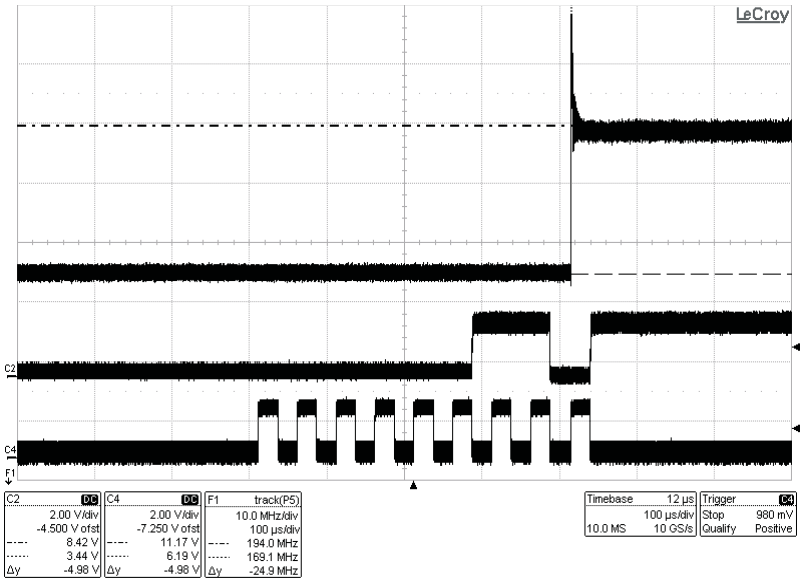
If I²C mode is active, as explained in a previous section, as S2 and S1 are internally set to 0, S0 selects the bit in FS that activates the PLL setup, i.e., if S0 = 1, then if bit 1 in FS is 0, PLLsetup0 is active, and if bit 1 in FS is 1, then PLLsetup1 is active. The VCO frequency is set by N, R, Q, and P defined by each PLLsetup. Changing only N or R results in a fine modification of fout; a modification in Q or P causes bigger changes in fout.

Table 1. Configuration Register Byte Addresses for PLL1

PLL	Registers	Configuration Register Byte Address
PLL1	FS1	13xh
	PLLSetup0	18xh (sets N), 19xh (sets N and R), 1Axh (sets R and Q) and 1Bxh (sets Q, P)
	PLLSetup1	1Cxh (sets N), 1Dxh (sets N and R), 1Exh (sets R and Q) and 1Fxh (sets Q, P)

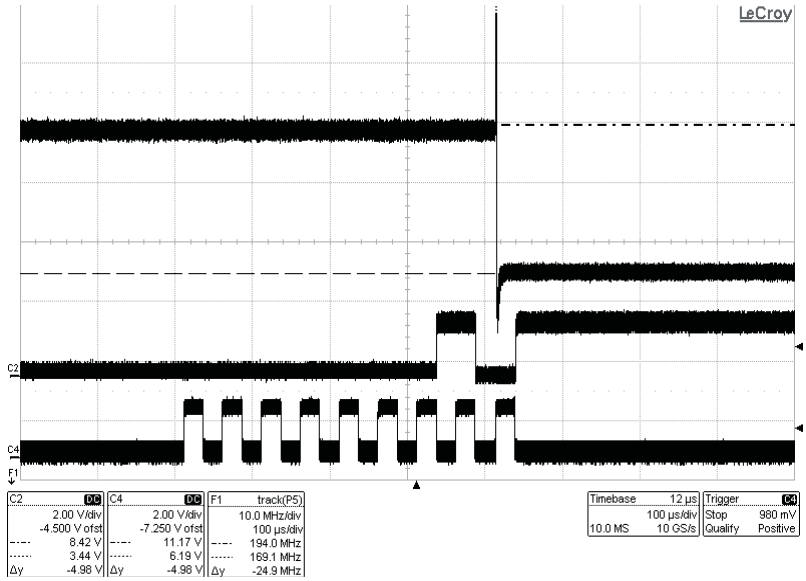
To change the output frequency in one step from F1 to F2 by using the I²C protocol, Texas Instruments recommends changing a bit in the FSn byte. This is because FSn is the byte that associates the PLLn to an output. Using I²C to change the active PLLsetup may cause unwanted intermediate frequency changes before the final F2 is achieved. For this reason, change the PLLSetup when it is inactive. The PLLnSetup1 is inactive when the FSn active bit is set to 0. The PLLnSetup0 is inactive when FSn active bit is set to 1. It is then feasible to change the output frequency at once from F1 to F2 (see Figure 3) or from F2 to F1 (see Figure 2) by just changing a bit into the FSn byte.

In order to change the VCO frequency from F1 to F2, the PLL may need to relock, depending on the clock jitter and the targeted frequency leap (F2-F1). The PLL relocking can be seen on Figure 2 and Figure 3 during the change of frequency from F1 to F2. PLL does not need to relock in most cases where the frequency step is small and a clean clock source is used. Fine tuning can be achieved by only changing the R.



C2 is I2C_SDA, C4 is I2C_SCK, and F1 is the frequency on Y1. When byte FS1 (address 13h) is written to 3xh, PLL1 active setup changes from PLL_setup0 to PLL_setup1. In this plot, PLL_setup0 Y1's frequency is set to 170 MHz, and PLL_setup1 Y1's frequency is set to 194 MHz.

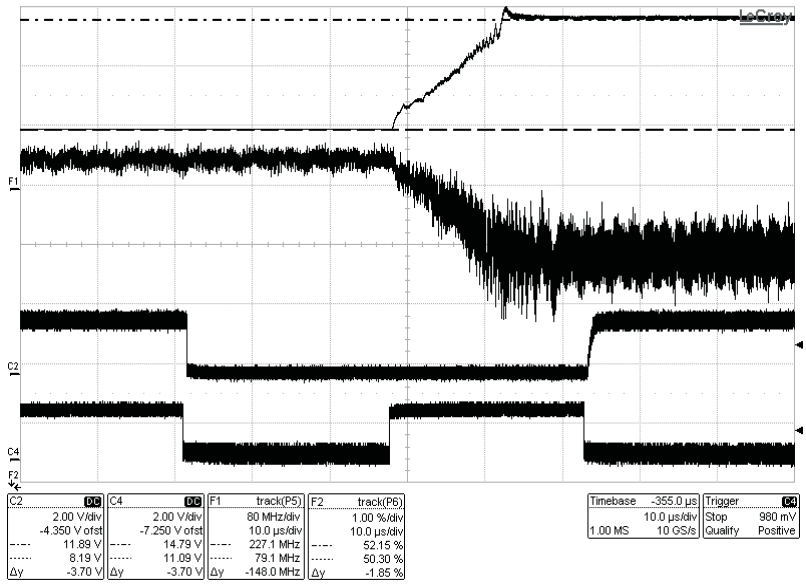
Figure 2. Smooth CDCE949 Output Frequency Changed by I²C



C2 is I2C_SDA, C4 is I2C_SCK, and F1 is the frequency on Y1. When byte FS1 (address 13h) is written to 1xh, PLL1 active setup changes from PLL_setup1 to PLL_setup0. In this plot, PLL_setup0 Y1's frequency is set to 170 MHz, and PLL_setup1 Y1's frequency is set to 194 MHz.

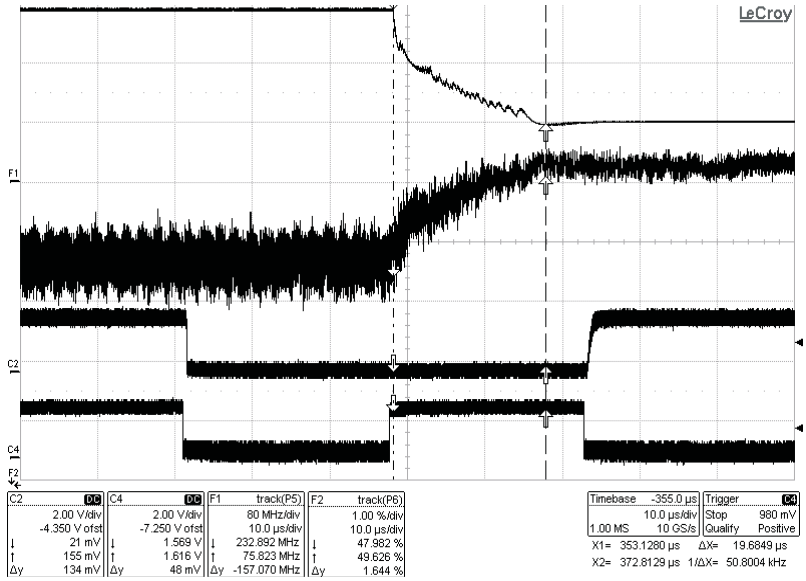
Figure 3. Smooth CDCE949 Output Frequency Changed by I²C

The lock time of the PLL is similar when using an external signal on S0 to trigger the change of the active PLLsetup. In Figure 4 and Figure 5 can be seen a lock time or 19.68 µs when the VCO frequency changes from 80 MHz to 230 MHz. The variation of the duty cycle during the locking stays within 50% and 48%. Note that the VCO output is connected directly to Y1 for all the measurements (Pdiv1 = 1).



C2 is I2C_SDA, C4 is I2C_SCK, F1 is the Y1 frequency, and F2 is Y1 duty cycle. When byte FS1 (address 13h) is written to 03xh, the PLL1 active setup changes from PLL_setup1 to PLL_setup0. In this plot, the PLL_setup0 Y1's frequency is set to 80 MHz, and the PLL_setup1 Y1's frequency is set to 230 MHz.

Figure 4. Smooth CDCE949 Maximum VCO Frequency Changed by I²C



C2 is I2C_SDA, C4 is I2C_SCK, F1 is Y1´s frequency and F2 is Y1´s duty cycle. When byte FS1 (address 13h) is written to 01xh, PLL1 active setup changes from PLL_setup1 to PLL_setup0. In this plot, PLL_setup0 Y1's frequency is set to 230 MHz and PLL_setup1 Y1's frequency is set to 80 MHz.

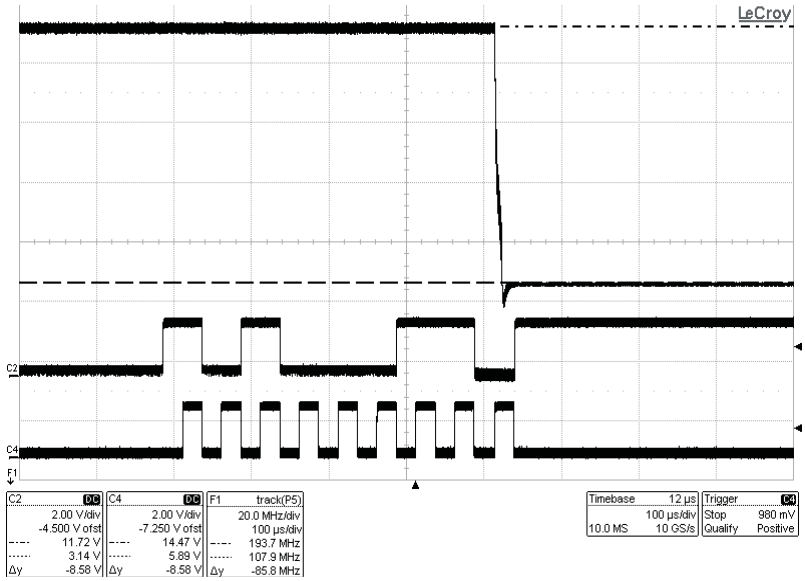
Figure 5. Smooth CDCE949 Output Frequency Changed by I²C

When modifying the active PLLsetup by I²C, the order in which the configuration register is written might result in more than one frequency change. That is the case when more than one byte of the PLLsetup needs to be modified in order to reach the final PLLsetup.

During a write byte or block write, each byte of data patterned is updated after its last bit has been sent. Therefore, if more than one byte in the active PLLsetup is required to change in order to go from F1 to F2, then other intermediate unwanted PLLsetups are active. The second column in Table 2 shows that one intermediate frequency is seen while changing the active setup from F1 to F2. Figure 6 and Figure 7 shows F1 to FI and FI to F2, as opposed to Figure 3 where Y1 changes from F1 to F2 in one step by changing only one bit in FS (having previously stored F2's settings in the inactive PLL1setup).

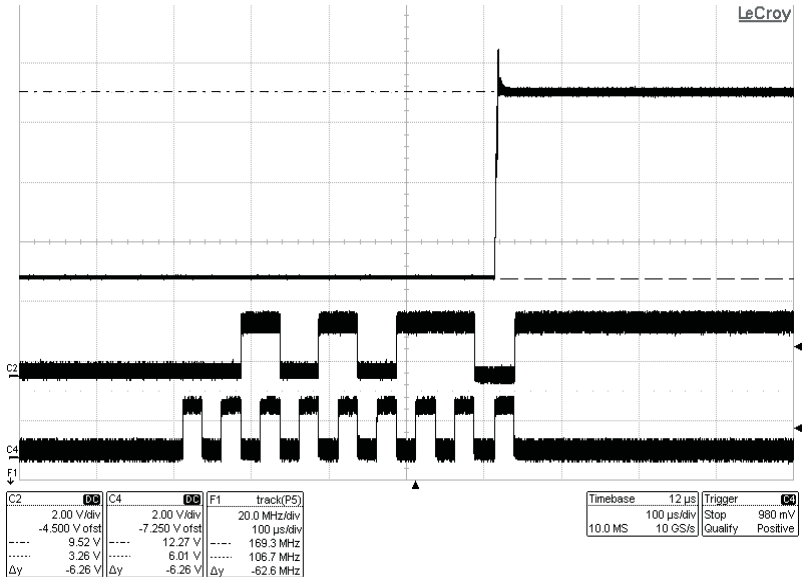
Table 2. PLL1Setup of F1 and F2

	F1's PLL1Setup	FI	F2's PLL1Setup
CR(18xh)=	40xh	40xh	40xh
CR(19xh)=	0Fxh	0Fxh	0Fxh
CR(1Axh)=	A6xh	A3xh	A3xh
CR(1Bxh)=	CFxh	CFxh	2Bxh



Step 1 to change from 194 MHz to 170 MHz. I2C writeByte a3xh on address 1axh (cr(1axh)=a3xh); the previous contents on that address was a6xh. The change is effective when the last bit on the address 1axh is patterned. C2 is I2C_SDA, C4 is I2C_SCK, and F1 is the frequency on Y1.

Figure 6. CDCE949 Changing Frequency by I²C Directly on the Active PLL_setup; Intermediate Frequency Changes May Be Seen



Step 2 to change from 194 MHz to 170 MHz. I2C writeByte 2bxh on address 1bxh (cr(1bxh)=2bxh); the previous contents on that address was cfxh. The change is effective when the last bit on the address 1bxh is patterned. C2 is I2C_SDA, C4 is I2C_SCK, and F1 is the frequency on Y1.

Figure 7. CDCE949 Changing Frequency by I²C Directly on the Active PLL_setup; Intermediate Frequency Changes May Be Seen

In the CDCE906/CCE907, the PLLsetup is always active. Therefore, when updating R, Q, P, and N via I²C on the fly. intermediate output frequency changes between initial and final output frequency can occur.

3 S1 and S2 Tolerant to 3.3-V LVCMOS

The I²C block is powered by the core supply Vdd = 1.8 V. For this reason, to program a CDCE(L)913, CDCE(L)925, CDCE(L)937, or CDCE(L)949 Vddout does not need to be supplied. Although the I²C block is powered with 1.8 V, S1 and S2 are 3.3-V LVCMOS tolerant. When 3.6 V is connected to these pins, some current (approximately 3.6 mA) flows to the supply because of the pullup resistor. The internal pullup resistor (500 kΩ) and the type of transistor makes these pins compatible up to 3.6 V.

4 TMS320C645X Code to Generate I²C Protocol for CDCE(L)949, CDCE(L)937, CDCE(L)925, CDCE(L)913, and CDCE906/907

The following code changes the active frequency in Y1 from F1 = 170 MHz to F2 = 194 MHz.

```
#define CDCE949                          (0x6C)

int change_y1_clock_frequency ()
{

* As S2 and S1 are acting as SDA and SCL, the status selected depends
* on the voltage level of S0. As S0 is left floating the internal pull up will
* set S0 to 1. Therefore the current active status is S2=0, S1=0 and S0=1.
* FS1 selects the PLL setup active, in order to change smoothly the output
* frequency FS register should be used. In the FS register the bit 2 corresponds to
* 001xb status selection. This bit selects the active PLL setup.

* Initially FS is set to 00xh and PLL1Setup0 is active for Y1, where VCO frequency
* is set to 170MHz.

* While PLL1Setup0 is active on registers 18xh, 19xh, 1Axh and 1Bxh, we update
* PLL1setup1 on registers 1Cxh, 1Dxh, 1Exh and 1Fxh to generate 194MHz
            unsigned char val2[2];
            int err = 0;



                        val2[0] = 0x40|0x80;;
                        val2[1] = 0x1C;
                        err = davinci_i2c_write(2, val2, CDCE949);

                        val2[0] = 0x0F|0x80;;
                        val2[1] = 0x1D;
                        err = davinci_i2c_write(2, val2, CDCE949);

                        val2[0] = 0xA3|0x80;;
                        val2[1] = 0x1E;
                        err = davinci_i2c_write(2, val2, CDCE949);

                        val2[0] = 0x2B|0x80;;
                        val2[1] = 0x1F;
                        err = davinci_i2c_write(2, val2, CDCE949);
* Set bit two from register FS to 1 to change Y1 frequency from 170MHz to 194MHz
* by activating the PLL1setup1

                        val2[0] = 0x02|0x80;
                        val2[1] = 0x13;
                        err = davinci_i2c_write(2, val2, CDCE949);

* after the previous instruction if err=0 Figure 2 displays Y1´s frequency change

                        mdelay(200);
                        return err;
}
```

5 References

1. *CDCE906, Programmable 3-PLL Clock Synthesizer/Multiplier/Divider* data sheet (SCAS814)
2. *CDCE949, CDCEL949, Programmable 4-PLL VCXO Clock Synthesizer With 1.8V, 2.5V and 3.3V LVCMOS Outputs* data sheet (SCAS844)

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