Application Report
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Overview of JEDEC RawCards for DDR3 RDIMM

Christian Schmoeller, Christian Harrieder — *CDC - Clock Distribution Circuits*

ABSTRACT

This application report gives an overview on the currently defined DDR3 RDIMM RawCards by JEDEC. It is a summary of the register-relevant parameters of each RawCard Specification.

Because JEDEC DDR3 standardization is still ongoing, this report presents information available to date.

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1 Overview on JEDEC DDR3 RDIMM RawCards

In Table 1 and Table 2, register-related parameters of most common JEDEC DDR3 RDIMM RawCards are summarized.

Table 1. Summary of JEDEC DDR3 RDIMM RawCards (Low Profile)

RawCard	Topology	DRAM Package Technology	Number of		Compliant TI Register	LOADS [Number of Dies]			R_Feedback [Ω]	C_Feedback [pF]
			DRAMS	Registers		ADDR/ CMD	CTRL	CK		
A	1Rx8	planar	9	1	SN74SSQE32882ZALR	5/4	5/4	5/4	75	0
B	2Rx8	planar	18	1	SN74SSQE32882ZALR	10/8	5/4	5/4	75	0
C	1Rx4	planar	18	1	SN74SSQE32882ZALR	10/8	10/8	10/8	75	0
D	2Rx4	stacked (2H)	36	1	SN74SSQE32882ZALR	20/16	10/8	10/8	75	0
E	2Rx4	planar	36	1	SN74SSQE32882ZALR	20/16	10/8	10/8	75	0
F	4Rx4	stacked (2H)	72	2	SN74SSQE32882ZALR	20/16	10/8	10/8	75	0
G	4Rx8	stacked (2H)	36	1	SN74SSQE32882ZALR	20/16	5/4	10/8	80	0
H	4Rx8	planar	36	1	SN74SSQE32882ZALR	20/16	5/4	10/8	75	0
J	2Rx4	planar	36	1	SN74SSQE32882ZALR	20/16	10/8	10/8	75	0
T	2Rx4	planar	36	1	SN74SSQE32882ZALR	20/16	10/8	10/8	75	0
W	4Rx4	stacked (2H)	72	2	SN74SSQE32882ZALR	20/16	10/8	10/8	75	0
Y	4Rx8	planar	36	1	SN74SSQE32882ZALR	20/16	5/4	10/8	75	0
AA	4Rx4	stacked (2H)	72	1	SN74SSQE32882ZALR	40/32	20(10)/ 16(8)	20/16	75	0
AB	4Rx4	stacked (2H)	72	2	SN74SSQE32882ZALR	20/16	10/8	10/8	75	0

Table 2. Summary of JEDEC DDR3 RDIMM RawCards (Very Low Profile)

RawCard	Topology	DRAM Package Technology	Number of		Compliant TI Register	LOADS [Number of Dies]			R_Feedback [Ω]	C_Feedback [pF]
			DRAMS	Registers		ADDR/ CMD	CTRL	CK		
K	1Rx8	planar	9	1	SN74SSQE32882ZALR	5/4	5/4	5/4	75	0
L	2Rx8	planar	18	1	SN74SSQE32882ZALR	10/8	5/4	5/4	75	0
M	1Rx4	planar	18	1	SN74SSQE32882ZALR	10/8	10/8	10/8	75	0
N	2Rx4	stacked (2H)	36	1	SN74SSQE32882ZALR	20/16	10/8	10/8	75	0
P	2Rx4	planar	36	1	SN74SSQE32882ZALR	20/16	10/8	10/8	75	0
R	4Rx4	stacked (4H)	72	2	SN74SSQE32882ZALR	20/16	10/8	10/8	75	0
U	4Rx4	stacked (4H)	72	1	SN74SSQE32882ZALR	40/32	10/8	20/16	75	0
V	4Rx8	stacked (4H)	36	1	SN74SSQE32882ZALR	20/16	5/4	20/16	75	0

2 Explanations on RawCard Parameters

This section gives an explanation on the parameters shown in Table 1 and Table 2.

- **RawCard**
  The JEDEC committee standardizes Dual Inline Memory Modules (DIMM) including their population, routing, and performance specification. A complete specification of a DIMM is called a RawCard (R/C).
- **Topology**
  The topology reflects the number of Memory Ranks on the module as well as the width of the DRAMs.
  Example: 2Rx4: 2 Ranks, 4-bit-wide DRAMs
- **DRAM Package Technology**
  DRAMs can be assembled in planar packages (one die per package) or stacked packages (multiple dies per package).
- **Number of DRAMs**
  Number of DRAM dies on one module. In case of using stacked packages, the number of DRAM packages is smaller than the number of DRAM dies.
- **Number of Registers**
  Number of Register/PLL devices on one module.
- **Compliant TI Register**
  Register/PLL from Texas Instruments that can be used on that particular RawCard
- **ADDR/CMD loads**
  Number of DRAM loads (= Number of Dies) on each Address and Command output of the register (A-side/B-side).
- **CTRL loads**
  Number of DRAM loads (= Number of Dies) on each Control output of the register (A-side/B-side).
- **CK loads**
  Number of DRAM loads (= Number of Dies) on each Clock output of the register (A-side/B-side).
- **R_Feedback**
  Termination of the feedback loop.
- **C_Feedback**
  Feedback Loop Capacitor. In previous memory generations (e.g., DDR1 or DDR2), the feedback capacitor was used for zero delay tuning (see SCAA093). But in DDR3, this is unnecessary. The feedback loop is used only for voltage and temperature compensation. Therefore, on all JEDEC RawCards, the feedback capacitor is 0 pF.

3 References

1. *SN74SSQE32882, 28-Bit to 56-Bit Configurable Registered Buffer with Address-Parity Test* data sheet (SCAS857)
2. *JEDEC Solid State Technology Association, Registered DIMM Design Specification* (JESD21)

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