CDCx706/x906 Termination and Signal Integrity Guidelines

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ABSTRACT

This application report shows and evaluates different termination schemes for the

- CDCE706 (EEPROM, f_{max} = 300 MHz, industrial temperature range)
- CDCE906 (EEPROM, f_{max} = 167 MHz, commercial temperature range)
- CDC706 (ROM, f_{max} = 300 MHz, industrial temperature range)
- CDC906 (ROM, f_{max} = 167 MHz, commercial temperature range)

Guidelines for optimizing the series termination are discussed. Additionally, this report describes how the CDCx706/x906 family can be used to drive 1.8-V clock inputs.

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1 Clocking Solution for DaVinci™ Digital Media System-on-Chip (TMS320DM644x)

Modern applications usually require a large number of clocks. However, for cost-driven applications, it is often unsuitable to use a dedicated clock source for every clock that a system requires. Different I/O voltages can further complicate the clocking scheme. Therefore, what is wanted is a flexible clock generator that generates several clocks from one clock source with the added potential of selecting different I/O voltage levels. As an example, Figure 1 shows a clocking scheme for an Internet protocol set-top box (IP-STB).

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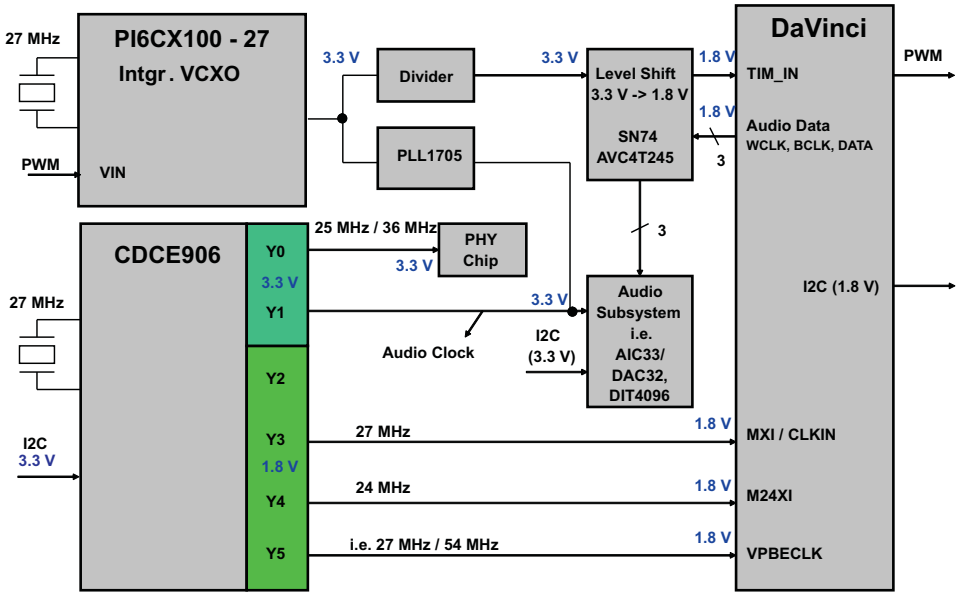

Figure 1. Clocking Scheme of an IP-STB

In this example, many different clocks at 3.3 V and 1.8 V are needed. The CDCE906 provides most of the clocks. For a clock with 3.3-V I/Os, level shifters are needed to address the 1.8-V I/Os of the DaVinci™ digital signal processor (DSP). The CDCE906 is specified to drive 3.3-V and 2.5-V I/Os. A 1.8-V interfacing is also possible, which spares any additional level shifters.

2 Series Termination for 3.3-V and 2.5-V Clocks

Series termination is a common method to maintain the signal integrity for LVCMOS drivers, if connected to a receiver with a high-impedance input. For series termination, a series resistor, R_S, is placed close to the driver. The sum of the driver impedance Z_{out} and R_S should be close to the transmission line impedance Z_0. If this is the case, the transmission line is properly terminated at the beginning and signal integrity is maintained – even if the transmission line is long.

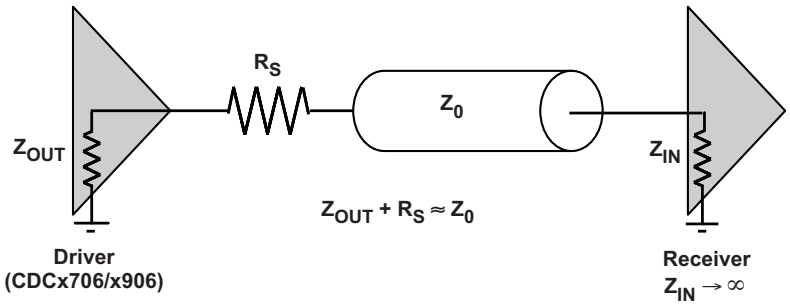

Figure 2. Series Termination

To determine the correct value for R_S, it is necessary to know the output impedance Z_{out}. Table 1 shows the typical output impedance during the transition for different transmission lines impedances. PU (pullup) is the impedance for the rising edge, while PD (pulldown) is the impedance for the falling edge. Because PU and PD are representing two different internal transistors, the impedances can be slightly different. The value for R_S should be chosen to get a good matching to the transmission line impedance for PU and PD.

Table 1. Output Impedance of the CDCx706/x906

CDCx706/x906 Output Impedance (Typical)					
Z_0 (Ω)	Type	3.3 V (Fastest Slew Rate)		2.5 V (Fastest Slew Rate)	
		Impedance (Ω)	Proposed R_S (Ω)	Impedance (Ω)	Proposed R_S (Ω)
35	PU	49	0	62	0
	PD	45		67	
50	PU	45	5	57	0
	PD	42		58	
75	PU	43	10	51	0
	PD	38		49	
100	PU	41	12	49	5
	PD	35		44	

Table 1 shows a basic value for R_S. Signal Integrity simulations, e.g., with IBIS models, are useful to optimize the value of the series resistor by including the receiver and board parasitics. Further, with simulations, the series termination can be proved under corner conditions like the weak and strong process corners of the IC.

The CDCx706/x906 has an built-in slew rate control. The slew rate control allows enlarging the rise and the fall time in order to reduce electromagnetic interference (EMI) on the board. An increase of the output impedance of the CDCx706/x906 is necessary to achieve slower transitions. Due to this, series termination is only possible for the fastest slew rate of the CDCx706/x906. A special termination scheme for the slower slew rates is discussed later in this report.

3 Driving 1.8-V Inputs With a Voltage Divider

1.8-V I/Os are common in today's applications. DSPs like DaVinici™ are running at 1.8 V to reduce the power consumption and the EMI at higher clock rates. Therefore, it is important to find simple solutions to interface with 1.8-V I/Os. One method is to use the driver at a V_{CC_OUT} of 3.3 V or 2.5 V by reducing the swing at the receiver side with a simple voltage divider.

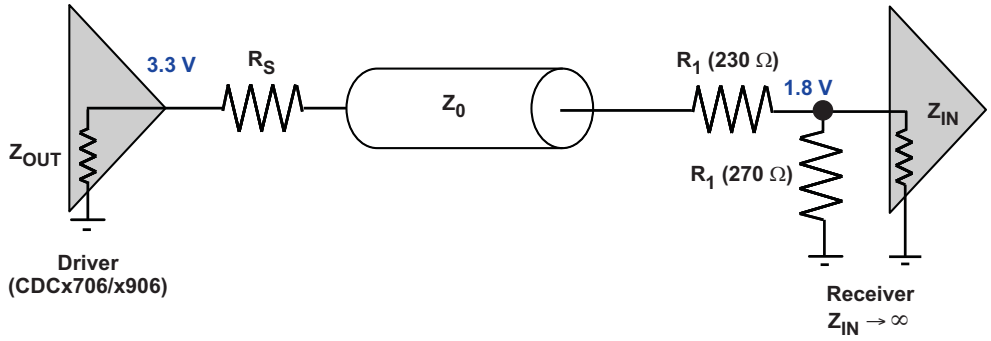

Figure 3. 1.8-V Voltage Divider

Figure 3 shows how this voltage divider can look. For this example, the AC-load is 500 Ω to GND, which is similar to the AC load that results from the data-sheet test load. Therefore, the AC parameters stay close to the values mentioned in the data sheet.

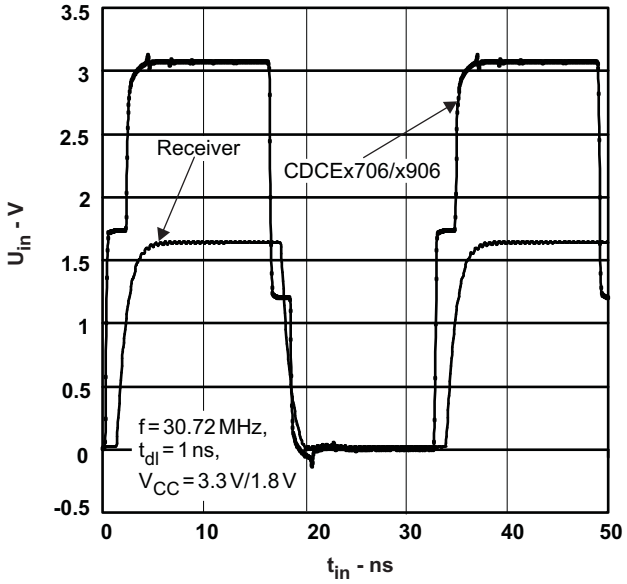

Figure 4. Simulation Results of the Voltage Divider

Figure 4 shows simulation results for this 1.8-V interfacing solution. The CDCx706/x906 output and a receiver with input parasitics similar to the CDCL6010 CLKP input in the single-ended mode was used. The simulation shows that the transmission line is properly terminated, and the signal integrity at the receiver is good. Therefore, this solution is well-suited to address 1.8-V clock inputs for devices like the CDCL6010 or the DaVinci™ DSP.

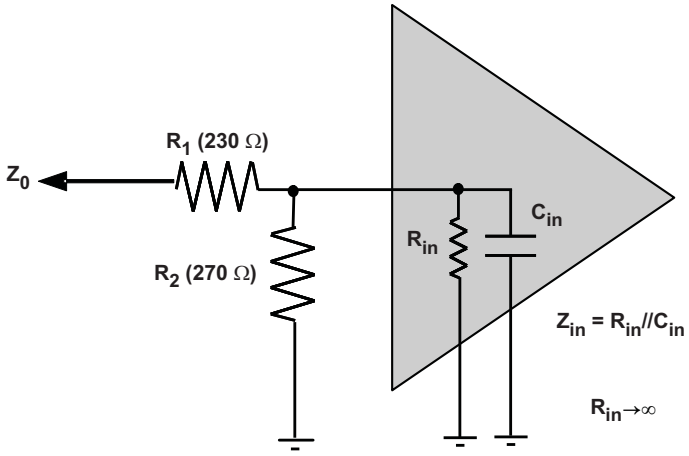

Figure 5. Parasitic Capacitance of a Receiver

The external voltage divider and the input impedance of the receiver appear as a low-pass filter. Therefore, it is important to consider the corner frequency for a given input capacitance C_{in} as shown in Figure 5. Higher order harmonics that are beyond the corner frequency are cut off. This can reduce the slew rate of the clock, if the clock frequency and/or the input capacitance of the receiver are high. Table 2 shows the corner frequency under certain conditions. Signal integrity simulation can further help to check whether the slew rate is high enough. However, current designs like the CDCL6010 or the DaVinci™ DSP have an input capacitance of around 2 pF, which allows using the voltage divider at even higher frequencies.

Table 2. Corner Frequency for Varying C_{in}

Receiver Corner Frequency		
C_{in} (pF)	F_{3dB} (MHz)	F_{6dB} (MHz)
1	1300	2200
2	649	1110
4	322	553
8	163	278

In case of internal biasing, there can be additional leakage currents, by using an external voltage divider. Therefore, it is important to have some basic knowledge about the input stage that is used.

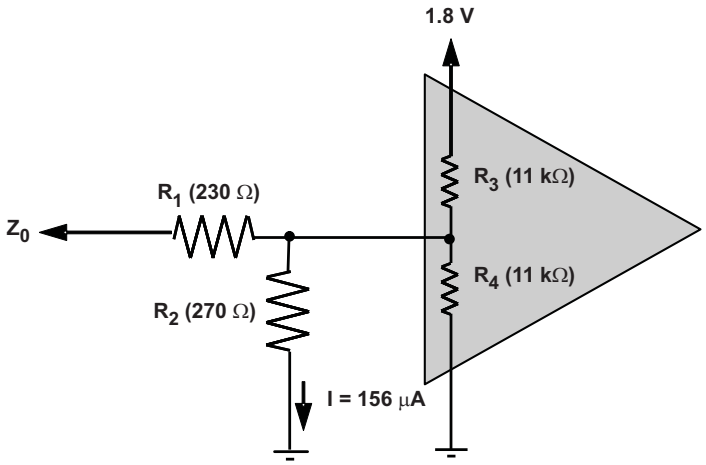

Figure 6. Current Through Internal Structures

Figure 5 shows an example in which an additional current of 156 µA is caused by the internal voltage divider. The driver is assumed to be in 3-state mode. This shows that the internal structure of the receiver must be known, to estimate the additional current that is caused. Usually, LVCMOS inputs have large pullup/pulldown resistors, and therefore the additional currents are negligible.

4 Driving 1.8-V Inputs Directly

Another option to connect the CDCx706/x906 to a 1.8-V input is to supply V_{CC_OUT} with 1.8 V. Even if 1.8 V is not a specified parameter of the CDCx706/x906, the output can handle 1.8 V but at a limited drive capability. Especially for applications with limited space, or in cases where a voltage divider at the input is not possible, this can be a good, working solution. The fastest slew rate should be used in this case.

Because the output impedance at V_{CC_OUT} of 1.8 V is higher than 50 Ω, series termination is not possible anymore. Therefore, the CDCx706/x906 must be placed as close as possible to the receiver input to avoid reflections from the unterminated transmission line. An additional resistor, R_f, can be placed close to the receiver to reduce the effects of reflections.

An additional series termination resistor, R_S, can be placed close to the driver, to avoid overshoot at the receiver. This could happen if the driver is running at its strong corner (1.9 V V_{CC_OUT}/minimum temperature)

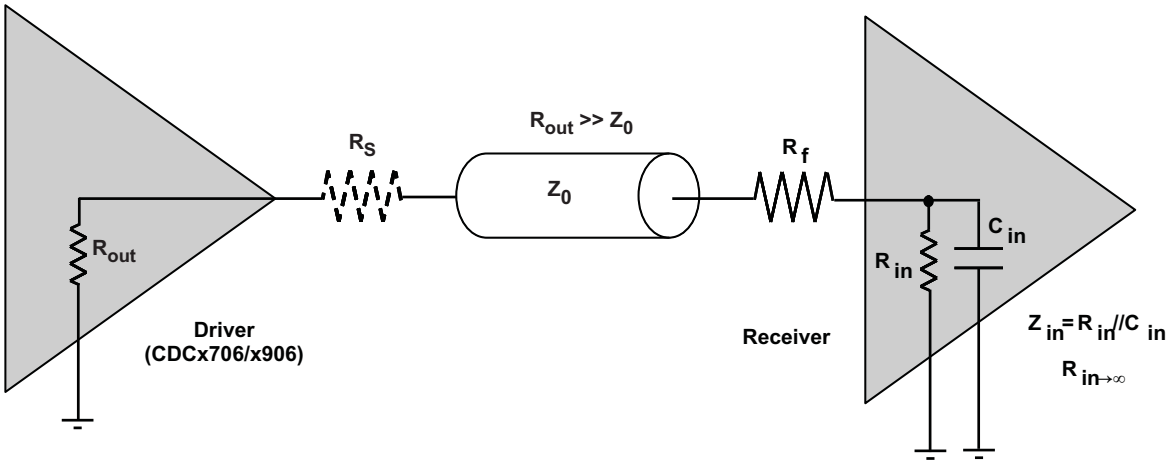

Figure 7. Direct 1.8-V Interface

R_f and C_{in} combine to make a low-pass filter that smooths steps in the rising and falling edge at the receiver, which are caused by line reflections. This low-pass filter can be optimized to avoid steps in the threshold, which could cause the receiver to oscillate or to switch several times due to noise. R_f is usually in the range of 200 Ω to 300 Ω, but must be matched to the individual application.

Rf depends on the output impedance R_{out} of the driver, the transmission line impedance Z_0, and the receiver input impedance Z_{in}. Therefore, it is difficult to find a general rule to determine R_f. The most suitable way is to do simulations. Adequate IBIS models are available at the TI external Web site (www.ti.com).

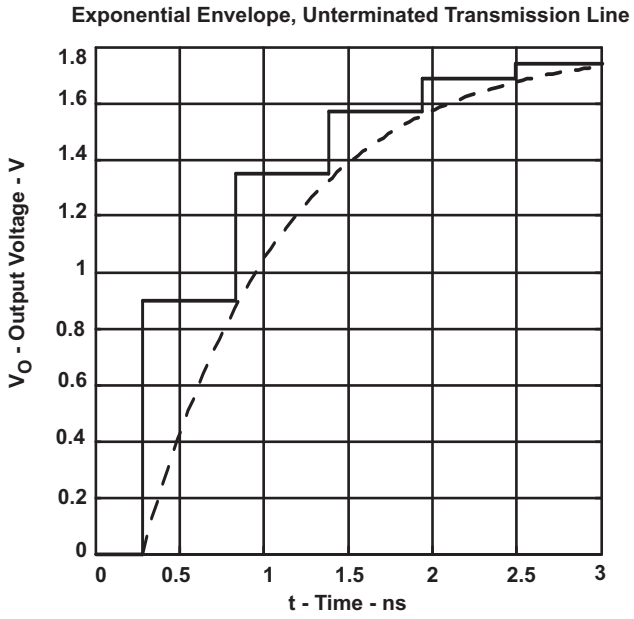

Figure 8. Effect of R_f on an Unterminated Transmission Line

Figure 8 shows the effect of R_f on an unterminated transmission line. The step-line shows the rising edge of a clock signal on a transmission line without termination. The smoothed line shows the clock on an unterminated transmission line with adjusted R_f. As a result, the rise time remains almost equal for the filtered signal, but the steps during the transition are filtered.

Simulations confirmed that this termination scheme meets the input requirements of the DaVinci™ DSP for the clock inputs MXI, M24XI, TIM_IN, and VPBE clock. A transmission line length of approximately 50 mm showed good results. Therefore, it is possible to do a direct 1.8-V interface to the DaVinci™ DSP, which can be used in applications like that shown in Figure 1.

5 Slew Rate Control for EMI Reduction

The CDCx706/x906 uses four different slew rates to adjust the transition time of the output. A longer rise and fall time of the clock edges reduces the higher order harmonics and therefore reduces the EMI at higher frequencies.

However, an increase in the output impedance is necessary to get a longer rise and fall time. Therefore, series termination is unsuitable for slew rates slower than the fastest (= default slew rate). If EMI reduction is necessary by setting the slew rate to a lower value, a termination scheme as shown in Figure 7 is required. The same considerations as discussed in the previous section are valid here.

6 Conclusion

Today's applications often need complex clocking structures. The clocking structure becomes more complicated if different I/O voltages are required. The CDCx706/CDCx906 is specified to drive 3.3-V and 2.5-V I/Os. Also, 1.8-V interfacing is possible, which spares any additional level shifters.

Different terminations have been demonstrated for all three voltage levels. This application report shows further, that the CDCx706/x906 is well-suited as a clock driver for DSPs like the DaVinci™ TMS320DM644x or jitter cleaner like the CDCL6010.

7 References

1. *CDCE706 Programmable 3-PLL Clock Synthesizer/Multiplier/Divider* data sheet (SCAS815D)
2. *CDCE906 Programmable 3-PLL Clock Synthesizer / Multiplier / Divider* data sheet (SCAS814C)
3. *CDCE906/706 Performance Evaluation Module User's Guide* (SCAU016)
4. *TMS320DM6446-594: TMS320DM6446 Digital Media System-on-Chip* data sheet (SPRS283A)
5. H. W. Johnson and M. Graham, *High-Speed Digital Design*, PTR Prentice-Hall, New Jersey, 1993
6. M. Mirmak, IBIS *Modeling Cookbook for IBIS Version 4.0*, The IBIS Open Forum, September 15, 2005.

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