Application Note

Design Flexibility of TPS7A1408 to Variable Vout and Stability Check

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ABSTRACT

TPS7A14 is a small, ultra low-dropout regulator with excellent transient response and can provide sourcing current up to 1-A peak. Normally, key design performance of LDO includes high PSRR, low noise, low ripple, fast transient response, low quiescent at no load condition, good line and load regulation. And also, the stability is always necessary for LDO. TPS7A14 specifies these requirements superior and can be useful for the application of low input and low dropout power rails. It features NMOS pass element and fixed Vout so for optimized package and schematic size. This application note addresses the flexibility to adjustable Vout configuration and followed concerns on loop stability.

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1 Introduction

TPS7A14xx is available for a wide range of output voltages but in fixed steps of 25 mV, and it is changeable through OTP process. However, in some applications, applying multiple TPS7A14 for variable power rails, there is a need to have them unified for design flexibility as well as management matters. Starting from understanding of inside blocks, users can easily configure adjustable Vout rails

1.1 TPS7A14 Functional Block Diagram

Figure 1-1 shows how internal circuitry is connected and its functional blocks. Generally, NMOSFET pass transistor has low impedance at output stage. Hence it can provide low noise performance since NMOS LDO has a low spike/ripple at output which is dependent on output impedance. Unit gain Opamp named as EA (error amplifier) monitors output voltage directly via SENSE pin and its reference_Vref at non-inverting input comes from the additional Op amp loop. It has a dedicated gain to make Vref follow desired Vout in 25-mV steps and it can be trimmed through OTP process adjusting RB of its resistor network. Bandgap 1.2 V is supplied from external biasing accommodating ultra low dropout at low output voltages. Section 1.2 will address the reason why NMOS LDO needs external biasing.

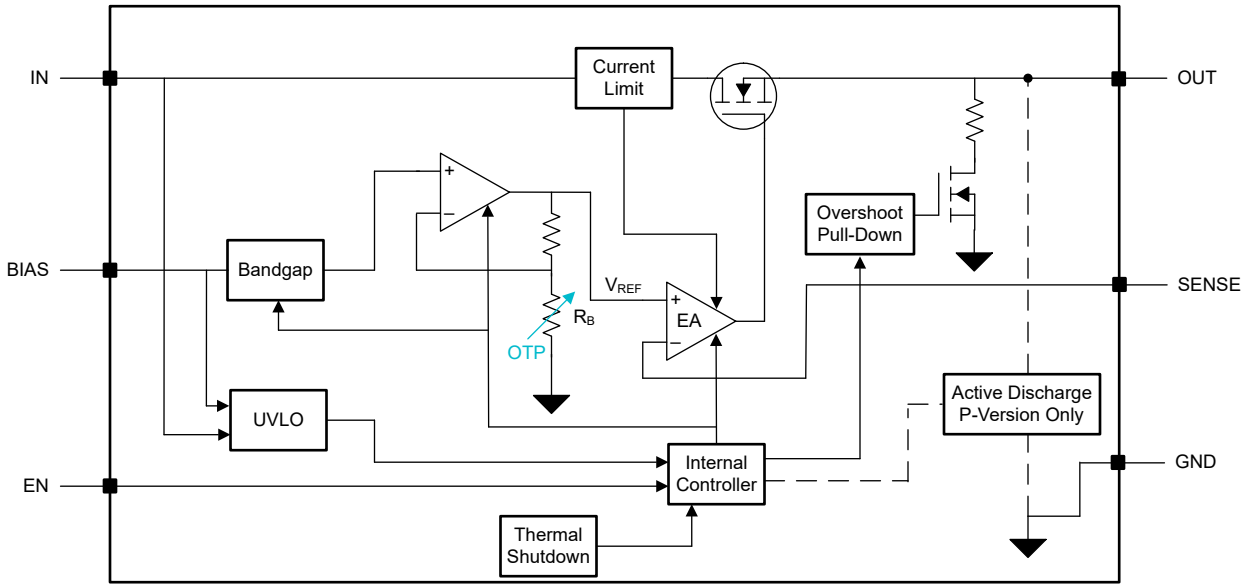

Figure 1-1. Functional Block Diagram

1.2 Biasing Rail for NMOS LDO

LDO, especially pass element(dealing MOSFET only here) works in the linear region to reduce the input voltage down to the required output voltage and it is controlled by error amplifier changing FET's gate to the appropriate operating point at a given load condition, or accordingly when the input voltage changes. Key note is that the pass element behaves like a simple resistor. We understand drain-to-source resistance Rds is moving its value inside linear region area of MOSFET. If we consider only pass element, conventional background says that N-type power stage has higher dropout limitation than that of P-type and it's true that because error amplifier will saturate at the input supply voltage as Vin approached to Vout. Figure 1-2 illustrates the mechanism.

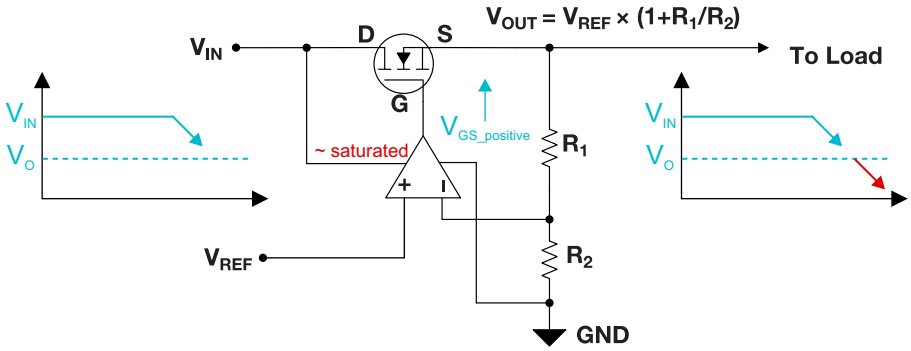

Figure 1-2. Dropout Limitation of NMOS LDO

As Vin approaches Vout, error amplifier compensates it through lowering the Rds in order to maintain regulation. However, since the collapsing Vin supplies the amplifier VGS cannot be more positively increased at a certain point. It results in unregulated Vout. Limited Rds multiplied by output load current will derive more dropout from nominal Vout. That's because there are two options to overcome this challenge. One is to have external biasing for gate driving and the other one is a charge pump.

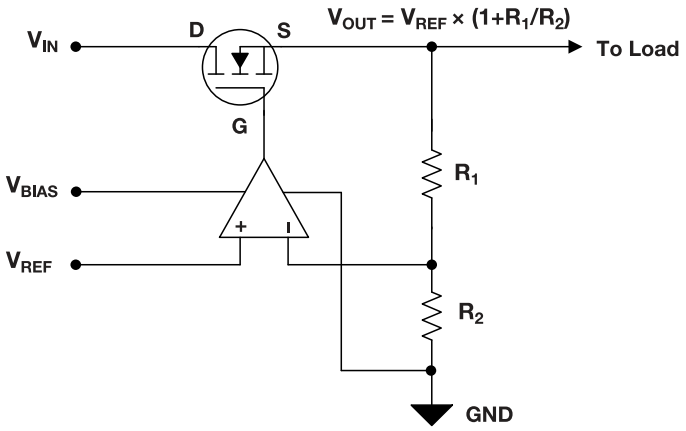

Figure 1-3. NMOS LDO with an External Biasing

VBIAS serves as the positive supply rail for error amplifier and allows its output to swing up to VBIAS. Now though Vin approaches Vout, driver circuit enables maintaining a high VGS. This makes Rds lower achieving ultra low dropout performance. Note that minimum bias voltage above the nominal desired Vout must be maintained. The information about minimum VBIAS headroom is provided commonly in the product data sheet.

2 Design and Considerations to Check

2.1 Configuring External Resistor Network

As shown in Section 1.2, users can configure external resistor network providing scaled Vout information into feedback control loop. To modify fixed programmed Vout for variable power rails, set one reference device. This note deals building 1.2 V output from TPS7A1408. As stated in previous Section 1.1, TPS7A14 has a unit gain error amplifier forcing sensed Vout to be equal to VREF. It tells that TPS7A1408's VREF is 0.8V. Following common Equation 1, good starting point for R2 is a 10 kohm based on tradeoff of noise immunity and leakage.

$$\text{Vout} = \text{Vref} * \left(1 + \frac{\text{R1}}{\text{R2}}\right) \tag{1}$$

With R2 = 10 kohm, yields calculated R1 as 5 kohm.

2.2 Feed-forward Capacitor for Loop Stability

Alternative ways from original product design could cause unwanted stability issues. In other words, users who apply those changes should take all the possible operating environments into account. Whole operating temperature range and multiple corner cases of product in silicon level should be considered. However, these efforts are only accessible by product designers. The best way for users is to perform a load transient test and observing the amount of ringing on the output in time domain and then measure a Bode plot to see if control loop satisfies stability criteria and wave-forming in frequency domain. Paralleling a capacitor with R1 creates additional one pole and one zero respectively and it's a basic approach to improve the loop stability by boosting phase lead. And also, it is natural that ac signal on Vout can pass through feed-forward capacitor to the VFB, meaning fast response for control loop from any fluctuation during load transient condition, eventually improving the bandwidth of feedback loop. Figure 2-1 is an open loop small-signal model of NMOS LDO.

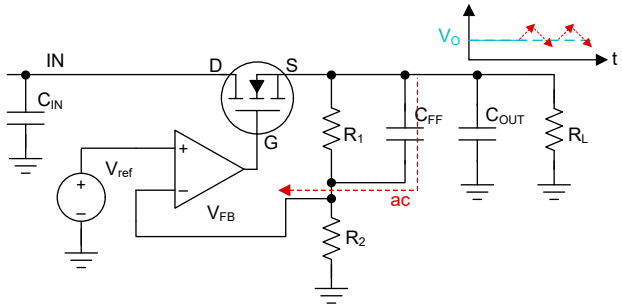

Figure 2-1. Open Loop Small-Signal Model of NMOS LDO

Defining small-Signal analysis is out of scope of this application note. In spite of that, users need to understand how C_{FF} contributes to frequency response. Equation 2 and Equation 3 represent frequency of the zero and pole And they give a hint that this zero (Z_{FF}) always position at lower frequency than P_{FF}.

$$\text{ZFF} = \frac{1}{(2\pi * R1 * CFF)} \tag{2}$$

$$\text{PFF} = \frac{1}{(2\pi * (R1 // R2) * CFF)} \tag{3}$$

For further details about the LDO stability, see *AN-1482 LDO Regulator Stability Using Ceramic Output Capacitors* application note. And for further information about using C_{FF}(feed-forward capacitor), see *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

2.3 IR Drop Compensation by Remote_Sense

SENSE pin monitors Vout and helps control loop compensate voltage drop caused by the parasitic resistance resident on trace from OUT pin terminal to actual point of loads. This feature is useful when the load is placed a bit far from OUT pin and is to provide accurate output level to the load which minimizes the IR drop impact. Figure 2-2 illustrates the function.

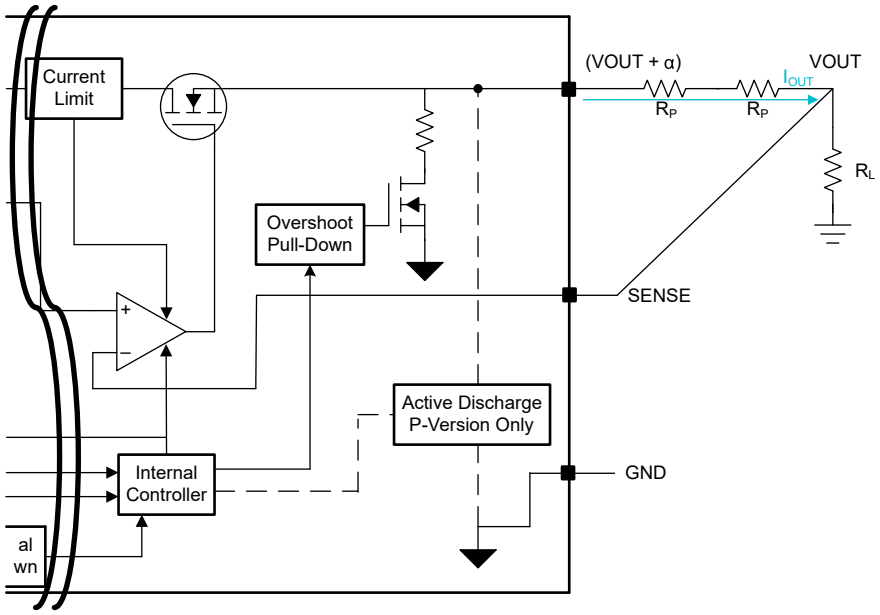

Figure 2-2. IR Drop Compensation by Remote_Sense

As shown in Figure 2-3, flexible schematic change for adjustable Vout can pursue same functioning through connecting the VFB node from the point of load. Note that placing resistor network is recommended to be close to SENSE pin while the remote sensing trace requires Kelvin connection in care.

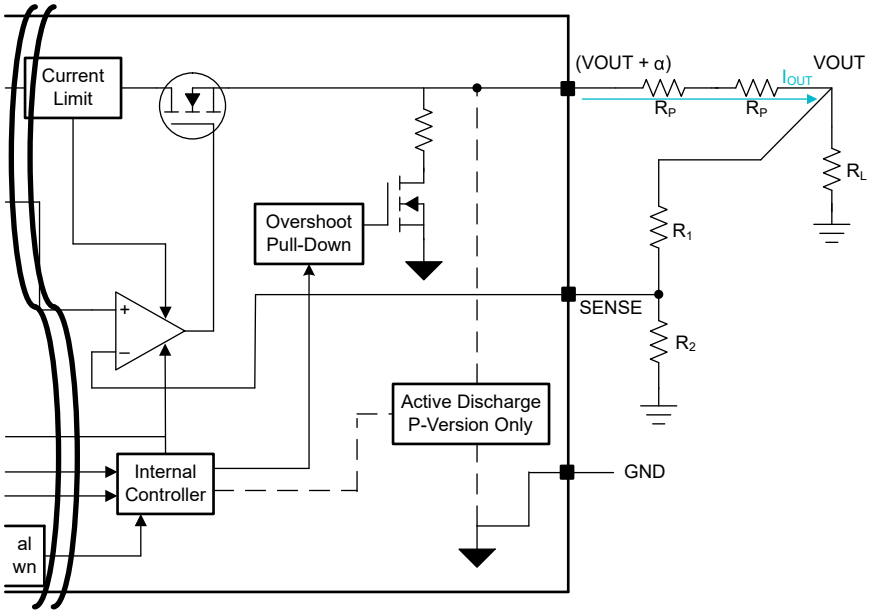

Figure 2-3. IR Drop Compensation by Remote_Sense with Resistor Network

3 Stability Verification

3.1 Simulated Bode Plot vs. Evaluated Bode Plot

As mentioned in Section 2.2, verifying stability of control loop should include whole operating conditions such as corner cases of silicon variations, temperature range as well. In detail, it also requires considering quiescent current of feedback network and feedforward value. Figure 3-1 is a simulated Gain and Phase plot in product design level. Each curve represents temperature and three CMOS process variation as weak, normal and strong. Simply, it turns out about 540-kHz UGB (unit gain bandwidth) and 35° PM (phase margin) at 100 mA output load current. Meanwhile, same measurement using frequency analyzer on TPS7A1408EVM after modifying schematic with 10nF feedforward capacitor shows UGB of about 590 kHz and 81° PM. It can be left for further tune by users.

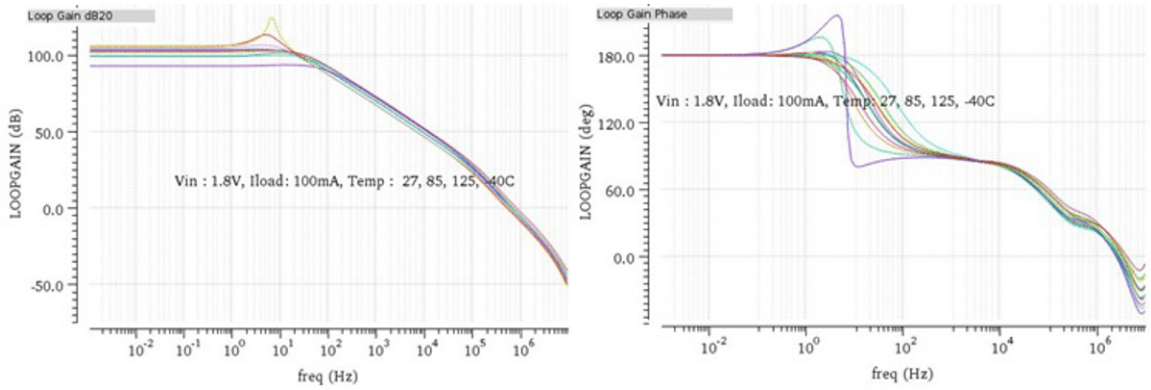

Figure 3-1. Simulated Bode Plot (Vin=1.8 V, Vo=1.2 V, Iout=100 mA)

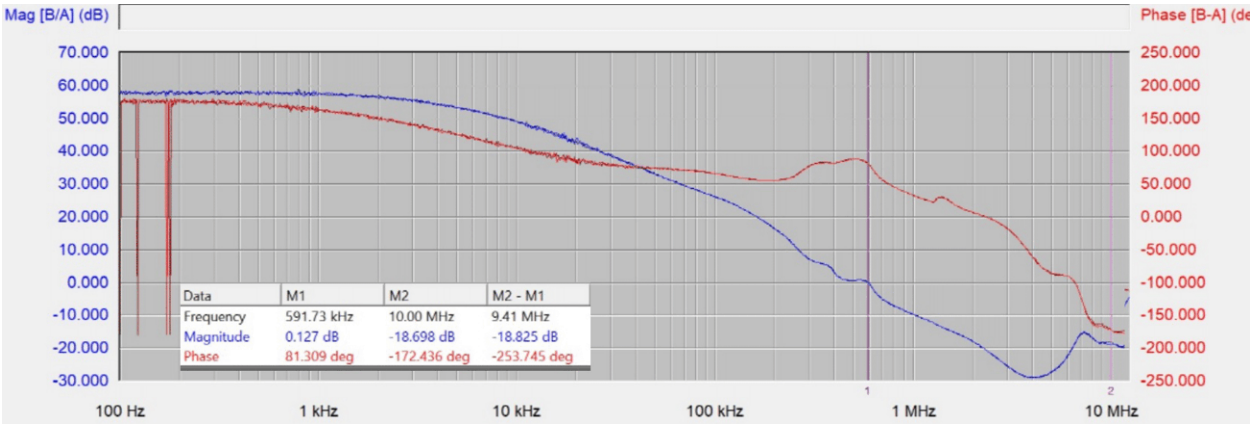

Figure 3-2. Evaluated Bode Plot on EVM (Vin=1.8 V, Vo=1.2 V, Iout=100 mA)

3.2 Transient Response in Time Domain

Figure 3-3 shows that added CFF can improve the load transient performance. The amount of ripple tells the improvement. Test condition has a transient of 10 mA to 1.0 A and A/us slew rate. It can be left for further tune by users.

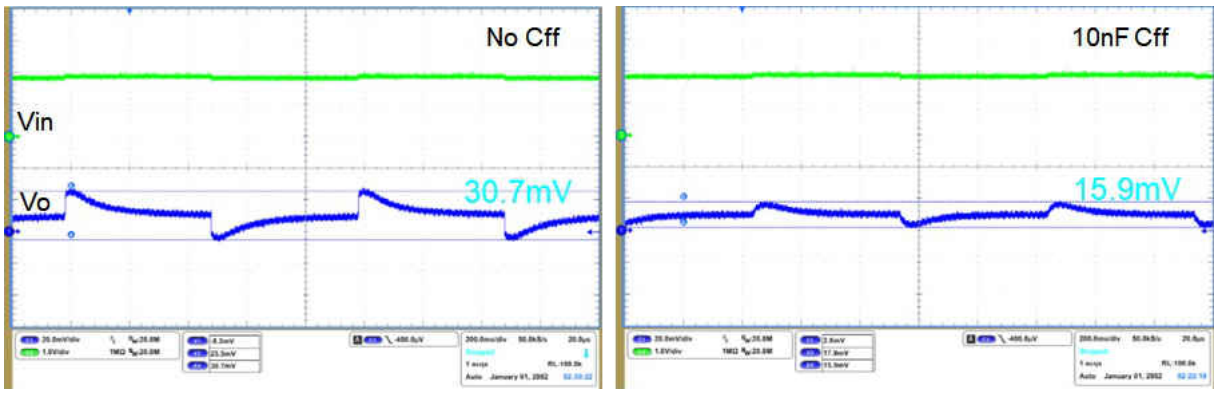

Figure 3-3. Load Transient Performance Comparison

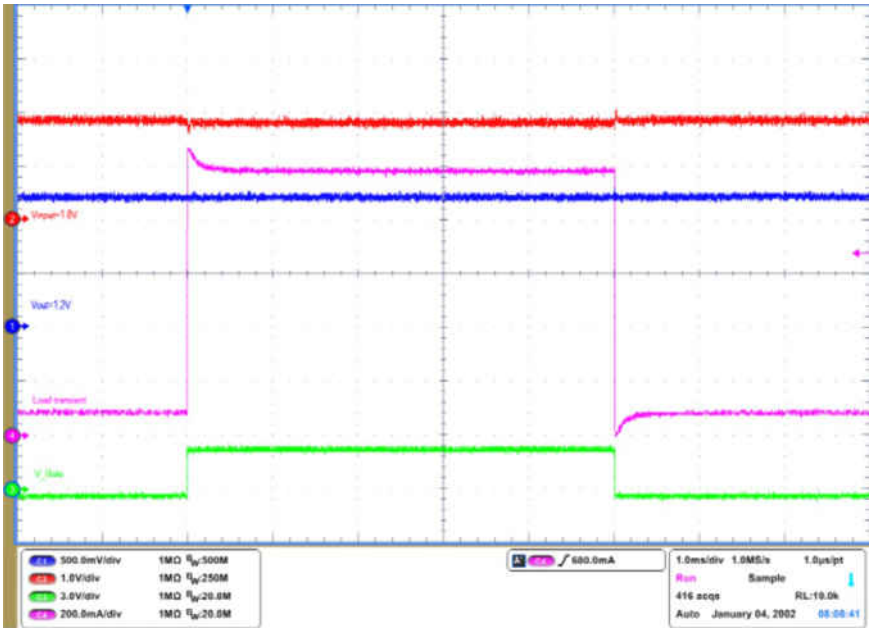

Figure 3-4. Transient Response of Modified Vout=1.2 V (with 10 nF C_{ff})

4 Summary

TPS7A14xx features a fixed Vout but can support external resistor divider to provide a flexibility for adjustable Vout. This application note addresses its feasibility and design considerations to check. Stability can be improved by adding loop compensation, simply by feedforward capacitor. It is known as providing reducing output noise and better PSRR as well.

5 References

- Texas Instruments, *Stability Analysis of Low-dropout Linear Regulators with a PMOS Pass Element*, technical article.
- Texas Instruments, *AN-1148 Linear Regulators Theory of operation and Compensation,* application note.
- Texas Instruments, *AN-1482 LDO Regulator Stability using Ceramic Output Capacitors*, application note.
- Texa Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, application note.
- Texas Instruments, *TPS7A14 1-A, Low V_{IN}, Low V_{OUT}, Ultra-Low Dropout Regulator*, data sheet.

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