Application Report
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LDO Performance Near Dropout

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ABSTRACT

This application report explains how the performance of a PMOS low-dropout (LDO) regulator changes when the input-to-output voltage decreases to approach the dropout voltage. Specifically, the effect on several key electrical characteristics is examed: line and load regulation, power-supply rejection ratio (PSRR), control loop stability and transient response, and quiescent current. These performance changes can be generalized across all other linear regulators based on both NMOS and bipolar pass transistor architectures.

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1 Introduction

Figure 1 shows the simplified block diagram for a typical LDO regulator and its related external circuitry. The LDO circuit functions as a control loop to provide a dc regulated voltage, V_{OUT}, at the load (R_{Load}) by controlling current through the pass FET. Loop gain is the product of three factors: the voltage divider gain [$\beta = R_2 / (R_1 + R_2)$]; the gain of the Error Amplifier (G_A); and the voltage gain of the common-source FET amplifier ($G_F = g_m \cdot [r_O \,||\, (R_1 + R_2) \,||Z_O]$), where g_m is the transconductance gain of the FET.

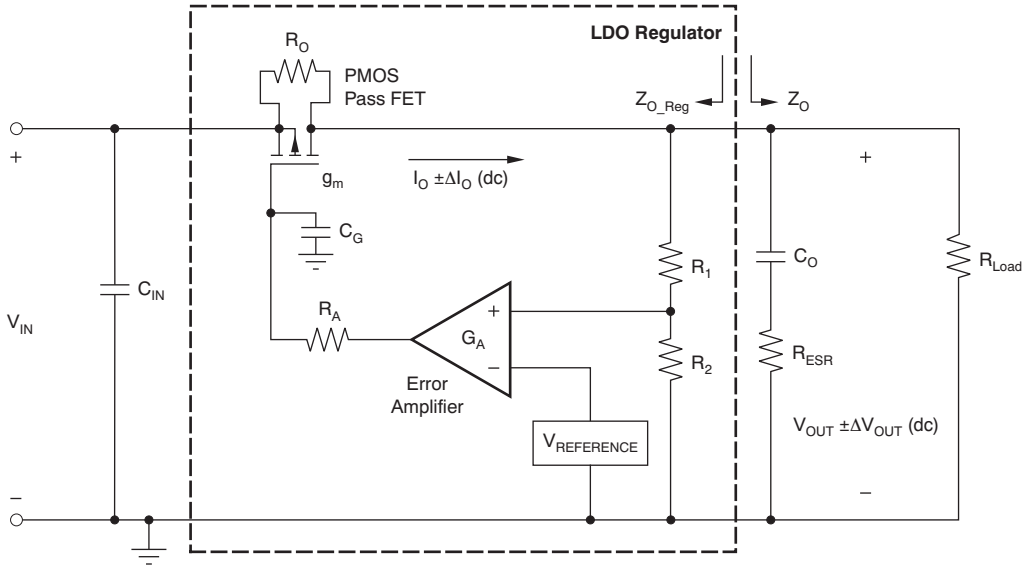
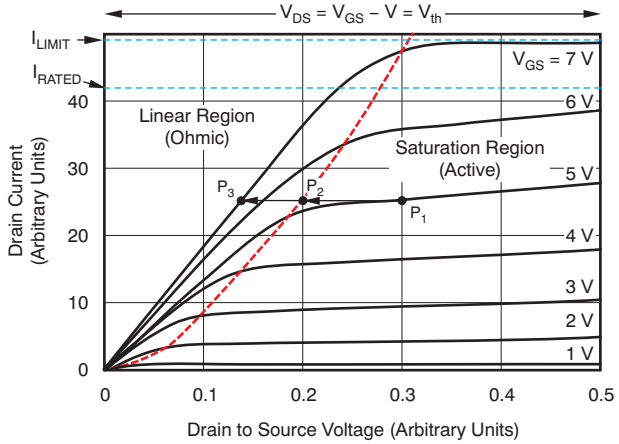


Figure 1. Basic LDO Circuit Diagram

The ability of the control loop to achieve characteristic specifications is a function of the designed loop bandwidth, loop gain, the accuracy of the reference voltage, and most significantly, the region of operation of the pass FET: that is, the *saturation region* or the linear region approaching dropout (V_{DO}). Operation of the LDO with the FET biased in the active saturation region affords optimal ac performance of the loop while operation in the linear (ohmic) region, near dropout, yields poorer performance, albeit better efficiency.

See Figure 2 for a depiction of a set of characteristic curves for a MOSFET; these performance curves are essentially the same as those for the pass FET of the LDO. As the drain-source voltage decreases from operating point P1, the pass FET transitions from its saturation region through its linear region, beginning at P2, to finally reach the dropout voltage (V_{DO}) at P3 where the FET acts only as a linear, drain-source resistance. In the saturation region (on the right-hand side of the red dashed line), the voltage gain of a FET amplifier is at its maximum as a result of both the high transconductance gain ($g_m = \Delta I_{DS}/\Delta V_{GS}$, shown here as an increasing function of drain-source current) and the high output impedance, r_O, illustrated by the flat, similarly-sloped curves. In the linear region (to the left of the red dashed line), the physics of the transistor change: the FET changes from a transconductance gain stage to something similar to a voltage-controlled resistor stage. This effect is illustrated by the narrower spacing between curves, indicative of very low transconductance, and the wider variations in slope that indicate multiple resistances. For an LDO with its pass FET at dropout, then, its input-output resistance, r_O, is at minimum; the gate-source drive voltage is at maximum limit; and the LDO ceases to regulate the output ($V_{OUT} = V_{IN} – I_O \cdot R_{DSon}$, where $R_{DSon} = r_O$ at minimum).



Note: The figure illustrates the relative dependence of the drain-source current, I_{DS}, on the gate-source voltage, V_{GS}, and drain-source voltage, V_{DS}.

Figure 2. Typical Pass FET Characteristic Curves

2 DC Load and Line Regulation Near Dropout

The dc, or low-frequency, model for an LDO can be understood from Figure 1, but with all reactive or capacitive components removed. This reduction greatly simplifies our analysis. This section discusses the effect of load and line regulation near dropout on several key electrical characteristics.

2.1 DC Load Regulation

Load regulation expresses the degree to which the regulated output voltage changes after a change to the load current occurs. When the dc load changes from I_{OUT} to $I_{OUT} \pm \Delta I_{OUT}$, the nominal output voltage then changes by some ΔV_{OUT} value, depending on the dc loop gain alone as shown by Equation 1 (Ref.1).

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{1}{g_m G_A \beta} \tag{1}$$

The larger the product of the tranconductance gain, the error amplifier gain, and the voltage divider gain, the smaller the output error (ΔV_{OUT}) will be for a given change in I_{OUT}. As the input-output voltage decreases toward dropout, the g_m decreases as the pass FET nears the linear region. Conversely, this decrease tends to increase the output error, ΔV_{OUT}. For the well-designed LDO, the gain of the error amplifier, G_A, is sufficiently large to ensure regulation (usually by a wide margin) until the drain-source voltage is very near to the dropout voltage. At dropout, the gate drive reaches its operational limit and the LDO stops regulating; the output voltage decreases with the input voltage minus the resistive voltage drop across the pass FET.

2.2 DC Line Regulation

Line regulation expresses the degree to which the regulated output voltage is influenced by a change to the input voltage, V_{IN}. When the dc input line voltage changes to $V_{IN} \pm \Delta V_{IN}$, then V_{OUT} again changes by some ΔV_{OUT} value as Equation 2 shows (Ref.1).

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{1}{[(r_O + R_{Load}) g_m G_A \beta]} \tag{2}$$

As the LDO approaches dropout, both the transconductance gain (g_m) and the output impedance of the pass FET (r_O) decrease, causing the ΔV_{OUT} error to increase. For the typical LDO, the overall loop gain allows the output to stay within specified regulation limits up to the point of dropout.

2.3 Power-Supply Rejection Ratio

The *power-supply rejection ratio* (PSRR) is the ability of the LDO control loop to reject input ripple (for example, 1 Hz to 10 MHz) on the V_{IN} rail by maintaining the output (V_{OUT}) in a ripple-free state. The PSRR function of the loop can be approximated at lower frequencies by modeling the LDO in isolation from its output impedance as a voltage divider circuit (Ref. 3). This characteristic is seen in Figure 3 as the impedance from input to output (r_O) and then the impedance of the regulated output to ground, Z_{O_Reg}. The PSRR has been derived in Equation 3 for the model shown in Figure 3 (Ref. 2). The loop gain is bandwidth-limited by the intenal pole, P_a, caused by R_A and C_G (refer to Figure 1) of the LDO, where $P_a = 1/2\pi R_A C_A$).

$$PSR = \frac{(Z_{O\_Reg})}{(r_O + Z_{O\_Reg})} \cdot \frac{(1 + \frac{s}{P_a})}{[G_A g_m \beta (1 + \frac{s}{P_a G_A g_m \beta})]} \quad (3)$$

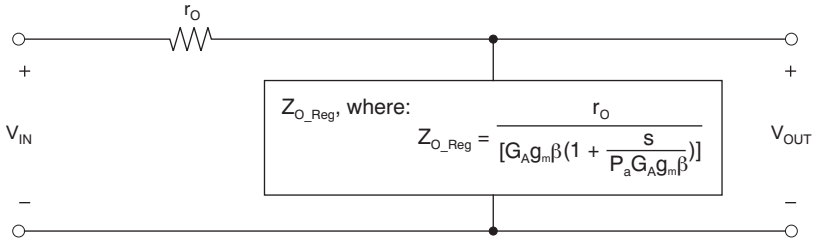
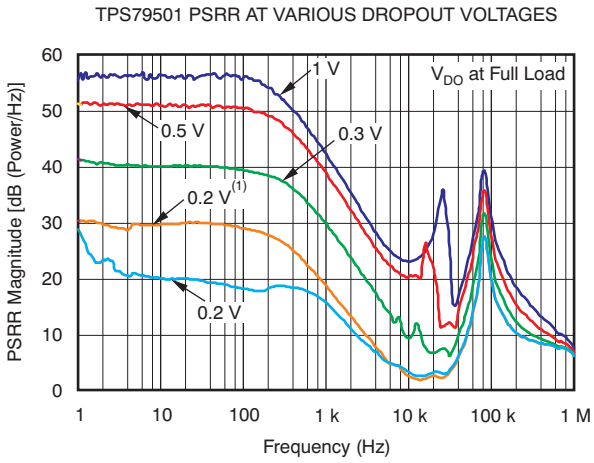


Figure 3. Low-Frequency PSRR Model (Output Impedance Ignored)

According to this model, PSRR is entirely a function of the loop gain and the one internal pole, P_a.

As the input-output voltage reduces to near dropout, the PSRR decreases dramatically (logarithmically) as a result of the reduction in transconductance gain of the pass FET, the reduced effect of the gate-source voltage on the drain current, and finally the inability of the Error Amplifier to vary the drain current near dropout. Figure 4 shows a set of typical PSRR plots, in this case for a TPS79501 LDO, to illustrate the reduction in gain as the input-output voltage approaches the point of full load dropout (where V_{DO}= 110 mV). These graphs show the suggested model of Figure 3 to be valid to about 100 kHz.



(1) Source sinusoidal stimulus reduced from 93 mV to 66 mV.

Figure 4. PSRR Plots Showing the Effect of Decreasing Dropout Voltage on Loop Gain

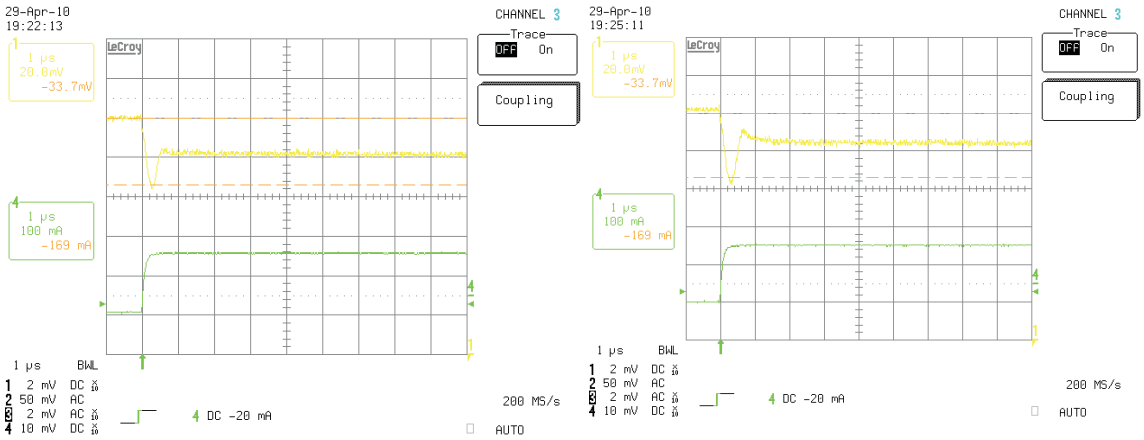
2.4 Loop Stability and Load Transient Response

The control loop for most recent LDOs consists of multiple, embedded loops with provision for small- and large-signal behavior. The basic loop model, however, will suffice here. Equation 4 gives the simplified open-loop gain equation for G_{OL}, based on the PMOS LDO of Figure 1.

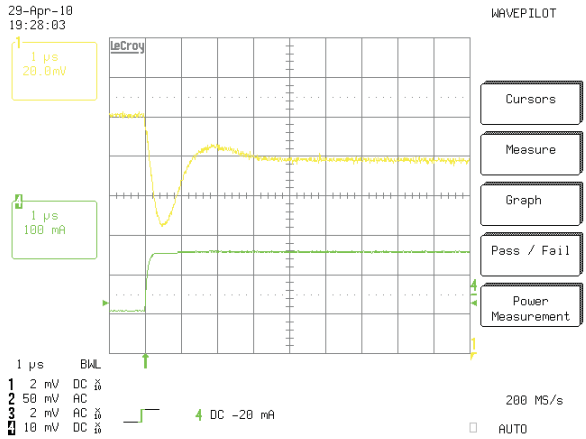
$$G_{OL}(s) = \beta \bullet G_A \bullet g_m \bullet R_p \bullet \frac{1 + sC_OR_{ESR}}{\left[(1 + sC_GR_A) \bullet [1 + sC_O(R_p + R_{ESR})]\right]} \quad (4)$$

Where $R_p = r_O \,||\, (R_1 + R_2) \,||\, R_{Load}$ and $\beta = R_2 / (R_1 + R_2)$.

Decreasing the input-output voltage to approach dropout reduces the loop gain and bandwidth, and shifts the frequency of the output pole [$F_{P\_OUT} = 1/2\pi C_O(R_p + R_{ESR})$]. Though it is beyond the scope of this report, it can be shown by Figure 1 that typically, a reduction in gain improves stability (that is, phase margin will increase) while significantly slowing or worsening the step load transient response as the bandwidth narrows. Figure 5 illustrates this change in step response by employing the TPS71728 LDO to drive a step load from 45 mA to 150 mA for three cases where the input-output voltage is decreased toward the dropout voltage.



(a) Input-Output Voltage = 1 V **(b)** Input-Output Voltage = 0.5 V



(c) Input-Output Voltage = 0.2 V

Note: Oscilloscope channel 4 shows the load current step, and channel 1 shows the V_{OUT} transient response.

Figure 5. TPS71728 Step Load Transient and Output Response

2.5 Quiescent Current

As the input-output voltage decreases to near dropout, the drive voltage to the gate of the pass FET and various other circuits is driven to their operating limits. At dropout, when all these internal circuits are then saturated, there is often a large rise in quiescent current. Some higher-end regulators, however, use balanced, differential drive circuitry that always draws the same current whether the device is operating at drive limits or not.

3 Conclusion

PMOS LDO performance is optimal when the input-to-output voltage difference is great enough to assure that the FET is operating in its saturation region. The transition between the saturation region and the linear region of FET operation is not abrupt. As the input-to-output voltage reduces to approach dropout (V_{DO}), the transconductance gain of the FET rolls off, the output impedance of the FET decreases, and the gate-source drive reaches practical limitations to effectively reduce or altogether limit LDO performance.

4 References

Unless otherwise noted, these documents are available for download from the TI website (www.ti.com).

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2. Gupta, V., Rincón-Mora, G.A., and P. Raha. (2004). Analysis and design of monolithic, high PSR, linear regulators for SoC applications. Downloaded from http://users.ece.gatech.edu/rincon-mora/publicat/journals/socc04_psr.pdf
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