



## ABSTRACT

This report presents the reliability and qualification results for the OPA4H014-SEP radiation tolerant 11-MHz, precision, low-noise, RRO, JFET amplifier. The OPA4H014-SEP is manufactured with a controlled baseline and has the following:

- An extended product life cycle
  - One assembly and test site
  - Product traceability
  - Extended product-change notification
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## Trademarks

All trademarks are the property of their respective owners.

## 1 Device Information

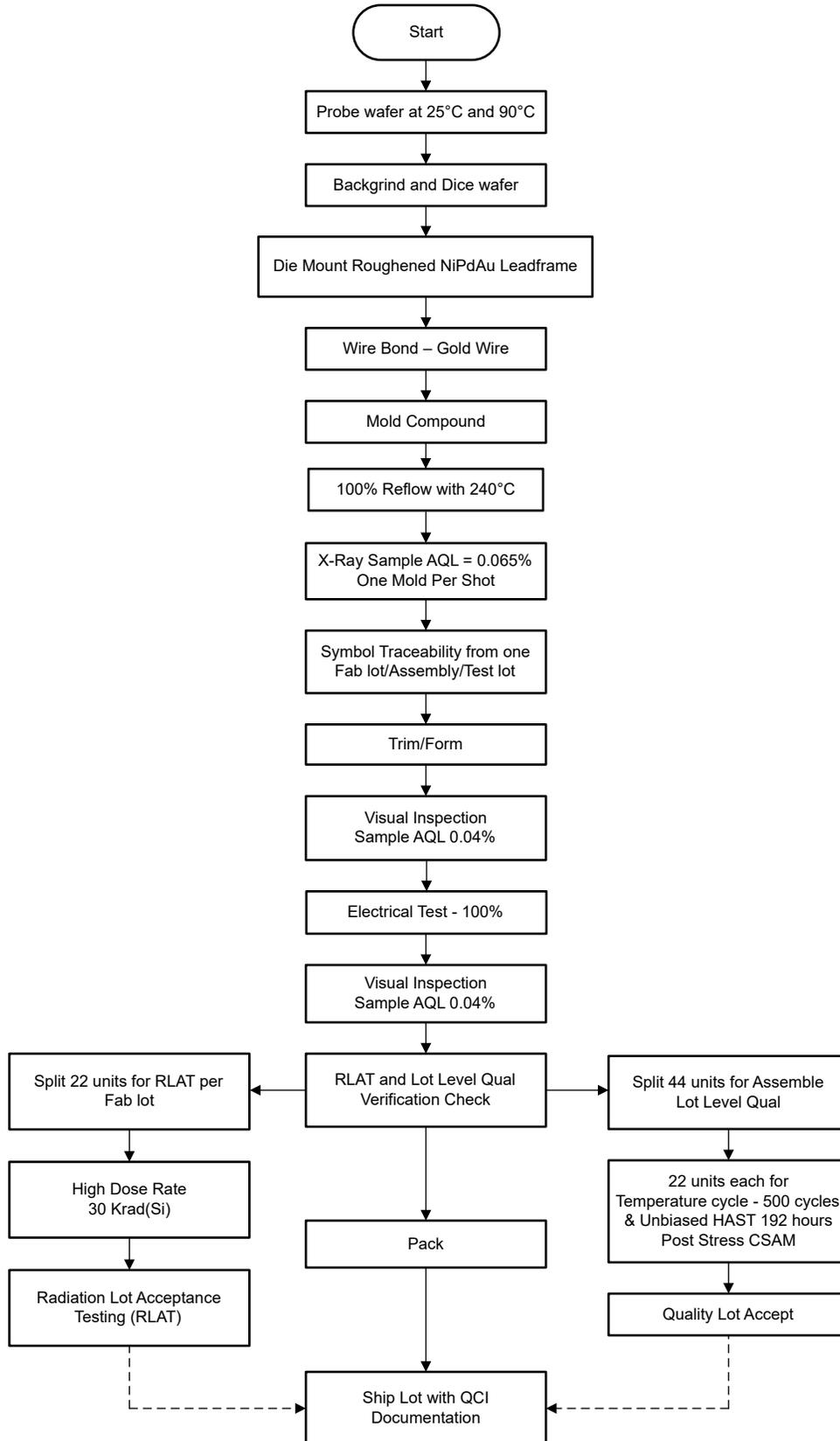
The OPA4H014-SEP is a low-power JFET input operational amplifier (op amp) that features good drift and low input bias current. With an input range that includes  $V^-$  and a rail-to-rail output, designers can take advantage of the low-noise characteristics of JFET amplifiers while interfacing to single-supply, precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The OPA4H014-SEP achieves 11-MHz unity-gain bandwidth and 20-V /  $\mu$ s slew rate, while consuming only 1.8 mA (typical) of quiescent current per amplifier. This device runs on a single 4.5-V to 18-V supply or dual  $\pm 2.25$ -V to  $\pm 9$ -V supplies.

The op amp is built in a plastic, 14-pin, TSSOP package with radiation hardness up to 43 MeV  $\times$  cm<sup>2</sup> / mg (SEE) and is ELDRS-free up to 30 krad(Si). Radiation lot acceptance testing (RLAT) for the LMP7704-SP is performed with high dose rate. Condition A as specified in MIL-STD-883, Method 1019. The radiation end point limits for the specified parameters are maintained only for the conditions as specified in MIL-STD-883, Method 1019, Condition A, to a maximum total dose of 30 krad(Si).

## **2 Texas Instruments Enhanced Product Qualification and Reliability Report**

TI qualification testing is a risk mitigation process that is engineered to assure device longevity in customer applications. Wafer fabrication process and package level reliability are evaluated in a variety of ways that may include accelerated environmental test conditions with subsequent derating to actual use conditions. Manufacturability of the device is evaluated to verify a robust assembly flow and assure continuity of supply to customers, TI Enhanced Products are qualified with industry standard test methodologies performed to the intent of Joint Electron Devices Engineering Council (JEDEC) standards and procedures. Texas Instruments Enhanced Products are certified to meet GEIA-STD-0002-1 [Aerospace Qualified Electronic Components](#).

### 3 Space Enhanced Plastic Production Flow



**Figure 3-1. Space Enhanced Plastic Production Flow**

## 4 Qualification by Similarity (Qualification Family)

A new device can be qualified either by performing full scale quality and reliability test on the actual device or using previously qualified device(s) through "Qualification by Similarity" (QBS) rules. By establishing similarity between the new device and those qualified previously, repetitive test will be eliminated, allowing for timely production release. When adopting QBS methodology, the emphasis is on qualifying the differences between a previously qualified product and the new product under consideration. The QBS rules for a technology, product, test parameter or package shall define which attributes are required to remain fixed in order for the QBS rules to apply. The attributes which are expected and allowed to vary will be reviewed and a QBS plan shall be developed, based on the reliability impact assessment above, specifying what subset of the full complement of environmental stresses is required to evaluate the reliability impact of those variations. Each new device shall be reviewed for the conformance to the QBS rule sets applicable to the device. See JEDEC JESD47 for more information.

**Table 4-1. Device Baseline** <sup>1</sup>

TI Device	OPA4H014-SEP	Assembly Site	TI Malaysia
DLA VID:	V62/21607	Test Site:	TI Malaysia
Wafer Fab:	TI FFAB	Pin/Package Type:	TSSOP (PW)  14
Fab Process:	BICOM-3XHV	Leadframe:	Cu
Fab Technology:	BICMOS	Termination Finish:	NiPdAu
Die Revision:	C	Bond Wire:	24.4 μm Au
ESD CDM:	±500 V	Moisture Sensitivity:	MSL 2 / 260°C
ESD HBM:	±2000 V		

1. Baseline information in effect as of the date of this report.

**Table 4-2. Space Enhanced Products New Device Qualification Matrix <sup>1</sup>**

Description	Condition	Sample Size Used and Rejects	Lots Required	Test Method
Electromigration	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules
Wire Bond Life	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules
Electrical Characterization	TI Data Sheet	10	3	N/A
Electrostatic Discharge Sensitivity	HBM	3 units/voltage	1	EIA/JESD22-A114
	CDM			EIA/JESD22-C101
Latch-up	Per Technology	3/0	1	EIA/JESD78
Physical Dimensions	TI Data Sheet	5/0	1	EIA/JESD22- B100
Thermal Impedance	Theta-JA on board	Per Pin-Package	N/A	EIA/JESD51
Bias Life Test	125°C / 1000 hours or equivalent	77/0	3	JESD22-A108 <sup>(2)</sup>
Biased HAST	130°C / 85% / 96 hours	77/0	3	JESD22-A110 <sup>2</sup>
Extended Biased HAST	130°C / 85% / 250 hours (for reference)	77/0	1	JESD22-A110 <sup>2</sup>
Unbiased HAST	130°C / 85% / 96 hours	77/0	3	JESD22-A110 <sup>2</sup>
Temperature Cycle	-65°C to +150°C non-biased for 500 cycles	77/0	3	JESD22-A104 <sup>2</sup>
Solder Heat	260°C for 10 seconds	22/0	1	JESD22-B106
Resistance to Solvents	Ink symbol only	12/0	1	JESD22-B107
Solderability	Condition A (steam age for 8 hours)	22/0	1	ANSI/J-STD-002-92
Flammability	Method A / Method B	5/0	1	UL-1964
Bond Shear	Per wire size	5 units × 30/0 bonds	3	JESD22-B116
Bond Pull Strength	Per wire size	5 units × 30/0 bonds	3	ASTM F-459
Die Shear	Per die size	5/0	3	TM 2019
High Temp Storage	150 °C / 1,000 hours	15/0	3	JESD22-A103-A <sup>2</sup>
Moisture Sensitivity	Surface Mount Only	12	1	J-STD-020-A <sup>2</sup>
Radiation Response Characterization	Total Ionization Dose, and Single-Event Latchup	5 units/dose level	1	MIL-STD-883/Method 1019
Outgassing Characterization	TML (Total Mass Lost), CVCM (Collected Volatile Condensable material), WVR (Water vapor recorded)	5	1	ASTM E595

- Note that qualification by similarity (“qualification family”) per JEDEC JESD47 is allowed.
- Precondition performed per JEDEC Std. 22, Method A112/A113.

## 5 Outgas Test Report

Outgassing testing was performed on leadless units at Pacific Testing Laboratories in Valencia, California. 35 devices were submitted with leads removed, of which a total sample mass of approximately 1 g was used ( $n \geq 15$ ). A total mass loss (TML) of 1.00% and collected volatile condensable material (CVCM) of 0.10% were used as screening levels for rejection of spacecraft materials. The outgas test was performed in a vacuum environment of less than  $5 \times 10^{-5}$  torr according to ASTM E 595, for a duration of 24 hours, at 125°C. The TML, CVCM, and the amount of Water Vapor Recovered (WVR) were measured after the test.

**Table 5-1. Outgas Test Results**

Sample	TML (%)	CVCM (%)	WVR (%)
OPA4H014-SEP	0.09	0.03	0.04

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