

Application Brief

Understanding the SPI Bus



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The Serial Peripheral Interface (SPI) bus is a widely used synchronous communication protocol that enables high-speed, full-duplex data transfer between a controller device and one or more peripheral devices. SPI was developed by Motorola in the 1980s and has since become a standard interface for connecting peripherals in embedded systems. Its simplicity, versatility, and efficiency make it an essential tool for engineers designing systems that require reliable and fast communication. Figure 1 illustrates the typical diagram of SPI connections on the bus.

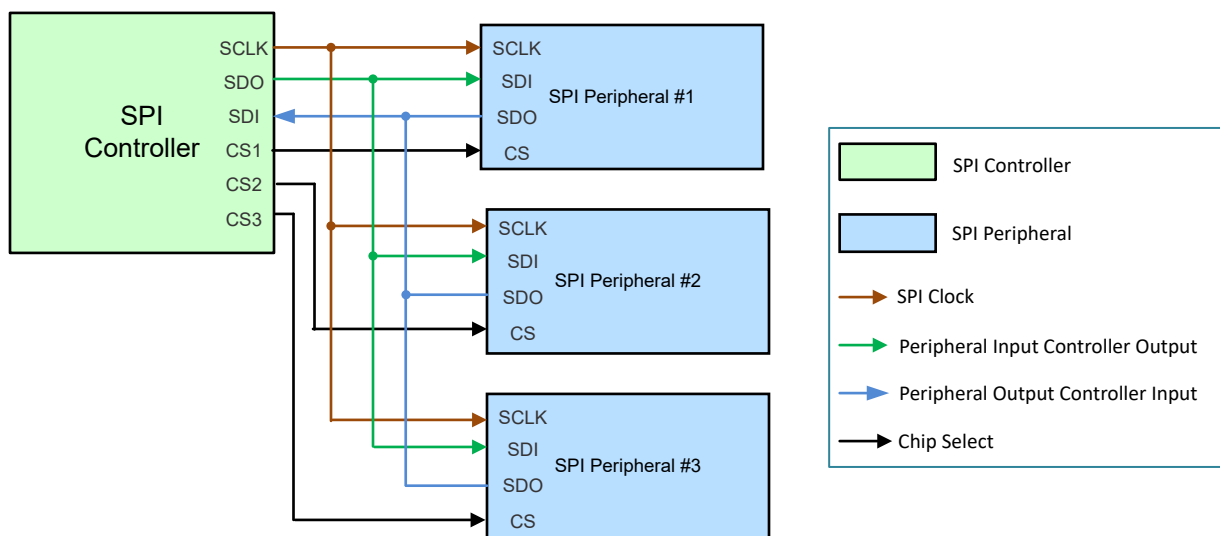


Figure 1. Example SPI Bus

The SPI communication is synchronized using a shared clock signal, ensuring precise data transfer timing. Unlike other serial protocols such as inter-integrated circuit (I2C), serial peripheral interface (SPI) does not define a standard communication format, allowing developers to tailor the protocol to specific application requirements. Table 1 shows the difference of SPI, I2C and universal asynchronous receiver/transmitter (UART).

Table 1. Comparison With Other Protocols

Feature	SPI	I2C	UART
Communication Type	Synchronous	Synchronous	Asynchronous
Data Transfer Mode	Full-Duplex	Half-Duplex	Full-Duplex
Clock Signal	Yes	Yes	No
Addressing	Chip-Select (CS) Line	Addressing Protocol	Not Applicable
Speed	High	Medium	Low

SPI Basics

SPI enables full-duplex communication, meaning data can be sent and received simultaneously. The protocol uses a set of primary signals to establish communication, which can vary based on the SPI configuration.

Table 2. SPI Bus Signals

Signal Name	Usage
PICO (Controller SDO, Peripheral SDI)	Send data from the controller to the peripheral
POCI (Controller SDI, Peripheral SDO)	Send data from the peripheral to the controller
SCLK (Serial Clock)	Generated by the controller to synchronize data transfer
CS (Chip Select)	An active-low signal used by the controller to select and enable a specific peripheral device

SPI Bus Architecture

The architecture of the SPI bus is straightforward, consisting of one **controller** and one or more **peripheral** devices. The controller initiates communication, controls the clock, and selects the peripheral to communicate with. The architecture supports three main configurations:

- **Single Controller, Single Peripheral:**
 - Simplest setup, where the controller communicates with only one peripheral device.
 - Requires four lines (PICO, POCI, SCLK, and CS).
- **Single Controller, Multiple Peripherals (Independent Chip Select):**
 - Each peripheral has a dedicated chip-select (CS) line.
 - The controller activates the CS line for the intended peripheral device while others remain inactive.
- **Daisy Chain Configuration:**
 - Peripherals are connected in series, with the output of one device feeding into the input of the next.
 - Reduces the number of required CS lines, as only one is needed for the entire chain.
 - Data is shifted through all devices in the chain during each clock cycle.
- **3-Wire SPI Configuration:**
 - Combines the PICO and POCI lines into a single bi-directional data line, often called **Data Input/Output (DIO)**.
 - This configuration reduces the number of wires to three: SCLK, CS, and DIO.

Data Transfer Modes

SPI supports four modes of operation, determined by the clock polarity (CPOL) and clock phase (CPHA). These modes shown in [Table 3](#) define the behavior of the clock signal and the timing of data sampling.

Table 3. SPI Data Transfer Modes

Mode	CPOL	CPHA	Description
Mode 0	0	0	Data is sampled on the rising edge of the clock, and the clock idles low.
Mode 1	0	1	Data is sampled on the falling edge of the clock, and the clock idles low.
Mode 2	1	0	Data is sampled on the falling edge of the clock, and the clock idles high.
Mode 3	1	1	Data is sampled on the rising edge of the clock, and the clock idles high.

SPI Data Transmission

As SPI is a synchronous full-duplex communication protocol that allows data exchange between a controller and one or more peripheral devices. TI's TXE8116/24 device uses a fixed 24-bit SPI transaction format, transmitted MSB first, in SPI mode 0 (CPOL = 0, CPHA = 0). The device supports full-duplex operation, where incoming command frames and outgoing data or status frames are exchanged simultaneously. Each SPI transaction must begin with the CS signal pulled low, and remain low for the entire 24-bit sequence. Figure 2 illustrates the SPI data frame in TXE8116/24 device.

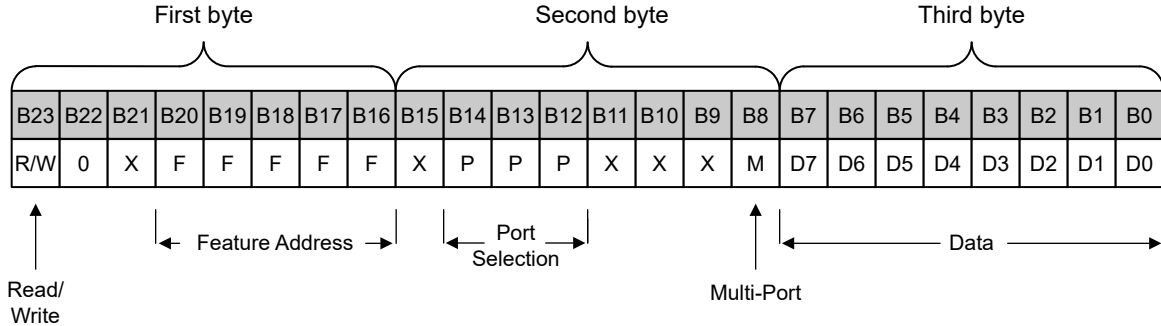


Figure 2. TXE8116/24 SPI Data Frame

Writing to a Peripheral

To write to a register, the controller transmits a 24-bit word with the MSB (bit 23) set to 0. The register address is encoded in bits [22:16], and bits [15:8] select the target GPIO port or configure multi-port mode. The final 8 bits [7:0] carry the actual data to be written.

- **Example: Configure Port 0 as Output**
 - Register Address: 0x04 (Direction Register)
 - Port Select: 0x00 (Port 0)
 - Data: 0xFF (All pins as output)
- **PICO:**
 - Bit [23] R/W = 0 (Write)
 - Bit [22:16] Address = 0x04
 - Bit [15:8] Port = 0x00
 - Bit [7:0] Data = 0xFF
- **Final Frame = 0x0400FF**
- **POCI Response:**
 - Bit [23:22] = 0x3 (Indicating it's a status segment)
 - Bit [21:16]: the Fault Status register
 - Bit [15:8]: all 0
 - Bit [7:0]: the previous register data

Reading From a Peripheral

To read from a register, the host sets bit 23 to 1 and transmits the desired register address. The lower 16 bits can contain dummy data. During this same transfer, the TXE8124 returns the current value of the addressed register on the POCI line.

- **Example: Read GPIO Input Status from Port 1**
 - Register Address: 0x02 (Input Port Register)
 - Port Select: 0x01 (Port 1)
 - Data: 0x00 (Dummy)
- **PICO:**
 - Bit [23] R/W = 1 (Read)
 - Bit [22:16] Address = 0x02
 - Bit [15:8] Port = 0x01
 - Bit [7:0] Dummy = 0x00

- **Final Frame = 0x820100**
- **POCI Response:**
 - Bit [23:22] = 0x3 (Indicating it's a status segment)
 - Bit [21:16]: the Fault Status register
 - Bit [15:8]: all 0
 - Bit [7:0]: the read data

Key Timing Requirements in TXE8116/24

Parameter	Description	Typical Value
t_{SCLK}	SPI clock period (3.3V < VCC < 5.5V)	100ns (10MHz)
t_{CSS} / t_{CSH}	CS setup/hold time	≥ 50 ns
$t_{V(SDO)}$	POCI valid after SCLK edge	≤ 27 ns
$t_{DIS(SDO)}$	POCI high-Z after CS deasserted	≤ 50 ns

All SPI transactions must meet minimum timing constraints as specified in the [TXE81xx-Q1 Automotive 24-Bit SPI Bus I/O Expander with Interrupt Output, Reset Input, and I/O Configuration Registers Data Sheet](#) to maintain correct communication.

Notes

- All transactions are full-duplex; each SPI clock transfers one bit on both PICO and POCI.
- Data is captured on the rising edge of SCLK and driven on the falling edge.
- Always make sure CS is held low for the duration of the 24-bit frame; toggling CS mid-frame can corrupt the transaction.
- Multi-port addressing is possible via specific port bits in [15:8].

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