Functional Safety Information

TLV900x-Q1 Functional Safety FIT Rate, FMD, and Pin FMA

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1 Overview

This document contains information for TLV9002-Q1 (SOIC (8) and VSSOP (8) packages) and TLV9004-Q1 (SOIC (14) and SOT-23 (14) packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

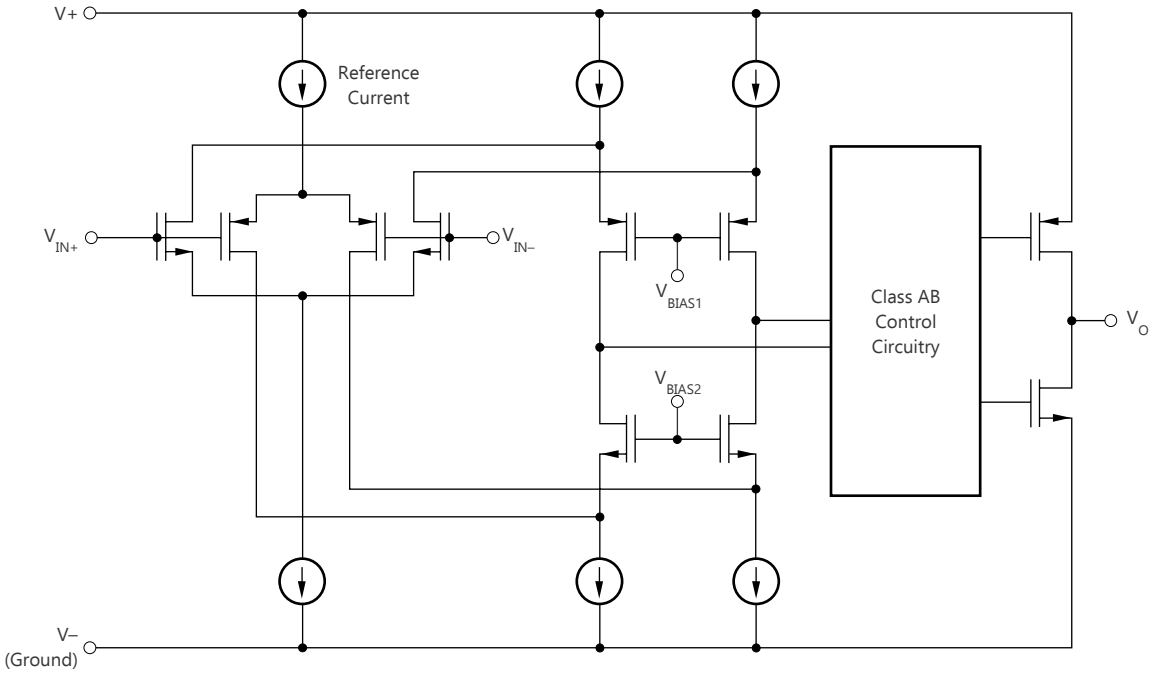

Figure 1-1. Functional Block Diagram

TLV9002-Q1 and TLV9004-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC (8) Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOIC (8) package of TLV9002-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	11
Die FIT Rate	3
Package FIT Rate	8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VSSOP (8) Package

This section provides Functional Safety Failure In Time (FIT) rates for the VSSOP (8) package of TLV9002-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 SOIC (14) Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOIC (14) package of TLV9004-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	18
Die FIT Rate	3
Package FIT Rate	15

The failure rate and mission profile information in Table 2-5 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.4 SOT-23 (14) Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOT-23 (14) package of TLV9004-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-7. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 2-5 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-8. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLV9004-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Out open (HIZ)	20%
Out saturate high	25%
Out saturate low	25%
Out functional not in specification voltage or timing	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLV9002-Q1 (SOIC (8) and VSSOP (8) packages) and TLV9004-Q1 (SOIC (14) and SOT-23 (14) package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to (V-) (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-9)
- Pin short-circuited to (V+) (see Table 4-5 and Table 4-8)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 SOIC (8) and VSSOP (8) Packages

Figure 4-1 shows the TLV9002-Q1 pin diagram for the SOIC (8) and VSSOP (8) packages. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TLV9002-Q1 data sheet.

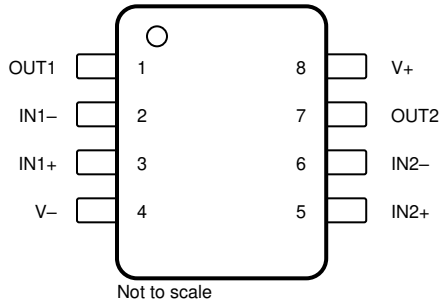

Figure 4-1. Pin Diagram (SOIC (8) and VSSOP (8) Packages)

Table 4-2. Pin FMA for Device Pins Short-Circuited to (V-) Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause overheating.	B
IN1-	2	Input at V- is valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V- is valid input, however, desired application result is unlikely.	C
(V-)	4	Normal operation.	D
IN2+	5	Input at V- is valid input, however, desired application result is unlikely.	C
IN2-	6	Input at V- is valid input, however, desired application result is unlikely.	C
OUT2	7	May cause overheating due to output short circuit current.	B
(V+)	8	Diodes from input to V+ may turn due to input signal and cause EOS.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output can't be used by application.	C
IN1-	2	Floating input, circuit will likely not function as expected.	C
IN1+	3	Floating input, circuit will likely not function as expected.	C
(V-)	4	Lowest voltage pin will try to power internal ground via ESD diode to ground.	B
IN2+	5	Floating input, circuit will likely not function as expected.	C
IN2-	6	Floating input, circuit will likely not function as expected.	C
OUT2	7	Output can't be used by application.	C
(V+)	8	Highest voltage pin will try to power internal ground via ESD diode to VCC.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	IN1-	Negative feedback, creates unity gain buffer.	C
IN1-	2	IN1+	No damage to device, application circuit won't work.	C
IN1+	3	(V-)	Input at V- is valid input, however, desired application result is unlikely.	C
(V-)	4	IN2+	Input at V- is valid input, however, desired application result is unlikely.	C
IN2+	5	IN2-	No damage to device, application circuit won't work.	C
IN2-	6	OUT2	Negative feedback, creates unity gain buffer.	C
OUT2	7	(V+)	May cause overheating.	B
(V+)	8	OUT1	May cause overheating.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to (V+)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause overheating.	B
IN1-	2	Input at V+ is valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V+ is valid input, however, desired application result is unlikely.	C
(V-)	4	Diodes from input to V- may turn due to input signal and cause EOS.	B
IN2+	5	Input at V+ is valid input, however, desired application result is unlikely.	C
IN2-	6	Input at V+ is valid input, however, desired application result is unlikely.	C
OUT2	7	May cause overheating.	B
(V+)	8	Diodes from input to V+ may turn due to input signal and cause EOS.	D

4.2 SOT-23 (14) and SOIC (14) Packages

Figure 4-2 shows the TLV9004-Q1 pin diagram for the SOT-23 (14) and SOIC (14) packages. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TLV9004-Q1 data sheet.

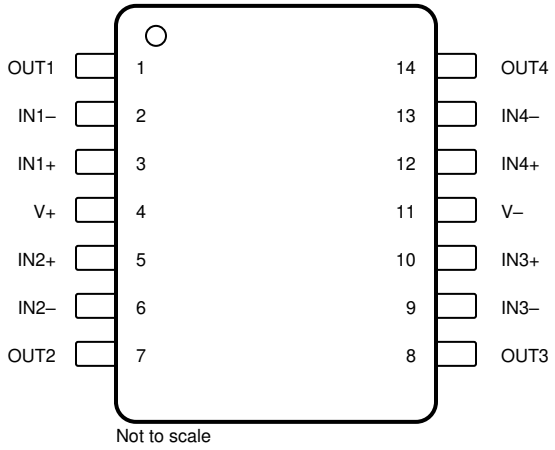

Figure 4-2. Pin Diagram (SOT-23 (14) and SOIC (14) Packages)

Table 4-6. Pin FMA for Device Pins Short-Circuited to (V-)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause overheating.	B
IN1-	2	Input at V- is valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V- is valid input, however, desired application result is unlikely.	C
(V+)	4	Diodes from input to V+ may turn due to input signal and cause EOS.	B
IN2+	5	Input at V- is valid input, however, desired application result is unlikely.	C
IN2-	6	Input at V- is valid input, however, desired application result is unlikely.	C
OUT2	7	May cause overheating.	B
OUT3	8	May cause overheating.	B
IN3-	9	Input at V- is valid input, however, desired application result is unlikely.	C
IN3+	10	Input at V- is valid input, however, desired application result is unlikely.	C
(V-)	11	Normal operation.	D
IN4+	12	Input at V- is valid input, however, desired application result is unlikely.	C
IN4-	13	Input at V- is valid input, however, desired application result is unlikely.	C
OUT4	14	May cause overheating.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output can't be used by application.	C
IN1-	2	Floating input, circuit will likely not function as expected.	C
IN1+	3	Floating input, circuit will likely not function as expected.	C
(V+)	4	Highest voltage pin will try to power internal ground via ESD diode to VCC.	B
IN2+	5	Floating input, circuit will likely not function as expected.	C
IN2-	6	Floating input, circuit will likely not function as expected.	C
OUT2	7	Output can't be used by application.	C
OUT3	8	Output can't be used by application.	C
IN3-	9	Floating input, circuit will likely not function as expected.	C

Table 4-7. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN3+	10	Floating input, circuit will likely not function as expected.	C
(V-)	11	Lowest voltage pin will try to power internal ground via ESD diode to ground.	B
IN4+	12	Floating input, circuit will likely not function as expected.	C
IN4-	13	Floating input, circuit will likely not function as expected.	C
OUT4	14	Output can't be used by application.	C

Table 4-8. Pin FMA for Device Pins Short-Circuited to (V+)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause overheating.	B
IN1-	2	Input at V+ is valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V+ is valid input, however, desired application result is unlikely.	C
(V+)	4	Normal operation.	D
IN2+	5	Input at V+ is valid input, however, desired application result is unlikely.	C
IN2-	6	Input at V+ is valid input, however, desired application result is unlikely.	C
OUT2	7	May cause overheating.	B
OUT3	8	May cause overheating.	B
IN3-	9	Input at V+ is valid input, however, desired application result is unlikely.	C
IN3+	10	Input at V+ is valid input, however, desired application result is unlikely.	C
(V-)	11	Diodes from input to V- may turn due to input signal and cause EOS.	B
IN4+	12	Input at V+ is valid input, however, desired application result is unlikely.	C
IN4-	13	Input at V+ is valid input, however, desired application result is unlikely.	C
OUT4	14	May cause overheating.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	IN1-	Negative feedback, creates unity gain buffer.	C
IN1-	2	IN1+	No damage to device, application circuit won't work.	C
IN1+	3	(V+)	Input at V+ is valid input, however, desired application result is unlikely.	C
(V+)	4	IN2+	Input at V+ is valid input, however, desired application result is unlikely.	C
IN2+	5	IN2-	No damage to device, application circuit won't work.	C
IN2-	6	OUT2	Negative feedback, creates unity gain buffer.	C
OUT2	7	OUT3	May cause overheating (pins on opposite sides, not adjacent).	B
OUT3	8	IN3-	Negative feedback, creates unity gain buffer.	C
IN3-	9	IN3+	No damage to device, application circuit won't work.	C
IN3+	10	(V-)	Input at ground is valid input, however, desired application result is unlikely.	C
(V-)	11	IN4+	CH 4 output high, if other input is valid common mode range.	C
IN4+	12	IN4-	No damage to device, application circuit won't work.	C
IN4-	13	OUT4	Negative feedback, creates unity gain buffer.	C
OUT4	14	OUT1	May cause overheating (pins on opposite sides, not adjacent).	B

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