Functional Safety Information

INA19xA-Q1 Functional Safety FIT Rate and Failure Mode Distribution and Pin FMA

1 Overview

This document contains information for INA19xA-Q1 (5-pin SOT-23 package) to aid in a functional safety system design. In this report, INA19xA-Q1 refers to the family of devices including:

- INA193A-Q1
- INA194A-Q1
- INA195A-Q1
- INA196A-Q1
- INA197A-Q1
- INA198A-Q1

Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device

Figure 1-1 shows the device functional block diagram for reference.

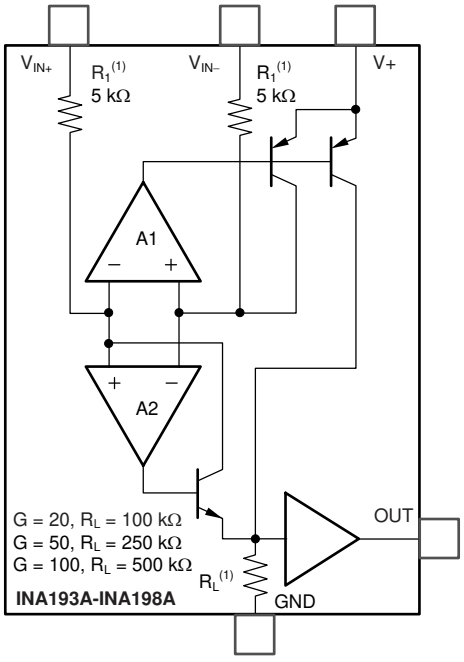

Figure 1-1. Functional Block Diagram

INA19xA-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for INA19xA-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 25 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators, Voltage Monitors	4 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA19xA-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	10%
OUT to GND	25%
OUT to V+	25%
OUT functional, not in specification	40%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA19xA-Q1 (5-pin SOT-23 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (seeTable 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pull-up resistor on $\overline{CS}$ to VDD
- RC filter on every analog input, AINx.

  Series resistors are sized to limit the input currents into the analog inputs to <10 mA in all circumstances, for example also in case device is unpowered and input signal is applied.
- Device is the only slave on the SPI bus.

4.1 INA193-Q1/INA194-Q1/INA195-Q1 5-Pin SOT-23 Package

Figure 4-1 shows the INA19xA-Q1 pin diagram for the 5-pin SOT-23 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA19xA-Q1 data sheet.

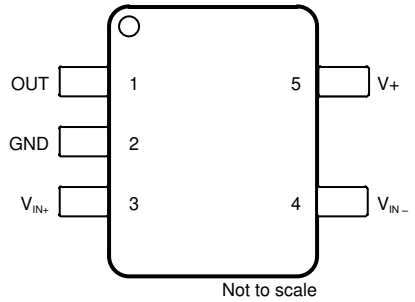

Figure 4-1. Pin Diagram (INA193-Q1/INA194-Q1/INA195-Q1 5-Pin SOT-23 Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction.	B
GND	2	Normal Operation.	D
VIN+	3	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low-side configuration, input pins are shorted.	B
VIN-	4	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low-side configuration, normal operation.	B in high-side; D in low-side
V+	5	Power supply shorted to ground.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
GND	2	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
VIN+	3	Input undefined, output will be anywhere between supply and ground.	B
VIN-	4	Input undefined, output will be anywhere between supply and ground.	B
V+	5	No power supply to device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	GND	Output will be pulled to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction	B
GND	2	VIN+	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. In low side configuration, input pins are shorted	B
VIN+	3	VIN-	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
VIN-	4	V+	In high-side configuration, high current will flow from bus supply to V+ or vice versa; in low-side configuration, V+ supply is shorted to GND.	A in high-side; B in low-side
V+	5	OUT	Output will be pulled to V+ and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self heating could cause die junction temperature to exceed 150°C.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled to V+ and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self heating could cause die junction temperature to exceed 150°C.	B
GND	2	Power supply is shorted to GND.	B
VIN+	3	In high-side configuration, device power supply shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND (through RSHUNT).	A in high-side; B in low-side
VIN-	4	In high-side configuration, device power supply shorted to bus supply (through RSHUNT), which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND.	A in high-side; B in low-side
V+	5	Normal operation.	D

4.2 INA196-Q1/INA197-Q1/INA198-Q1 5-Pin SOT-23 Package

Figure 4-2 shows the INA19xA-Q1 pin diagram for the 5-pin SOT-23-5 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA19xA-Q1 data sheet.

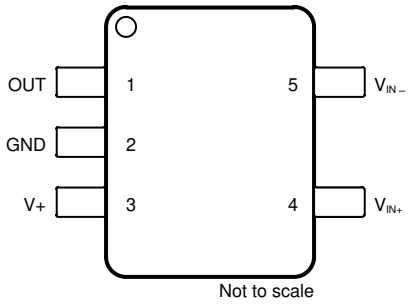

Figure 4-2. Pin Diagram (INA196-Q1/INA197-Q1/INA198-Q1 5-Pin SOT-23 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Normal Operation.	D
V+	3	Power supply shorted to ground.	B
VIN+	4	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low-side configuration, input pins are shorted.	B
VIN-	5	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low-side configuration, normal operation.	B in high-side; D in low-side

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output can be left open. There is no effect on the IC, but the output will not be measured.	B
GND	2	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
V+	3	No power supply to device.	B
VIN+	4	Input undefined, output will be anywhere between supply and ground..	B
VIN-	5	Input undefined, output will be anywhere between supply and ground.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	GND	Output will be pulled to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	V+	Power supply shorted to GND.	B
V+	3	VIN+	In high-side configuration, device power supply shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND.	A in high-side; B in low-side
VIN+	4	VIN-	Inputs shorted together. Output will stay close to GND.	B
VIN-	5	OUT	In high-side configuration, output pin is exposed to potential high voltage; in low-side configuration, output pin is shorted to GND.	A in high-side; B in low-side

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled to V+ and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Power supply is shorted to GND	B
V+	3	Normal operation	D
VIN+	4	In high-side configuration, device power supply shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND (through RSHUNT).	A in high-side; B in low-side
VIN-	5	In high-side configuration, device power supply shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND (through RSHUNT).	A in high-side; B in low-side

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (September 2020) **Page**

- Added *Pin Failure Mode Analysis (Pin FMA)* section..... 4

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