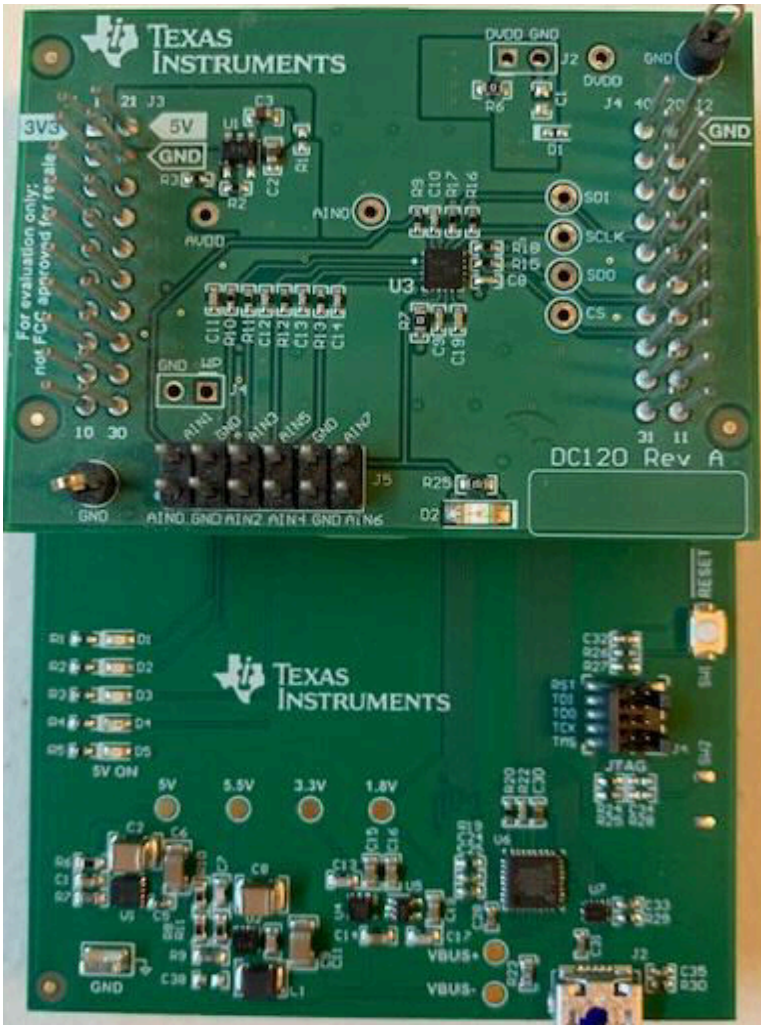
User's Guide

ADS7038Q1EVM-PDK Evaluation Module

ABSTRACT

The ADS7038-Q1 Evaluation Module (EVM) Performance Demonstration Kit (PDK) allows users to evaluate the functionality of Texas Instruments' ADS7038-Q1 12-bit, eight-channel programmable successive approximation register (SAR) analog-to-digital converter (ADC). The ADS7038-Q1 device showcases eight inputs, each configurable to an analog input, digital output, or digital input. This user's guide describes both the hardware platform showcasing the ADS7038-Q1 device and the graphical user interface (GUI) software used to configure the various modes of operation of this device. It includes complete circuit descriptions, schematic diagrams, and a bill of materials. The EVM-PDK eases the evaluation of the ADS7038-Q1 device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. The following figure shows the ADS7038Q1EVM-PDK.



ADS7038Q1EVM-PDK

The following related documents are available through the Texas Instruments website at www.ti.com

Device	Literature Number
ADS7038	SBAS979
ADS7038-Q1	SBAS981
TLV9061	SBOS839
TLV78001	SBVS083

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1 Introduction

The ADS7038-Q1 EVM is a fully-assembled evaluation platform designed to highlight the ADS7038-Q1 features and various modes of operation that make this device suitable for ultra-low-power, small-size sensor monitor applications. The accompanying Precision ADC Motherboard (PAMBoard) development kit is used as a USB-to-PC GUI communication bridge. This kit also serves as an example implementation of a master microcontroller (MCU) to communicate with the ADS7038-Q1 device through a serial-peripheral interface (SPI).

Note

The ADS7038-Q1 EVM requires an external master controller to evaluate the ADS7038-Q1 device.

The PAMBoard is controlled by commands received from the ADS7038-Q1 GUI, and returns data to the GUI for display and analysis. If the PAMBoard is not used, the EVM plug-in module format allows for an alternative external host to communicate with the ADS7038-Q1 by easily connecting through a pin header. The ADS7038-Q1 device incorporates all required circuitry and components with the following features:

- ADS7038-Q1 small general purpose, feature integrated, eight-channel ADC
- Buffered analog input drive circuit available on channel 0
- External power-supply connection available to provide DVDD power supply instead of the USB power
- Adjustable linear regulator, TPS78001, to generate stable output voltage to AVDD from the 5-V USB power from the PAMBoard
- SPI for communication and configuration of modes

Figure 1-1 shows the ADS7038-Q1EVM input circuity for the analog inputs.

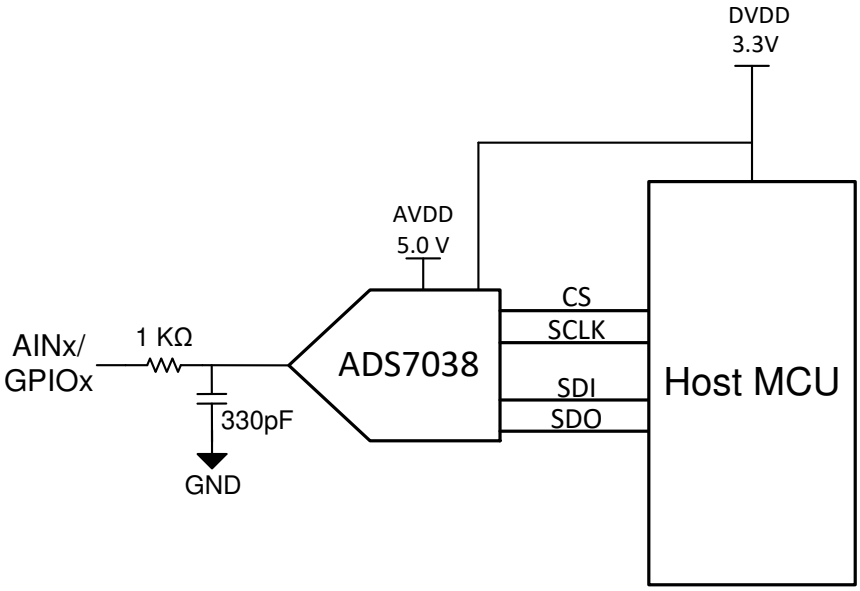

Figure 1-1. ADS7038-Q1EVM Input Circuity

2 ADS7038Q1EVM-PDK Overview

This section describes various onboard components that are used to interface the analog input, general purpose inputs/outputs (GPIOs), digital interface, and provide power supply to the ADS7038-Q1 device.

Figure 2-1 shows an ADS7038Q1EVM-PDK board overview.

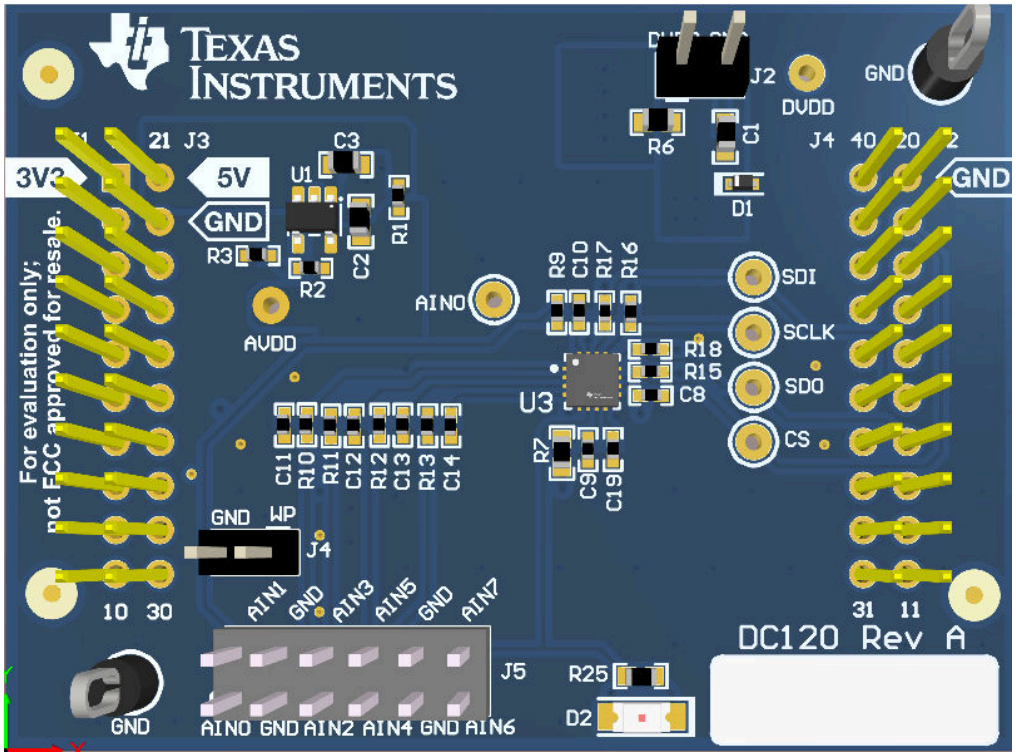

Figure 2-1. ADS7038Q1EVM-PDK Top Layer Overview

2.1 Connections to Input Channels

The ADS7038Q1EVM-PDK is designed for easy interface to an external, analog single-ended source, or to GPIOs through a 100-mil header. Connector J5 provides a connection to the device channels. Table 2-1 lists the channel connections. The AIN0 channel features an operational amplifier, TLV9061, to drive the analog input. This is further explained in Section 4. Channels AIN1 through AIN6 have a resistor and capacitor filter circuit to condition the analog input, as Figure 1-1 shows. Channel 7 is hardware configured to demonstrate GPIO functionality. GPIO7 has a resistor and light-emitting diode (LED) to visibly demonstrate and monitor digital output channel state. The LED illuminates when the GPIO7 is logic LOW.

Table 2-1. Channel Connections

J5 Connector Pin	Description
J5:1	Single-ended analog input with buffer
J5:2	Single-ended analog input or GPIO for channel 1 of the ADC
J5:5	Single-ended analog input or GPIO for channel 2 of the ADC
J5:6	Single-ended analog input or GPIO for channel 3 of the ADC
J5:7	Single-ended analog input or GPIO for channel 4 of the ADC
J5:8	Single-ended analog input or GPIO for channel 5 of the ADC

Table 2-1. Channel Connections (continued)

J5 Connector Pin	Description
J5:11	Single-ended analog input or GPIO for channel 6 of the ADC
J5:12	LED GPO for channel 7 of the ADC
J5:3 and J5:4; J5:9 and J5:10	EVM ground

2.2 Digital Interface

As noted in Section 1, the ADS7038Q1EVM interfaces with the PAMBoard, which in turn communicates with the computer over the USB. The two devices on the EVM that communicate over SPI are the ADS7038-Q1 ADC (U3) and the electrically erasable programmable read-only memory (EEPROM) (U4). The EEPROM is preprogrammed with the information required to configure and initialize the ADS7038 platform. Once the hardware is initialized, the EEPROM is no longer used.

2.3 ADS7038Q1EVM-PDK PAMBoard Interface

The ADS7038Q1EVM-PDK supports the digital SPI and functional modes as detailed in the ADS7038 Small, 8-Channel, 12-bit ADC with SPI Interface, GPIOs, and CRC data sheet. The PAMBoard is capable of operating at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC.

2.4 Power Supplies

The device supports a wide range of operation on its analog supply. The AVDD can operate from 3 V to 5.5 V. The DVDD operates from 1.65 V to 5.5 V, independent of the AVDD supply. A voltage regulator available on the PAMBoard is used to create a regulated 5-V supply for the EVM. AVDD is created from this supply using a low-dropout (LDO) voltage regulator to create a clean +3.3 V. DVDD is provided directly from the PAMBoard at 3.3 V. There is an option to use an external power supply for DVDD through J2.

3 ADS7038Q1EVM-PDK Initial Setup

The instructions to set up the ADS7038Q1EVM-PDK are described in the following sections.

3.1 EVM Plug-In Hardware Setup Instructions

The EVM and PAMboard should come packaged together. If they are not, for correct functionality, the boards need to be installed together properly.

To install the EVM to the PAMboard, stack the ADS7038Q1EVM board on the PAMBoard. Make sure the 20-pin connector (J1, J3) on the ADS7038Q1EVM is mapped to left connector on the PAMBoard, and the EVM connector (J4, J2) is mapped to right connector on the PAMBoard. The silk screen on the ADS7038-Q1 must match with the PAMBoard. Figure 3-1 shows the correct installation. The board headers must be flush. Make sure the USB is not plugged in during board connections. After matching the boards together, connect the PAMBoard micro USB data port to an available USB port on the PC.

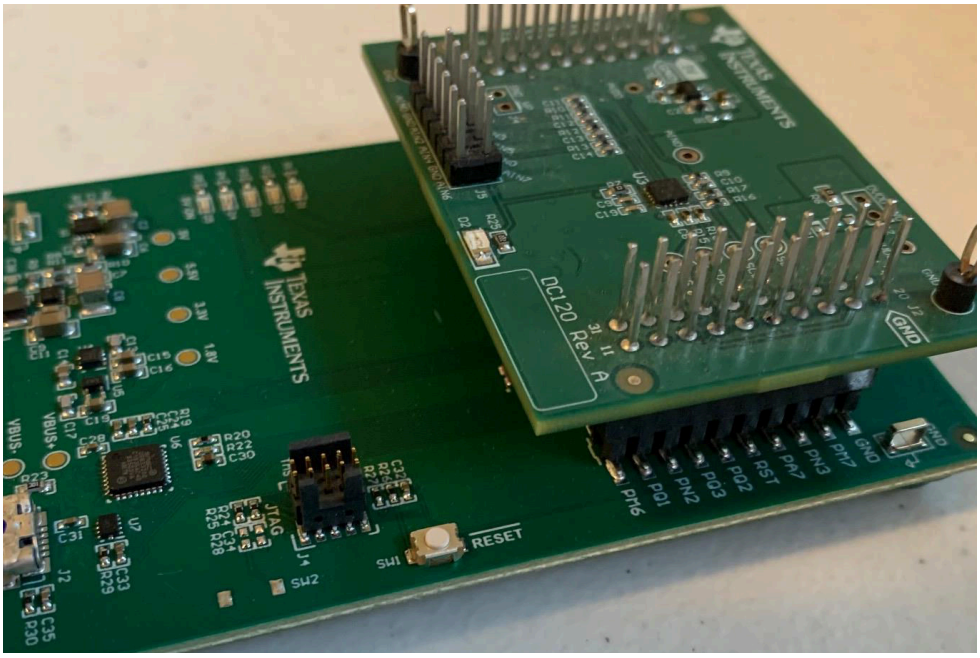

Figure 3-1. ADS7038Q1EVM Lined up With PAMBoard

3.2 The ADS7038 GUI Online and TI Cloud Agent Application Installation

The following steps describe the ADS7038 GUI software installation:

1. Plug in the included micro USB to USB cable to the PAMBoard and a USB port on the computer, respectively.
2. On the ADS7038Q1EVM-PDK landing page, the software is available through a web-based GUI. Connecting to the GUI may require login to a user account for access.
3. First-time users may be prompted to download and install the browser extension for Firefox™ or Google Chrome™ and the TI Cloud Agent Application as Figure 3-2 shows. Do so if need be, this is a one time download.

4. Refresh the GUI, if need be, and the GUI should connect to the hardware. A green signal will be displayed, and at the left bottom, *Hardware Connected* shows.

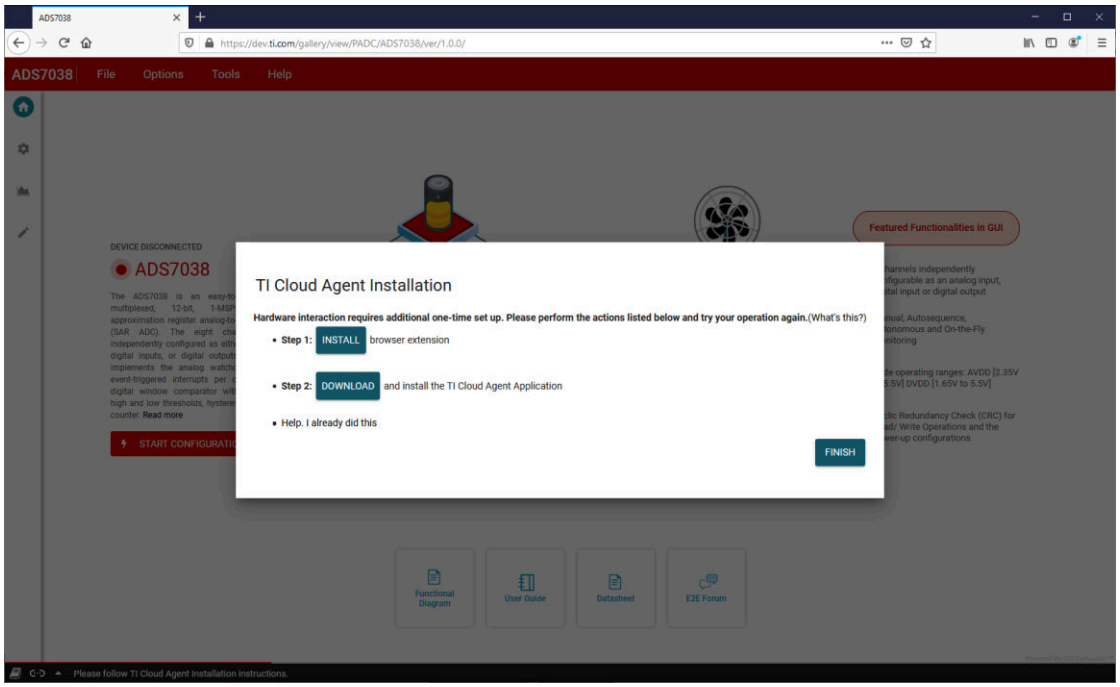

Figure 3-2. Browser Extension and TI Cloud Agent Installation

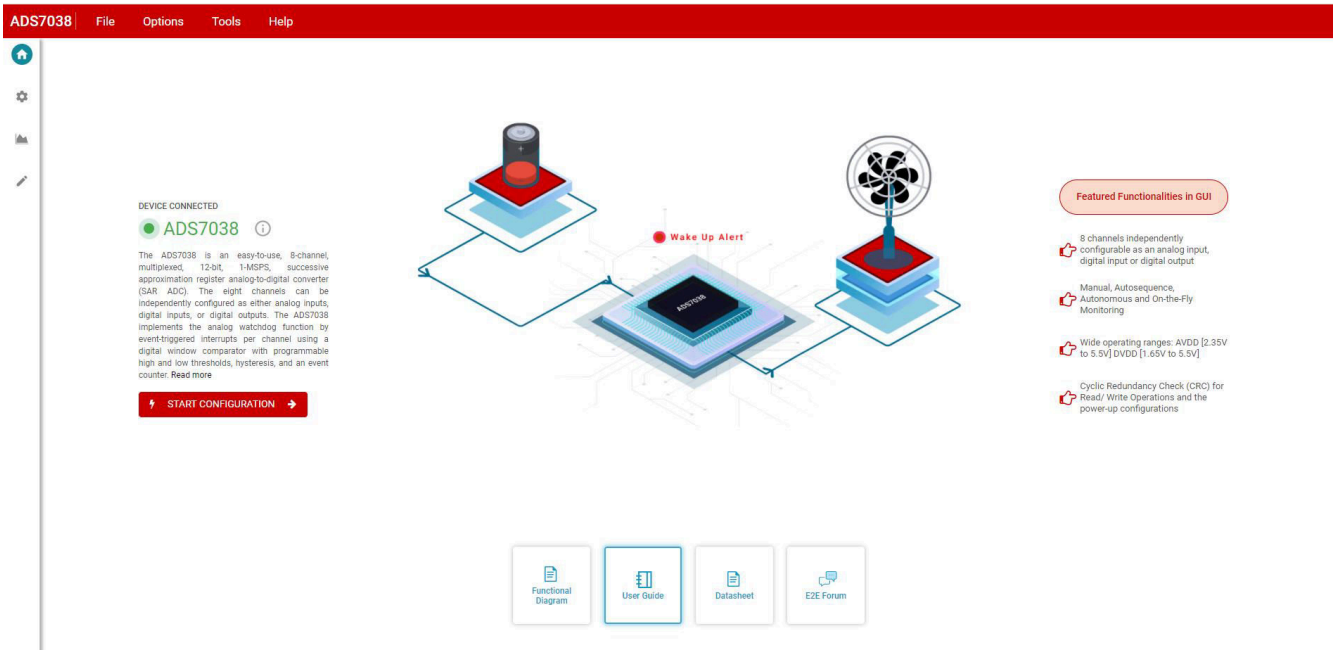

Figure 3-3. Hardware Connected Successfully to GUI

3.3 ADS7038Q1EVM-PDK GUI Overview

3.3.1 ADS7038Q1EVM-PDK GUI Landing Page

Figure 3-4 shows the GUI landing. This page provides a high-level overview of the ADS7038 device. The left corner (highlighted by the green rectangle) shows the tabs to navigate through the GUI: home, function configurations, data capture, and register map. When the ADS7038Q1EVM is stacked on the PAMBoard and connected to the PC via the micro USB cable, the GUI detects the EVM module by reading the onboard EEPROM. When detected and connected, the GUI indicates this status as *Connected*. At the bottom left corner of the GUI, there is an option to connect and disconnect the hardware from the GUI.

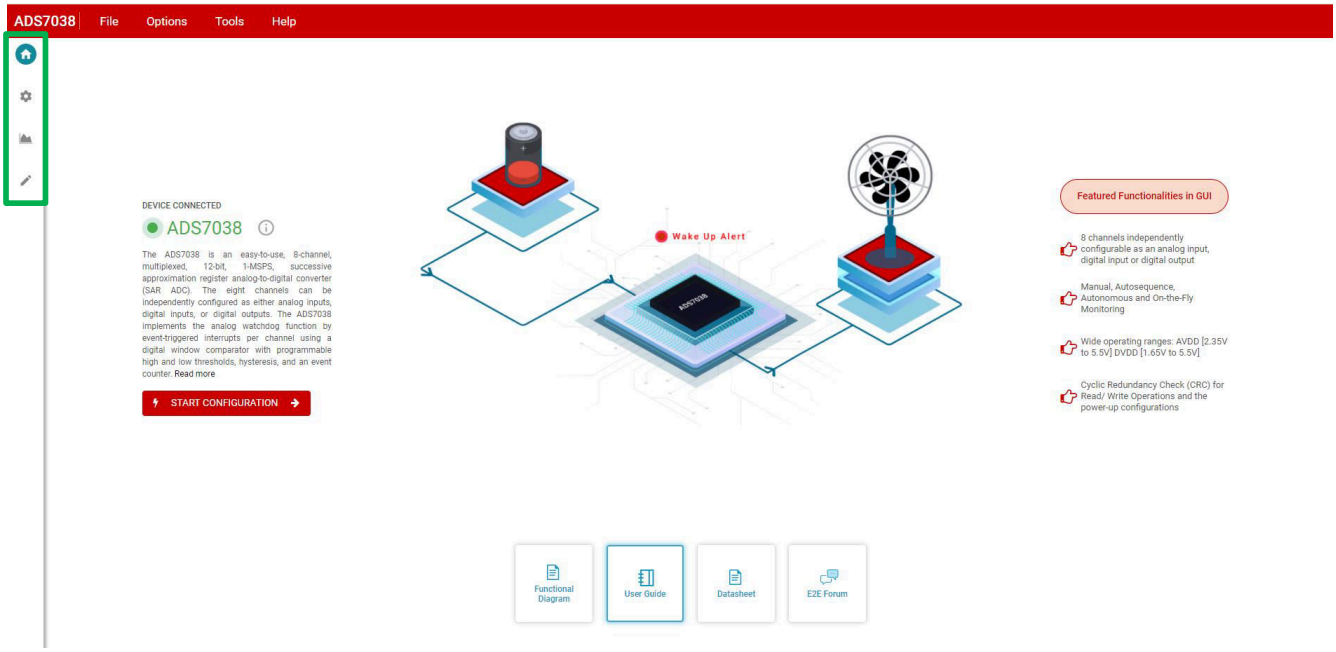

Figure 3-4. ADS7038Q1EVM-PDK GUI Landing Page

3.3.2 ADS7038 Functional Configuration

As Figure 3-5 shows, the ADS7038Q1EVM device configuration tab has two sections. The left section lists the multiple functions the user can configure. These options enable the user to navigate through the various functions of the ADS7038 in a structure and clear manner. The main section displays the configuration options for each function.

The Device Configurations available are: Mode Configuration, Channel Selection, Channel Configuration, Averager&Statistics, and Cyclic Redundancy Check (CRC).

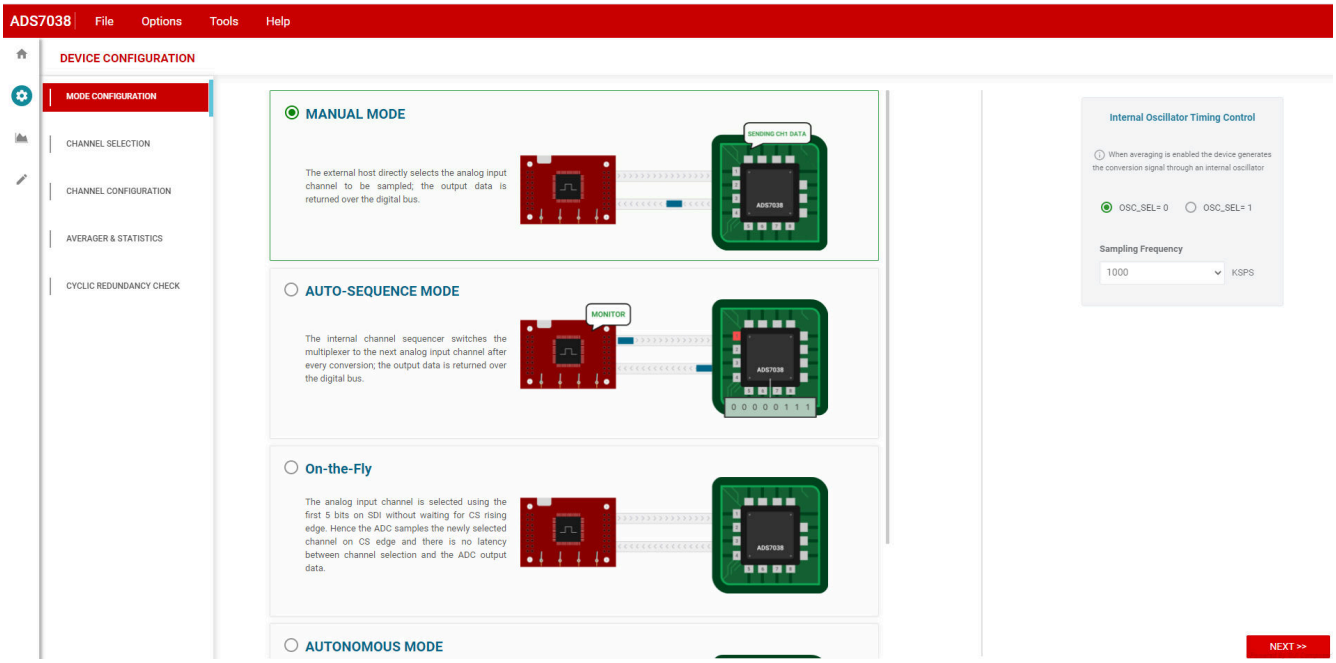

Figure 3-5. Device Configuration tab

3.3.2.1 Device Mode Configuration

The ADS7038 can operate in four sampling modes. The mode configuration tab (Figure 3-5) allows the user to select the device mode of operation.

The ADS7038 device has the following sampling modes:

- Manual Mode: Allows the external host processor to directly request and control when data is sampled. The host provides SPI frames to control conversions and the captured data are returned over the SPI bus after each conversion.
- Auto-Sequence Mode: The host can configure the device to scan through the enabled analog input channels. The host must provide continuous clocks (SCLK) to the device to scan through the channels and to read the data from the device. The MUX automatically switches through the predetermined channel sequence, and the data conversion results are sent through the data bus.
- On-the-Fly Mode: The first 5 bits of SDI select the first channel to be sampled before the CS rising edge. There is no latency between channel selection and ADC output data since the ADC samples the next channel on the rising edge of CS.
- Autonomous Mode: In autonomous mode, the device can be programmed to monitor the voltage applied on the analog input pins of the device and generate an ALERT signal internal to the device when the programmable high or low threshold values are crossed.

The device powers up in manual mode and can be configured into any of the functional modes by writing the configuration registers for the desired mode.

3.3.2.2 Channel Selection

The channel selection configuration option allows the user to configure each of the 8 channels. The default configuration is analog input, but through the drop-down options, each channel can be configured as a digital input or output instead. If using Auto Sequence mode, individual channels can be selected to be included in the sequence, by checking Select for Auto-Seq. The EVM hardware has channel 7 hardwired as a digital output with an LED connected to channel 7 to visually display a high or low digital output state.

To configure for a digital function, change the Pin-Config drop down and select Digital. A second drop-down option will appear in line with the channel, I/O Config. This drop-down option allows to select Input or Output functionality. If output functionality is selected, as shown for channel 7 in Figure 3-6, configuration options will appear in line with the channel. User will be able to select the Pin Value as high or low, and the Pin Type as open drain or push pull. The EVM has an LED connected to channel 7 to display this functionality; changing the Pin Value on channel 7 will turn on or off the LED (D2). As an example to help use the GUI and for Figure 3-6, and throughout the remainder of this document, channel 0 to 5 will be selected as analog inputs, channel 6 as a digital input, and channel 7 as a digital output.

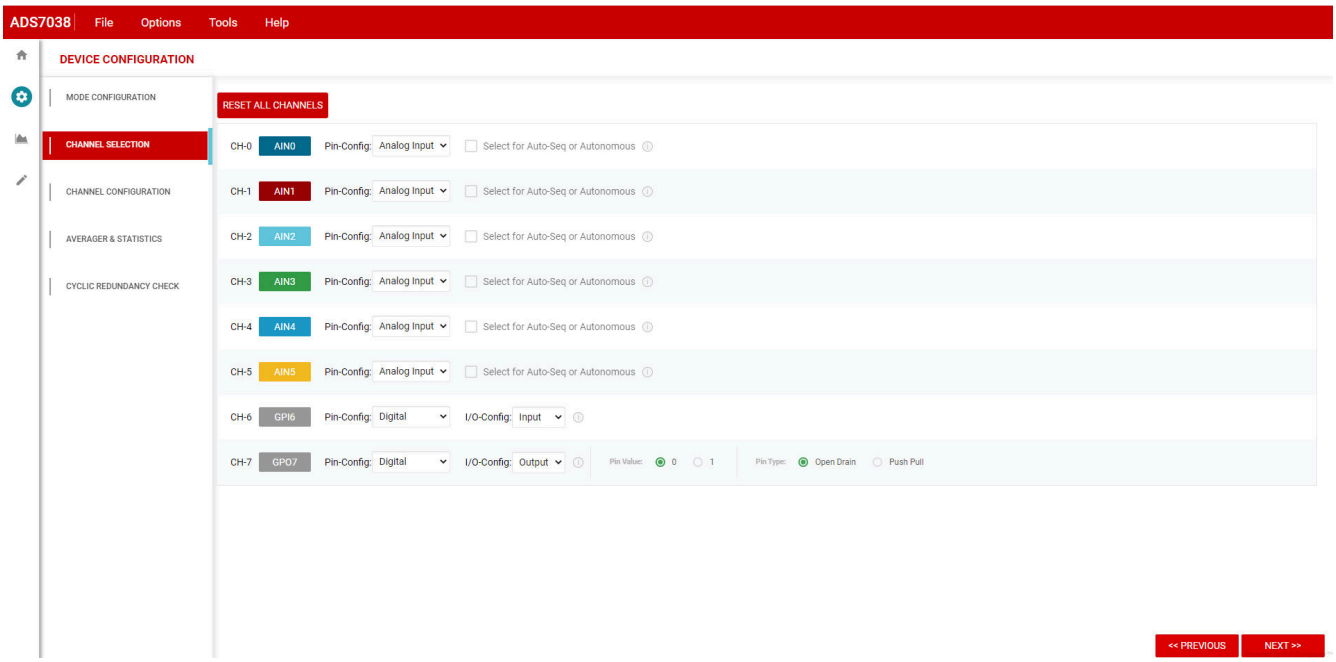

Figure 3-6. Channel Selection tab

3.3.2.3 Channel Configuration

There are three tabs in the channel configuration page which allow the respective configuration of the:

- Analog Input and Digital Inputs
- Digital Outputs
- Alert Mapping and Configurations

The Input Channels tab is displayed first by default.

3.3.2.3.1 Input Channel Configuration

The analog input and digital input channel settings are configured on the input channels tab as shown in Figure 3-7. Channels configured in the *Channel Selection* section as analog (CH0–CH5) and digital inputs (CH6) will be displayed. For analog inputs, users can select the high and low thresholds, hysteresis settings. The Alert counter and out-band/in-band settings can be configured by clicking the additional advanced configuration icon. Digital

inputs can be configured for different alarm triggers. As an example, the high and low thresholds for CH0 were set to codes 3000 and 1000, respectively which will later be used in the Alert Configuration.

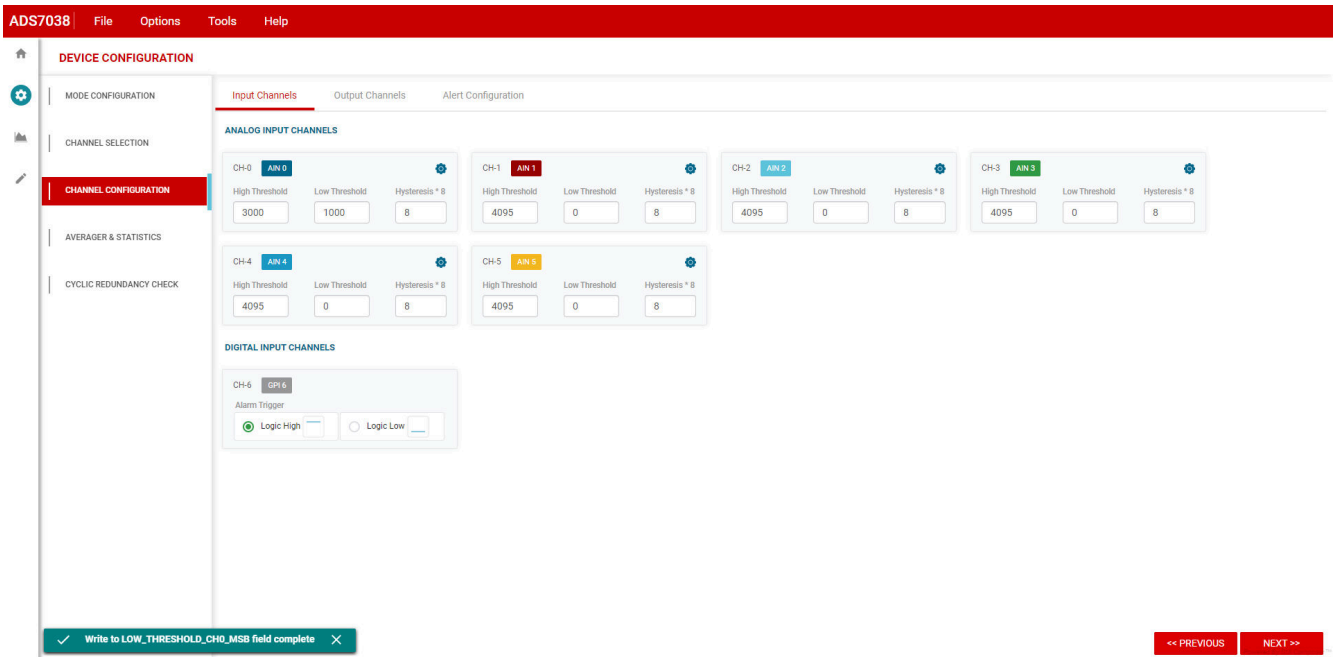

Figure 3-7. Channel Configuration tab - Input Channels

3.3.2.3.2 Output Channel Configuration

The digital output channel settings are configured on the output channels tab as shown in Figure 3-8. Channels configured as digital outputs (CH7) in the *Channel Selection* section will be displayed on this page. Enabled digital outputs can be configured for different trigger sources and the trigger output conditions.

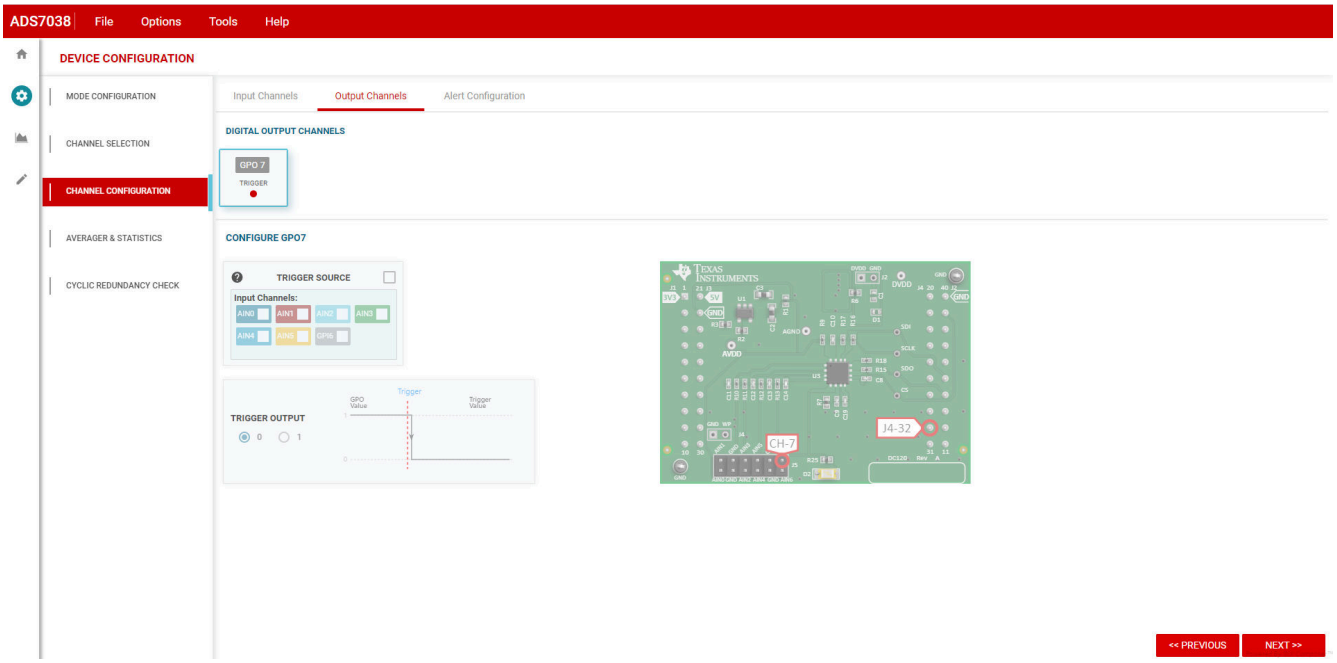

Figure 3-8. Channel Configuration tab - Output Channels

3.3.2.3.3 Alert Configuration

Alerts can be enabled and configured on the Alert Configuration tab as shown in Figure 3-9. Channels configured as digital outputs (CH7) in Section (Channel Selection) can be enabled as the Alert output channel. In Figure 3-9 the Alert is mapped to CH-7 and will trigger based on the threshold levels for CH0 (AIN0) that were configured in Section (Input Channel Configuration).

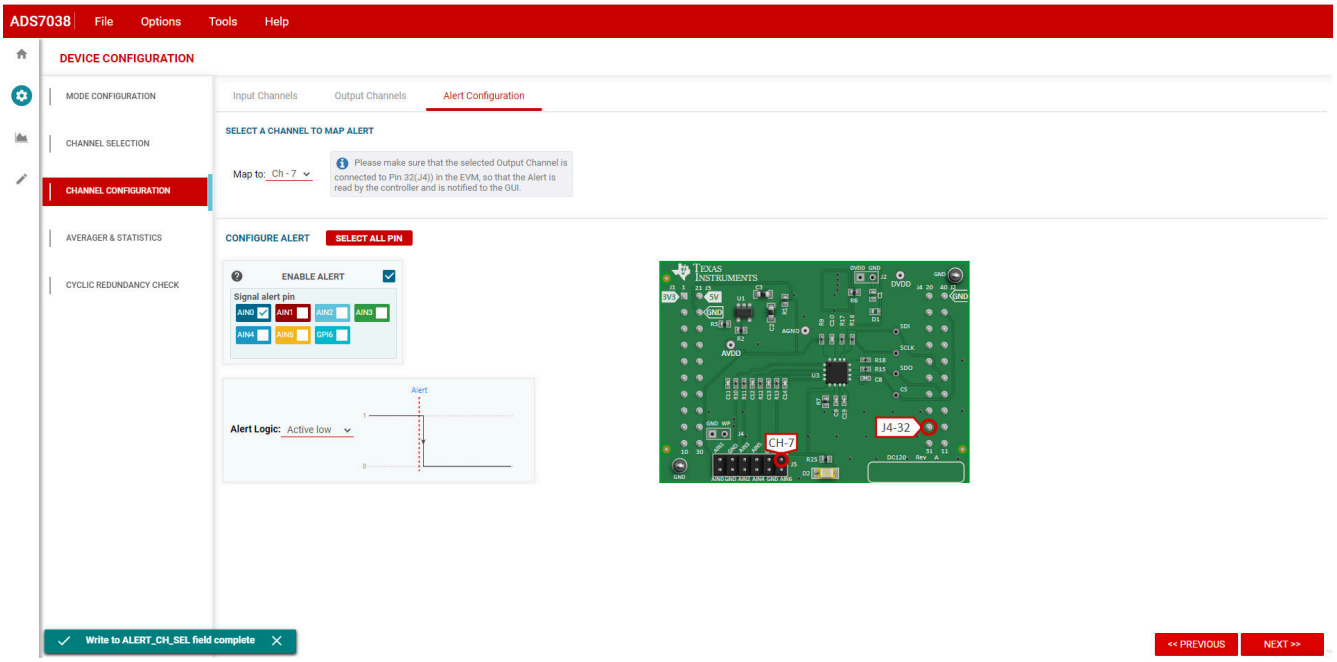

Figure 3-9. Channel Configuration tab - Alert Configuration

3.3.2.4 Averaging & Statistics

Within the averaging function page, as Figure 3-10 shows, the oversampling ratio can be selected through the drop-down option. The oversampling ratio applies to all analog input channels enabled. Statistics to show the minimum, maximum, and latest codes can also be enabled here.

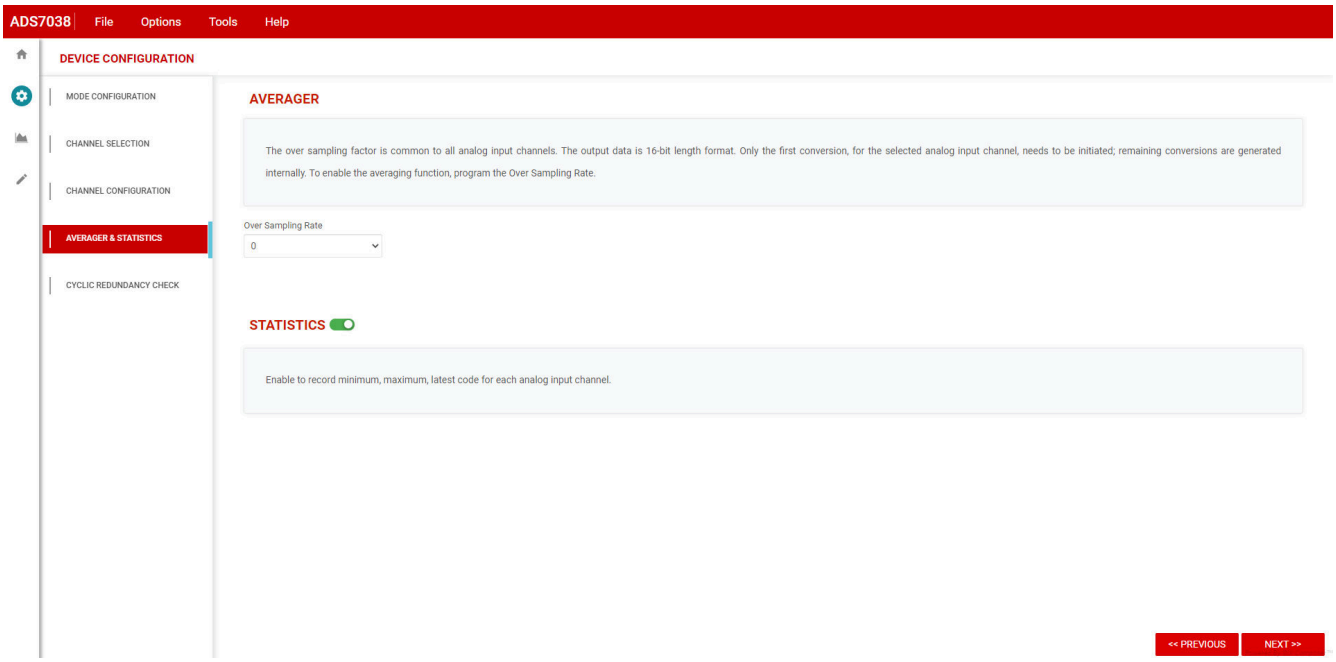

Figure 3-10. Averaging & Statistics Page

3.3.2.5 Cyclic Redundancy Check (CRC)

The ADS7038 device supports CRC to check the integrity of data transfer. When CRC is enabled, an 8-bit output is appended to the end of the data transfer. The polynomial is calculated on the CRC-8-ATM as shown in the page in Figure 3-11.

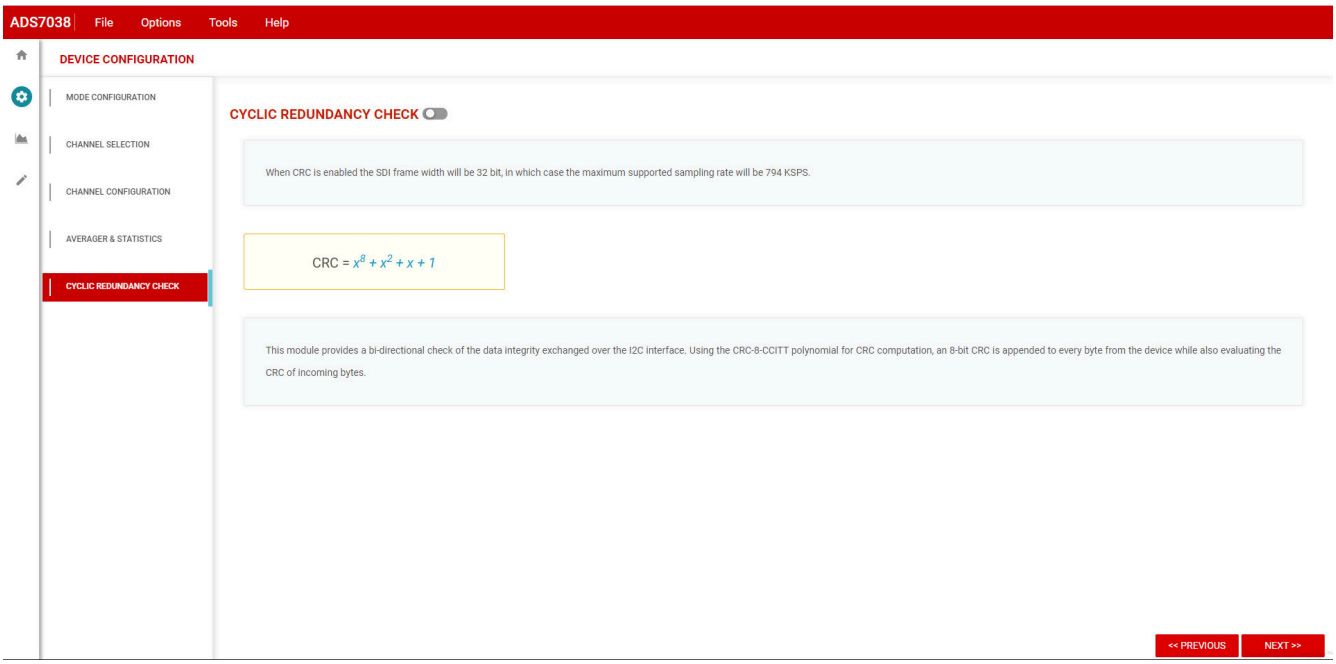

Figure 3-11. CRC Page

3.3.3 Data Capture Tab

The data capture tab displays the conversion results of the sampled data of the enabled channels. As Figure 3-12 shows, clicking the red Capture Data button commences a sample data set. This page also displays the sampling mode configuration used to capture the data. There is also a checkmark option to repeatedly capture the sample size selected. This tab features two pages to display both the analog input and the digital inputs:

- Analog Inputs: The sample and conversion results for each enabled analog input is displayed in this page. The results can be displayed in three methods: time domain, Fast Fourier transform (FFT), and histogram.

- Digital Inputs: The enabled digital input channels are displayed in this page and can be polled for the current logic state.

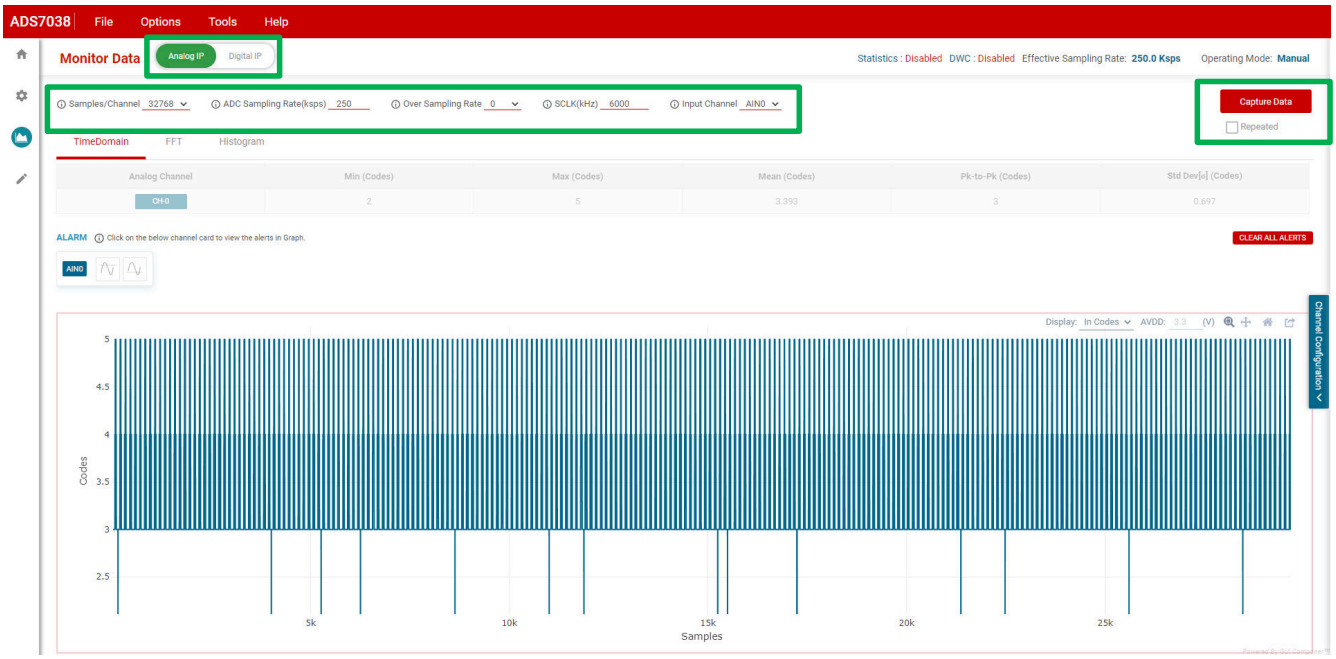

Figure 3-12. Data Capture tab

3.3.3.1 Analog Input Data Capture Features

This section describes the features available in the Analog IP (input) data capture display of the GUI. This page auto updates to reflect the channel-specific input configurations selected in the *Channel Selection* section.

The analog input page provides an interface to the conversion results of the analog input channels.

Analog data is captured, as shown in Figure 3-12, by clicking on the *Capture Data* button. The analog inputs page also provides user options for the following:

- Number of samples per the enabled analog input channels
- A drop-down option for increasing the oversampling rate
- A drop-down option to change the SCLK frequency
- A drop-down option for entering the desired sampling rate
- A drop-down option for selecting input channel displayed when in manual mode. When in Autosequence, all channels selected would be displayed simultaneously

A table is also available with helpful attributes of the sampled data including, the minimum, maximum, and mean sample codes along with the peak-to-peak range of the sampled data and standard deviation. These values are populated after every data capture.

Within the Analog IP page, the captured samples can be displayed in three different formats:

- Time Domain
- Fast Fourier Transform (FFT)
- Histogram

3.3.3.1.1 Time Domain Display

The time domain graph displays the conversion results of an analog input channel of the sampled data set. The data captured is displayed as code value vs sample number. The number of samples can be increased in the Samples/Channel drop-down menu. The data can also be displayed in the volt equivalent of sample captured instead of the code value, based on the ideal +3.3-V AVDD voltage.

When in manual mode, the graph can only display one analog input conversion results at a time; the drop-down option *Input Channel* allows changing which channel is displayed. When the device is operating in auto-sequence mode, all the analog input channels selected will be displayed on the graph.

The data can also be exported by clicking the last icon at the right corner of the graph display. Figure 3-13 shows the time domain display.

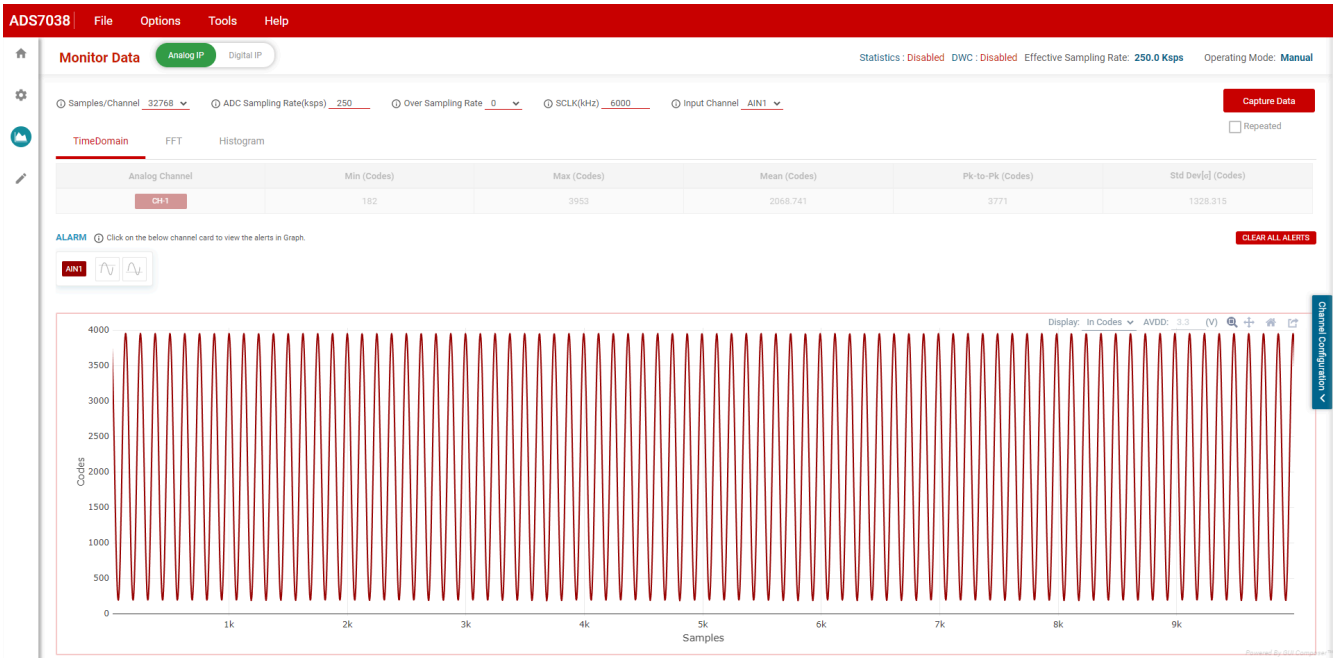

Figure 3-13. Time Domain Data Analysis Display

3.3.3.1.2 FFT

The Analog IP can display the FFT of the data captured. This will only display results if the input signal is determined to be an AC signal. Figure 3-14 shows the FFT data analysis display.

The FFT tab displays a table with the fundamental frequency of the input, followed by the noise floor level, SNR, SFDR, THD, and SINAD. The effective number of bits (ENOB) and the number harmonics shown is also displayed in the table.

Figure 3-14. FFT Data Analysis Display

3.3.3.1.3 Histogram Display

The conversion results can also be shown as a histogram through the histogram tab within the Analog IP page. Figure 3-15 shows the histogram data analysis display.

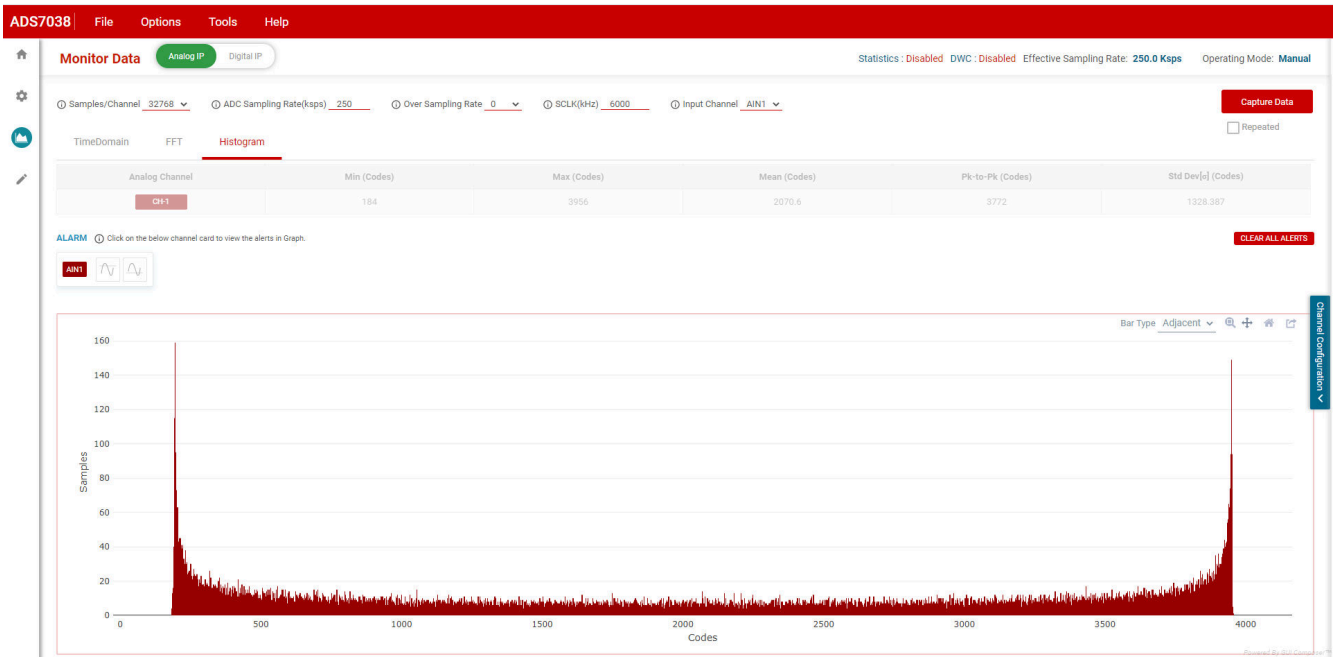

Figure 3-15. Histogram tab

3.3.4 Digital Input Page

The digital input page displays the enabled digital input channels as configured in Figure 3-16. As an example channel 6 was configured as a digital input. All digital input channels enabled will be displayed on this page with the present logic state applied to them.

Figure 3-16. Digital Inputs

3.3.5 Register Map

Figure 3-17 shows the register map for the ADS7038 device. On the top right corner are options to read registers individually or read all the registers, or write an individual register. Users can choose to have the register values modified in the GUI to be written on the device instantaneously by selecting the Immediate Write option or later using the Deferred Write drop-down option. In the field view, the registers are broken down into the configurable bits it controls. When making changes in the Field View, the bit being changed is highlighted in yellow in the register map.

The register settings can also be saved in an external file to be loaded back into the GUI through the File → Save Registers menu selection. This allows for different setting configurations to be saved and easily implemented into the GUI by loading it back through the File → Load Registers menu item.

The register configurations can also be saved as a comma-separated values (CSV) file containing the register address and content as configured in the GUI. This allows the user to configure the device easily through the GUI as desired, and then export the respective register addresses and content to reference when creating firmware.

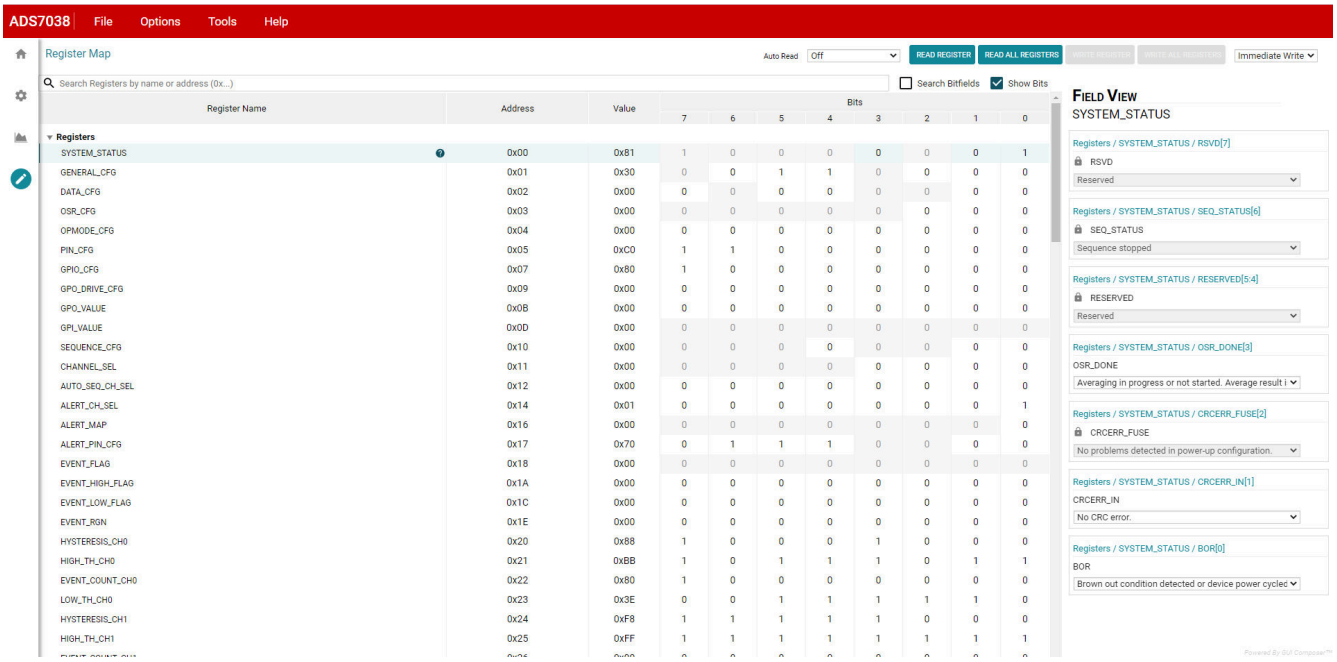

Figure 3-17. Register Map

4 Input Signal-Conditioning Circuitry on the ADS7038Q1EVM

For applications where the input signal requires additional conditioning or drive strength before the ADC input, the ADS7038Q1EVM has an onboard ADC path on channel 0. The input signal header, J5 is connected to the amplifier input, TLV9061. By default, this signal-conditioning block is populated on the evaluation board as a non-inverting buffer using the TLV9061 device. The board has a provision to bypass the operational amplifier (U5) based on the signal conditioning requirement. To bypass this block, remove the R21 0-Ω resistor and populate R26. See the *Schematics* section for more details. Figure 4-1 displays a simplified CH0 input drive circuit.

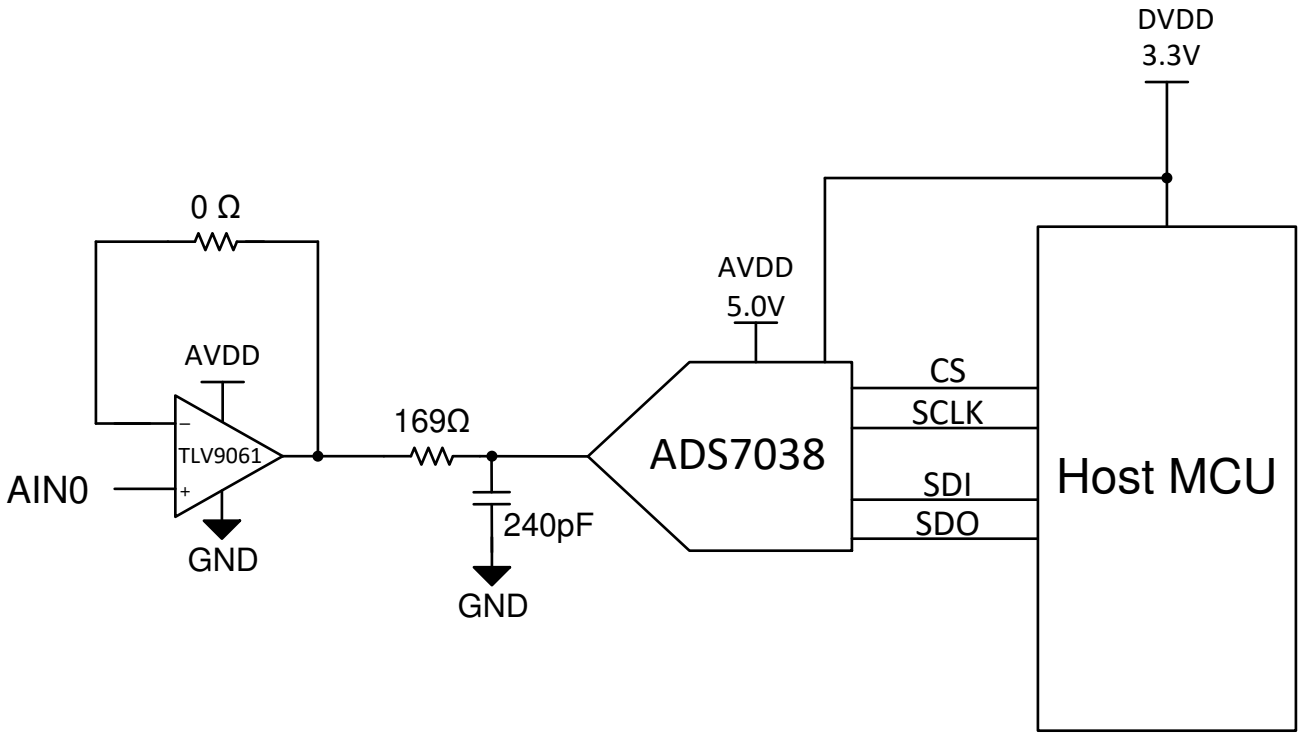

Figure 4-1. Channel 0 Input Signal Buffer Circuit

5 Bill of Materials, Printed Circuit Board Layout, and Schematics

This section contains the ADS7038Q1EVM-PDK bill of materials (BOM), printed circuit board (PCB) layout, and schematics.

5.1 Bill of Materials

Table 5-1 lists the bill of materials (BOM) for the ADS7038Q1EVM-PDK.

Table 5-1. ADS7038Q1EVM-PDK BOM

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number(1)	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		DC120	Any		
C2, C3	2	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet		
C8, C9, C19	3	1uF	CAP, CERM, 1 uF, 6.3 V, +/- 20%, X7R, 0402	0402	GRM155R70J105MA12D	MuRata		
C10, C11, C12, C13, C14, C15	6	330pF	CAP, CERM, 330 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1H331JA01D	MuRata		
C16, C18	2	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	0603	GRM188R72A104KA35J	MuRata		
C17	1	240pF	CAP CER 240PF 50V C0G/NP0 0402	0402	C0402C241J5GAC7867	Kemet		
D2	1	Red	LED, Red, SMD	1206	LTST-C150CKT	Lite-On		
FID4, FID5, FID6	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J1, J3	2		Receptacle, 2.54mm, 10x2, Tin, TH	10x2 Receptacle	SSQ-110-03-T-D	Samtec	CRD-081413-A-G	Major League Electronics
J5	1		Header, 100mil, 6x2, Tin, TH	Header, 6x2, 100mil, Tin	PEC06DAAN	Sullins Connector Solutions		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady		
R2	1	1.69Meg	RES, 1.69 M, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021M69FKED	Vishay-Dale		
R3, R27	2	1.00Meg	RES, 1.00 M, 1%, 0.1 W, 0402	0402	ERJ-2RKF1004X	Panasonic		
R6, R7	2	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo		
R9, R10, R11, R12, R13, R14, R15, R16, R17, R18	10	1.00k	RES, 1.00 k, 1%, 0.0625 W, 0402	0402	RC0402FR-071KL	Yageo America		
R20, R21	2	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc		
R22	1	169	RES, 169, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402169RFKED	Vishay-Dale		
R23, R24	2	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America		

Table 5-1. ADS7038Q1EVM-PDK BOM (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number(1)	Alternate Manufacturer
R25	1	2.20k	RES, 2.20 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K2L	Yageo		
TP4, TP5	2		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone		
U1	1		Single Output LDO, 150 mA, Adjustable 1.22 to 5.25 V Output, 2.2 to 5.5 V Input, with 500 nA Quiescent Current, 5-pin SOT (DDC), -40 to 125 degC, Green (RoHS & no Sb/Br)	DDC0005A	TPS78001DDCR	Texas Instruments		
U3	1		Small, 8-Channel, 12-Bit ADC With SPI Interface, GPIOs, and CRC	WQFN16	ADS7038IRTET	Texas Instruments		
U4	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm		
U5	1		10-MHz, RRIO, CMOS Operational Amplifier for Cost-Sensitive Systems, DBV0005A (SOT-23-5)	DBV0005A	TLV9061IDBVR	Texas Instruments		Texas Instruments
C1	0	10uF	CAP, CERM, 10 µF, 16 V,+/- 10%, X5R, 0603	0603	GRM188R61C106KAALD	MuRata		
D1	0	5.1V	Diode, Zener, 5.1 V, 300 mW, SOD-523	SOD-523	BZT52C5V1T-7	Diodes Inc.		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J2, J4	0		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions		
R1, R26	0	0	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America		
R19	0	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc		

(1) Unless otherwise noted in the Alternate Part Number or Alternate Manufacturer columns, all parts may be substituted with equivalents.

5.2 PCB Layout

Figure 5-1 illustrates the EVM PCB layouts.

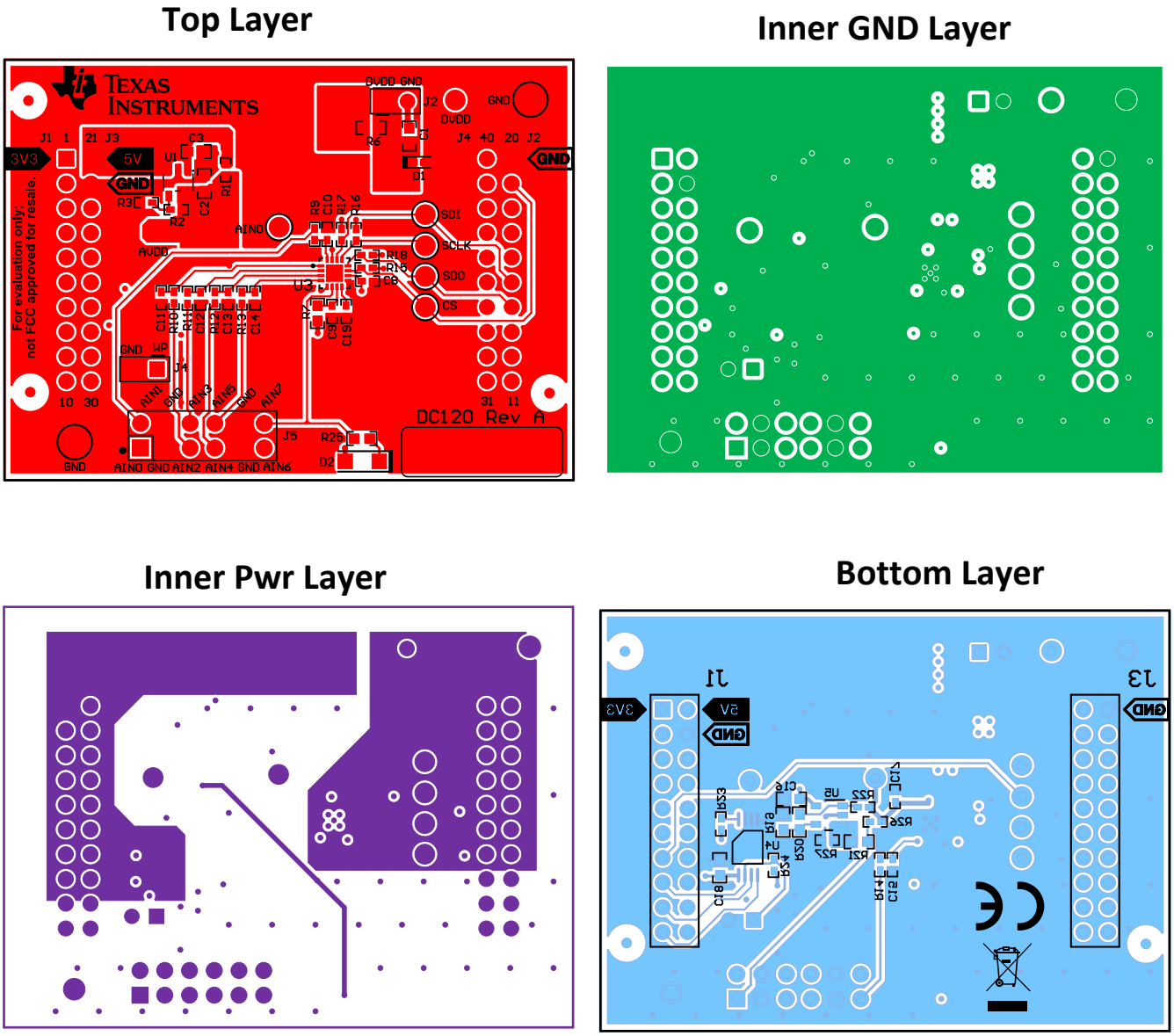

Figure 5-1. PCB Layouts

5.3 Schematics

Figure 5-2 illustrates the ADS7038Q1EVM-PDK schematics.

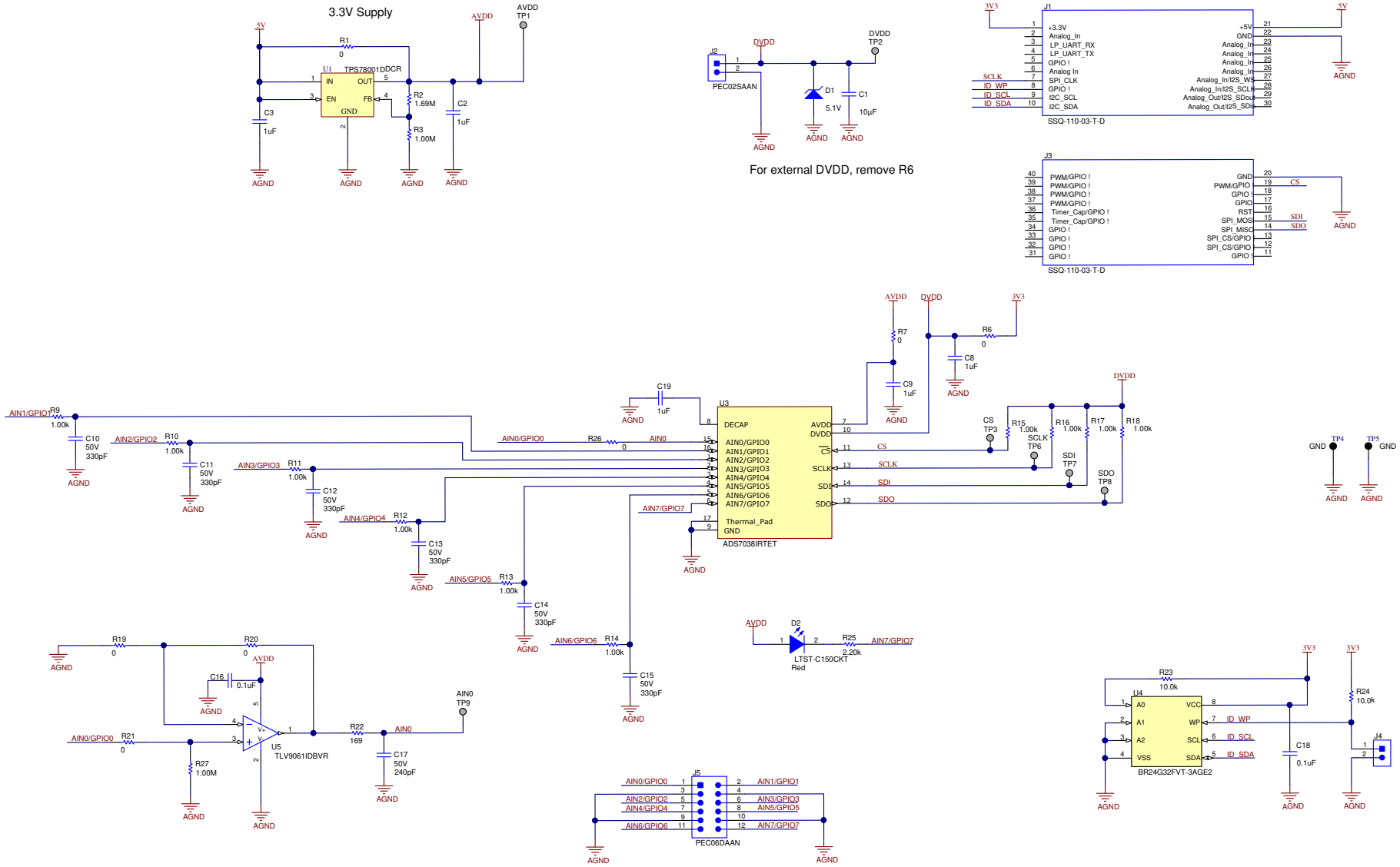

Figure 5-2. ADS7038Q1EVM-PDK Schematics

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