

# ADS1241MEVM

This user's guide describes the characteristics, operation, and use of the ADS1241MEVM. This EVM is a 24-bit analog-to-digital converter evaluation module. A complete circuit description, schematic diagram, and bill of materials are included.

The following related documents are available through the Texas Instruments web site at www.ti.com.

## **EVM-Compatible Device Data Sheets**

Device	Literature Number
ADS1241	SBAS173
REF1004	<u>SBVS002</u>
OPA350	SBOS099
SN74LVC1G126	SCES224

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#### 1 EVM Overview

#### 1.1 Features

- Full-featured evaluation board for the ADS1241 24-bit analog-to-digital converter
- On-board reference and oscillator circuits
- · Modular design for use with a variety of DSP and microcontroller interface boards

### 1.2 Introduction

The ADS1241MEVM is in Texas Instruments' modular EVM form factor, which allows direct evaluation of the ADS1241 performance and operating characteristics, and eases software development and system prototyping. This EVM is compatible with the 5-6K Interface Board (SLAU104) from Texas Instruments and additional third-party boards such as the HPA449 demonstration board from SoftBaugh, Inc. (www.softbaugh.com) and the Speedy33<sup>™</sup> from Hyperception, Inc. (www.hyperception.com).

## 2 Analog Interface

For maximum flexibility, the ADS1241MEVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J1. This header/socket provides access to the analog input pins of the ADS1241. Consult Samtec at <a href="https://www.samtec.com">www.samtec.com</a> or call 1-800-SAMTEC-9 for a variety of mating connector options.

Pin Number	Signal	Description
J1.1	ANO-	ADS1241 AN1
J1.2	AN0+	ADS1241 AN0
J1.3	AN1-	ADS1241 AIN3
J1.4	AN1+	ADS1241 AIN2
J1.5	AN2-	ADS1241 AIN5
J1.6	AN2+	ADS1241 AIN4
J1.7	AN3-	ADS1241 AIN7
J1.8	AIN3+	ADS1241 AIN6
J1.10	AIN4+	ADS1241 AINCOM
J1.15	VCOM	Tied to onboard 2.5V reference
J1.18	REF(-)	External reference source low side
J1.20	REF(+)	External reference source input (2.5V NOM)
J1.9-J1.19 (odd)	GND	Analog ground connections (except J1.15)
J1.12-J1.16 (even)	Unused	

**Table 1. Analog Interface Pinout** 

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## 3 Digital Interface

The ADS1241MEVM is designed to easily interface with multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the ADS1241. Consult Samtec at <a href="www.samtec.com">www.samtec.com</a> or call 1-800-SAMTEC-9 for a variety of mating connector options.

**Table 2. Digital Interface Pinout** 

Pin Number	Signal	Description
J2.1	DSYNC	Synchronization control
J2.2	PWDN	Power down
J2.3	SCLK	Serial clock
J2.4	DGND	Digital ground
J2.5	Unused	
J2.6	GPIO1	Oscillator kickstart (see Section 5.3.1.1)
J2.7	CS	Chip select - Active low signal, enables data transfer. Frame sync on DSP host systems.
J2.8	GPIO2	Oscillator kickstart enable (see Section 5.3.1.1)
J2.9	Unused	
J2.10	DGND	Digital ground
J2.11	DIN	Serial data input to ADS1241 from host
J2.12	BUFEN	Buffer enable
J2.13	DOUT	Serial data output from ADS1241 to host
J2.14	POL	Serial clock polarity
J2.15	DRDY	Data ready
J2.16	SCL	I <sup>2</sup> C bus serial clock
J2.17	TOUT	External clock input to ADS1241
J2.18	DGND	Digital ground
J2.19	RESET	Resets ADS1241 device
J2.20	SDA	I <sup>2</sup> C bus data line

## 4 Power Supplies

J3 provides connection to the common power bus for the ADS1241MEVM. Power is supplied on the pins listed in Table 3.

**Table 3. Power Supply Pinout** 

Signal	Pin Number		Signal
Unused	1	2	Unused
+5VA	3	4	Unused
AGND	5	6	DGND
Unused	7	8	Unused
+3.3VD	9	10	+5VD

When power is supplied to J3, J4 allows for either 3.3V of 5V to be applied to the digital sections of the ADS1241. J4 also provides for a method of measuring AVDD and DVDD supply currents if the shunts on J4.1-2 and J4.3-4 are removed and a current meter is connected between the appropriate pins. See the schematic and Figure 1 for details.



#### 4.1 ADC Power

Power for the ADS1241 analog supply voltage (AVDD) comes from +5VA, which is supplied through J3.3. The shunt from J4 pins 1 to 2 applies this supply to the ADS1241 device.

The ADS1241 digital supply voltage (DVDD) is selected using J4. When a shunt is applied from J4 pins 5 to 6, +5VD is selected, and this power comes from J3.10. If a shunt is placed from J4 pins 7 to 8 (the default factory setting), +3.3VD is selected, which is provided from J3.9. J4 pins 9 and 10 provide a way to connect the analog and digital grounds; these pins are connected by default when the EVM is shipped from the factory.

#### **CAUTION**

Verify that all power supplies are within the safe operating limits shown on the ADS1241 data sheet before applying power to the EVM. Note that a shunt should only be connected between J4 pins 7 and 8 OR pins 5 and 6, but never both; doing so would short the +3.3V supply to the +5V digital supply.

## 4.2 Stand-Alone Operation

When used as a stand-alone EVM, the analog power can be applied to J4.1, referenced to J4.10. DVDD can be applied to J4.3, referenced to J4.10. Note that this EVM uses only a single ground plane.

### 4.3 Reference Voltage

The ADS1241 requires an external voltage reference. Two switches, S6 and S7, select the source of the reference for the ADS1241. An external reference may be supplied through J1 pin 20 on the ADS1241MEVM. A 2.5V reference is provided on the EVM for convenience, or the supply voltage may also be used as the device reference voltage. These different reference sources can be selected using S6 and S7, as shown in Table 4. Note that the ADS1241 reference is differential, so both VREF+ and VREF- pins may take on several voltages. Refer to the ADS1241 data sheet.

#### CAUTION

Verify that the external reference voltage is within the safe operating limits shown on the ADS1241 data sheet before applying power to the EVM.

Table 4. Reference Selection Options - S6 and S7

S6 Position	S7 Position	VREF+	VREF-	Comment
Left	Left	External (J1.20)	External (J1.18)	
Middle	Left	2.5V	External (J1.18)	
Right	Left	AVDD	External (J1.18)	
Left	Middle	External (J1.20)	Ground	
Middle	Middle	2.5V	Ground	
Right	Middle	AVDD	Ground	
Left	Right	External (J1.20)	2.5V	
Middle	Right	2.5V	2.5V	This results in a 0V reference - not a very useful setting.
Right	Right	AVDD	2.5V	

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### 5 EVM Operation

The following section provides information on the analog input, digital control, and general operating conditions of the ADS1241MEVM. Refer to Figure 1 for switch and jumper locations, and the meanings of *left*, *middle*, and *right* for switch settings in the following discussion.

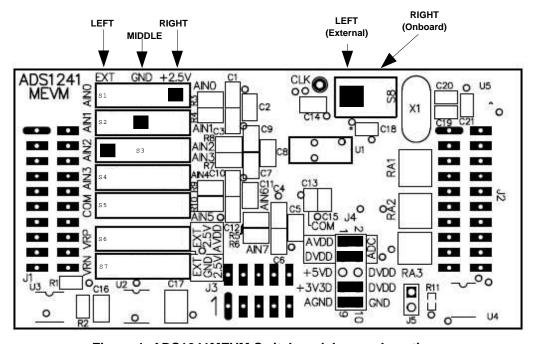


Figure 1. ADS1241MEVM Switch and Jumper Locations

## 5.1 Analog Input

The analog input sources can be applied directly to J1 (top or bottom side) or through optional amplifier and signal-conditioning modules. Consult the ADS1241 data sheet to determine the maximum analog input range. Switches S1-S5 can be used to select the source for inputs AIN0-3, as shown in Table 5. AINCOM is selected by S5, as shown in Table 6.

Table 5. Input Selection Options - S1 through S4

Switch Position	Input Selected
Left	J1.2 for AIN0 J1.1 for AIN1 J1.4 for AIN2 J1.3 for AIN3
Middle	Ground for AIN0-3
Right	2.5V for AIN0-3

Table 6. AINCOM Selection Options - S5

Switch Position	Input Selected
Left	J1.10
Middle	Ground
Right	2.5V



### 5.2 Digital Control

The digital control signals can be applied directly to J2 (top or bottom side). The modular ADS1241MEVM can also be connected directly to a DSP or microcontroller interface board, such as the HPA449. For a current list of compatible interface and/or accessory boards for the EVM or the ADS1241, see the relevant product folder on the TI web site.

#### 5.3 Clock Source

#### 5.3.1 Onboard Oscillator

The ADS1241 requires a clock. A 4.9152MHz crystal is provided on the EVM, and may be selected as the clock source for the device when switch S8 is in the right-hand position.

## 5.3.1.1 Oscillator Kickstart (Experimental)

Because the ADS1241 is a low power device, its clock oscillator circuit does not have extremely strong drive capabilities. Using the crystal and load capacitor values provided on the EVM, the clock oscillator starts up and works reliably. However, some users may wish to try a different crystal or load capacitor values, and in some cases the ADS1241 clock oscillator will take a long time to start up.

To help decrease startup time, the circuit built around U5 is provided on the EVM. This is only for experimental purposes and has not been proven nor is it recommended; it is provided only as a possibility for decreasing oscillator startup times. This *kickstart* circuit is designed to provide a pulse of energy to the crystal to help get it started oscillating.

In use, the enable for the kickstart circuit (GPIO2) would be pulled high to activate the circuit. A rising edge would then be applied to GPIO1, which should result in a pulse appearing at the output of C19. Once the crystal has begun oscillating, GPIO2 should be brought low to remove the kickstart circuit from the oscillator.

#### 5.3.2 External Oscillator

When S8 is switched to the left, the clock source for the ADS1241 is provided from J2.13.

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## 6 EVM Bill of Materials and Schematic

The following table contains a complete bill of materials for the modular ADS1241MEVM.

Table 7. ADS1241MEVM Bill of Materials

Reference Designator	Description	Manufacturer	Mfg. Part Number
R3, R4, R5, R6, R7, R8, R9, R10	0Ω 1/8W 5% Chip Resistor	Panasonic	ERJ-6GEY0R00V
R2, R11	10KΩ 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ103V
R1	24.9KΩ 1/16W 1% Chip Resistor	Panasonic	ERJ-3EKF2492V
RA1, RA2, RA3	100Ω 1/8W 5% 4 Resistor, 8 Terminal Network	CTS Corporation	744C083101JTR
C21	12pF 50V Ceramic Chip Capacitor, ±5%, C0G	TDK	C1608C0G1H120J
C19, C20	18pF 50V Ceramic Chip Capacitor, ±5%, C0G	TDK	C1608C0G1H180J
C2, C5	0.01µF 50V Ceramic Chip Capacitor, ±10%, X7R	TDK	C2012X7R1H103K
C13	1μF 16V Ceramic Chip Capacitor, ±10%, X5R	TDK	C1608X5R1C105K
C14, C16	1μF 16V Ceramic Chip Capacitor, ±10%, X7R	TDK	C2012X7R1C105K
C15, C18	4.7μF 6.3V Ceramic Chip Capacitor, ±20%, X5R	TDK	C1608X5R0J475M
C17	22µF 16V Ceramic Chip Capacitor, ±20%, X5R	TDK	C3225X5R1C226M
C1, C3, C4, C6, C7, C8, C9, C10, C11, C12	Ceramic Chip Capacitor - Not Installed		
X1	4.9152MHz Crystal, Thru-hole	CTS	ATS042
U1	Analog to Digital Converter	Texas Instruments	ADS1241E
U2	Op Amp	Texas Instruments	OPA350UA
U3	2.5V Reference	Texas Instruments	REF1004I-2.5
U4	256K I <sup>2</sup> C EEPROM	MicroChip	24LC256-I/SN
U5	Tri-State Buffer, Single Gate	Texas Instruments	SN74LVC1G126DBV
	ADS1241MEVM PCB	Texas Instruments	6462006
J1A, J2A	20-pin SMT Plug	Samtec	TSM-110-01-L-DV-P
J1B, J2B	20-pin SMT Socket	Samtec	SSW-110-22-F-D-VS-K
J3A	10-pin SMT Plug	Samtec	TSM-105-01-L-DV-P
J3B	10-pin SMT Socket	Samtec	SSW-105-22-F-D-VS-K
J4	5 X 2 Position Header 0.1" spacing	Samtec	TSW-105-07-L-D
J5	1 X 2 Position Header 0.1" spacing	Samtec	TSW-102-07-L-S
S1, S2, S3, S4, S5, S6, S7	SP3T Ultra-miniature switch	NKK Switches	SS14MDP2
S8	DPDT Ultra-miniature switch	NKK Switches	SS22SDP2
TP1	Miniature Test Point Terminal	Keystone Electronics	5000
	Header Shorting Block	Samtec	SNT-100-BK-T

## 6.1 ADS1241MEVM Schematic

The schematic diagram is provided as a reference.

3 REVISION HISTORY
ENGINEERING CHANGE NUMBER GPIO0 CLKX AVDD DVDD CS DIN DOUT SCLK DRDY PDWN RESET DSYNC BUFEN POL XIN XOUT DGND GPIO0 DGND GPIO1 GPIO2 DGND GPIO3 GPIO4 SCL DGND SDA CNTL
CLKX
CLKR
FSX
FSR
DX
DR
INT
TOUT
GPIO5 VREF+ VREF-AIN0/D0 AINO
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7 AIN1/D1 AIN2/D2 AIN3/D3 AIN4/D4 AIN5/D5 AIN6/D6 AIN7/D7 AINCOM R10 0 AINCOM AGND 1 3 AN1-AN0+ AN1+ 5 AN1- AN1+ 5 AN2- AN2+ 7 AN3- AN3- AN3+ 9 AGND AN4+ 111 AGND AN6+ 121 AGND AN6+ 122 VCOM AN7+ 123 AGND REF-124 AGND REF+ 8 10 12 14 16 18 AN4+ REF-REF+ C20 F 4.9152MHz ANALOGHDR S8 NKK\_SS22SDP2 VCC SDA SCL GND MCP\_24LC256-I/SN = U2 OPA350 +5VA -5VA AGND DGND +1.8VD VD1 +3.3VD +5VD U3 | C16 | T10 | T6 | T10 | T10 | T6 | T10 TEXAS INSTRUMENTS DATA ACQUISITION PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP 6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA ENGINEER M. ASHTON ADS1241MEVM DRAWN BY M. ASHTON DOCUMENT CONTROL NO. 6462007 SIZE B DATE 22-Sep-2004 REV A SHEET 1 OF 1 FILE D:\ads1241mevm\ads1241mpm.ddb - ads1241mevm.sch 2 3 4 5

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It is important to operate this EVM within the input voltage range of 2.7 V to 5 V and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30 °C. The EVM is designed to operate properly with certain components above 85 °C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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