ADS5421/22EVM

User's Guide

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Texas Instruments

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Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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ADS5421/22EVM

The ADS5421/22 evaluation module is designed for ease of use when evaluating the high-speed, analog-to-digital converters (ADCs) ADS5421 and ADS5422. Both converters offer 14 bits of resolution with sampling rates of up to 40MSPS for the ADS5421 and up to 62MSPS for the ADS5422. This EVM features two independant sections: one is configured for ac input coupling using a transformer; the other allows for dc-coupling by employing a differential amplifier. Each section is completely assembled and operational, featuring a dedicated layout; no reconfiguration by the user is needed. The data output of the ADS5421/22 converter is decoupled from the connector by a CMOS logic buffer.

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1.1 EVM Basic Functions

The ADS5421/22 evaluation module consists of 2 sections and each of the sections can be operated independently. The first section features an ac-coupled transformer input configuration, whereas the second part of the EVM implements a differential amplifier to allow for a dc-coupled front end. The configuration and layout of each of the two parts are optimized for their specific purpose.

The analog input signal is connected to the EVM via an SMA connector. Similarly, the clock is applied to a terminated SMA connector.

The digital outputs are provided in parallel form via a 32-pin connector. The output bus is buffered such that the converter is not directly driving the cable or load that is connected at the header.

Using screw-on terminals on the board makes power connections to the EVM.

1.2 Power Requirements

To provide optimal performance, the EVM is powered with independent analog, digital, and I/O supplies. The ADS5421/22 converter itself operates with a +5V analog supply and a +3.3V supply for its output driver. Both supplies are connected using terminal J2 or J201 (labeled 5V DUT, GND, 3V DUT). Also, the board requires a +5V supply for the clock circuit and a +3.3V supply for the digital output buffer (SN74x16244). Connect the corresponding supply voltage to terminal J1 or J200 (labeled Output DRV, GND, Clk). To operate the section of the EVM that includes the differential amplifier, an additional ±5V supply must be connected to terminal J202 (labeled +5V OpAmp, GND, –5V OpAmp).

1.3 Signal Inputs

The evaluation module provides the option to evaluate the ADC with either an amplifier-based differential interface, or with a transformer-couple interface.

1.3.1 Transformer Coupled Input

The transformer is used to convert the single-ended input signal applied to SMA connector J5 into a differential signal suitable to interface to the converter. Note that the transformer model used on the EVM has a step-up voltage ratio of 1:2 (primary to secondary) and a 1:4 impedance ratio. The default setting of the converter full-scale input range is 4Vp–p. The primary side of the transformer is terminated with 50Ω. The secondary side uses a simple RC filter (R15, R16, C34) before going into the differential inputs of the ADC. The installed values have been established to provide good performance results. However, depending on the system requirements, the component values may be adjusted for further optimization.

1.3.2 Amplifier Input

The second section of the EVM provides for a dc-coupled interface to the ADC. To implement this, the THS4503 differential amplifier is used and gain is set for 2V/V. Coming from an appropriate source, the single-ended input signal is applied to SMA connector J205. The input impedance seen by the source is approximately 50Ω. It is important to note that the source impedance must be at 50Ω as well and be of a resistive nature. This is because the differential gain of the amplifier assumes this 50Ω value and any deviation from this value will result in an additional offset term at the output of the amplifier. This in turn can cause the data from the ADC to be shifted and out-of-range. Details for configuring the gain on the differential amplifier correctly, as well as using the amplifier as an active low-pass filter (with C214 and C1218) can be found in the THS4503 product datasheet located at www.ti.com.

1.4 Input Full-Scale Range Selection

By using the V_{REF}, SEL1 and SEL2 pins, the full-scale range of the ADS5421/22 can be set to 2Vp–p, 3Vp–p, or 4Vp–p.

Table 1. Reference and Full-Scale Range Select

Desired Full-Scale Range	SEL1	SEL2	Internal V_{REF}
4Vp–p	GND	GND	2V
3Vp–p	GND	$+V_S$	1.5V
2Vp–p	V_{REF}	GND	1V

NOTE: For external reference operation, tie V_{REF} to $+V_S$. The full-scale range will be 2x the reference value. For example, selecting a 2V external reference will set the full-scale values of 1.5V to 3.5V for both IN and $\overline{IN}$ inputs.

Changes to the full-scale range can easily be made by reconfiguring the corresponding jumpers.

1.5 Clock

The ADS5421/22EVM requires an external clock signal applied to either SMA connector J204 or J304, depending on which section of the EVM is evaluated. Both sections feature an active clock conditioning circuit using the IC SN65LVDS101 high-speed translator. The input clock signal can be either a sine wave or a square wave signal with a minimum amplitude of 500mVp–p. The translator is configured to provide a low-jitter, low-skew differential clock output feeding into the differential clock input pins of the ADC. The clock inputs of the converter are internally biased and in order to maintain this common-mode voltage, the clock signal is ac-coupled.

1.6 Data Output

The data output of the converter is buffered by a 3.3V, low-voltage CMOS buffer (SN74ALB16244 or equivalient).

1.7 External Reference

The ADS5421/22EVM can be configured for external reference operation. To disable the internal reference, the V_{REF} pin of the converter must be tied to logic high (V_{REF} > 3.5V). External top- and bottom-reference voltages (REFT and REFB) can now be connected to the test points located on the EVM (REFT – TP1 or TP200, REFB – TP2 or TP201). If not already connected, the ground/return path of the reference voltages must be connected to the EVM ground to ensure proper operation.

1.8 PCB Layout

The ADS5421/22EVM is constructed on a 5-layer printed circuit board using FR-4 material. The dimension of the board is approximately 91mm (3.6inch) x 100mm (4inch).

Figure 1. Top Layer with Silkscreen

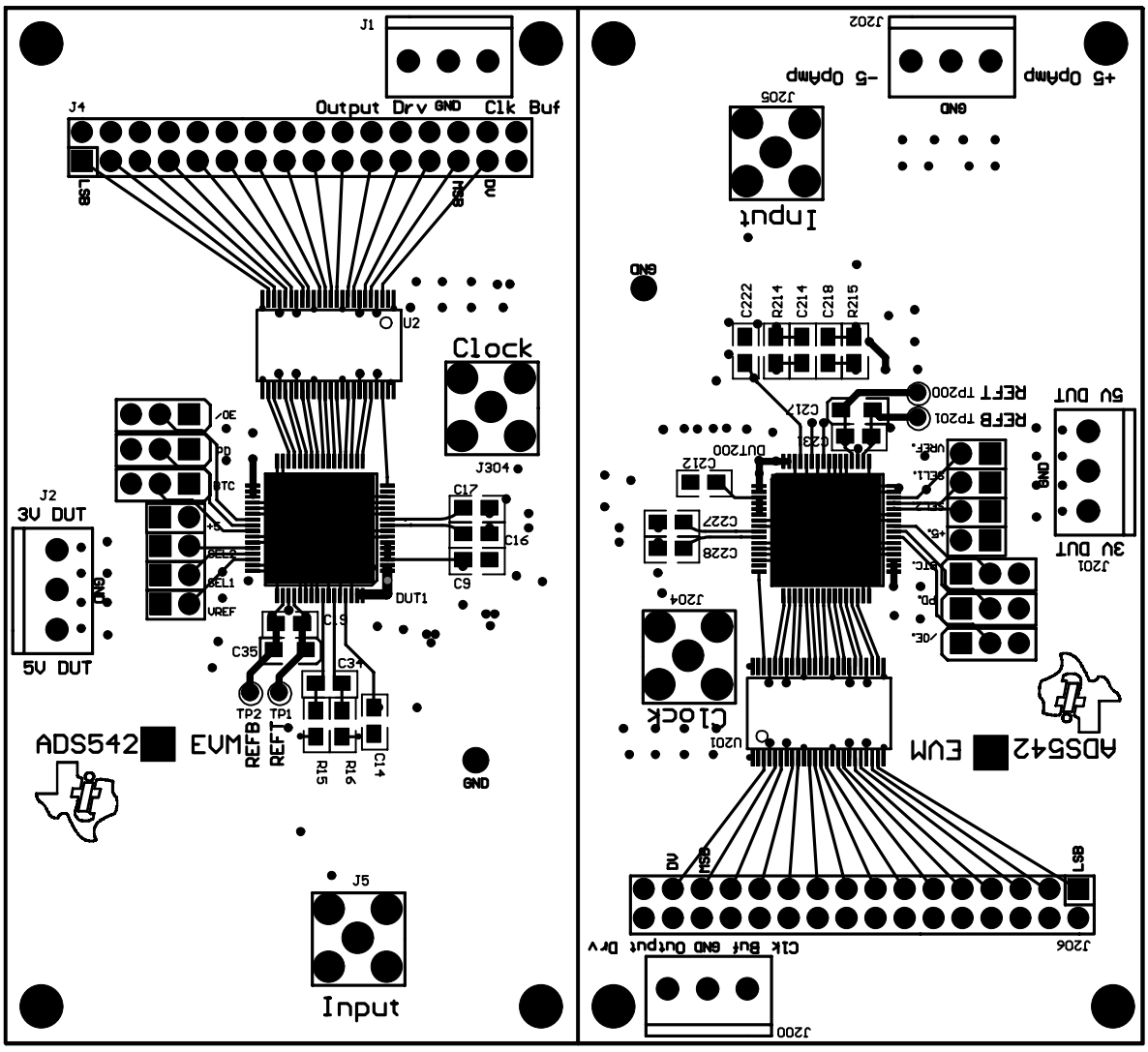


Figure 2. Ground Plane—Inner Layers 1 and 3

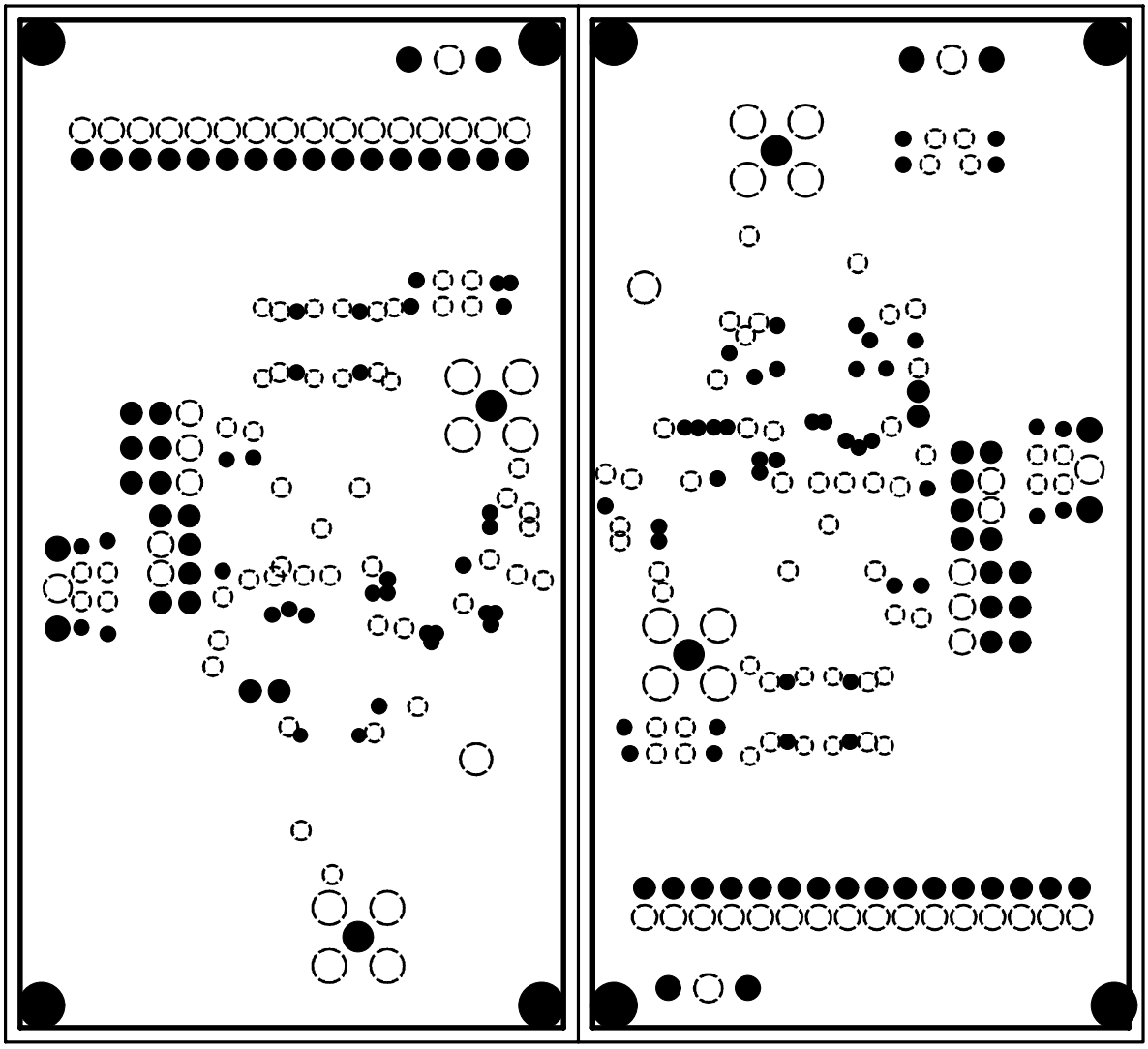


Figure 3. Power Plane—Inner Layer 2

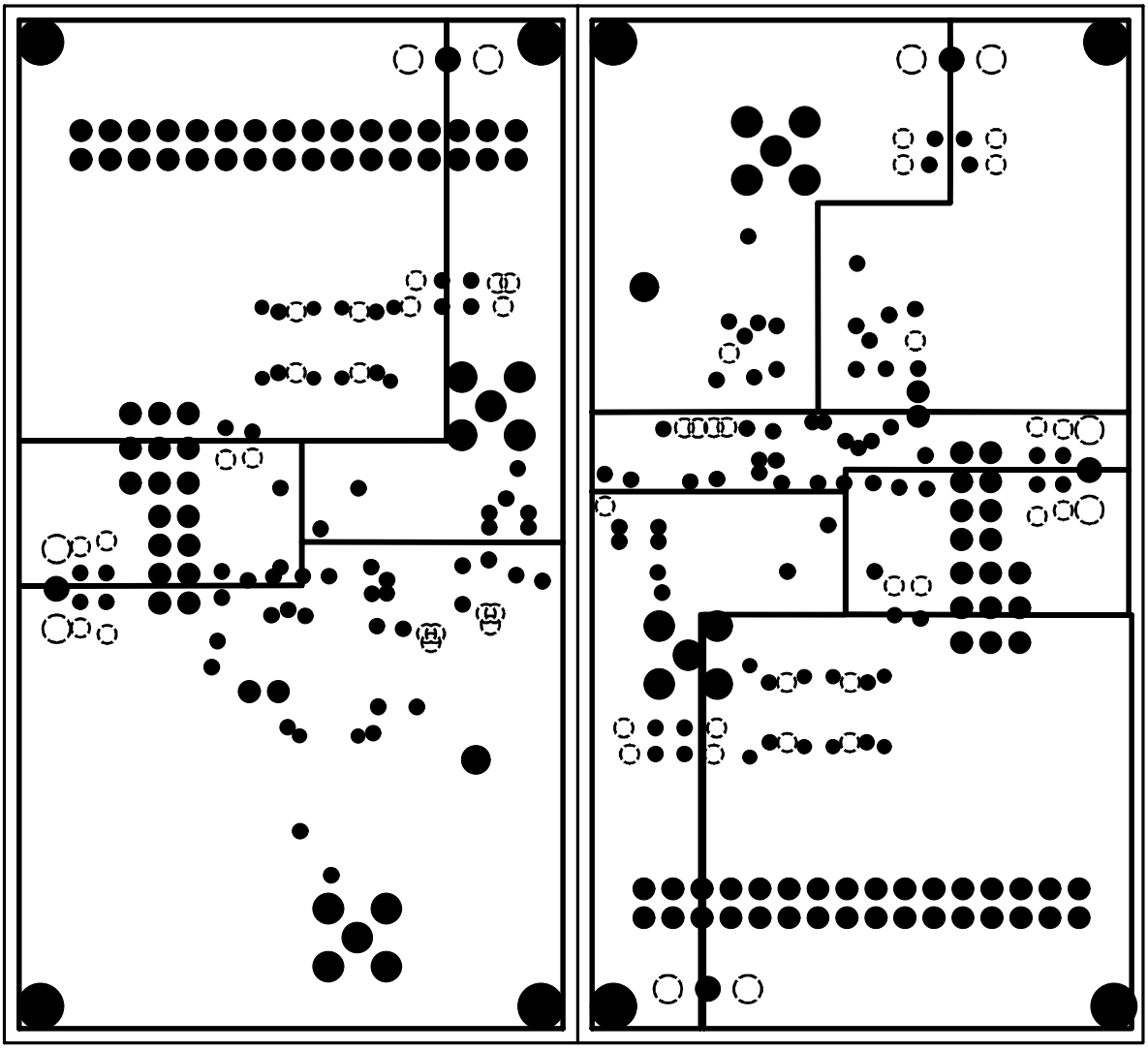


Figure 4. Bottom Layer with Silkscreen

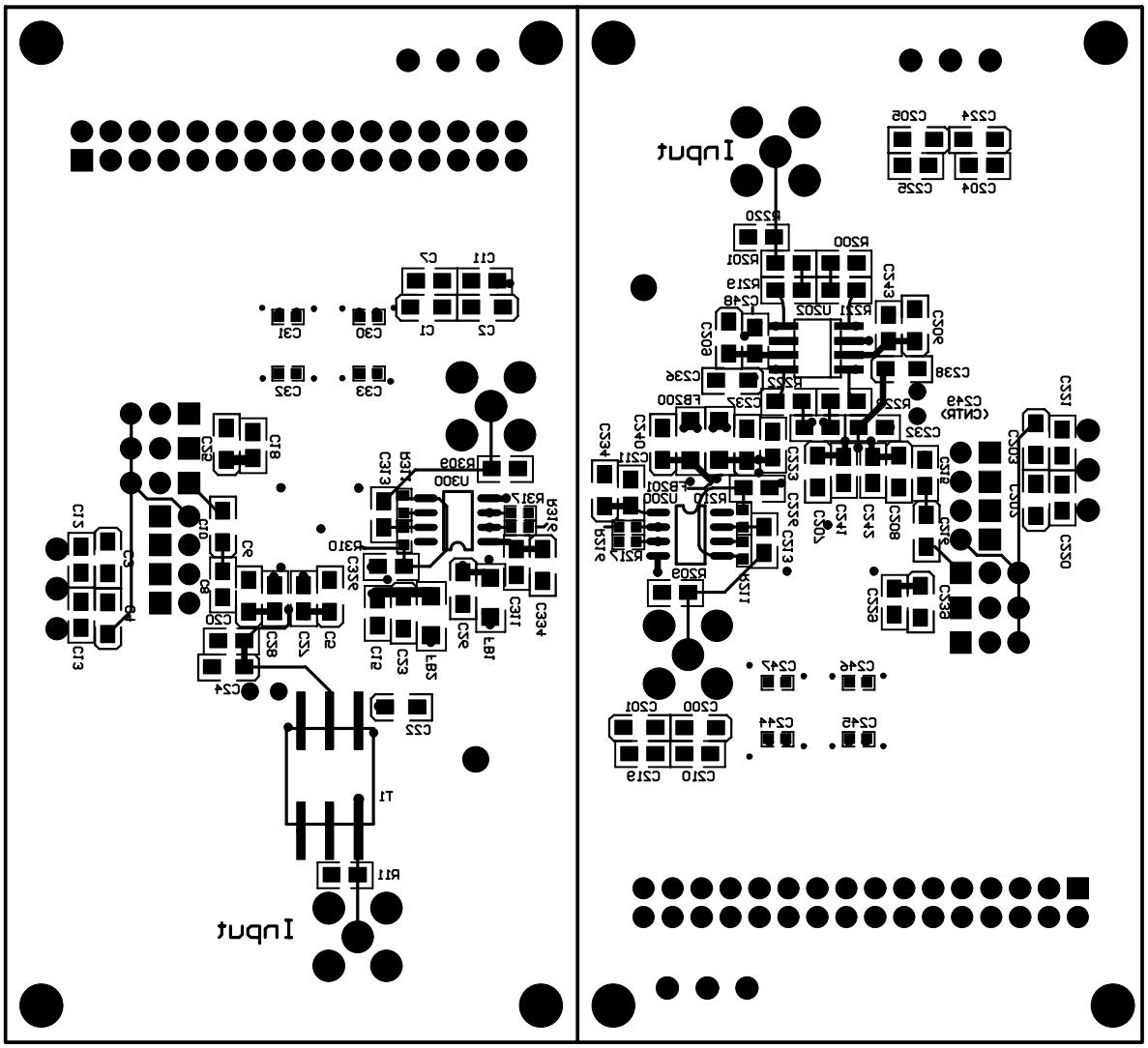


Figure 5. Schematic for Transformer-Coupled Interface

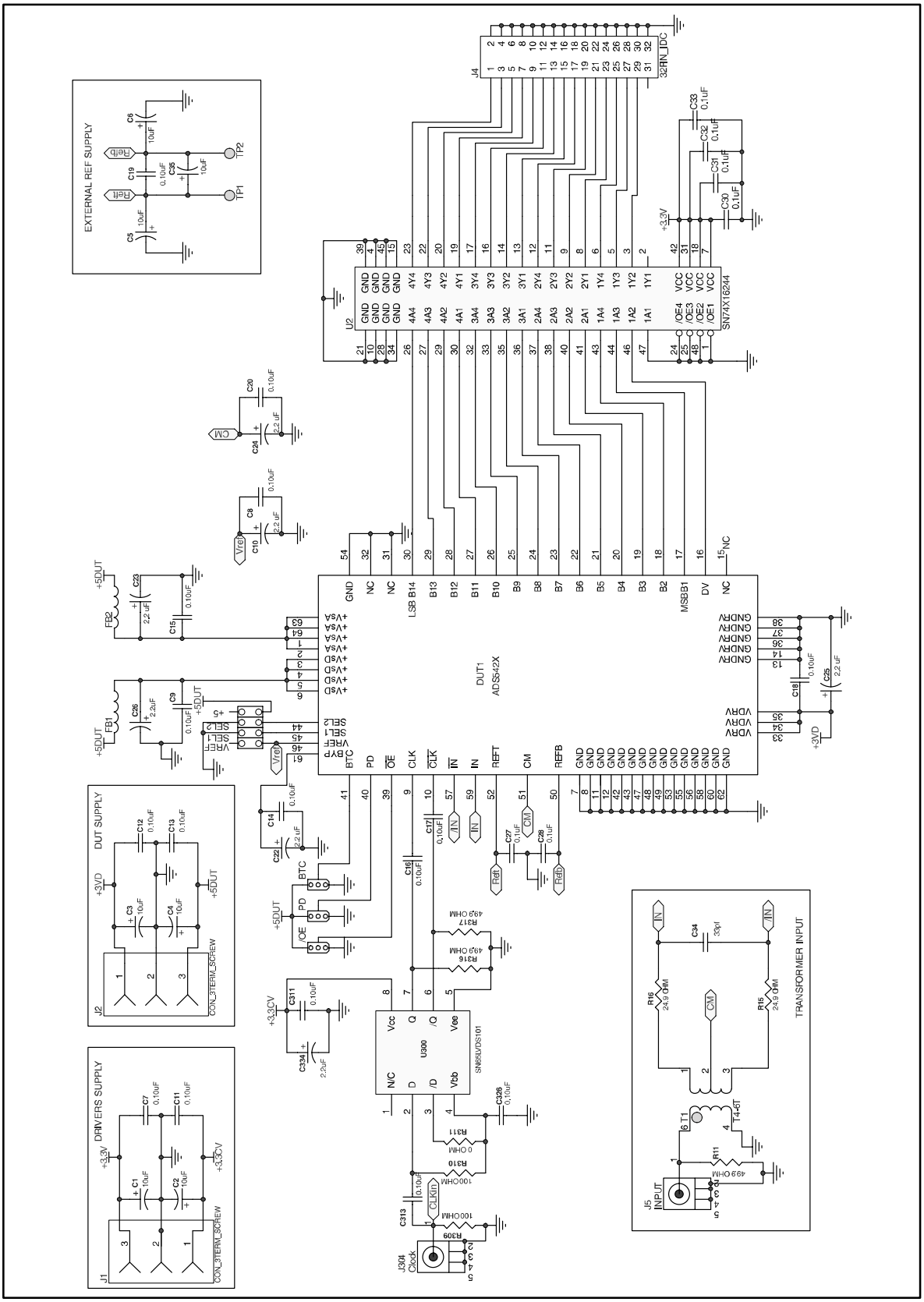
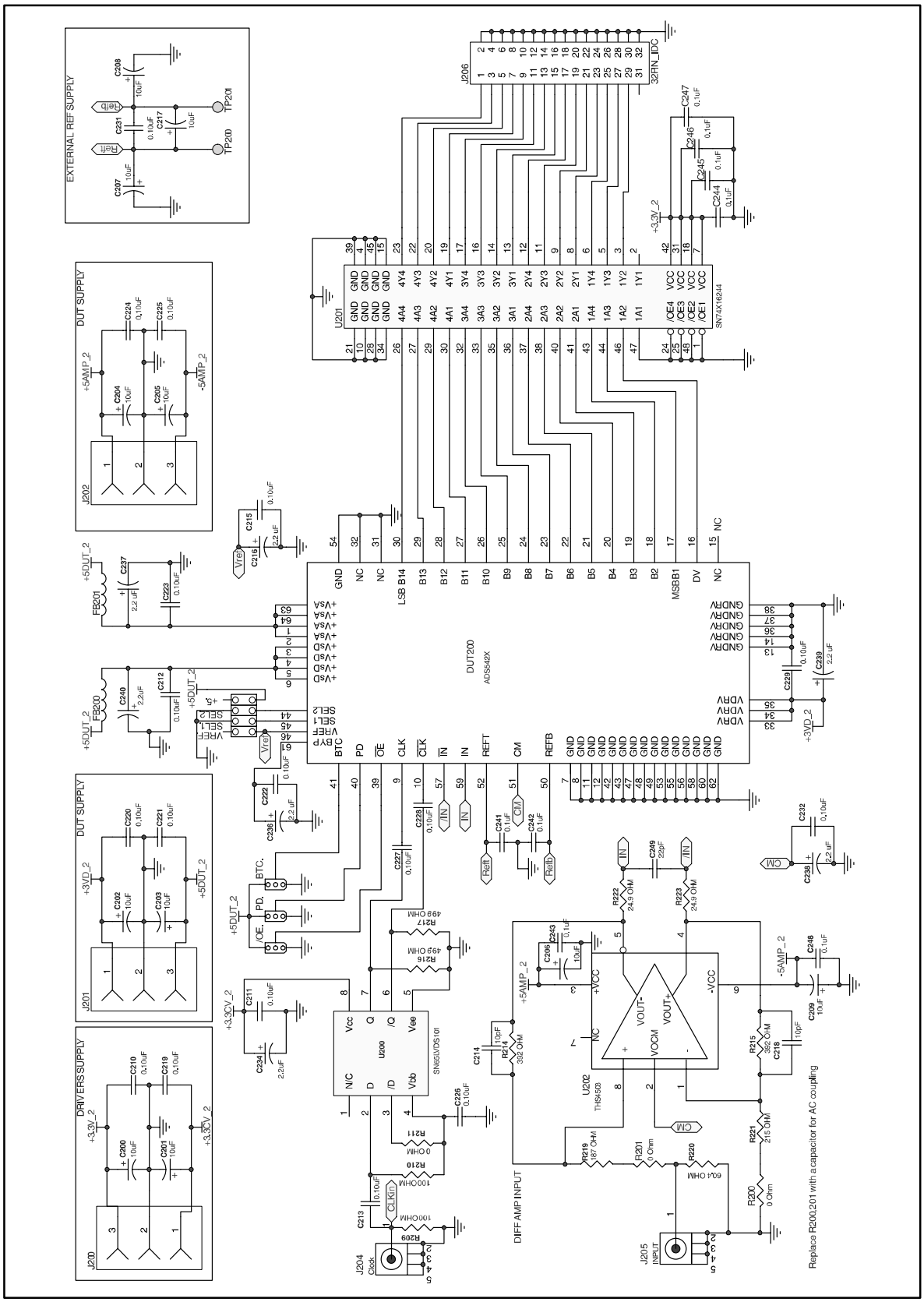


Figure 6. Schematic for Amplifier-Based Differential Interface



1.9 Component List

Table 2. Component List

Qty	Part Type	Designator	Footprint	Mfg	Part Number	Description
8	0.1µF	C30–C33, C244–C247	603	Digi-Key	PCC1762CT-ND	MultiLayer ceramic – variable footprint
40	0.1µF	C7–C9, C11–C20, C27, C28, C210, C211, C215–C232, C241–C243, C248, C311, C326	805	Digi-Key	399–1171–1–ND	MultiLayer ceramic – variable footprint
2	10pF	C214, C218, C313	805	Digi-Key	311–1099–1–ND	MultiLayer ceramic – variable footprint
2	0Ω	R200, R201	805	Digi-Key	311–0.0ACT–ND	1/10W 0805 chip resistor
2	0Ω	R211, R311	603	Digi-Key	P0.0GCT–ND	1/16W 5% 0603 SMD
2	100Ω	R210, R310	603	Digi-Key	P100GCT–ND	1/16W 5% 0603 SMD
14	2.2µF	C10, C22–C26, C216, C234, C237–C240, C334	3216	Digi-Key	399–1586–1–ND	Low profile tantalum capacitor
8	2POS_JUMPER	SEL1, SEL1., SEL2, SEL2.	2pos_jump	Digi-Key	A26542–ND	CONN HDR 2POS 30AU STRGHT PCB
6	3POS_JUMPER	$\overline{OE}$, $\overline{OE}$., BTC, BTC., PD, PD.	3pos_jump	Digi-Key	A26544–ND	CONN HDR 3POS 30AU STRGHT PCB
18	10µF	C1–C6, C35, C200–C209, C217	3216	Digi-Key	PCS2106CT–ND	Low profile tantalum vapacitor
1	22pF	C249	805	Digi-Key	311–22CCT–ND	MultiLayer ceramic – variable footprint
4	24.9Ω	R15, R16, R222, R223	805	Digi-Key	311–24.9CCT–ND	1/10W 0805 chip resistor
2	32PIN_IDC	J4, J206	16X2X.1	Digi-Key	1–103186–6–ND	CONN HDR 32POS STRGHT PCB
1	33pF	C34	805	Digi-Key	399–1115–1–ND	Multilayer ceramic – 0805 Size
4	49.9Ω	R216, R217, R316, R317	603	Digi-Key	P49.9CCT–ND	1/10W 0603 chip resistor
3	49.9Ω	R11	805	Digi-Key	RR12Q49.9DCT–ND	1/10W 0805 chip resistor
1	60.4Ω	R220	805	Digi-Key	P60.4CCT–ND	1/10W 0805 chip resistor
2	100Ω	R209, R309	805	Digi-Key	P100CCT–ND	1/10W 0805 chip resistor
1	187Ω	R219	805	Digi-Key	P187CCT–ND	1/10W 0805 chip resistor
1	215Ω	R221	805	Digi-Key	P215CCT–ND	1/10W 0805 chip resistor
2	392Ω	R214, R215	805	Digi-Key	P392CCT–ND	1/10W 0805 chip resistor
2	ADS542X	DUT1, DUT200	PQFP-64 (PM)	TI	ADS5421/ADS5422	ADS5421/ADS5422 (as required)
5	CON_3TERM_SCREW	J1, J2, J200–J202	3P-TERM	Digi-Key	ED–1515–ND	3-terminal screw connector
4	SMA_JACK	J5, J204, J205, J304	SMA_JACK	Johnson	142–0701–231	SMA_JACK_STRAIGHT
4	FERRITE	FB1, FB2, FB200, FB201	1206	Digi-Key	P10437CT–ND	Ferrite Bead
2	SN65LVDS101	U200, U300	SO-8	TI	SN65LVDS101	Differential translator, repeater
2	SN74ALVCH16244	U2, U201	TSSOP-48 (DGG)	TI	SN74ALVCH16244	16-bit buffer, tri-state
1	T4–6T	T1	TTWB	MiniCircuits	T4–6T	Transformer
1	THS4502	U202	SO-8 (D)	TI	THS4502	Op amp