Application Brief

Dynamic Voltage Scaling (DVS) Using TPS6282xA and TPS62830x

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What is DVS?

Dynamic Voltage Scaling (DVS) in a buck converter is a control technique where the output voltage of the converter is dynamically adjusted in real-time based on changing load conditions or system requirements. This feature is used to improve energy efficiency, reduce power consumption, and adapt to varying performance demands. For example, lower the voltage during light-load or idle conditions to save power and increase the voltage during high-performance tasks to meet computational demands as illustrated in Figure 1.

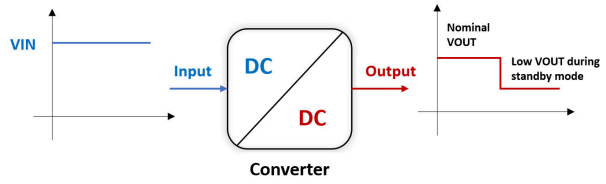


Figure 1. Dynamic Voltage Scaling (DVS) in DC/DC converter

How DVS works?

There are several methods to adjust the output voltage of a buck converter during steady-state operation:

Digital Interfaces

Protocols like I²C, PMBus, or proprietary interfaces enable the system to send voltage adjustment commands to the buck converter. Applications such as solid-state drives (SSDs), smartphones, and optical modules use these interfaces to dynamically adjust the core voltage of the main processor, optimizing performance and power consumption.

Feedback Pin Current Injection

The output voltage can be modified by externally sourcing or sinking current into the feedback node using an analog control voltage with a series resistor. This analog control voltage can be generated from:

- A discrete voltage reference (for example, TLV431)
- An MCU's internal voltage reference
- A digital-to-analog converter (DAC)
- A PWM signal filtered with an RC network

This method allows for continuous voltage adjustment, making it ideal for dynamic voltage scaling (DVS) in applications like CPUs, where the voltage is reduced during low-power states and increased during high-performance tasks.

Feedback Resistor Divider Adjustment

In this method, the output voltage is adjusted by modifying the feedback divider network's resistance. This can be done by:

- Adjusting the bottom feedback resistor (R_2)
- Adjusting the top feedback resistor (R_1)

A switch-controlled resistor (in parallel with R_1 or R_2) is used to vary the output voltage. This approach is best suited for systems requiring two fixed voltage levels (high/low), such as USB Type-C® power delivery or low-power MCUs switching between active and sleep modes.

This application brief describes how to dynamically change the output voltage by toggling a switch in the feedback network as illustrated in Figure 2. This method enables dynamic transition of output voltages between the converter's lowest possible output, which is feedback voltage and a higher preset output voltage. Adding another series resistance with the switch enables other voltage combinations.

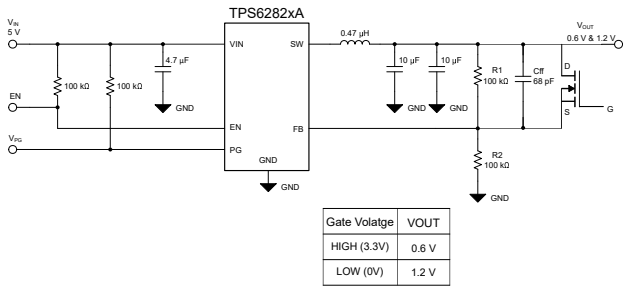


Figure 2. Example Application for DVS With TPS62826A

The TPS6282x is available in two flavors. The first includes an automatically entered power save mode to maintain high efficiency down to very light loads for extending the system battery run-time. The second runs in forced-PWM maintaining a continuous conduction mode to make sure of the least ripple in the output voltage and a quasi-fixed switching frequency.

For Dynamic Voltage Scaling (DVS), forced-PWM operation is required during high-to-low output voltage transitions to maintain rapid and controlled discharge of the output capacitors. When stepping down the voltage, excess stored charge on the output capacitors must be actively removed by sinking negative inductor current to GND through the low-side MOSFET and to VIN via the high-side MOSFET.

In non-forced-PWM modes (PFM or DCM), the converter stops switching when the actual output voltage is higher than the target output set by the feedback network and internal reference voltage. This leaves no low impedance path to discharge the output capacitors and results in slow voltage decay reliant on parasitic resistances or load current. Forced-PWM avoids this by maintaining continuous conduction, ensuring the synchronous rectifier remains active to provide a dedicated discharge path.

A simple N-channel MOSFET (SI1300BDL) is connected in parallel with the upper feedback resistor (R1) to enable Dynamic Voltage Scaling (DVS). When a 3.3V gate drive (relative to GND) is applied, the MOSFET turns on, shorting R1 and forcing the feedback node to regulate at the reference voltage (0.6V). A feedforward capacitor (Cff) is critical across R1 to maintain control-loop stability during voltage transitions, compensating for the abrupt impedance change and mitigating transient oscillations.

The feedforword capacitor (Cff) value must be empirically adjusted during bench testing to balance transition speed and loop stability. Too small a value risks undershoot/ringing, while too large a value slows the response. Optimal selection depends on the converter's crossover frequency, load step characteristics, and observed transient behavior during DVS transitions.

Figure 3 shows the DVS behavior of TPS62826A with 5V input voltage, 0A load current and 68 pF Cff.

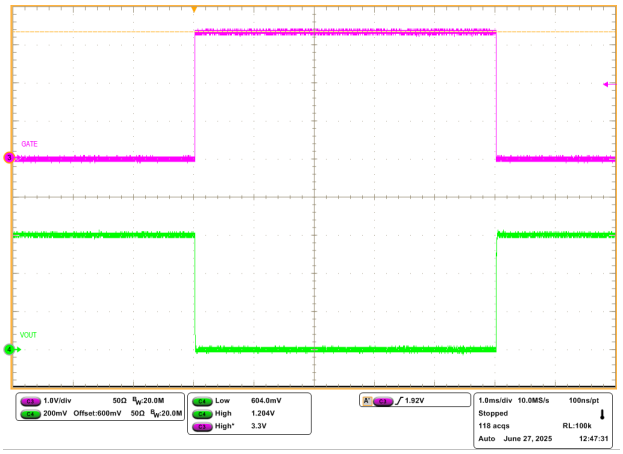


Figure 3. TPS62826A DVS

Figure 3 demonstrates the DVS operation, where the output voltage transitions from the default 1.2V down to the feedback-regulated standby voltage (0.6V) when a 3.3V gate drive signal (with 10ns rise/fall times) is applied to the N-channel MOSFET.

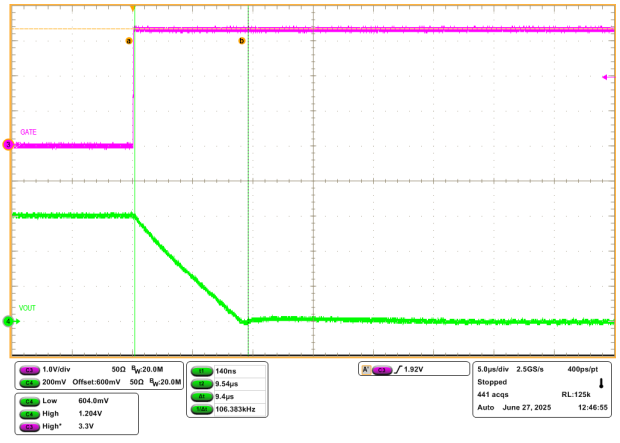


Figure 4. TPS62826A DVS (VOUT falling transition)

Figure 4 (VOUT falling edge zoom) shows the output voltage transition from 1.2V to 0.6 within 10µs. This time depends upon the low-side FET negative current limit during output capacitor discharge.

Figure 5 (VOUT rising edge zoom) demonstrates the output voltage transition from 0.6V to 1.2V within 20µs. This transition time to charge the output capacitors to the new output voltage is determined by Cff and the control loop bandwidth.

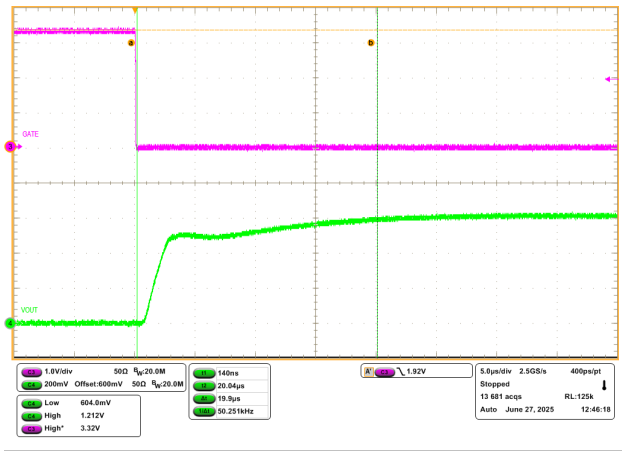
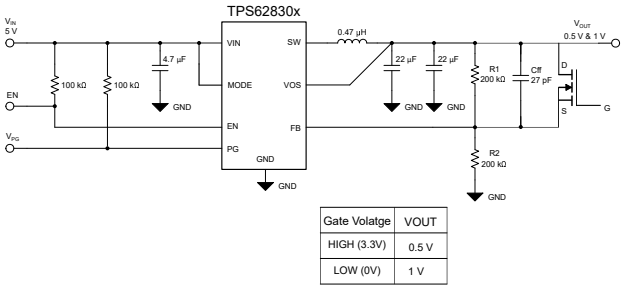


Figure 5. TPS62826A DVS (VOUT raising transition)

Implementing DVS With TPS62830x

Unlike TPS6282x, TPS62830x has a MODE pin to control the device mode of operation. The device runs in PSM/PWM mode when this pin is pulled low and in forced-PWM mode when pulled high. The mode pin can also be toggled when the device is in operation. The TPS62830x family is natively supporting an output voltage of 0.5V when the feedback is directly connected to VOUT. The circuit diagram of TPS628303 for DVS using feedback network is shown in Figure 6.



Gate Volatge	VOUT
HIGH (3.3V)	0.5 V
LOW (0V)	1 V

Figure 6. Example Application for DVS With TPS628303

The TPS62830x integrates an internal feedforward capacitor, eliminating the need for an external Cff in typical applications. However, when implementing Dynamic Voltage Scaling (DVS) via feedback network adjustment, a small external feedforward capacitor is required to prevent overshoot during low-to-high voltage transitions (0.5V to 1V).

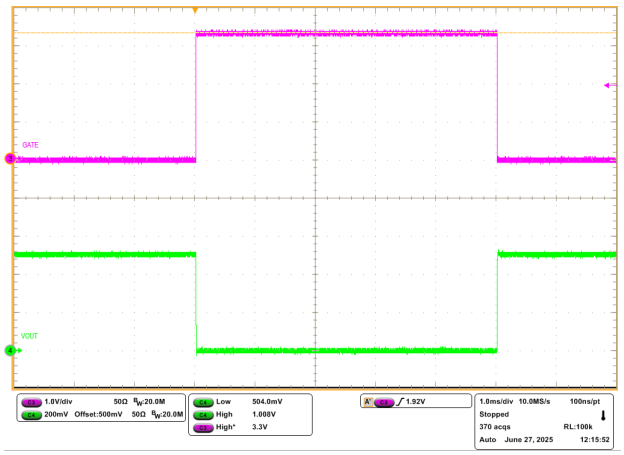


Figure 7. TPS628303 DVS

Figure 7 demonstrates the DVS operation, where the output voltage transitions from the default 1V down to the feedback-regulated standby voltage (0.5V) when a 3.3V gate drive signal (with 10ns rise/fall times) is applied to the N-channel MOSFET (SI1300BDL).

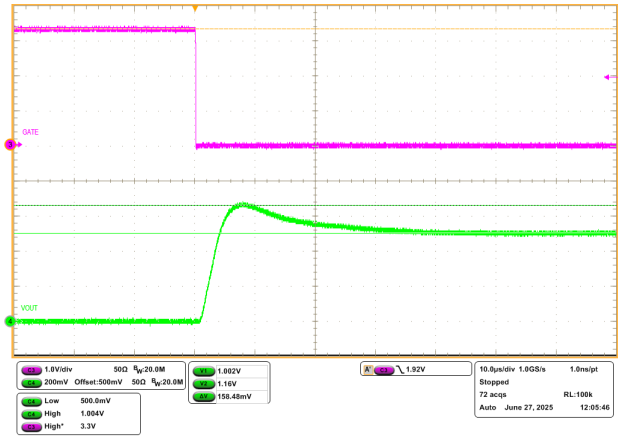


Figure 8. TPS628303 DVS Without Feedforward Capacitor (Cff)

Figure 8 (VOUT rising edge zoom) shows the output voltage recovery from 0.5V to 1V without an external feedforward capacitor (Cff). The transition completes in approximately 4µs but exhibits a 160mV overvoltage. In contrast, Figure 9 demonstrates the same voltage transition after adding a small external Cff (27pF) across the top feedback resistor (R1), which eliminates the overshoot while maintaining an optimal transition time of 10µs.

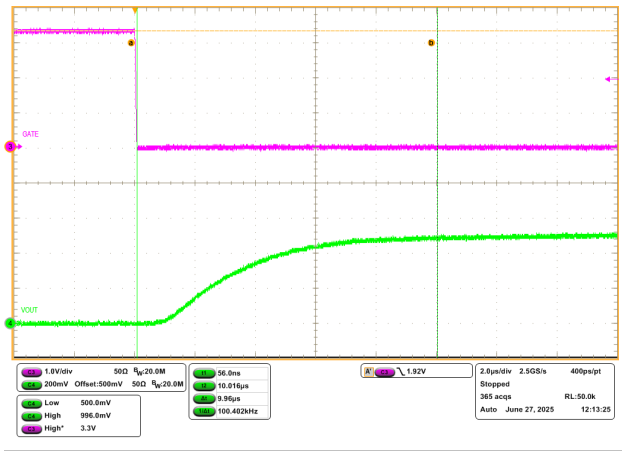


Figure 9. TPS628303 DVS With Feedforward Capacitor (Cff)

TPS628303 has faster transition time compared to TPS62826A because of it is dedicated output voltage sense (VOS) path which improves transient response. Along with the dedicated VOS pin, there are other factors such as, bandwidth, compensation which are influencing the loop response in TPS62830x.

TPS62830x – Dual Source Package

The TPS62830x device family is available in two package types (QFN and SOT583), which are layout compatible. When considered in the design phase, the board designers can overlap both package footprints like in Figure 10. This overlap provides flexibility to switch between packages and mitigate any potential supply issues.

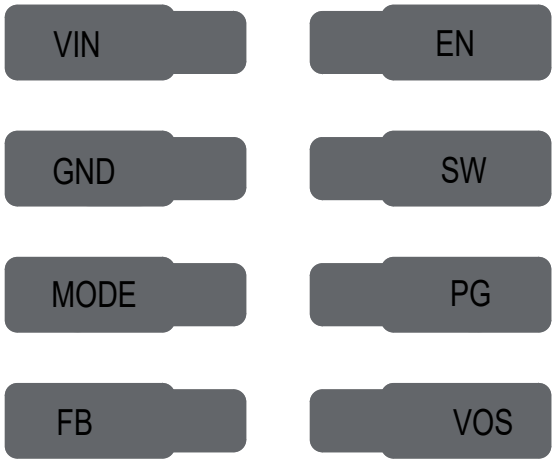


Figure 10. Overlapped QFN and SOT583 Footprints

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