Application Note

Cold Sparing of the AFE7950-SP/SEP



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ABSTRACT

This document describes the AFE7950-SxP device cold sparing care-abouts for RF input ports, clocks, SYSREF, SerDes and GPIO pins. Cold sparing is a common scenario in space applications where the AFE device is in a powered-off state but the ports are driven by FPGA, clock chips, and RF LNA drivers, for example. The key requirement in this device state is that the AFE ports are not damaged as a result of the signals being applied.

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1 Introduction

Space satellites typically deploy a main module and a backup module. This redundant backup module is activated by the onboard computer only when the main module encounters issue and is powered off. Cold sparing is a fault-tolerant technique where the backup AFE7950-SxP is kept powered off and non-operational until it is needed to replace the main AFE7950-SxP. This method is used to maintain system uptime and verify continued operation in the unlikely event of component failures. This application note details all of the care that must be taken when the AFE is powered off but is still being driven by peripheral drivers such as an FPGA driving GPIOs, SerDes, Dev/RefCLK and SYSREF on the clocking paths, and LNA drivers on the receiver (Rx) path. The objective is to make sure that the AFE is not electrically over-stressed, which prevents damage to the device.

2 Cold Sparing for AFE Ports

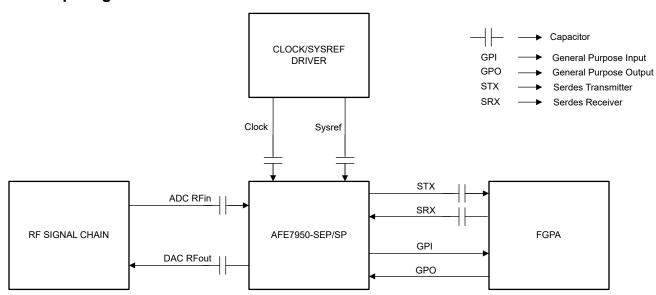


Figure 2-1. Simplified Block Diagram of AFE7950-SxP with Peripheral Drivers



2.1 RF Rx Input Port

The RF input ports have ESD protection diodes connected to the analog voltage supply. The max current handling capacity limit of the diode is 10mA. As the input port is always AC coupled, there are no DC current requirements. For AC signals, maintain the RF signal at the Rx port to be under the reliability limit of approximately 17dBm.

Table 2-1. Max Full Scale Power at Rx Pins

P _{FS_CW,MAX}	MAX Full scale input power - reliability limited at device pins	f _{IN} = 830MHz	16.7	dBm
		f _{IN} = 1760MHz	17	dBm
		f _{IN} = 2610MHz	18	dBm
		f _{IN} = 3610MHz	18.5	dBm
		f _{IN} = 4910MHz	19.3	dBm

2.2 Dev/RefClock and SYSREF Ports

The Dev and RefClock and SYSREF ports have ESD protection diodes connected to an internally regulated 1V supply. The maximum power into these ports is limited to 10dBm for AC coupling mode of the Dev and RefClock and SYSREF inputs. The maximum current handling capacity limit of the diode is 10mA for DC coupling mode of the SYSREF and clock inputs. TI recommends to bring up the external reference clock and SYSREF driver after powering up the AFE supply rails to avoid cold sparing on these ports.

2.3 GPIO Input Ports

All GPIO inputs ports have ESD diodes connected to VDDGPIO1p8V. TI recommends using 100Ω in series with the external FPGA driver to limit current drive.

An alternative approach is to configure the FPGA outputs as *inputs* when the AFE is powered down. In the normal use case, the SPI ports are driven by an FPGA towards the AFE. During cold sparing, these ports can be configured as inputs on FPGA at power up (so there is no driver to AFE) and after the AFE is powered up, re-configure them as outputs to initiate the programming of the AFE.

Similarly, this approach can be taken for the AFE LVDS SYNC input pins.

2.4 GPIO Output Ports

TI recommends using a 100Ω current limiting resistor in series for all GPIO output ports to protect the FPGA input ports.

2.5 SerDes Rx Ports

SerDes Rx ports have ESD diodes connected to VDDA 1.8V. The maximum current handling capacity limit of the diode is 10mA. SerDes Rx ports are typically AC coupled and must be limited to a differential swing of 1Vpp.



3 Summary

This application note captures the key requirements for cold sparing of the AFE7950-SxP for space applications. This document provides the requirements for RF inputs and outputs, GPIOs and SerDes inputs that must be addressed when the AFE is powered off, but driven by the peripheral drivers.

4 References

• Texas Instruments, AFE7950-SxP 4T6R Space-grade RHA RF Sampling AFE, data sheet.

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