Implementing HART in PLC Analog Input Modules for Real-Time Communication in 4-20mA Systems

Garrett Satterfield

Introduction

HART enabled field devices are ubiquitous in factory automation and process control applications, allowing bidirectional digital communication over the 4-20mA analog current signal. Often, HART is used to transmit diagnostic or calibration information but can also be used to transmit additional control variables to the PLC. To take full advantage of HART enabled field devices, a HART enabled PLC analog input module (AI) is required to communicate with the field device in real-time. A HART enabled analog input module consists of an ADC and sense resistor to measure the analog current, and a HART modem to modulate an demodulate the HART data.

The DAC874xH family of devices are standalone modems supporting HART, Foundation Fieldbus, and Profibus PA. These HART certified modems feature SPI/UART interface options, internal filtering, and additional SPI features that add flexibility interfacing with the host MCU, making DAC874xH an excellent option for analog input module designs requiring HART.

Overview of HART in AI Modules

Figure 1 illustrates a simplified diagram of a HART enabled analog input module. R1 is the sense resistor that both senses the loop current and enables HART communication. The HART physical layer specification requires R1 to be between 230 Ω and 600 Ω. R2 and C1 form a low pass filter to ensure the ADC only measures the DC loop current and the HART modulation is sufficiently attenuated. Depending on the ADC selection, additional filtering can be achieved with the ADC internal digital filter. C2 and C3 AC couple the HART modem input and output to the load resistor.

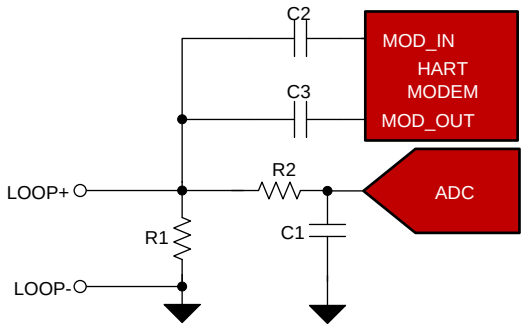

Figure 1. Simplified Analog Input Module with HART

The HART communication protocol is a master/slave communication scheme. The input module acts as the master and sends requests for data to the slave transmitter or field device. The slave transmitter regulates the loop current and transmits HART as a 1mApp sinusoidal waveform that is converted to a voltage signal by R1 and demodulated by the HART modem at the analog input module. When the analog input module transmits HART it directly couples the voltage signal to the load resistor, creating a HART voltage waveform that is demodulated by the HART modem in the field device.

Design Considerations

When designing an input module with HART it is critical to meet requirements outlined by the HART specification while also meeting the input requirements for the ADC selected. The simplified circuit shown in Figure 1 shows a single load resistor, but it is often more practical to split the load resistor in to three series resistors. At full-scale loop current the voltage at LOOP+ will be outside the range of most precision ADCs if a single resistor is used. This allows flexibility in meeting the input requirements for the ADC while still maintaining the required overall resistive load required for HART. Another advantage of the split load resistor configuration is decreasing the sense resistor value which reduces self heating and drift, minimizing error in the loop current measurement over the current input range.

Figure 2 illustrates a practical example of a HART enabled analog input module that uses separate current sense and HART load resistors. DAC8740H is the UART interfaced HART modem. ADS1260 is a delta-sigma ADC with internal programmable gain amplifier (PGA) that measures the voltage across the current sense resistor to calculate the DC loop current. The HART signal is modulated and demodulated across the sum of the three resistors. R2 is the current sense resistor and R3 is used to bias the voltage at the negative input of the ADC as the PGA cannot inputs cannot go to ground. The internal PGA allows for use of a smaller current sense resistor reducing self-heating error. For ADS1260 the input requirements arise from the internal PGA headroom requirements. Resistors R3 and R2 must be selected to appropriately set the voltage at both inputs of the ADC. The voltage requirements at the PGA inputs

must be satisfied over the entire input current range. The PGA's absolute input voltage requirements depend on the input supply, differential input voltage, and the PGA gain setting. R1 is required to ensure the minimum HART load resistance requirement is met.

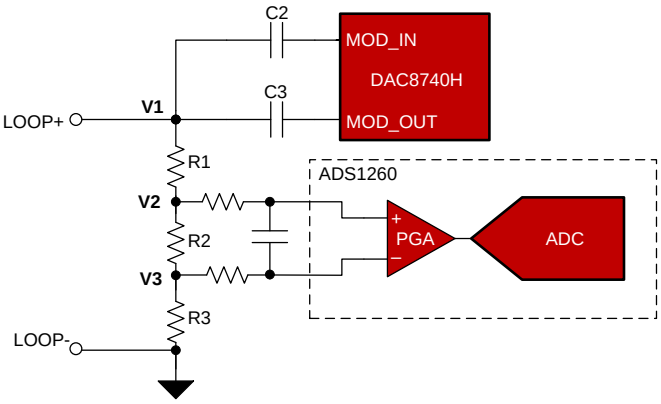

Figure 2. Load Resistor Considerations

Equation 1 shows the voltage present at the ADC inputs after the internal PGA gain. The loop current measurement is only dependent on the differential voltage across R2. Equation 2 and Equation 3 calculate the voltage at V2 and V3 respectively. These values are chosen first based on the absolute PGA input requirements, differential input voltage, input current range, and PGA gain. R1 is chosen based on Equation 4 to meet the HART load resistance requirement.

$$V_{ADC} = I_{LOOP} \times R2 \times GAIN \quad (1)$$

$$V2 = I_{LOOP} \times (R2 + R3) \quad (2)$$

$$V3 = I_{LOOP} \times R3 \quad (3)$$

$$230\Omega \le R1 + R2 + R3 \le 600\Omega \quad (4)$$

C2 and C3 isolate the DC loop current value from DAC8740H and allow the HART signal to pass. The recommended value for C2 is 2.2nF as it forms the required HART filter along with components internal to DAC8740H. This filter ensures any change in the DC value does not impact the HART demodulation and also attenuates high frequency noise while requiring few external components. C3 forms a high pass filter with the total load resistance. C3 is chosen to be large enough that the cutoff frequency does not impact the modulated HART signal. Typically, 2.2 µF is an appropriate value for C3.

HART Physical Layer Compliance

When designing a HART enabled analog input module, physical layer test requirements must be met for HART certification. The HART specification defines the test setup and pass criterion for each device type. Figure 3 shows the test setup for a low impedance current input device or analog input module, and Figure 4 shows a 1200-Hz waveshape measurement example. A DC voltage source and high impedance current source are used to set the DC operating point of the input module. The HART physical layer tests for an analog input module include waveshape, output noise, receive/send impedance, and noise sensitivity among other test requirements. For full information on the testing process and test results see the HART analog input module Reference Design.

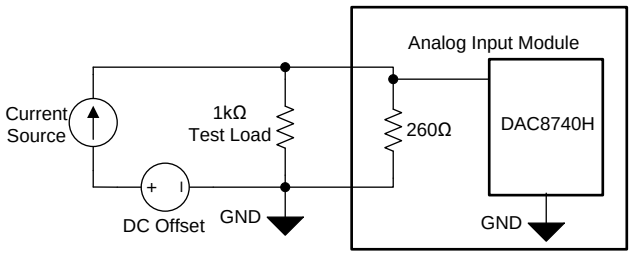

Figure 3. HART Current Input Test Setup

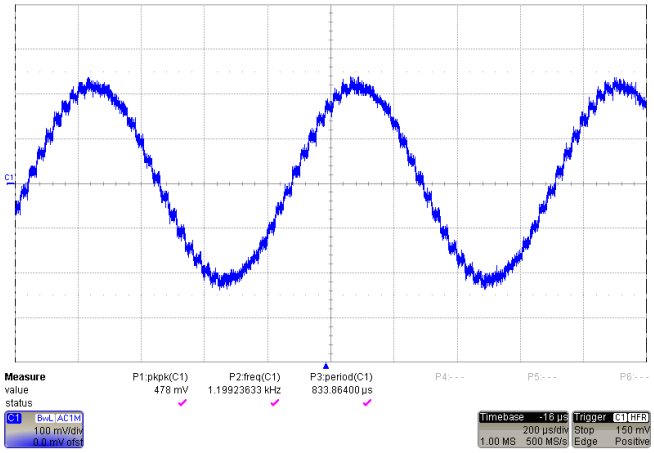

Figure 4. Measurement of HART 1200-Hz Waveshape

Conclusion

With an increase in HART enabled field transmitters, using a HART enabled analog input module offers the advantage of continuous, real time communication between field devices and the PLC. The HART certified DAC874xH family of modems enable designers to implement HART in analog input module designs with few additional system level considerations for HART compliance. The devices offer flexibility with multiple interface options and feature internal HART filtering to minimize external circuitry.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265