Application Report
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Obtaining 17 Bits Of Resolution Using a Low-Cost/Low-Power, Integrated 12-Bit A/D System on a Chip

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ABSTRACT

Integrated data acquisition systems can provide many benefits over discrete component designs. Superior performance, power, and cost savings, along with shorter development times, are among these benefits. Features such as integrated programmable gain amplifiers and averaging can provide added resolution. This application note includes information on how to achieve 17 bits of effective resolution using a 12-bit analog-to-digital converter.

Contents

List of Figures

1 Introduction

Sensors allow us to measure real-world analog parameters such as temperature, pressure, motion, light, and weight. Sensor data acquisition systems are typically configured as illustrated in Figure 1.

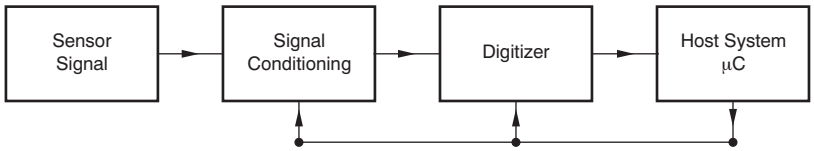

Figure 1. Typical Sensor Data Acquisition System

Sensor signals from thermocouples, resistive temperature devices (RTDs), diodes, microelectromechanical (MEM) devices, and others are usually low-voltage, nonlinear, and in some cases, noisy.

The signal conditioning circuitry can perform various functions on the sensor output such as filtering, buffering, and providing gain or attenuation. This conditioning allows for more accurate and repeatable results from the digitizer.

The digitizer, or analog-to-digital converter (ADC), converts the conditioned, analog signal into a digital format that can be used by the host system for analysis.

1.1 Resolution

Many sensors provide incremental changes in output as the parameter of interest varies. An example would be that of a diode V_{BE} voltage as its ambient temperature varies, as shown in Figure 2. Many diodes exhibit approximately a –2-mV change for a 1°C change in temperature.

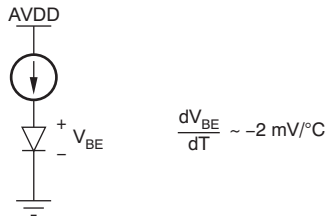

Figure 2. V_{BE} of Diode

A 12-bit ADC with a 4.096-V reference will have a 1-LSB resolution of $4.096\ V/2^{12} = 1$ mV. This resolution would allow us to resolve changes in temperature of 0.5°C. If the required temperature measurement sensitivity is 1/8°C, then a 12-bit converter may prove to be inadequate for this system. Options for addressing this problem include adding gain to the signal conditioning circuit, reducing the ADC reference, or even purchasing a 14-bit ADC.

1.2 Solution Performance and Cost

Cost is a major consideration when designing a data acquisition system. The sensor, signal conditioning, and digitizer circuits should be optimized for the necessary performance at a minimum cost.

In the temperature sensor example, the cost of the ADC can increase significantly as higher resolutions are required. A 14-bit or 16-bit ADC will generally cost more than a 12-bit converter. Adding further components such as operational amplifiers, multiplexers, voltage references, and other devices will increase the system cost and the solution development time.

1.3 Signal Conditioning

We must also consider the signal conditioning circuit. Many sampling ADC circuits have capacitive inputs that sample input signals at set sampling frequencies (for Delta-Sigma [ΔΣ] converters) or at random time intervals, as is generally the case with successive-approximation register (SAR) converters. Either way, the sensor circuit is loaded by these capacitive ADC inputs, which can affect its output during sampling events, as illustrated in Figure 3.

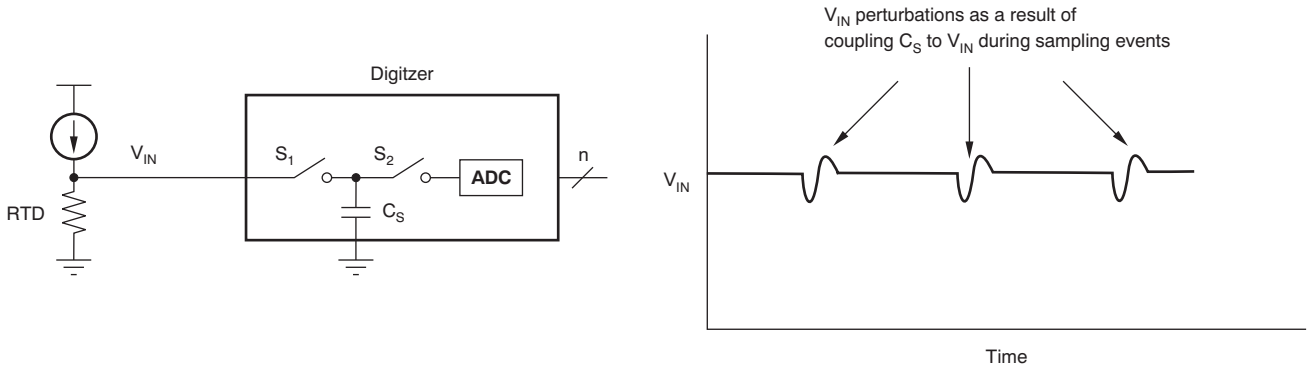

Figure 3. Capacitively Loaded Sensor Circuit

Thus, in many cases, a signal conditioning cell such as an operational amplifier is used as a buffer between the sensor and the ADC. The op amp provides a high-impedance load to the sensor while driving the ADC input. (Note that in many cases, a high-performance op amp is required in order to ensure that its output settles to within 1 LSB of the resolution of the ADC, given a full-scale change in input. This situation often occurs with multiplexed inputs.)

The sensor circuit output must also settle after being perturbed by the capacitive input of the ADC when a sampling event begins. Again, the need for *high-performance* components can translate to higher costs and higher power requirements.

The conditioning circuit affects the sensor output signal by adding offset, noise, gain error, and other errors.

1.4 Adding Signal Gain to Increase Resolution

Figure 4 shows an amplifier configured for a gain of 4 interfaced with the diode temperature sensor.

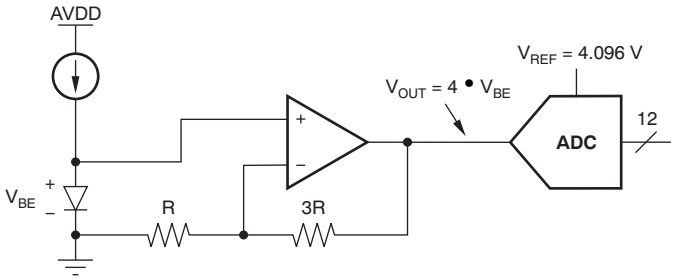

Figure 4. Temperature Sensor Using Op Amp in Gain = 4

This circuit can sense temperature changes of 1/8°C. This capability can be determined by noting the following (simplified) assumptions:

- The 12-bit ADC with a 4.096-V reference has a resolution of 1 LSB = 1 mV.
- A 1°C change in diode temperature translates to a change in V_{BE} of 2 mV.
- A 1/8°C change in diode temperature is 2 mV/8 = 0.25 mV.
- Given a 1/8°C change in ambient temperature at the diode site, the change in output of the op amp with gain = 4 is (0.25 mV x 4) = 1 mV.

Therefore, when the ADC output changes by 1 LSB, we see a change in ambient temperature at the diode site of 1/8°C.

While adding gain in the signal conditioning block can increase overall system resolution, it does so at the expense of reducing the full-scale input range of the system. For example, if a signal conditioning circuit and ADC operate with a full-scale input range of 4.096 V, adding gain in front of the ADC reduces the input full-scale range by 4.096 V/Gain, as Figure 5 shows.

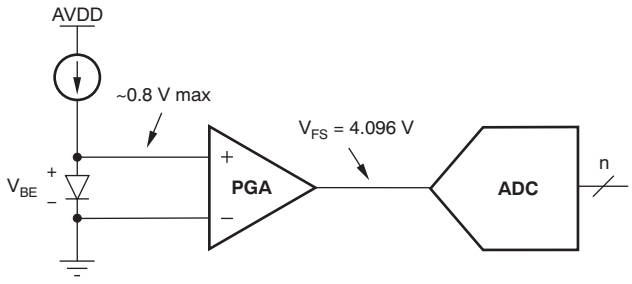

Figure 5. Diode Temperature Sensor with Signal Conditioning Gain

In Figure 5, the amount of gain that can be added is limited to V_{FS}/V_{BE}max, where V_{FS} is the full-scale input range of the ADC. For example, if the maximum V_{BE} voltage expected over temperature is 0.8 V and V_{FS} = 4.096 V, then the maximum gain allowed is 4.096/0.8 = 5.12.

Many sensors have an output full-scale range of less than 1 V. This low range allows for gain to be used to increase system resolution. In some cases, a pedestal voltage can also be used as shown in Figure 6, to allow for differential measurements where incremental changes from the sensor can be amplified further.

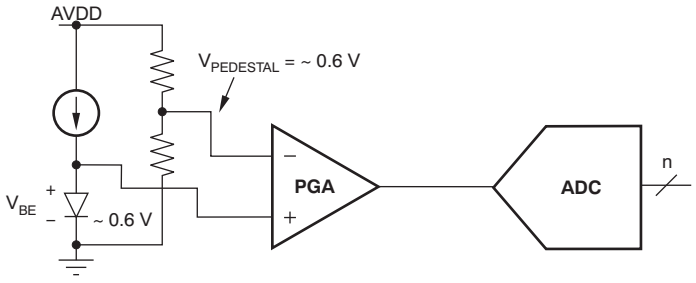

Figure 6. Differential Signal Using Pedestal Voltage

Here, the output of the diode is measured differentially using a $V_{PEDESTAL}$ voltage of 0.6 V and a programmable gain amplifier (PGA) or an instrumentation amplifier (INA) . In this case, the maximum gain can be increased based on the expected maximum difference between V_{BE} and $V_{PEDESTAL}$. This calculation is 4.096/(V_{BE}max – $V_{PEDESTAL}$) = 4.096/0.2 = 20.48. The ability to detect smaller voltage changes on the sensor is enhanced with higher gains.

It should be noted that differential measurements can also yield negative results. This type of result would occur with this circuit if $V_{BE} < V_{PEDESTAL}$. Single-supply devices in particular generally require additional circuitry to compensate for this possibility.

Other factors are also introduced when adding gain circuitry. For example, the noise contribution of the amplifiers used to add gain typically shows a proportional increase. The input-referred offset is also gained up at the output. Mismatches in the gain setting resistors (see Figure 4) also introduce gain error into this system. Although these issues can be addressed with system calibration techniques and filtering, they add cost and development time to the system overhead.

2 ADS8201: An Integrated Data Acquisition System

The ADS8201 (illustrated in Figure 7) is an integrated data acquisition system that consists of an eight-channel multiplexer (mux), a time-continuous programmable gain amplifier (G = 1, 2, 4, 8), provisions for external signal conditioning between the PGA output and ADC input, and a low-power, 12-bit SAR ADC.

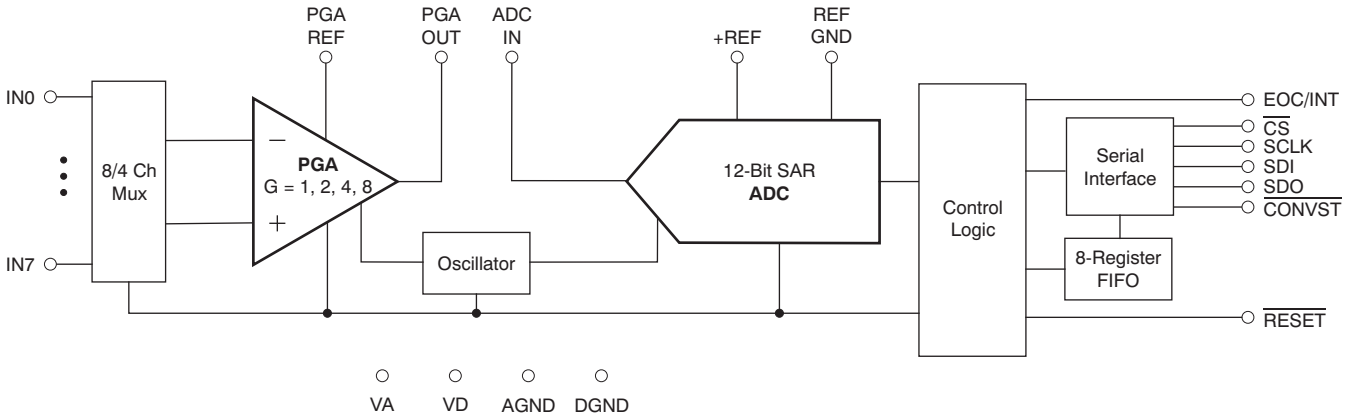

Figure 7. ADS8201 Data Acquisition System

The primary advantage of an integrated system such as the ADS8201 is that all the components have been optimized for both cost and performance. Single-channel throughput is 100 kSPS. Faster throughputs are possible for input signals that do not vary much over time. Other enhancements include:

- Integrated power-up and power-down conditions for all components in order reduce power at lower throughput rates; the power-down current is less than 1 μA.
- A time-continuous, low-power, chopper-stabilized PGA that effectively reduces low-frequency noise and offset.
- An eight-register FIFO for storing conversion results. This feature allows for storing data and entering a powered-down state to conserve power. Results can be later accessed by the host system when needed.
- An averaging function (up to 16 samples) that allows for a noise reduction of $1/\sqrt{\text{Number of samples}}$. This feature also provides for two extra bits of output, thus giving a 14-bit result. Additionally, resolutions of up to 17 bits are possible with a PGA gain of 8.

Many design challenges for the system architect are addressed with the ADS8201. The PGA is optimized for driving the 12-bit ADC. Using internal timing techniques generated from its digital core, the PGA can begin to respond to other channels while the ADC is converting the previously acquired sample. See the *PGA Settling Time and the Delay Mux Feature* section for details.

2.1 Using the Programmable Gain Amplifier

Figure 8 shows the mux, PGA, and SAR ADC elements of the ADS8201. The PGA is a time-continuous, chopper-stabilized amplifier with programmable gains of 1, 2, 4 and 8. Data can be taken differentially or single-ended. Care must be taken to ensure that the PGA is configured such that 0 V ≤ PGA OUT ≤ +REF (+REF being the reference voltage for the ADC). This condition is achieved by using Equation 1.

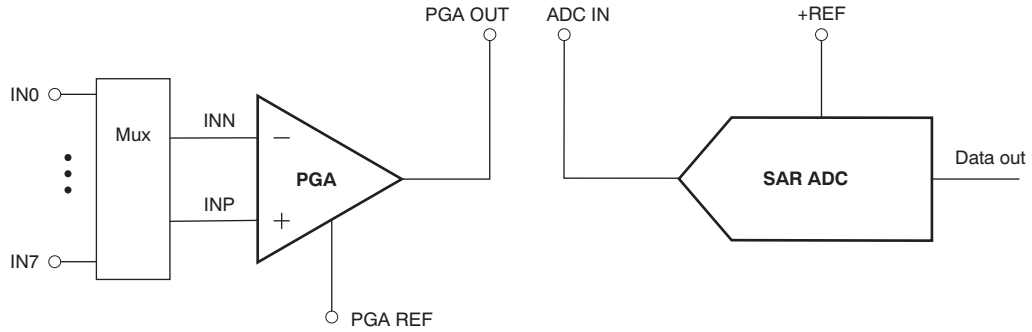

Figure 8. ADS8201 Multiplexer, PGA, and SAR ADC

$$\text{PGA OUT} = (\text{INP} - \text{INN}) \bullet \text{PGA Gain} + \text{PGA REF} \quad (1)$$

2.2 Single-Ended Applications

Single-ended operating modes are selected using the Channel CCR Registers (ADDR = 00h to 03h). When enabled, the selected channel signal is coupled to the noninverting input (INP) of the PGA. The inverting input is internally coupled to ground. The PGA REF pin is grounded in single-ended applications with the ADS8201, as Figure 9 illustrates.

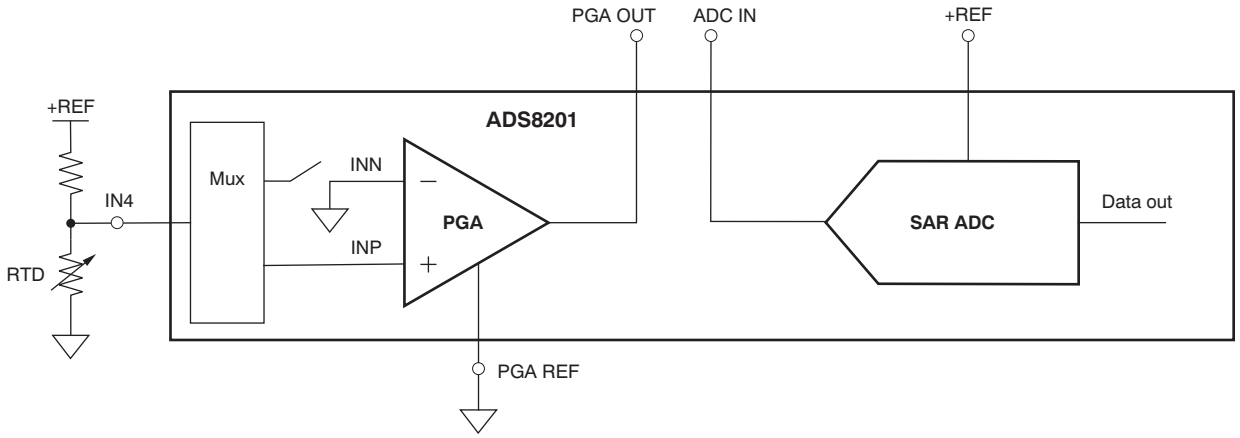

Figure 9. ADS8201 Single-Ended Application

2.3 Differential Applications

Differential configurations such as the one shown in Figure 10 can also be set up using the Channel CCR Registers (ADDR = 00h to 03h). The common-mode voltage of the signals seen at CH0 and CH1 are rejected. Only the differential signal times the programmed gain plus the PGA reference voltage on the PGA REF pin is seen at the PGA OUT pin.

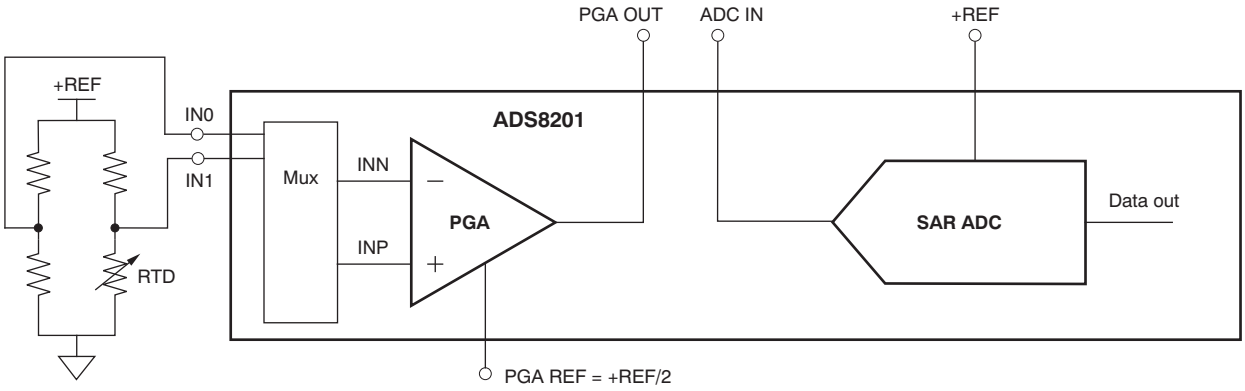

Figure 10. ADS8201 Differential Configuration

For example, if the pins shown in Table 1 are driven with the listed voltages, PGA OUT can be determined using Equation 1.

Table 1. PGA OUT

INN	INP	PGA REF	PGA Gain	PGA OUT
2.5 V	2 V	2 V	2	1 V
2 V	2.1 V	2 V	4	2.4 V
0 V	0.5 V	0 V	8	4 V

As noted earlier, differential signals can yield negative outputs. This result occurs when INP – INN < 0. In single-supply systems such as the ADS8201, output voltage levels cannot go below ground. In this case, it is necessary to drive the PGA REF pin with a voltage that ensures the PGA output remains within a valid output range. Typically, this condition can be achieved by driving this pin with an op amp set for an output of +REF/2, as shown in Figure 11.

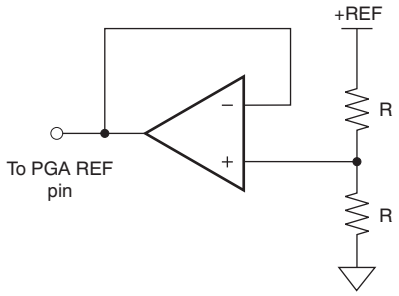

Figure 11. PGA REF Pin Driver

The PGA REF pin should be driven with a low-impedance signal source. Coupling the resistor divider shown in Figure 11 directly to the PGA REF pin without the op amp would yield poor results. The input impedance of the PGA REF pin is ~80 kΩ.

When this pin is driven with +REF/2 V, a full-scale differential input range of ±REF/2 is possible.

2.4 PGA Settling Time and the Delay Mux Feature

Changing mux channels requires that the system allow for a PGA settling period. The PGA is designed to settle within 10 µs to 12 bits of resolution given a maximum full-scale input signal range of 0.1 V to (AVDD – 0.1 V). Figure 12 illustrates this architecture.

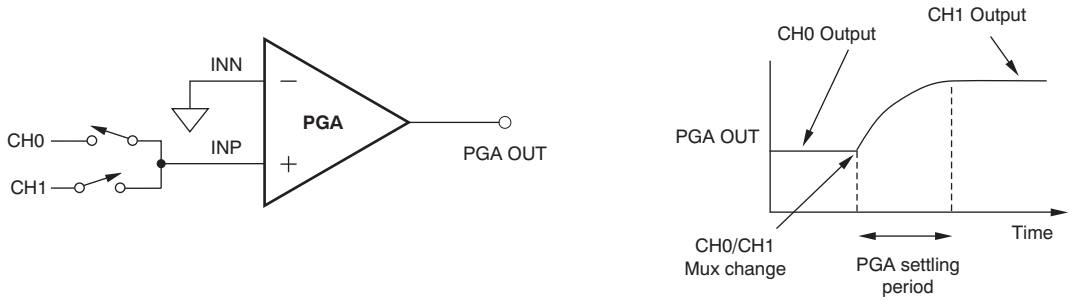

Figure 12. PGA Settling Time

Conversion of analog-to-digital data is done in two phases: a sampling period followed by a conversion period. During the sampling period, the PGA output is coupled to the ADC input-sampling capacitors. The PGA output must have settled to within an LSB of its steady-state value once this period ends. The conversion period is the time in which the ADC is actually converting the sampled signal to a digital word. Any signals seen at the ADC input during this phase are ignored.

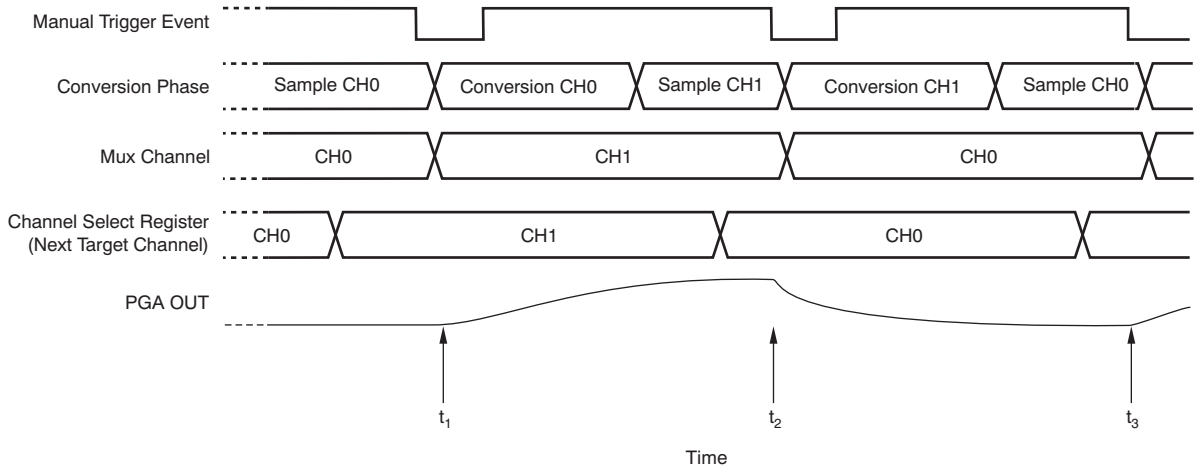

Figure 13. ADS8201 Sample and Conversion Timing

Figure 13 illustrates the timing for continuously digitizing signals from channels 0 and 1 (see Ref. 1). In order to achieve 100-kSPS throughput, the PGA must begin settling to its new target value once the sampling phase of the previous channel is complete. Time points t_1, t_2, and t_3 indicate the end of these sampling periods. For example, at time t_1, the ADC goes into its conversion phase and begins digitizing Channel 0 data. Note also that the mux channel goes to Channel 1 and the PGA begins to settle to its new target voltage from Channel 1.

This activity is managed automatically by the ADS8201 when using the auto-trigger/auto-channel update modes in the ADC Trigger SCR (ADDR = 08h).

When the ADC Trigger SCR is set for manual channel select mode, the next target channel must be supplied by the user via the serial interface (SPI) by writing to the Channel Select Register (04h) before the manual-triggering event occurs as shown in Figure 13.

If this feature is not enabled when manual channel modes of operation are selected, then 100-kSPS throughput cannot be achieved. See Example 3 for more information on implementing this feature.

2.5 Using the Channel Select Register

The Channel Select Register (ADDR = 04h) can be used to select a channel pair as single-ended or differential inputs. The gain can be set for each channel or channel pair. If a differential mode is selected, then the gain set for the lower channel is the default. Even or odd polarity determines which differential input is coupled to the inverting and noninverting pins of the PGA. The even-valued channel is coupled to the noninverting input by default.

2.6 Using the Averaging Function

Setting the ADC SCR Register (ADDR = 05h) allows for averaging outputs of 4, 8, or 16 samples. Fast averaging provides throughputs of up to 4 µs times the number of samples per channel. This mode can be used for slow or low-frequency signals where the PGA does not need 10 µs to settle (see the *PGA Settling Time and the Delay Mux Feature* section). Accurate averages have a throughput of 10 µs times the number of samples per channel.

The averaging feature allows for up to two extra bits of output data. Also, note that noise is reduced by $1/\sqrt{N}$ where *N* is the number of samples. This feature is very useful in resolving noisy input signals. See Example 3 and Appendix A for more information.

2.7 Programming the INT/BUSY Pin

The ADC SCR Register sets the INT/BUSY pin to act as an interrupt signal indicating that an event has occurred or as a busy signal showing that the ADC is in its conversion phase of operation (see the *PGA Settling Time and the Delay Mux Feature* section).

2.8 Programming the Interrupt Control Register

The Interrupt System Control Register can be used to set the ADS8201 into a powered-down condition. This state results in quiescent current being reduced to less than 1 µA. This mode is very useful in battery applications where power consumption must be minimized. Data in the FIFO registers are retained and can be retrieved once the part is powered up again.

This register also controls the way in which the INT/BUSY pin can function when programmed as an interrupt. The interrupt can be defined to occur as a single pulse (edge-triggered) or a change of state (level change) which does not reset itself until the user begins to read the output results. See Example 1 and Appendix A for information on ways of programming this setting in the Interrupt Control Register.

2.9 Using the Conversion Delay SCR Register (ADDR = 0Ah)

The system throughput rate is optimized and specified at 100 kSPS. This translates to 10 µs per conversion. The PGA is designed to settle to within 1 LSB for a full-scale change in input within this period. As a result of variations in the internal oscillator, this period can vary by up to ±20%.

This register can be used to *trim in* the throughput period if required by the host system. For example, the default value for the Conversion Delay SCR Register D[2:0] is **010**. If the internal oscillator is operating 20% slower than nominal, writing ***001*** to this register adjusts the throughput rate to be closer to the expected 100 kSPS.

2.10 Programming the ADC Trigger SCR

The ADC Trigger System Control Register controls the way in which data are obtained. Conversions can be triggered manually or automatically by setting this register.

Manual-triggering can be done by bringing the $\overline{\text{CONVST}}$ pin from a logic 1 to logic 0. Manual-triggering can also be done via the serial interface by reading conversion results. Note that these modes are set with D[0] in the System Control Register (ADDR = 05h).

Auto-triggering occurs by writing to this register. Single-scanning of all channels (starting with the channel selected in the Channel Select Register) or continuous scanning can be done. Auto-triggering using the delay mux feature can also be enabled.

The ADC Idle mode should be set when changing configuration registers or upon device power-up when registers are being configured.

3 ADS8201 Serial Interface

Reading and writing to the ADS8201 registers is accomplished using the serial interface. For timing and other information, refer to the ADS8201 product data sheet (see Ref. 1).

3.1 Register Read

Figure 14 shows the format for reading from any of the ADS8201 registers. Data from the SDI pin should be transmitted MSB first. The first two bits indicate that a register read is requested.

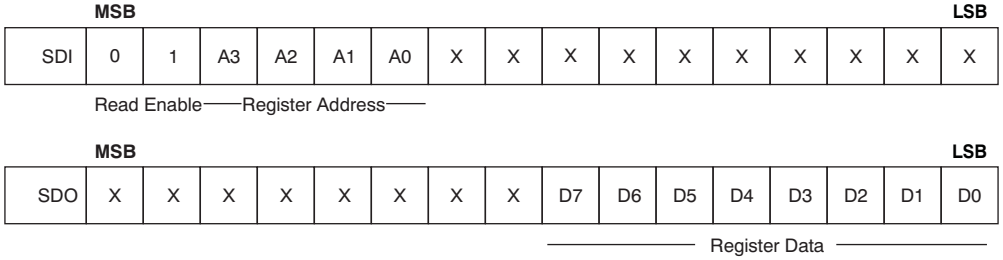

Figure 14. ADS8201 Register Read

3.2 Register Write

Figure 15 illustrates the format for writing data into any of the ADS8201 registers. Data from the SDI pin should be transmitted MSB first. The first two bits indicate that a register write is requested.

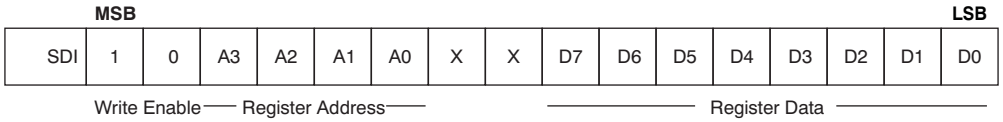

Figure 15. ADS8201 Register Write

3.3 Reading Conversion Results

Reading the output register begins with bringing the $\overline{CS}$ pin low and enabling SCLK. Setting the first two SDI bits to '0' as shown in Figure 16 configures the ADS8201 to provide conversion results to the SDO pin.

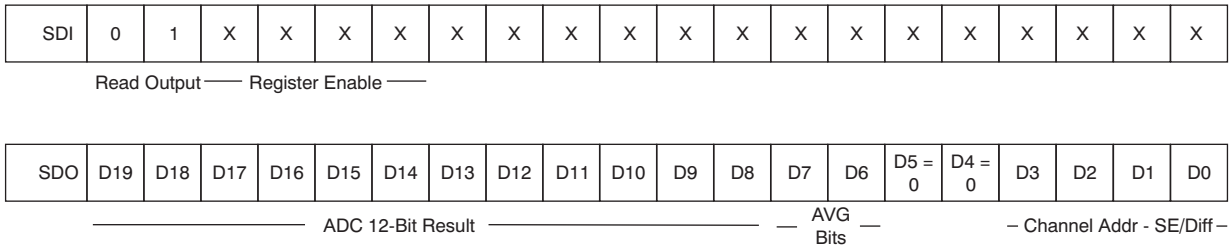

Figure 16. Reading Output Register

The user can retrieve the 12 bits of ADC data, two extra bits from the internal averaging function as well as the channel address, and the configuration information (SE/Diff) set up for this channel and result. The user can also truncate this 20-bit result by setting the $\overline{CS}$ pin high after the desired number of bits are received. For example, if only the 12-bit ADC result is desired, then set $\overline{CS}$ high after bit D8 is transmitted (see Ref. 1).

4 Application Examples

This section presents several application examples with specific, step-by-step instructions on how to set up and use the internal configuration registers to achieve the desired mode of operation. The reader is advised to download the most current version of the ADS8201 product data sheet (literature number SLAS534), which includes serial interface timing and other information that can assist in achieving optimum results and performance. Note that SDI data transmission to the ADS8201 is done with the MSB value (shown with each example) sent first.

4.1 Example 1: Temperature Measurement

A data acquisition system using diodes to monitor temperature at different remote locations is presented in Figure 17.

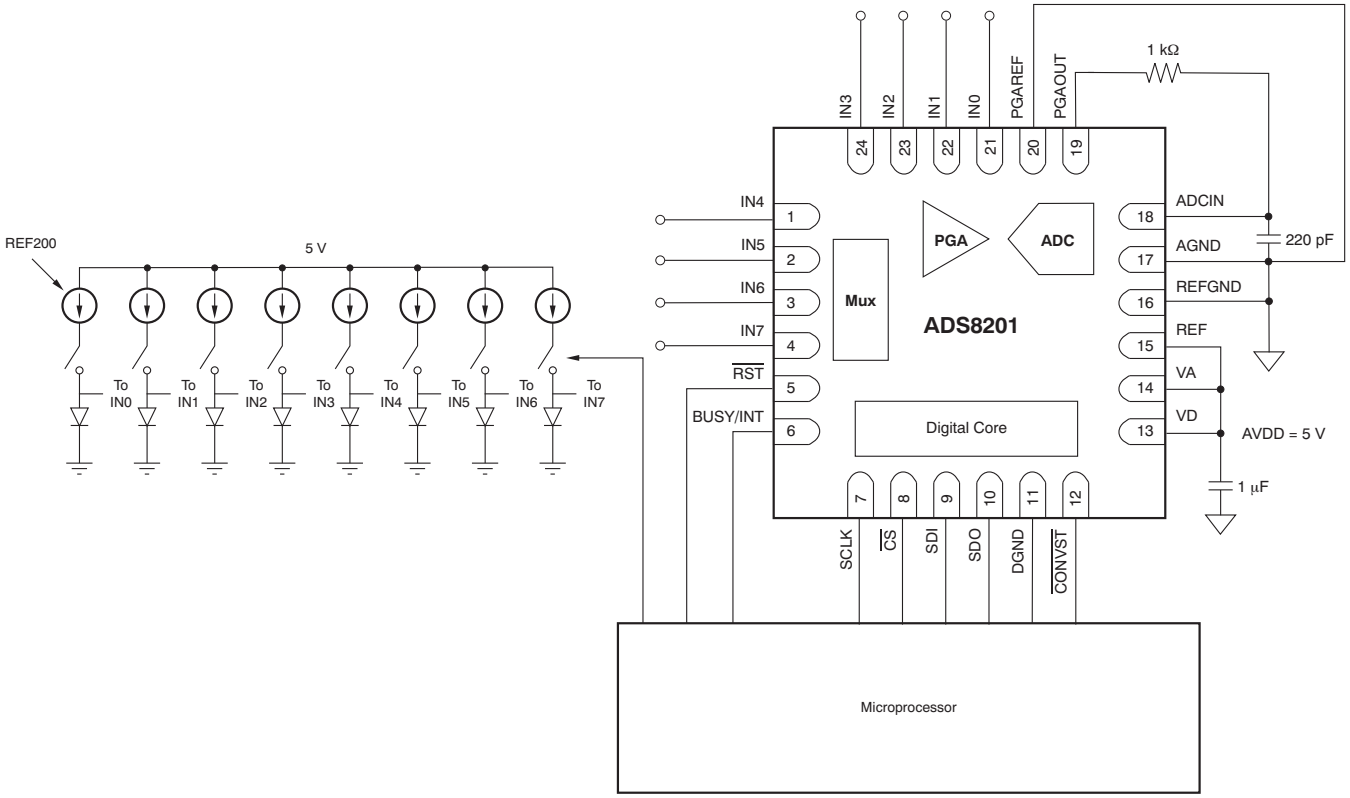

Figure 17. Temperature Data Acquisition System

The objective is to measure the eight diode voltages that are driven by current sources. This data can then be used to determine the temperature and/or the change in temperature at the location of each diode. A scanning event will be triggered that takes data from all eight channels coupled to each diode. The data are then placed in the FIFO registers. The ADS8201 is then placed in a power-down mode (I_Q < 1 µA) until the host system or µC is ready to retrieve this data.

Upon applying power to the ADS8201, the device waits 40 µs before collecting data. This wake-up period allows the internal analog circuitry to power up and the device to settle into its nominal biasing condition before sampling and digitizing input signals.

4.1.1 Register Set Up

1. Set ADC Trigger SCR (Addr = 08h) for Idle Mode.

   This step is recommended whenever writing to and/or reconfiguring register data. It ensures that the ADC is not in the process of initiating conversions while the configuration registers are being updated.

   SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

2. Set Channel Select Register (Addr = 04h) for Channel 0.

   Note that Channel Select Registers 00h through 03h are setup configuration registers for all input channels. Gain, single-ended, differential, inverting, or noninverting input configurations can be set here. Because the default configuration modes are for single-ended, noninverting inputs with a gain of 1, no data are needed to set up these registers for this example.

   By setting the Channel Select Register for CH0, the scan sequence will begin with CH0 and terminate with CH7.

   SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

3. Set the ADC SCR (Addr = 05h) for FIFO Enable, SPI Triggering, and Edge Interrupt.

   This configuration will transfer conversion data to the FIFO registers. The Edge Interrupt bit (D4) sets the interrupt signal to be a single pulse.

   SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	0	0	0	0	0	1	0	0	1	1

4. Set the Interrupt SCR (Addr = 06h) for Scan Data Ready.

   This step enables the INT pin (active low by default) once a scan of all the channels is complete and available in the FIFO registers for retrieval.

   SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0

5. Set ADC Trigger SCR (Addr = 08h) for Auto Trigger/Single-Scan.

   Writing to this register initiates the conversion of all channels.

   SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1

6. Retrieve the data from the FIFO.

   Once the INT pin indicates that all channels have been converted, the data are ready for retrieval. This procedure can be done by setting both $\overline{CS}$ and SDI = 0 and enabling SCLK. Note that up to 20 bits of information (see Figure 16) per channel can be obtained. Note also that the $\overline{CS}$ pin should be set high, as shown in Figure 18, after the desired number of bits of data per channel have been obtained. This configuration must be done in order to retrieve FIFO data results from the next channel.

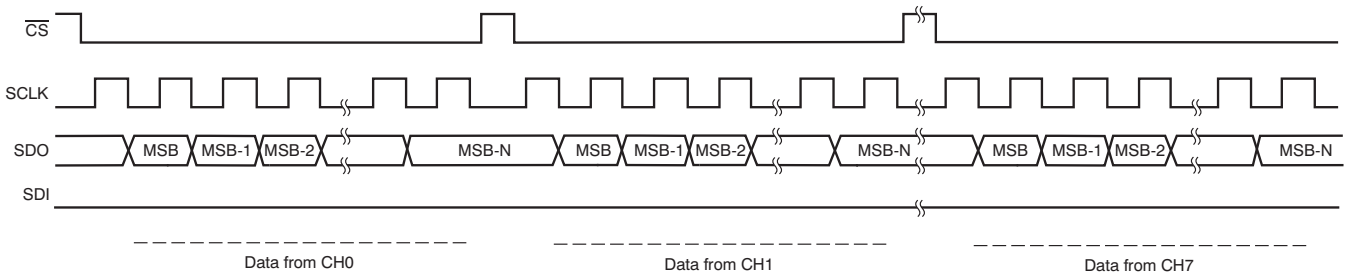

Figure 18. ADS8201 FIFO Read

7. Once the data are obtained, the ADS8201 can be put into power-down mode by writing to the Interrupt SCR (Addr = 06h) and enabling bit 7.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0

4.2 Example 2: GPS Application

Figure 19 illustrates a GPS application where gyro and accelerometer sensors are used to determine motion or a change in location from a previously known location.

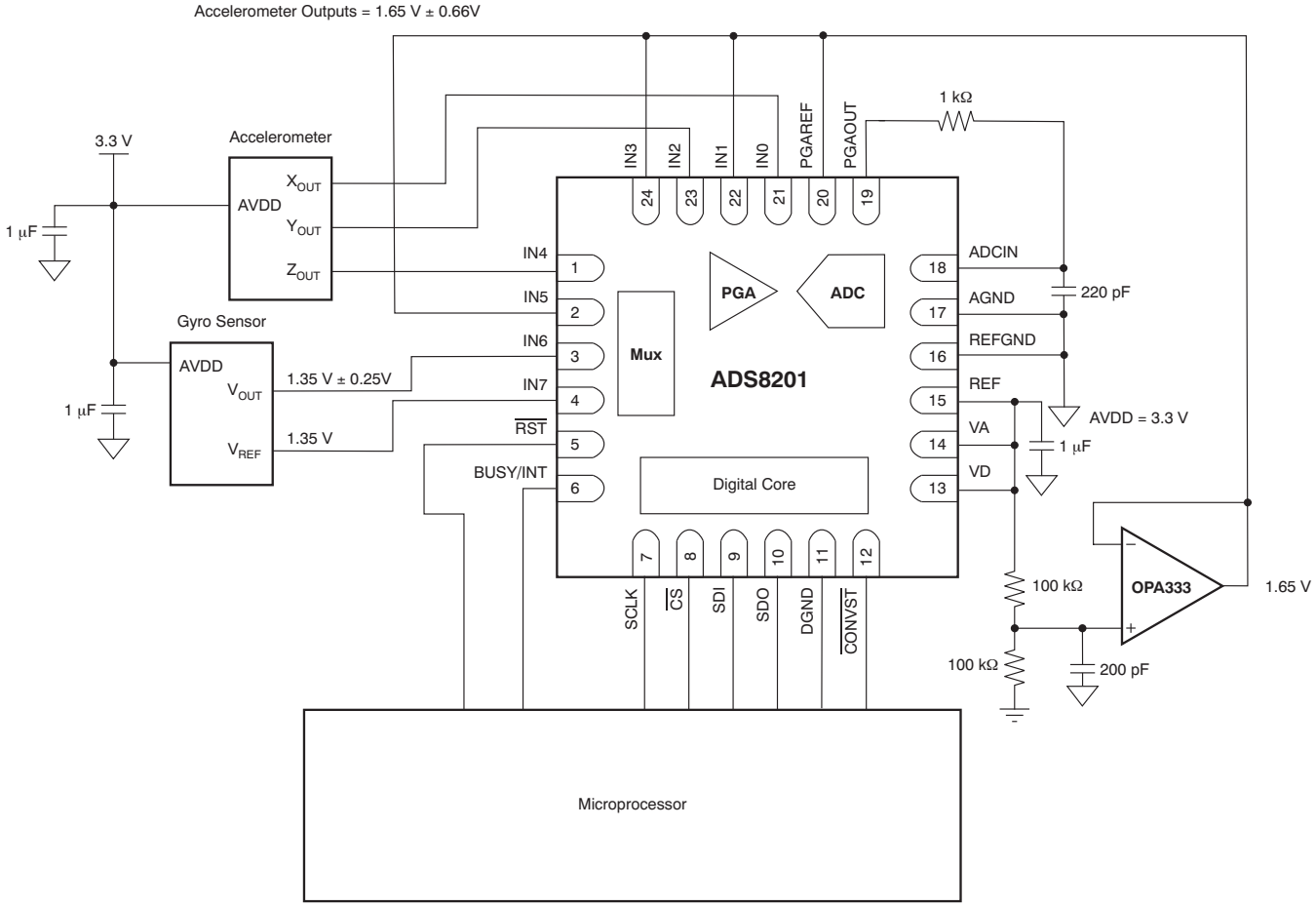

Figure 19. ADS8201 GPS Application

The accelerometer has an output range of AVDD/2 ± AVDD/5 which translates to ± 2 g of acceleration full-scale. The gyro sensor has an output range of 1.35 V ±0.25V, which corresponds to ±100°/sec. This part also provides an output reference voltage of 1.35 V.

This application makes differential measurements of the accelerometer outputs using an external op amp (OPA333) and two 100-kΩ resistors to create a 1.65-V pedestal voltage. The gyro sensor output is also measured differentially using its internal 1.35-V reference as a pedestal voltage.

Channels 0 and 1 are used to monitor the accelerator X_{OUT} signal, channels 2 and 3 are used for the Y_{OUT}, and channels 4 and 5 for the Z_{OUT}. The gyro sensor signals are monitored on channels 6 and 7.

In order to increase the system resolution in monitoring changes in each sensor output, the accelerometer signals (CH0 through CH5) are gained up by a factor of two. The gyro sensor signal can be gained by a factor of four. The AVDD supply voltage is 3.3 V. This supply is also used as the voltage reference (REF pin); therefore, it should be a clean, well-regulated voltage source.

4.2.1 Register Setup

1. Set ADC Trigger SCR (Addr = 08h) for Idle Mode.

   This step is recommended whenever writing to and/or reconfiguring register data. It ensures that the ADC is not in the process of initiating conversions while the configuration registers are being updated.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

2. Set Channel Configuration Register 0 for CH0/CH1 differential measurement, gain = 2, and even polarity (CH0 = +IN, CH1 = –IN).

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

3. Set Channel Configuration Register 1 for CH2/CH3 differential measurement, gain = 2, and even polarity (CH2 = +IN, CH3 = –IN)

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1

4. Set Channel Configuration Register 2 for CH4/CH5 differential measurement, gain = 2, and even polarity (CH4 = +IN, CH5 = –IN).

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1

5. Set Channel Configuration Register 3 for CH6/CH7 differential measurement, gain = 4, and even polarity (CH6 = +IN, CH7 = –IN).

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0

6. Set Channel Select Register (Addr = 04h) for Channel 0.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

7. Set ADC SCR Register (Addr = 05h) for FIFO Enable, SPI triggering, and Edge Interrupt.
   This configuration transfers conversion data to the FIFO. The Edge Interrupt bit sets the interrupt signal to be a single pulse.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	0	0	0	0	0	1	0	0	1	1

8. Set Interrupt SCR (Addr = 06h) for Scan Data Ready.
   This step enables the INT pin (active low by default) once a scan of all the channels is complete and data are available in the FIFO for retrieval.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0

9. Set ADC Trigger SCR (Addr = 08h) for Auto-Trigger/Single Scan.
   Writing to the register initiates the conversion of all channels.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1

10. Retrieve data from FIFO.
    See *Retrieve Data from the FIFO* from Section 4.1.

4.3 Example 3: 16-Bit Resolution Temperature Measurement

The same circuit from Section 4.1 is used to monitor temperature (see Figure 17). Only channels 0 and 7 are monitored. The system continuously cycles between each channel and collects data. 16 bits of resolution are required for this application.

This resolution can be achieved by setting the PGA for a gain of 4 and taking the average of 16 samples from each channel. The PGA gain of 4 adds two effective bits of resolution. The averaging function allows for two more bits that can be obtained from the output register (see Figure 16). The delay mux feature (see *PGA Settling Time and the Delay Mux Feature*) is enabled and a manual-trigger using the $\overline{\text{CONVST}}$ pin is used.

1. Set ADC Trigger SCR (Addr = 08h) for Idle Mode.
   This step is recommended whenever writing to and/or reconfiguring register data. It ensures that the ADC is not in the process of initiating conversions while the configuration registers are being updated.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

2. Set Channel 0/1 CCR (Addr = 00h) for channel 0 with a gain of 4.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

3. Set Channel 6/7 CCR (Addr = 03h) for channel 7 with a gain of 4.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0

4. Set ADC SCR Register (Addr = 05h) for $\overline{\text{CONVST}}$ manual-trigger, Edge Interrupt, and fast averaging of 16 results.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	0	0	0	1	1	1	0	0	0	0

5. Set Interrupt SCR Register (Addr = 06h) for ADC Data Ready Interrupt.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1

6. Set Channel Select Register (Addr = 04h) for channel 0.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

7. Set ADC Trigger SCR Register (Addr = 08h) for manual-trigger and delay mux (mode 3).

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1

8. Set Channel Select Register (Addr = 04h) for channel 7.
   This sets channel 7 as the next target channel after the ADC begins converting data from channel 0.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1

9. Begin a conversion by bringing the $\overline{\text{CONVST}}$ pin low for at least 40 ns.
   Once the INT period signals that the results are ready (INT goes low for ~250 ns), issue 14 SCLK pulses to retrieve results from channel 0. Note that this output is 14 bits, where the last two LSBs are from the averaged 16 results. This 14-bit output, along with the PGA gain of four (which adds another two bits of resolution), provides an effective output resolution of 16 bits.

10. Set Channel Select Register (Addr = 04h) for channel 0.

    This step sets channel 0 as the next target channel after the ADC begins converting data from channel 7.

SDI Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

11. Begin a conversion by bringing the $\overline{\text{CONVST}}$ pin low for at least 40 ns.

After retrieving the results from channel 7 (see the *Reading Conversion Results* section), repeat the above sequence of setting the Channel Select Register for the next target channel and then initiate a conversion of the currently-selected channel.

5 References

1. ADS8201 product data sheet. Literature number SLAS534B. Available for download at www.ti.com.

Appendix A Using the ADS8201 Configuration Registers

There are 10, 8-bit user registers that can be used for configuring the ADS8201 for specific modes of operation. Each section in this appendix gives a description of these features.

A.1 Channel 0/1 Configuration Register (Address 00h)

D[7:6]	**Not Used**
	[0:0]
D[5:4]	**Channel 1 Gain Single-Ended**
	00: G = 1 (default)
	01: G = 2
	10: G = 4
	11: G = 8
D[3]	**Channel 0 Differential Odd/Even Polarity**
	0: Even polarity (default)
	1: Odd polarity
D[2]	**Channels 0/1 Single-Ended/Differential**
	0: Ch0/1 Single-ended (default)
	1: Ch0/1 Differential
D[1:0]	**Channel 0 Gain**
	00: G = 1 (default)
	01: G = 2
	10: G = 4
	11: G = 8

A.2 Channel 2/3 Configuration Register (Address 01h)

D[7:6]	**Not Used**
	[0:0]
D[5:4]	**Channel 3 Gain Single-Ended**
	00: G = 1 (default)
	01: G = 2
	10: G = 4
	11: G = 8
D[3]	**Channel 2 Differential Odd/Even Polarity**
	0: Even polarity (default)
	1: Odd polarity
D[2]	**Channels 2/3 Single-Ended/Differential**
	0: Ch2/3 Single-ended (default)
	1: Ch2/3 Differential
D[1:0]	**Channel 2 Gain**
	00: G = 1 (default)
	01: G = 2
	10: G = 4
	11: G = 8

A.3 Channel 4/5 Configuration Register (Address 02h)

D[7:6]	**Not Used**
	[0:0]
D[5:4]	**Channel 5 Gain Single-Ended**
	00: G = 1 (default)
	01: G = 2
	10: G = 4
	11: G = 8
D[3]	**Channel 4 Differential Odd/Even Polarity**
	0: Even polarity (default)
	1: Odd polarity
D[2]	**Channels 4/5 Single-Ended/Differential**
	0: Ch4/5 Single-ended (default)
	1: Ch4/5 Differential
D[1:0]	**Channel 4 Gain**
	00: G = 1 (default)
	01: G = 2
	10: G = 4
	11: G = 8

A.4 Channel 6/7 Configuration Register (Address 03h)

D[7:6]	**Not Used**
	[0:0]
D[5:4]	**Channel 7 Gain Single-Ended**
	00: G = 1 (default)
	01: G = 2
	10: G = 4
	11: G = 8
D[3]	**Channel 6 Differential Odd/Even Polarity**
	0: Even polarity (default)
	1: Odd polarity
D[2]	**Channels 6/7 Single-Ended/Differential**
	0: Ch6/7 Single-ended (default)
	1: Ch6/7 Differential
D[1:0]	**Channel 6 Gain**
	00: G = 1 (default)
	01: G = 2
	10: G = 4
	11: G = 8

A.5 Channel Select Register (Address 04h)

D[7:3]	**Not Used**
	[0:0]
D[2:0]	**Select Mux Input Channel/Start Channel Number if in Auto-Scan Mode**
	000: Channel 0 (default)
	001: Channel 1
	010: Channel 2
	011: Channel 3
	100: Channel 4
	101: Channel 5
	110: Channel 6
	111: Channel 7

A.6 System Configuration Register (SCR) Map (Address 05h)

D[7:5]	**Average Select**
	000: No average (default)
	001: Fast average of four results
	010: Fast average of eight results
	011: Fast average of 16 results
	100: No average
	101: Accurate average of four results
	110: Accurate average of eight results
	111: Accurate average of 16 results
D[4]	**Interrupt Select**
	0: Level triggered (default)
	1: Edge triggered. Period of pulse is 250ns.
D[3]	**BUSY/INT Level**
	0: Active low (default)
	1: Active high
D[2]	**BUSY/INT Select**
	0 : INT (default)
	1: BUSY
D[1]	**FIFO Buffer Enable**
	0: FIFO buffer disabled (default)
	1: FIFO buffer enabled
D[0]	**RD/CONVST Trigger**
	0 : Issue CONVST from the pin (default)
	1: Convert start is issued through the SPI after the first read of the ADC. Ignore the first read.

A.7 Interrupt SCR (Address 06h)

D[7]	**Power-Down Control**
	0: Normal conversion mode (default)
	1: Power-down idle mode
D[6:4]	**Always Reads '0'**
D[3]	**FIFO Buffer Not Empty Interrupt**
	Read 0: Interrupt not generated (default)
	Read 1: Interrupt generated when FIFO buffer is not empty
	Write 0: Disable interrupt
	Write 1: Enable interrupt
D[2]	**FIFO Buffer Full Interrupt**
	Read 0: Interrupt not generated (default)
	Read 1: Interrupt generated when FIFO buffer is full
	Write 0: Disable interrupt
	Write 1: Enable interrupt
D[1]	**Scan Data Ready Interrupt**
	Read 0: Interrupt not generated (default)
	Read 1: Interrupt when scan data are ready. Only applicable in auto channel and auto-trigger mode.
	Write 0: Disable interrupt
	Write 1: Enable interrupt
D[0]	**ADC Data Ready Interrupt**
	Read 0: Interrupt not generated (default)
	Read 1: Interrupt generated when ADC data are ready.
	Write 0: Disable interrupt
	Write 1: Enable interrupt

A.8 Status SCR (Address 07h)

D[7:4]	**FIFO Buffer Level: Number of Entries**
D[3]	**FIFO Buffer Not Empty**
	0: FIFO buffer empty
	1: FIFO buffer not empty
D[2]	**FIFO Buffer Full**
	0: FIFO buffer not full
	1: FIFO buffer full
D[1]	**Scan Data Ready**
	0: Not ready
	1: Ready
D[0]	**ADC Data Ready**
	0: Not ready
	1: Ready

The Status SCR Register is a read-only register where information regarding FIFO, scan, and ADC data availability can be obtained.

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