Application Report
SBAA150A–April 2008–Revised October 2016

Design for a Wideband, Differential Transimpedance DAC Output

Michael Steffes *High-Speed Products*

ABSTRACT

High-speed digital-to-analog converters (DACs) commonly offer a complementary current output signal. Most output interface implementations use either a resistive load and/or a transformer to convert this current source signal to a voltage. Where a DC-coupled interface is required, a carefully designed differential transimpedance stage can offer an attractive alternative. Design considerations and options will be shown using first wideband dual operational amplifiers (op amps), then using the newer fully differential amplifiers (FDA). Example circuits and simulated performance will then be developed.

NOTE: This article was originally published on Analog Zone.

Contents

List of Figures

1 Typical DAC Output Circuits

High-speed DACs have migrated to using a complementary current source output structure. Sometimes called *current steering*, a fixed maximum current is steered between two outputs based on the digital code presented to the DAC inputs. This type of output can be characterized as two current source outputs having a fixed DC current equal to half of the maximum reference current (I_R) with a differential current signal (I_S) imposed on top of this DC level, as shown in Figure 1. The term *complementary* current outputs is intended to distinguish from a purely *differential* output in that these outputs are sitting on top of a DC common-mode current, (I_R/2).

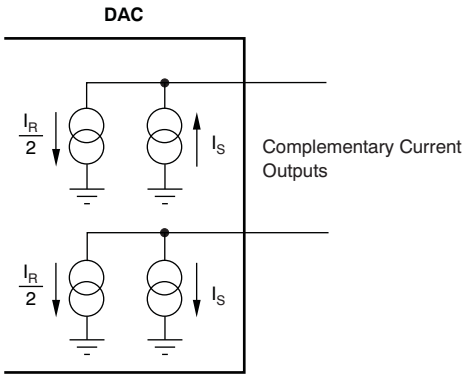

Figure 1. Current Source Model for the DAC Output Signal

In this case, the I_R/2 currents are shown sinking into the DAC outputs where the maximum value for I_S = I_R/2. There are also DACs that source current from their outputs where a ground referenced load is then specified. A typical DC-coupled interface from the DAC5675A data sheet (which is a sinking current source output) is shown in Figure 2.

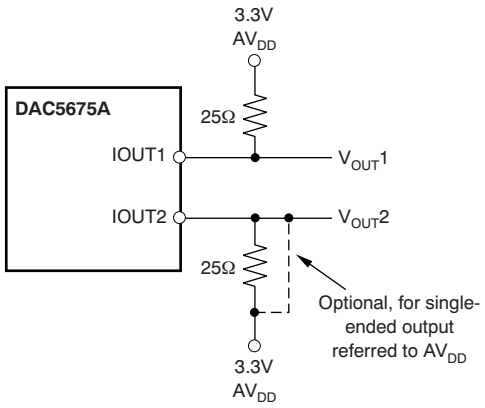

Figure 2. DC-Coupled Differential Output Interface

Neglecting the optional short to AV_{DD} on IOUT2 (using the 25Ω load on both sides), this circuit would be sitting at a common-mode voltage of 3.3V – 25Ω • (I_R/2). The DAC5675A specifies 20mA for I_R, which then places the common-mode voltage for $V_{OUT}1$ and $V_{OUT}2$ at 3.05V with a signal swing of ±(I_R/2) • 25Ω on each output (±0.25V), giving a differential voltage swing across the two outputs of ±0.5V. This is assuming an open, or high impedance, load at $V_{OUT}1$ and $V_{OUT}2$. Adding a DC-coupled load will need to be done carefully because it will both decrease the signal swing and probably shift the common-mode voltage.

This circuit is very simple, but is constrained on available voltage swing and source impedance settings. A second example is shown in Figure 3, where this resistive load is combined with a transformer to convert the differential voltage signal to single-ended and remove the common-mode voltage.

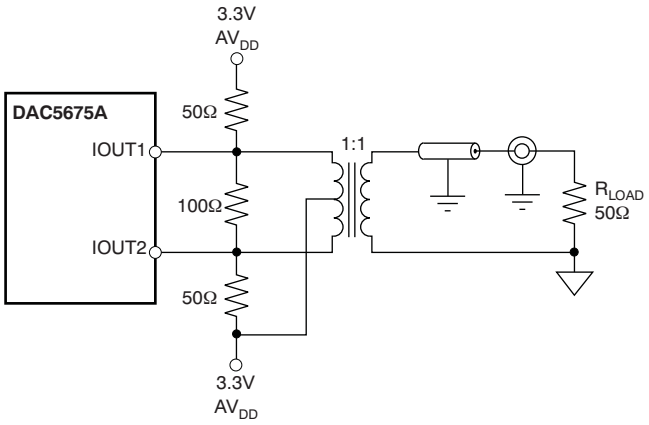

Figure 3. Resistive Load with Transformer Coupling

This implementation pulls the DC common-mode current (in this case I_R, because it will be the total from both outputs) from the transformer centertap. Since that is a low impedance path, the common-mode voltage at the DAC current source outputs will be AV_{DD} (3.3V). At higher frequencies, the transformer will reflect the 50Ω load through to appear across the transformer primary in parallel with the 100Ω resistor. This reflection, along with the two 50Ω resistors to 3.3V, will give a 25Ω differential load. This differential load can see a maximum of 20mA in one direction and 20mA in the opposite direction, giving a maximum differential voltage swing at the transformer of ±0.5V around 3.3V. Each output will be swinging ±0.25V to get this ±0.5V differential swing. Again, this configuration is a very simple interface that is now AC-coupled differential to single-ended, but somewhat constrained on gain and source impedance flexibility.

2 Transimpedance-Based Interface Circuits

One option occasionally shown in DAC data sheets is a current-to-voltage configuration for an op amp. Often, this configuration is shown as a single-ended implementation with the other output shunted off to ground or the supply, depending on the DAC output current polarity. Figure 4 shows a typical circuit from the DAC5675A data sheet. As usually occurs, there is minimal discussion in the data sheet of setting C_{FB} beyond limiting the sharp edge rates of the converter output.

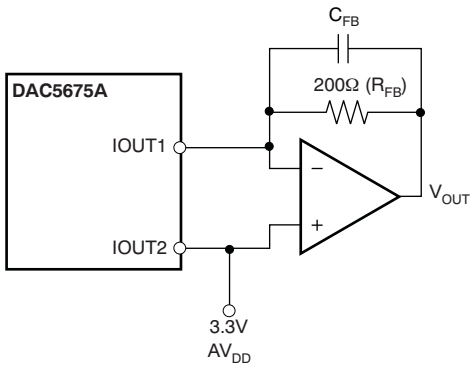

Figure 4. Typical DAC Output Transimpedance Interface

The intended advantages of this transimpedance design include a more flexible gain for the current output signal and impedance isolation from the DAC output currents to the load at V_{OUT}. The DAC output current source ideally would believe it is driving a low impedance referenced (in Figure 4) to AV_{DD}. This circuit wastes half of the available output current and leaves V_{OUT} referenced to AV_{DD}. As shown in Figure 4, this interface is also producing a unipolar V_{OUT} swing—from AV_{DD} with only a swing above AV_{DD}.

3 Enhanced Differential Transimpedance Interface Design

Where a differential output signal is desired, the circuit of Figure 4 can be adapted to provide a differential transimpedance gain stage with common-mode level shifting. Two possible implementations will be demonstrated; these possible configurations differ only in whether the input or output common-mode needs to be controlled by adding a current into the inverting summing junctions.

Figure 5 shows the first implementation using a dual, wideband voltage feedback op amp (VFB), while Figure 6 shows a similar implementation using a wideband FDA. Both configurations are shown where the current sinking output of the DAC5675A is assumed, but can be easily adapted to a current sourcing-type DAC.

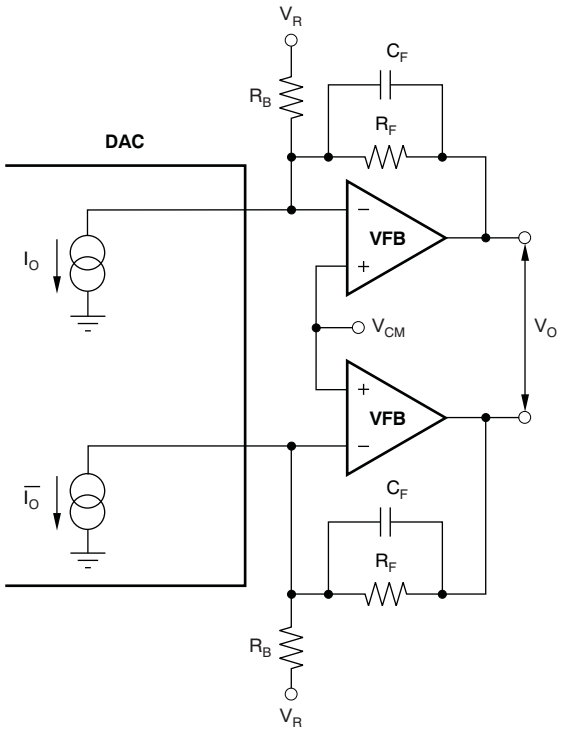

Figure 5. Differential Transimpedance Using a Dual VFB Op Amp

The DAC is shown in Figure 5 using another common nomenclature for DAC output currents. However, this configuration is still physically the complementary current output model of Figure 1.

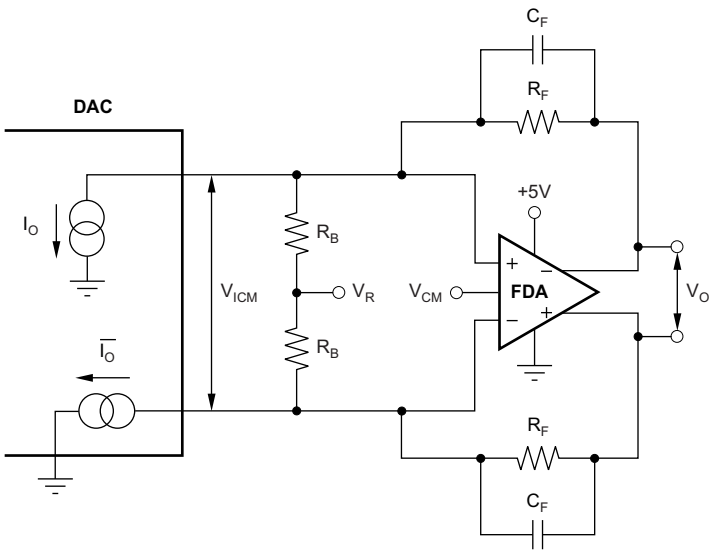

Figure 6. Differential Transimpedance Using a Wideband FDA

For designers new to FDAs, these devices are essentially differential input to differential output VFB amplifiers with a separate control for the DC common-mode output voltage (V_{CM} in Figure 6). They can also be thought of as a dual differential inverting op amp structure with an embedded output common-mode control loop. For a primer on FDA operation and applications, see Ref. 1.

Both circuits provide a signal gain set by R_F to the DAC current source outputs. The principal issue for the signal path in both cases is the proper selection of C_F. That analysis is presented below and will be the same for both implementations. In both cases, the input and output common-mode voltages will also need design consideration. The op amp circuit in Figure 5 sets the *input* common-mode voltage, which will also be the DAC compliance voltage (voltage that the DAC currents believe they are driving into), using the noninverting input bias voltage. This DC voltage will appear at the inverting nodes as a result of the separate feedback loop of each amplifier. From this input common-mode operating point, an added DC common-mode level shift current is one approach to reference the amplifier output to a desired common-mode operating voltage. This reference is provided via the R_B resistors to V_R.

In contrast, the FDA includes a V_{CM} control voltage to set the *output* common-mode voltage through a control loop incorporated internally to the design. From this reference voltage, the FDA controls its output common-mode voltage, and a similar current into the inverting inputs is required to set an *input* common-mode operating voltage that will make both the DAC and FDA operate correctly. In both circuits, a solution for R_B is required before a solution can be derived for C_F. The design sequence will be to select an R_F to give the desired maximum signal swing at the output of the amplifiers; then, a bias voltage will be set on the op amp inputs to control the inverting DC voltage (or, for the FDA, the output common-mode voltage). An R_B will then be resolved to satisfy the desired input or output common-mode targets. A C_F may then be resolved to hit a desired closed loop frequency response shape from the DAC current source outputs to the amplifier voltage outputs.

The desired frequency response from the DAC outputs into the final signal path is unique to each application. Normally, some sort of image frequency rejection filter is designed into the channel. Sometimes this filter includes a SinX/X correction in the frequency response shape. Here, it will be assumed that this filter follows the amplifier stage. This interface is intended to provide:

1. Common-mode level shift.
2. High dynamic range for the intended signal.
3. Stable operation for the amplifier with good frequency response flatness through the desired frequency range of interest.
4. Impedance isolation and gain flexibility. The DACs will always see a low impedance to the input common-mode voltage. The gain is set by a feedback resistor and the amplifiers can drive a load (normally a filter) with a low output impedance.

5. The slight peaking of a SinX/X equalization can be easily included in the second-order, low-pass design that will be described below. However, the image rejection filter is intended to follow this stage, because implementing the transimpedance stage as a low-pass filter for image rejection will reduce the loop gain and thereby increase distortion. It would be preferable that this stage pass the desired frequency band with quite a bit of added bandwidth to keep good loop gain in the desired frequency band.

This basic design benefits strongly from the differential design. Done correctly (Ref. 2), even-order harmonic suppression should be very good, leaving only odd-order harmonics at the output as a result of the amplifier and DAC.

4 Common-Mode Control

Since these are differential I/O designs, we must consider both the common-mode issues and the differential signal path issues. On the input side, the common-mode voltage will be shared by the DAC output current sources and the amplifier input stage, because for the transimpedance configuration there is no voltage drop from the DAC outputs to the amplifier inputs. Both the DAC and the amplifier will have an allowed range of DC voltage values. For the DAC, the common-mode voltage is often called a *compliance voltage range*, while for amplifiers it is often called a *common-mode input range* (CMIR). The issue for the DAC is: Over what range of compliance voltage will the DAC output current sources operate with best linearity? The issue for the amplifier is: Over what range of CMIR will the amplifier input stage operate in a fashion that also maintains good linearity?

There is generally very limited data for the DAC performance versus compliance voltage. Ideally, we would like to see a spurious-free dynamic range (SFDR) versus compliance voltage curve. Normally, we can expect this compliance voltage to be bounded by one of the DAC power supplies and some relatively small deviation from that supply. For a device such as the DAC5675A where the outputs are sinking current sources, the compliance voltage is specified from the positive supply +0.3V to that supply –1V. Operating beyond the stated supply range is sometimes specified, and is usually limited to either the turn-on voltage for any ESD steering diodes that might be on those pins or breakdown voltages for the CMOS drain output devices that make up the current sources. For DACs such as the DAC2932 where current is sourced out of the DAC, the compliance voltage is specified as –0.5V to +0.8V, which is typical for a high-speed current steering DAC with outputs driving current out of the device.

In either case, that same DC voltage will be the common-mode input voltage for the amplifier in the circuits shown in Figure 5 and Figure 6. Most amplifiers are specified with an input voltage range on specified power supplies. These limits are actually headroom specifications, and can be re-interpreted to set an allowable voltage range on other supply settings by taking the difference between the specified supply voltages to input voltage range in order to determine the required headroom for the amplifier.

For the op amp based circuit, once the power supplies are set and the noninverting input bias voltage is set to control the DAC compliance voltage and op amp input common-mode voltage, the desired output common-mode voltage will allow us to solve for the required level-shifting current from the V_R path. Lacking any other constraints, such as a DC bias voltage for a subsequent stage, the output common-mode voltage would most likely be set midscale between the two supply voltages for the op amp. This setting will balance the headroom on each side of the output swing around this common mode, usually giving the best SFDR. Once this target is set, the circuit of Figure 7 can be used to determine the R_B resistor value. Here, and in the compensation analysis to follow, half-circuit analysis is used; the results are simply duplicated to the other side for a differential interface.

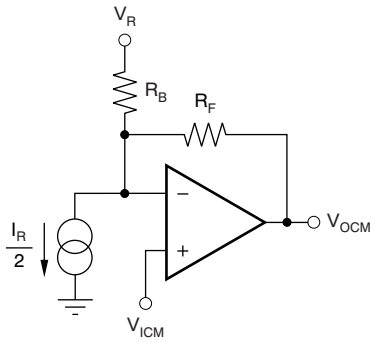

Figure 7. Output Common-Mode Analysis for the Op Amp Interface

The total output common-mode voltage is a superposition of the three sources summing at the inverting inputs. These three sources are V_{ICM} (the common-mode voltage applied to the noninverting inputs); $I_R/2$ (the common-mode current level coming out of the DAC); and V_R, through the R_B resistor. Essentially, with V_{ICM} set to make both the amplifier and DAC operate correctly, the DAC reference current will then level-shift the output positive (in the polarities of Figure 7) and a V_R is used to level-shift it back to a target V_{OCM} by solving for R_B.

The equation for V_{OCM} is shown as Equation 1, while Equation 2 solves this for a required R_B value.

$$V_{OCM} = V_{ICM} + \frac{I_R}{2} R_F - (V_R - V_{ICM}) \frac{R_F}{R_B} \quad (1)$$

$$R_B = \frac{V_R - V_{ICM}}{\frac{I_R}{2} - \frac{V_{OCM} - V_{ICM}}{R_F}} \quad (2)$$

The examples will illustrate selecting R_B, but in general we would like it to be greater than R_F. This additional common-mode control resistor at the input will change the DC noise gain for the amplifier. Designs that require $R_B < R_F$ will be operating at a higher noise gain at lower frequencies. This higher noise gain tends to reduce bandwidth, degrade distortion, and increase output noise over designs that keep $R_B > R_F$. This suggestion usually means that V_R should be selected as the highest supply (or lowest, if a negative supply is needed) available in the system.

An identical analysis can be performed for the FDA based interface. Here, it is the output common-mode voltage that is controlled using the V_{CM} input pin to the FDA. But similarly, current summing at the inverting input with a target V_{ICM} will allow R_B to be set in a fashion that will achieve that target V_{ICM}. Doing this analysis actually gets back to Figure 7 with Equation 2 being the correct equation for setting R_B.

5 Setting the Compensation Capacitor

The remaining element in the design is the required feedback capacitor C_F across the feedback resistor R_F. Contrary to most DAC descriptions of this capacitor, it is not really there to limit the fast edge rates of the DAC output current (while it may appear to have this effect); rather, this capacitor is included to control the closed loop frequency response of the amplifier circuit. Without this capacitor, most high-speed amplifiers will show a very peaked closed loop frequency response when driven from a capacitive source (C_S = DAC output capacitance + op amp and layout parasitic). If the closed loop frequency response is peaking, then each DAC step will cause an overshoot and ringing in V_O.

Figure 8 shows the Laplace analysis circuit for each half-circuit in the differential I/O interface where a single pole response for the amplifier is assumed. This assumption is reasonable in most cases, because the effect of the source capacitance along with the feedback capacitor will be to shape the noise gain to a higher level at crossover, pulling back the crossover frequency, and allowing the higher-order open loop amplifier poles to be initially neglected.

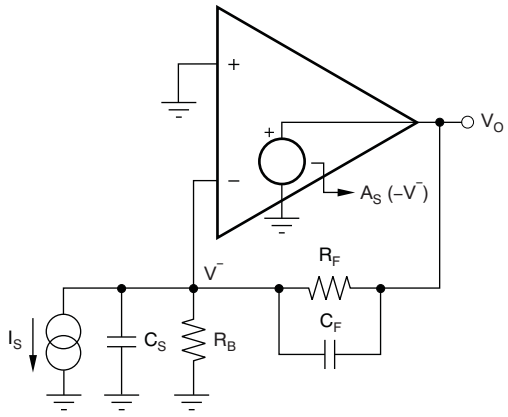

Figure 8. Frequency Response Analysis Circuit

Working with this single pole model for the VFB open loop response allows a second-order transfer function to be developed, as shown in Equation 3.

$$\frac{V_O}{I_S} = \frac{\dfrac{A_{OL}\omega_a}{C_S + C_F}}{s^2 + s\left(\dfrac{C_F}{C_S + C_F}A_{OL}\omega_a + \dfrac{1}{(R_F \parallel R_B)(C_S + C_F)} + \omega_a\right) + \dfrac{A_{OL}\omega_a}{R_F (C_S + C_F)}\left(1 + \dfrac{1 + \dfrac{R_F}{R_B}}{A_{OL}}\right)} \quad (3)$$

This equation models the Laplace single pole open loop gain of the op amp $A_{(s)}$ is modeled as:

$$A_{(s)} \equiv \frac{A_{OL}\omega_a}{s + \omega_a}$$

where $A_{OL}\omega_a$ is the Gain Bandwidth Product (here, in radians).

Looking at this transfer function, we can identify the key pieces as shown in Equation 4.

DC gain (s = 0) will be:

$$\frac{V_O}{I_S} = \frac{R_F}{1 + \dfrac{1 + \dfrac{R_F}{R_B}}{A_{OL}}} \quad (4)$$

Which is correct. This is essentially the desired gain of R_f with a 1/(1+1/LG) error term where the Loop Gain (LG) is set by the open loop DC gain of the amplifier divided by the noise gain ($1 + R_{Ff}/R_B$).

The characteristic frequency of the this second-order low-pass transfer function is given by Equation 5.

$$\omega_O^2 = \frac{A_{OL}\omega_a}{R_F (C_S + C_F)}\left(1 + \frac{1 + \dfrac{R_F}{R_B}}{A_{OL}}\right) \quad (5)$$

This will simplify considerably if we recognize again that the 1 + 1/LG term is approximately equal to 1, and drop the $(1+ R_f/R_b) / A_{OL}$ part of this expression.

The linear coefficient of the pole equation gives Equation 6:

$$\frac{\omega_O}{Q} = \omega_a\left(\frac{1}{1 + \dfrac{C_S}{C_F}}A_{OL} + 1\right) + \frac{1}{(R_F \parallel R_G)(C_S + C_F)} \quad (6)$$

Again, this will simplify later if the '1' in the first term is dropped, recognizing that the $\frac{A_{OL}}{(1 + \frac{C_S}{C_F})}$ term will be >> 1.

Making those simplifications in the transfer function will give Equation 7:

$$\frac{V_O}{I_S} = \frac{\frac{A_{OL}\omega_a}{C_S + C_F}}{s^2 + s\frac{C_F}{C_S + C_F}\left[A_{OL}\omega_a + \frac{1}{(R_F \parallel R_B)\, C_F}\right] + \frac{A_{OL}\omega_a}{R_F\,(C_S + C_F)}} \quad (7)$$

Now, let's identify a few of the pieces in this transfer function in terms that will be shown on a Bode plot of the open loop gain vs. the noise gain.

$$\frac{1}{R_F\,(C_S + C_F)} = Z_0$$

This will be the projection of the rising portion of the noise gain back to intersection with 0dB in order to give a zero frequency in the noise gain.

$$\frac{1}{R_F C_F} = P_1$$

This will be the pole frequency of the noise gain that we are trying to set.

$$1 + \frac{R_F}{R_B} = G1$$

This is the DC noise gain. $G1 \bullet Z_0$ is the actual zero in the noise gain.

$$1 + \frac{C_S}{C_F} = G2$$

This is the high-frequency noise gain.

The noise gain for this circuit transitions from a DC level set by $1 + R_F/R_B$ to a (normally) higher noise gain set by $1 + C_s/C_F$ where the zero frequency is $G1 \bullet Z_0 = Z_1$ and the pole frequency is P_1.

Rewriting the closed loop transfer function (Equation 7) in these terms, and using gain bandwidth product $GBW = A_{OL}\omega_a$, we get Equation 8.

$$\frac{V_O}{I_S} = \frac{\frac{A_{OL}\omega_a}{C_S + C_F}}{s^2 + s\frac{1}{G_2}\left[GBW + \frac{G_1}{P_1}\right] + GBW \bullet Z_0} \quad (8)$$

Equation 8 gives a reasonably simplified transfer function that will allow a solution for P_1, given a targeted Q in the desired frequency response. Before we pursue that, it is also useful to look at the Bode plot of the loop gain in these terms. To do this, we need to analyze the feedback voltage divider from the output pin to the inverting input; which, when inverted, will give us the noise gain that is usually plotted along with the open loop gain of the amplifier to show the loop gain as the delta between these two curves.

Figure 9 shows the feedback circuit while Equation 9 gives the transfer function from the output voltage back to the inverting input pin.

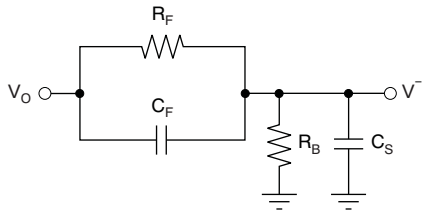

Figure 9. Analysis Circuit for the Feedback Divider

$$\frac{V^-}{V_O} = \frac{1}{1 + \frac{C_S}{C_F}} \bullet \frac{s + \frac{1}{R_F C_F}}{s + \frac{1 + \frac{R_F}{R_B}}{(C_S + C_F)R_F}} \tag{9}$$

Inverting this gives the noise gain expression as Equation 10 that can then plotted as 20 • log (noise gain magnitude) on a Bode plot and compared to the open loop gain of the amplifier.

$$\frac{V_O}{V^-} = \left(1 + \frac{C_s}{C_F}\right) \frac{s + \frac{1 + \frac{R_F}{R_b}}{(C_s + C_F)R_F}}{s + \frac{1}{R_F C_F}} = G_2 \frac{s + G_1 Z_0}{s + P_1} \tag{10}$$

Letting s = 0 (DC) in Equation 10 will reduce the noise gain to $1 + \frac{R_F}{R_B} = G1$.

As s →∞, the noise gain approaches $1 + \frac{C_S}{C_F} = G2$.

Plotting Equation 10 on a Bode plot with a generalized single pole open loop gain plot gives Figure 10.

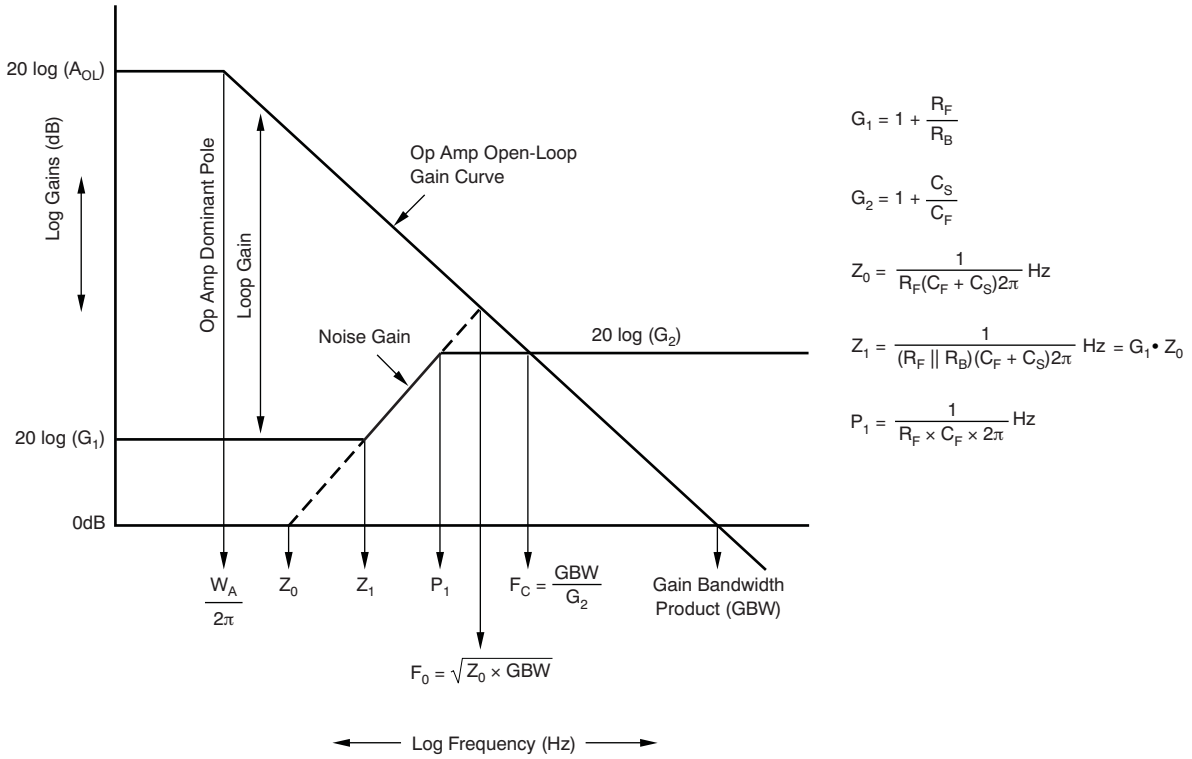

Figure 10. Bode Plot of Open Loop Gain and Noise Gain for Figure 8

Looking at this problem graphically, the common-mode level shift solution that gives R_B will also be setting the low frequency noise gain G_1. We would prefer that this be low in order to maximize the loop gain and reduce the output noise. Moving C_F around will be adjusting both Z_0 and P_1. Adjusting Z_0, with a fixed GBW, will be adjusting the characteristic frequency (F_0) as well.

Eventually, the noise gain transitions flat at what will normally be a higher level of $G2 = 1 + \frac{C_S}{C_F}$. This analysis is simplified quite a bit by ignoring the higher order poles of the open loop response. That is a reasonable approximation, as long as the added phase shift in the open loop response because of the higher frequency poles at the crossover frequency is < 20°. This will be an important final check once the design is done—particularly if non-unity gain stable amplifiers are applied to this interface. If this design check is not satisfied, the final solution will probably show more peaking than expected in the frequency response, thus giving a ringing pulse response.

The preceding discussion allows us to visualize what is happening inside this circuit from a loop gain standpoint. To get a solution for C_F, an algebraic solution is required. In this DAC transimpedance application, all of the terms with the exception of the feedback capacitor are already determined. R_F sets the desired gain; R_B is set from a common-mode operating voltage standpoint; C_s is set by the DAC and amplifier parasitics; and the GBW is set by the amplifier chosen. Assuming that a design with some level of peaking (or Q) in the frequency response is desired from a given amplifier, the only term left is the feedback capacitor, C_F. A solution for the feedback pole location can be derived where a target Q is desired and the resulting ω_0 is simply taken as what results.

We can estimate a minimum required GBW by noting that the F_0 is set by GBW and Z_0 (Figure 10). Even though we do not know Z_0 without setting C_F, we can estimate it using just C_s— where we will normally see C_F resolved to a lower value than C_s, moving Z_0 down slightly from this estimate. From a target F_{-3dB} and assuming that a near-Butterworth closed loop response is desired (a design that will give $F_{-3dB} = F_0$), we can estimate the lower limit on amplifier GBW by solving Equation 11 (in Hz).

$$\frac{(F_{-3dB})^2}{Z_0} = (F_{-3dB})^2 2\pi R_F C_S = \text{GBW } \textit{(Minimum)} \tag{11}$$

With an amplifier selected that offers a GBW product greater than that given by Equation 11, we can solve for an algebraic solution to get the required feedback pole that gives the target Q. That solution can be written as a quadratic of the time constant of the feedback pole (R_fC_f), as shown as Equation 12.

$$(R_FC_F)^2 + (R_FC_F)\frac{2Q^2G_1 - 1}{Q^2GBW} + \left(\frac{G_1}{GBW}\right)^2 - \frac{R_FC_S}{Q^2GBW} = 0 \quad (12)$$

Everything in this expression is already set except C_F. We know these terms:

- the desired transimpedance gain (R_F);
- we know the GBW of the amplifier selected (in radians, for Equation 12);
- we know the total capacitance on the inverting input of the op amp (C_s);
- we know the low frequency noise gain, $G_1 = 1 + \frac{R_F}{R_B}$;
- and we select a targeted Q

This equation will then give the required time constant of the feedback pole (R_FC_F) to achieve a particular Q. From this, a required C_F value can be determined; then, Equation 5 will give the resulting ω_0.

An alternative approach would be to target a particular frequency response by setting a target ω_0 and Q, then add an extrinsic C_s to the parasitics on the inverting inputs to give an added degree of freedom needed to set both Q and ω_0. This approach will work, but acts to peak the noise gain intentionally at lower frequencies to get the bandlimiting or shaping in this transimpedance stage. That will be reducing the loop gain and peaking up the noise to implement a filtered shape in the frequency response. It would probably be preferable to simply pick an amplifier with approximately the right GBW and then postfilter to achieve a bandlimited response, if desired.

6 Example Designs

To apply this approach to a particular design requirement introduces a few additional issues. The first concern is that the selected amplifier must have adequate slew rate to support the desired output signal. For instance, a 70MHz IF output, where the desired maximum differential V_{PP} output voltage is $4V_{PP}$, would require a differential slew rate set by Equation 13.

$$F_{max} \bullet (2\pi) \bullet V_{PEAK} = SR \text{ (slew rate)} \quad (13)$$

In this example, that works out to:

$70MHz \bullet (2\pi) \bullet 2V = 879V/\mu s$

This is what the signal would be asking for from the amplifiers. If very low distortion is also required, then some margin of capability above this value will be required in the amplifiers. Typically, for moderate distortion performance, at least a 4X margin is required; extremely low distortion normally requires greater than a 10X margin. If the required signal is a pulse-oriented signal, then this slew rate discussion can be recast in terms of a non-slew limited rise time. For this type of signal, we need the targeted amplifier bandwidth and the maximum step size. To avoid slew limiting in the pulse response, we would need the rise time implied by the bandwidth target to give a pulse transition rate for the maximum step size that does not exceed the slew rate. Linear operation by definition gives a step size-independent rise time. Hence, larger steps (ΔV) with a fixed rise time (ΔT) give an increasing transition rate ($\Delta V/\Delta T$). A good approximation (the 10% → 90%) for ΔT is $0.35/F_{-3dB}$, even for a second-order Butterworth type response. Then, from a maximum desired output step size (ΔV_{max}), we can compute the minimum required slew rate in the amplifier as Equation 14.

$$SR_{min} = \Delta V_{max} \bullet \frac{F_{-3dB}}{0.35} \tag{14}$$

For example, if a 100MHz bandwidth design is desired, and the maximum differential pulse step size is intended to be 4V, then the maximum pulse transition rate will be:

$$SR_{min} = 4 \bullet \frac{100MHz}{0.35} = 1143V/\mu s$$

In this case, not nearly as much design margin over this calculation is required. Normally, a 2X multiplier will be adequate. It is preferable to avoid a slew limited response, because slipping into slew limit can cause excessive overshoot and an extended settling time from what a linear response can provide.

It is important to apply this slew rate analysis correctly between FDA and VFB implementations. The specified slew rate for an FDA will be the differential slew rate, while all VFB op amps will be reporting the slew rate for each amplifier separately. Therefore, the available slew rate in a VFB implementation will be double the reported number.

6.1 Example 1

Use a DAC2932 low power, 40MSPS, dual 12-bit DAC to provide a large signal pulse oriented signal with up to 10MHz harmonic content using a dual voltage feedback op amp. In this case, the DAC2932 provides a complementary current source output that is sourcing current out of the two output pins. It is, then, looking for a grounded load in single-supply implementations.

One of the advantages of a differential transimpedance stage following a low power DAC is that very high full power bandwidth signals can be provided without using a lot of power in the DAC itself. The DAC2932 is only a 2mA reference current device. Each of the two DACs use only 29mW total power when clocked at 40MSPS on a 3V single supply. Now we will target up to a $14V_{PP}$ differential signal using a ±5V dual op amp interface. The design proceeds in this manner:

(a) Check the slew rate—each output is ±3.5V maximum, which (at 10MHz) requires a slew rate equal to: $3.5 \bullet 2\pi \bullet 10MHz = 220V/\mu s$ slew rate. It would be best to have a margin greater than 2X, so we will target an amplifier > 440V /μs.

(b) Use Equation 11 to estimate the minimum required gain bandwidth product. The DAC specifies 5pF output capacitance. Each output is intended to develop a $7V_{PP}$ swing from the 2mA full-scale current. This requires R_f to be set at 3.5kΩ. Estimate an added capacitance on the inverting nodes of 2pF for the amplifier and layout parasitics. To pass 10MHz harmonics with good performance, target an F_{-3dB} of 40MHz in the amplifier design. Plugging all of this into Equation 11 gives GBW_{MIN} = 240MHz.

To continue the design, set a target peaking in the response of 0.2dB which will imply a Q = 0.80. Recall that with only the feedback capacitor as a single frequency response control element, we can only target either the Q or ω_0 in the design. Here we are targeting a Q and taking what ω_0 results—but starting out with enough gain bandwidth to assure that we achieve a desired F_{-3dB}. Once this stage is correctly designed, a passive postfilter can be added to bandlimit the noise and smooth the DAC steps (which is another way of saying that the image frequencies need to be attenuated).

The DAC2932 has an output complementary current source structure that would like to drive into ground. Setting the input common-mode target to 0V and the output common-mode target to 0V in order to center the swing on a ±5V supply, the R_B resistor of Figure 7 needs to be set only to account for the midscale common-mode output current from the DAC = $I_R/2$ = 2mA/2 = 1mA. Using ±5V supplies for the OPA2690 gives us a –5V supply to satisfy the common mode Equation 2. Plugging into Equation 2 gives a required R_B to the –5V supply of 5kΩ. Essentially, this 5kΩ sinks the 1mA common-mode current coming out of each DAC output from the 0V common-mode set up by the grounded noninverting inputs of the OPA2690 to the –5V supply.

One concern might be –5V supply noise getting into the signal path through these 5kΩ R_B resistors. To the extent that the resistors in the two channels are matched, supply noise will show up at the output as common-mode noise. Whether this error source is an issue then becomes a question of common-mode rejection in the next stage. Supply noise will also get into the differential output, to the extent that the gains are mismatched between the two channels. To compute the effect of this mismatch, we must first look at the ideal gain from V_R to the outputs. In this case, that will be –3.5k/5k = –0.7V/V. Using ±1% resistors, the maximum gain from the common-mode V_R to a differential output will be 0.7 • (1.02 – 0.98) = 0.028 or –31dB common-mode to differential conversion. If this is inadequate to the application requirements, precision resistors may be required. This consideration adds to the earlier comment that relatively low DC noise gain is preferred in solving for R_B. Here, G1 solves to 1.7, which then gives a gain of 0.7 from V_R to the output; this helps to attenuate DC shifts and/or noise from the –5V supply to the outputs.

To continue the design, a more accurate estimate for C_s is required. The OPA2690 shows C_m = 0.6 and C_{diff} = 0.9. Adding those capacitors, plus 1pF layout parasitic to the 5pF specified for the DAC, gives 7.5pF total for C_s. Plugging all of these values into Equation 12 solves for an R_FC_F = 4.14ns. Solving this for the pole location gives 38.5MHz, which requires C_F = 1.2pF. This then gives a G_2 = 7.25. Figure 11 shows the completed design. Putting in the actual GBW and C_s value of the OPA2690 solution into Equation 5 gives an expected $\omega_o = 2\pi(39.65\text{MHz})$. Using standard second-order low-pass filter equations, this ω_o and Q should give an F_{-3dB} of 44.05MHz.

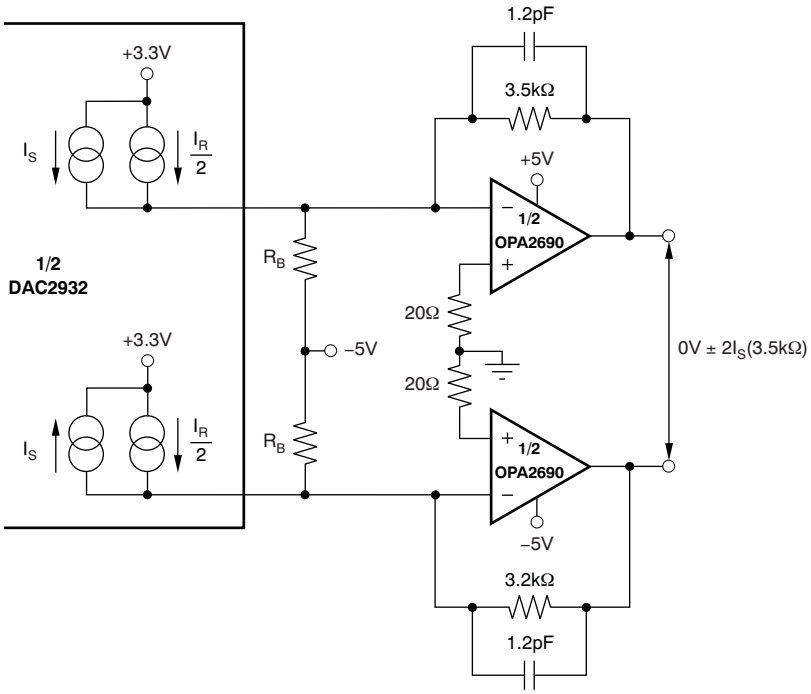

Figure 11. DAC2932 Interface Using the OPA2690

One important check to the design are the actual noise gain plots—essentially, Figure 10 using the real values for the design. That data is shown in Figure 12, where phase information is also included. Here we see exactly what we would expect: a non-zero, low-frequency noise gain (> 1V/V or 0dB) with a zero coming in, then a pole. This configuration shapes the phase to give the required phase margin at crossover to achieve complex poles, even though a single pole assumption was made for the op amp open loop gain model. The feedback pole here is critical to pull the phase back down the exact amount

necessary at crossover. Another important check here is that the added phase shift resulting from the actual higher-order poles of the op amp do not materially impact the overall phase margin of the design. The plot of Figure 12 estimates a crossover frequency at 51MHz, where the total phase margin is 57°. The open loop response has only detracted 5° from this amount at this low crossover frequency. The total open loop phase shift is 95° at 51MHz. This should give a closed loop response very close to that predicted in the simplified analysis presented here.

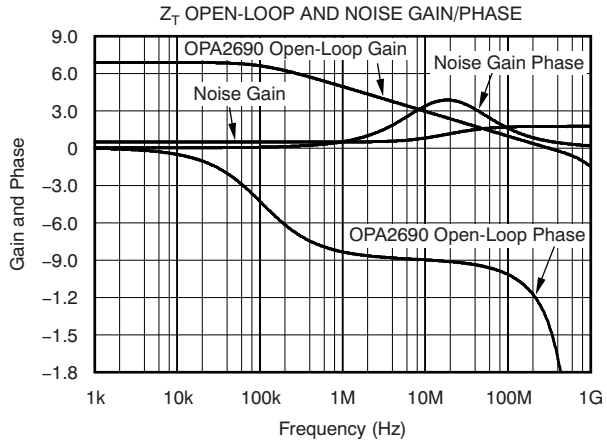

Figure 12. Loop Gain and Phase Analysis of Figure 10

The assumption used in deriving Equation 12 was that the op amp can be modeled by a single pole response. In Figure 12, this would mean that the amplifier open loop phase comes down to –90° and stays there. The actual plot shows the effect of higher order poles; but, because the noise gain intersected the open loop response at a relatively low frequency, the impact of these higher order poles was negligible. Higher frequency applications, or where non-unity gain stable amplifiers are applied, will deviate more from this ideal assumption. The closed loop response for one side of Figure 11 is shown as Figure 14. The total gain will actually be double this in the differential I/O implementation.

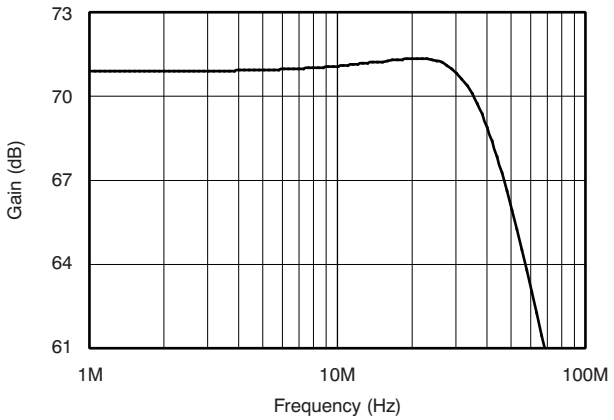

Figure 13. Small Signal Frequency Response of Example 1 in Figure 12

The low-frequency gain is 70.87dB, which is slightly below 20log(3.5kΩ) because of loop gain effects (Equation 4). From this, there is slightly more than the targeted 0.2dB peaking (0.46dB actual peaking) and the F_{-3dB} is very nearly equal to the expected 44.05MHz (43.9MHz). Through 10MHz, the plot shows less than 0.1dB deviation from flatness. This shows very good correlation to the expected result, which stems directly from the very slight added open loop phase shift at loop gain crossover (where the noise gain intersects the open loop gain). This circuit will be able to easily produce a $14V_{PP}$ differential waveform into 200Ω differential loads with excellent flatness and phase linearity through 10MHz. Using ±5V supplies, the OPA2690 adds 110mW quiescent power to the low 29mW used for each channel of the DAC2932.

6.2 Example 2

In this example, we will adapt the previous design to single +5V operation.

The OPA2690 holds up very well to reduced +5V operation. It is not, however, a rail-to-rail (RR) output design, and the input needs about 1.5V headroom to each supply to operate correctly. With no negative supply, the common-mode control will need to be through a resistor to ground, meaning that the input common-mode can no longer be at the preferred setting of 0V for the DAC2932. The DAC2932 specifies a maximum compliance voltage of 0.8V, but this low level (relative to ground) will be outside the OPA2690 input range. The 0.8V maximum limit on the input common-mode voltage leads towards RR output amplifiers that include the negative rail on the input range. In this case the OPA2355, a CMOS RR output, dual op amp seems applicable. The gain bandwidth product of 200MHz seems a bit low, but the slew rate of 300V/μs will be adequate to this reduced swing requirement. Specifically, if 10MHz flat bandwidth with a $4V_{PP}$ output is desired from each amplifier, the maximum signal slew rate will be 126V/μs for each side of the differential output—which is well below the specified 300V/μs. We will step through the same design steps that we used for Example 1.

Turning the 2mA full-scale current of the DAC2932 into $4V_{PP}$ on each OPA2355 output centered at 2.5V output common-mode voltage (giving an $8V_{PP}$ differential swing with 0.5V headroom to each supply) requires R_F = 2kΩ. To keep the DC noise gain (G1) as low as possible, the target input common-mode voltage needs to be as high as possible. Because the OPA2355 can swing to ground on the input, the maximum limit will be set by the DAC2932 +0.8V specification. Using Equation 2 to solve for R_B gives 432Ω; this value will give a relatively high initial G1 of 1 + 2000/432 = 5.6V/V.

Next, we need to get the total capacitance on the inverting nodes. C_s = 9pF (5pF for the DAC2932 + 1pF layout + 3pF common-mode + differential OPA2355 input capacitance). Table 1 summarizes the solution and computes the resulting response.

Table 1. Total Capacitance Calculation

TERM	NAME	VALUE
Quadratic solution for R_fC_f	$1/P_1$	.315ns
Resulting feedback pole location	P_1	505.66MHz
Required value for C_f	C_f	0.16pF
Computed Z_1 location	Z_1	48.91MHz
Computed value for F_0	F_0	41.70MHz
Computed high-frequency noise gain	G2	58.16V/V
Estimated second-order response Q	Q	0.80
Estimated F_{-3dB} bandwidth	F_{-3dB}	46.33MHz

The extremely high feedback pole seems odd, but a look at the loop gain plots will show what is going on. Figure 14 shows the resulting noise gain and phase plotted on top of the open loop gain and phase for the OPA2355.

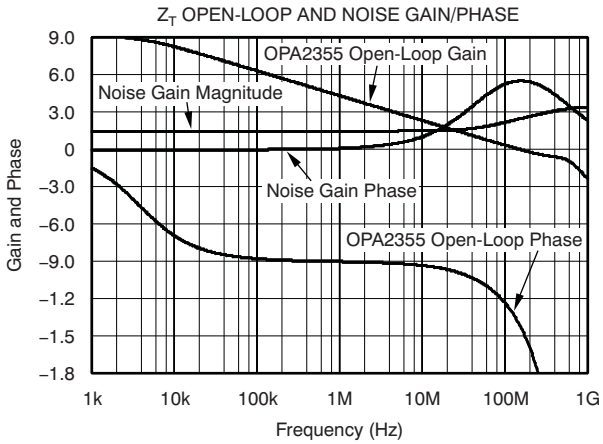

Figure 14. OPA2355 Loop Gain Plot

Here, the higher initial noise gain (G1) pushes Z_1 out to 49MHz, which causes the phase lead required at crossover (about 24.6MHz) to hit approximately a 58° phase margin at loop gain crossover. This effect, by itself, is adequate to hit the desired second-order response; the higher frequency pole in the feedback is really no longer a significant part of the design. In this solution, the common-mode level shift resistor actually provides the needed loop gain characteristic (along with the 9pF on the inverting node) with no feedback capacitor actually required. Figure 15 shows the completed circuit (where the inverting node capacitances are not explicitly shown, but must be present) while Figure 16 shows the simulated frequency response for one side of this circuit using the PSpice® models available on the TI web site.

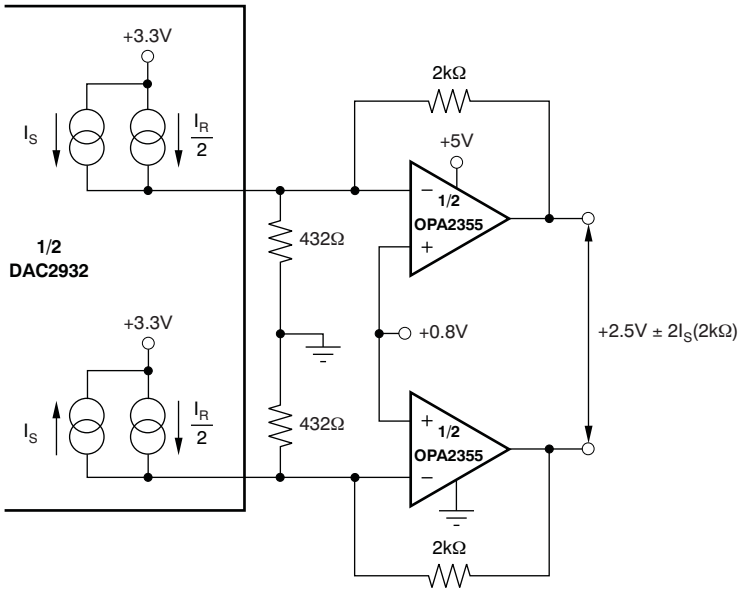

Figure 15. OPA2355 Single +5V Supply Solution

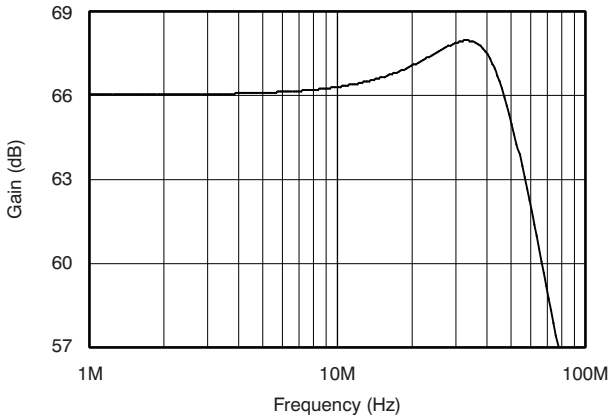

Figure 16. OPA2355 Single +5V Transimpedance Frequency Response

This result is showing quite a bit more peaking than anticipated from the 20log(2kΩ) = 66dB low frequency gain. This peaking arises from a macromodel that has considerably more open loop phase shift at crossover than anticipated from Figure 14. In any case, the flatness through 10MHz is acceptable and the closed loop bandwidth is adequate to the desired design goals. Postfiltering would be an acceptable solution to the added peaking if the physical design shows unacceptable pulse response overshoot and ringing.

6.3 Example 3

This example will use the DAC5675A to produce a 70MHz IF signal with high 70s, two-tone third-order intermodulation performance. Output single tone power level (at a matched load) is 4dBm for each tone. For single tone testing, this is $1V_{PP}$ at the load for each tone, and 4X that amount for the differential output swing at the amplifier outputs (or $4V_{PP}$ maximum differential swing across the amplifier outputs, if series 25Ω output resistors are assumed to a 50Ω load). At 70MHz, the output differential signal will be asking for:

$$70MHz \bullet (2\pi) \bullet \frac{4V}{2} = 879V/\mu s \text{ (slew rate)}$$

For a high 70s SFDR, we probably need a margin of about 6X, or 5274V/μs differential slew rate capability in the amplifier solution.

The DAC5675A shows 5pF output capacitance; we will add another 1pF for the layout and 2pF for the amplifier to get an estimated C_s = 8pF. For good flatness through 70MHz, we need at least 300MHz small signal bandwidth. With a full 20mA peak-to-peak on each output of the DAC5675A, we are trying to produce $2V_{PP}$ on each output, requiring R_f = 2/20mA = 100Ω. Using Equation 11 to estimate a minimum required BW, we get;

(300MHz)2 • (2π) • 100Ω • 8pF = 452MHz Minimum Gain Bandwidth Product (GBW)

This is actually an extremely demanding requirement (primarily from a slew rate standpoint). We need to find either an FDA with > 5000V/μs slew rate or a VFB with 2500V/μs slew rate, both with GBW > 500MHz.

One part that shows promise would be the THS4509 on a single +5V supply, where we see:

- Slew Rate: > 6600V/μs
- GBW Product: > 3GHz

Continuing the design with this device, the input headroom is 0.75V to each supply and the output headroom is 1.1V to each supply. If we set the output common-mode target to midsupply (2.5V), each output will be expected to swing between 1.5Vand 3.5V to generate the desired power level. This expectation seems reasonable, giving 0.4V margin to output swing limits. The THS4509 FDA includes a default common-mode output control voltage of midsupply; in this case, then, no actual external control of this output target for the common-mode voltage is required.

On the input side, the DAC5675A will operate with a compliance voltage of 3.0V from its 3.3V power supply. Therefore, we need to provide a common-mode level-shift from the input of 3.0V to the output 2.5V. Using the +5V supply for the THS4509 as V_R in Equation 2 and 20mA for I_R with R_F = 100Ω, we can solve from Equation 2 for an R_B = 133Ω. This will give a G1 = 1.75.

With R_B resolved to give an input common-mode voltage of 3V, we can then use Equation 12 to solve for the exact R_FC_F required to hit our desired frequency response. For this, we need to start out with the correct C_s. The DAC is 5pF, while the THS4509 shows both a common-mode and differential mode input capacitance. For the purposes of this analysis, we would break the differential capacitance in two by doubling it and adding it to the common-mode number. This technique is used in order to get the correct parasitic capacitance to add on each side of the half-circuit analysis, but what will eventually be a differential interface. The THS4509 data sheet shows:

- Differential input capacitance = 0.8pF
- Common-mode input capacitance = 0.5pF

We would then add 1.6pF + 0.5pF to the DAC, plus whatever layout estimate (for example, 1pF here) to get a total C_s = 8.1pF.

The final element required for Equation 11 is a target Q. While some peaking at very high frequencies is acceptable, it would be prudent to target a relatively flat response in this simplified analysis because additional peaking will result from the higher frequency open loop phase shift (not accounted for in this analysis).

Targeting a 0.2dB peaking again, and solving Equation 11, gives the results shown in Table 2.

Table 2. Total Capacitance Calculation

TERM	NAME	VALUE
Quadratic solution for R_fC_f	$1/P_1$	.197ns
Resulting feedback pole location	P_1	806.76MHz
Required value for C_f	C_f	1.97pF
Computed Z_1 location	Z_1	276.62MHz
Computed value for F_0	F_0	688.63MHz
Computed high-frequency noise gain	G2	5.10V/V
Estimated second-order response Q	Q	0.80
Estimated F_{-3dB} bandwidth	F_{-3dB}	765.09MHz

Again, it is instructive to look at the loop gain plots as shown in Figure 17 for this much higher frequency design.

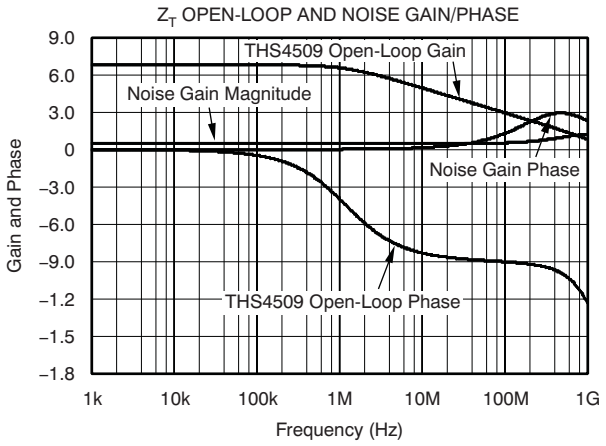

Figure 17. Loop Gain for THS4509 Interface to DAC5675A

In this case, there is a bit more added open loop phase shift as a result of the very high crossover frequency. In fact, while the targeted phase margin for this simplified analysis is about 61°, the actual design predicts approximately 43° phase margin at the 760MHz loop gain crossover frequency. In theory, a 43° phase margin should give about 2dB of closed loop peaking—quite a bit more than the intended 0.2dB peaking in the response. Figure 18 shows the simulated small signal frequency response for this design option (illustrated in Figure 19).

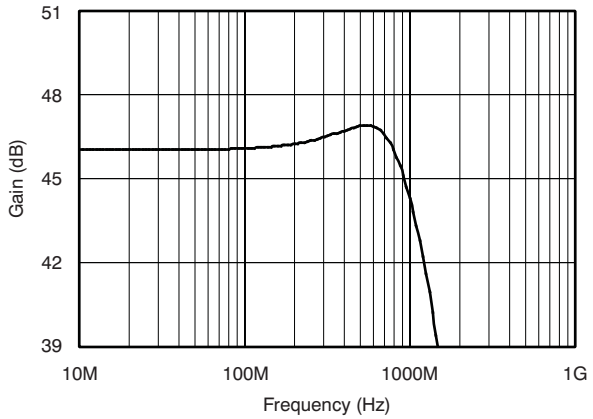

Figure 18. THS4509 Differential Transimpedance Frequency Response

This gain starts at 46dB =20log(2 • 100Ω),then in fact peaks at 750MHz to 47dBΩ, which is somewhat less than the predicted 2dB peaking that a 42° phase margin would predict. The F_{-3dB} is also high, at 1.2GHz

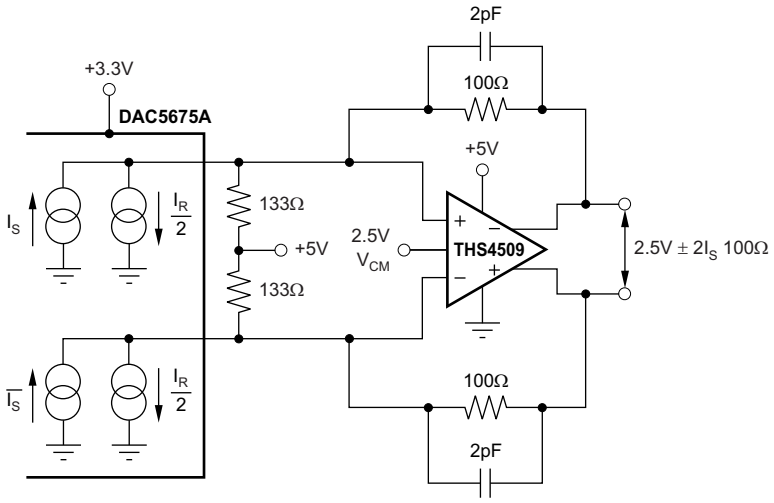

Figure 19. Differential DAC Interface Using an FDA

The actual response showed about 1dB peaking, which is probably acceptable for a 70MHz IF requirement but might have too much noise power bandwidth for the application. To reduce the closed loop bandwidth, one approach might be to add extrinsic capacitance on the inverting node, then recalculate for C_F. As a result of the considerable added bandwidth available in this design, this method will provide a direct means to slow this design down and move it towards lower noise power bandwidth. Adding another 12pF to ground on the inverting nodes of the THS4509 gives a new solution, summarized in Table 3.

Table 3. Total Capacitance Calculation

TERM	NAME	VALUE
Quadratic solution for R_fC_f	$1/P_1$	.352ns
Resulting feedback pole location	P_1	452.98MHz
Required value for C_f	C_f	3.52pF
Computed Z_1 location	Z_1	118MHz
Computed value for F_0	F_0	449.76MHz
Computed high-frequency noise gain	G2	6.72V/V
Estimated second-order response Q	Q	0.80
Estimated F_{-3dB} bandwidth	F_{-3dB}	499.70MHz

The new loop gain plot is shown in Figure 20, where a much lower crossover frequency is achieved with improved phase margin. Here, we see loop gain crossover at 562MHz, which improves the phase margin for the actual design to 51°. In theory, a 51° phase margin will give about 1.2dB peaking in the closed loop design.

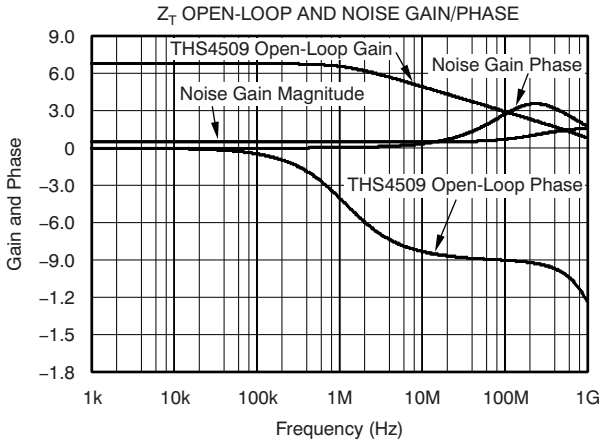

Figure 20. More Compensated THS4509 Design

The modified circuit is shown as Figure 21 (keep in mind that the DAC and amplifier parasitic capacitances are assumed to be present, but not shown.)

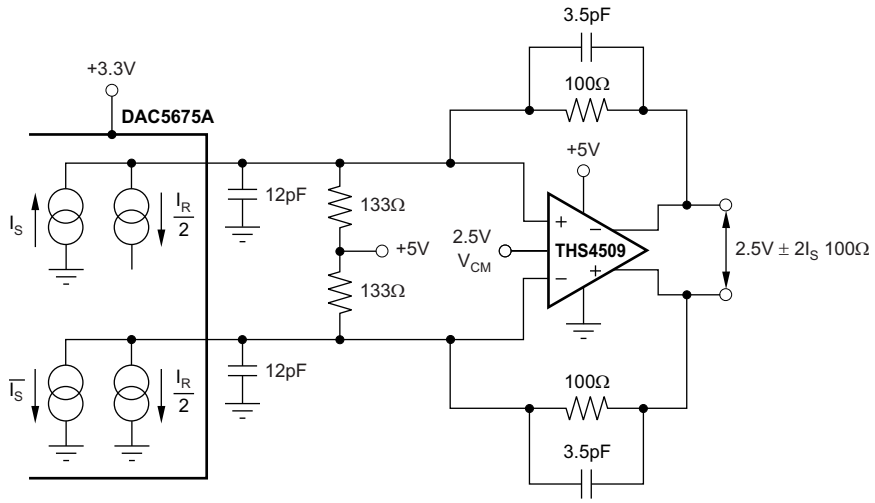

Figure 21. Band-Limited THS4509 Design

Both closed loop frequency response simulations are shown in Figure 22, where the lower bandwidth of the second design and lower peaking are apparent.

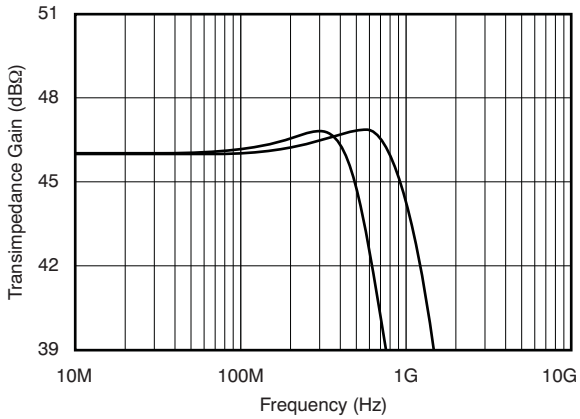

Figure 22. Original and More Compensated THS4509 Designs

It is clear that this technique is very effective at pulling the bandwidth back on the THS4509 solution. The approximate reduction in noise power bandwidth is 50% with minimal extra effort in the design. This approach is particularly useful here in that it still provides the full slew rate of the THS4509 and does not bring the zero frequency in below the desired signal at 70MHz. This configuration holds the loop gain up through the signal band (the loop gain plot shows about 27dB of loop gain at 70MHz) while shaping the higher frequency noise gain to bandlimit the design. (Ref. 3).

7 Conclusions

Wideband DAC designs that require a DC-coupled differential output interface can benefit from a dual op amp or FDA-based differential transimpedance design. The elements of this design require a careful control of the input and output common-mode operating voltages to maintain linear operation of the both the DAC and amplifier. One possible approach is to add a DC common-mode level-shift current into the inverting nodes to separately control the output common-mode voltage for an op amp solution or the input common-mode for an FDA solution. With these resistors set to control common-mode voltages, a closed form solution for the feedback pole location can be used to set C_F if the total capacitance on the inverting node is known and the targeted gain (R_F) and second-order response Q are set. The simplified analysis developed here neglects the phase effects of the amplifier's higher frequency poles, but will give reasonably good results over a wide range of design goals and amplifiers. It is important to check the simulated performance of the design to verify stability. Overpeaked responses can be overcompensated by slightly increasing C_F from the value derived here. This design approach can also be applied to single-ended transimpedance interfaces that only use one side of the DAC output signal. Where a DC-coupled differential to single-ended design is required, a single op amp solution has been shown in numerous sources. Reference 4 steps through an improved version of the single amplifier differential to single-ended design.

8 References

1. Karki, J. Fully differential amplifiers. Texas Instruments application note (SLOA054D).
2. Ramus, X. PCB layout for low distortion high-speed ADC drivers. Texas Instruments application note (SBAA113).
3. Steffes, M. (1997). Unique compensation technique tames high-bandwidth voltage-feedback op amps. *EDN*. 1997:8. Pp. 133-150.
4. Steffes, M. Wideband complementary current output DAC to single-ended interface. Texas Instruments application note (SBAA135).

NOTE: All parts referenced in this article have data sheets that are available for download at www.ti.com.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2008) to A Revision	Page
• Changed Figure 6 amplifier	5
• Changed Figure 19 amplifier	20
• Changed Figure 21 amplifier	22

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265