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APPLICATION BULLETIN
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USING THE CONTINUOUS PARALLEL MODE WITH THE ADS7824 AND ADS7825

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The ADS7824 and ADS7825 are 12-bit and 16-bit converters that have a four channel multiplexed front end. The channel selection on the analog input of these converters is programmable by way of the pins on the devices, A0 and A1 (see Table I). This feature provides the most flexibility by allowing the user to change to the preferred input channel on the fly. Additionally, the input channels can be cycled by utilizing the continuous mode of the converter. This mode is easily enabled by tying the CONTC pin high. In this mode, acquisition and conversions will take place continually, cycling through all four input channels without user intervention.

In the serial mode (PAR/$\overline{SER}$ = LOW), the continuous mode (enabled with CONTC = HIGH) will cause the device to acquire and converter the input signal and cycle through all four channels continually as long as $\overline{CS}$, R/$\overline{C}$ and PWRD are LOW (see Table II). Selection as to which input channel will be accessed first is done with either the PWRD function or the CONTC pin. If PWRD is cycled, the first channel that will be acquired will be channel 0, AIN_0. If CONTC is cycled, the register does not change and the current channel becomes the first in the sequence. When CONTC is HIGH, A0 and A1 address inputs become outputs. When $\overline{BUSY}$ rises at the end of a conversion, A0 and A1 will output the address of the channel that will be converted next. Additionally, data will be valid for the previous channel after $\overline{BUSY}$ rises. See Table II and Figure 1 for channel selection timing in the continuous, serial conversion mode.

A0	A1	CONTC	DESCRIPTION
0	0	0	Enables AIN_0. A0 and A1 are configured as input pins and the user provides instructions to the device to determine which input will be accessed. This channel address is updated just before $\overline{BUSY}$ rises.
0	1	0	Enables AIN_1. A0 and A1 are configured as input pins and the user provides instructions to the device to determine which input will be accessed. This channel address is updated just before $\overline{BUSY}$ rises.
1	0	0	Enables AIN_2. A0 and A1 are configured as input pins and the user provides instructions to the device to determine which input will be accessed. This channel address is updated just before $\overline{BUSY}$ rises.
1	1	0	Enables AIN_3. A0 and A1 are configured as input pins and the user provides instructions to the device to determine which input will be accessed. This channel address is updated just before $\overline{BUSY}$ rises.
0	0	1	Enables AIN_0. A0 and A1 are configured as output pins. A0 and A1 cycle sequentially from one channel to the next as long as CONTC is HIGH. The channel that is being acquired or converted is output on these address lines. Data is valid for the pervious channel. These channels are updated when $\overline{BUSY}$ rises.
0	1	1	Enables AIN_1. A0 and A1 are configured as output pins. A0 and A1 cycle sequentially from one channel to the next as long as CONTC is HIGH. Then channel that is being acquired or converted is output on these address lines. Data is valid for the previous channel. These channels are updated when $\overline{BUSY}$ rises.
1	0	1	Enables AIN_2. A0 and A1 are configured as output pins. A0 and A1 cycle sequentially from one channel to the next as long as CONTC is HIGH. The channel that is being acquired or converted is output on these address lines. Data is valid for the previous channel. These channels are updated when $\overline{BUSY}$ rises.
1	1	1	Enables AIN_3. A0 and A1 are configured as output pins. A0 and A1 cycle sequentially from one channel to the next as long as CONTC is HIGH. The channel that is being acquired or converted is output on these address lines. Data is valid for the previous channel. These channels are updated when $\overline{BUSY}$ rises.

TABLE I. Channel Selection Truth Table for Addresses A0 and A1.

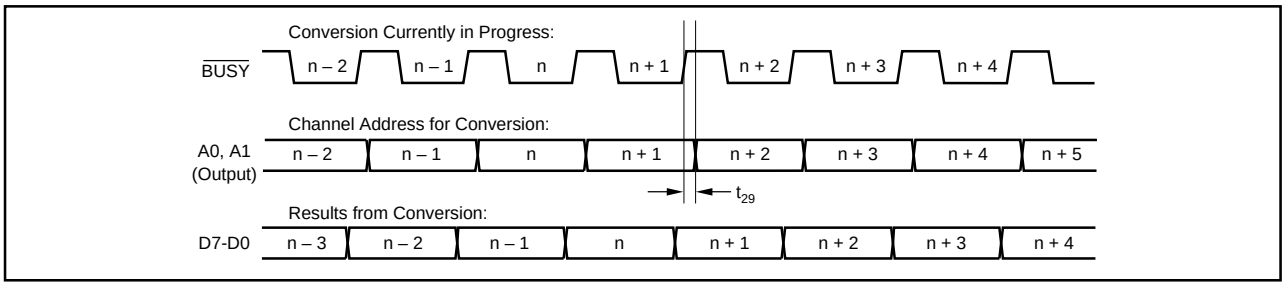

FIGURE 1. Channel Selection Timing for Continuous Serial Communication (t_{29} = 20ns (max))

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$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	PWRD	OPERATION
X	X	↑	0	The end of conversion 'n' (when $\overline{BUSY}$ rises) increments the internal channel latches and outputs the channel address for conversion 'n + 1' on A0 and A1.
X	X	0	0	Conversion in process.
0	↓	1	0	Restarts continuous conversion process on next input channel.
↓	0	1	0	Restarts continuous conversion process on next input channel.
X	X	X	1	All analog functions powered down. Conversion in process or initiated will yield meaningless data. Resets selected input channel for next conversion to AIN_0.
0	0	X	0	Places the converter in the serial out, continuous mode (PAR/$\overline{SER}$ = low)

TABLE II. Truth Table for the Continuous Mode when the A/D Converter is in the Serial Output Mode (PAR/$\overline{SER}$ = LOW). A0 and A1 become outputs in this mode. To remain in the continuous mode without interruption, CONTC = HIGH, $\overline{CS}$ and R/$\overline{C}$ = LOW.

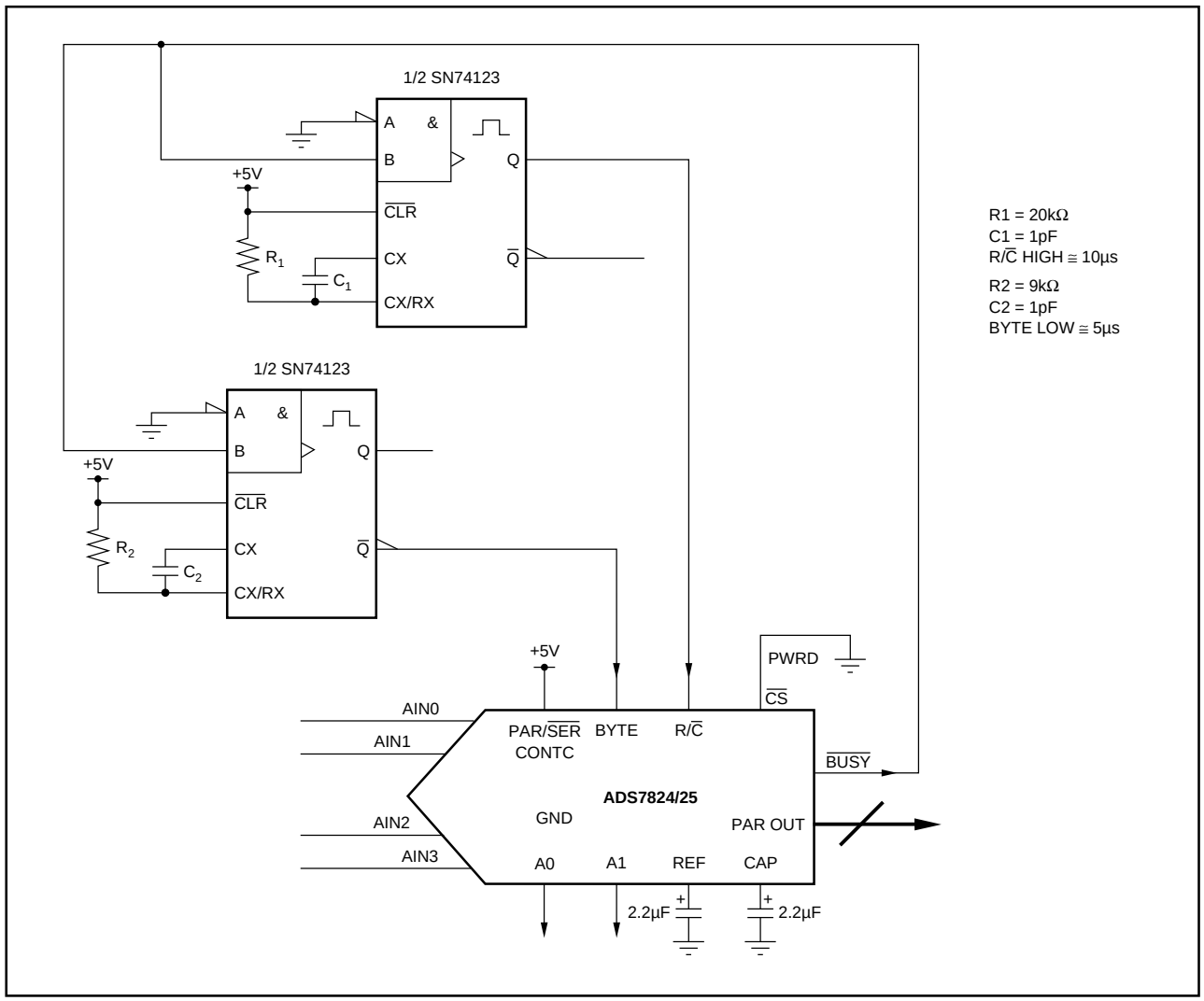


FIGURE 2. This Circuit can be Used to Place the ADS7824 or ADS7825 in the Continuous Mode if the Application Requires that these Devices be Configured for a Parallel Output.

In the parallel mode (PAR/$\overline{SER}$ = HIGH), the continuous mode (enabled with CONTC = HIGH) will cause the device to acquire and converter the input signal and cycle through all four channels continually as long as $\overline{CS}$ and PWRD are LOW (see Table III). In contrast to the serial mode, the parallel output pins are in a high impedance setting unless R/$\overline{C}$ is brought HIGH. Note that if R/$\overline{C}$ is kept HIGH, the converter will not be in the continuous mode. Additionally, the BYTE pin controls the output byte. The BYTE pin must be toggled while $\overline{BUSY}$ is HIGH if the total of 12 bits in the case of the ADS7824 and 16 bits in the case of the ADS7825 is required. Consequently, the continuous, parallel mode for these devices require some additional logic to toggle the R/$\overline{C}$ and BYTE pin.

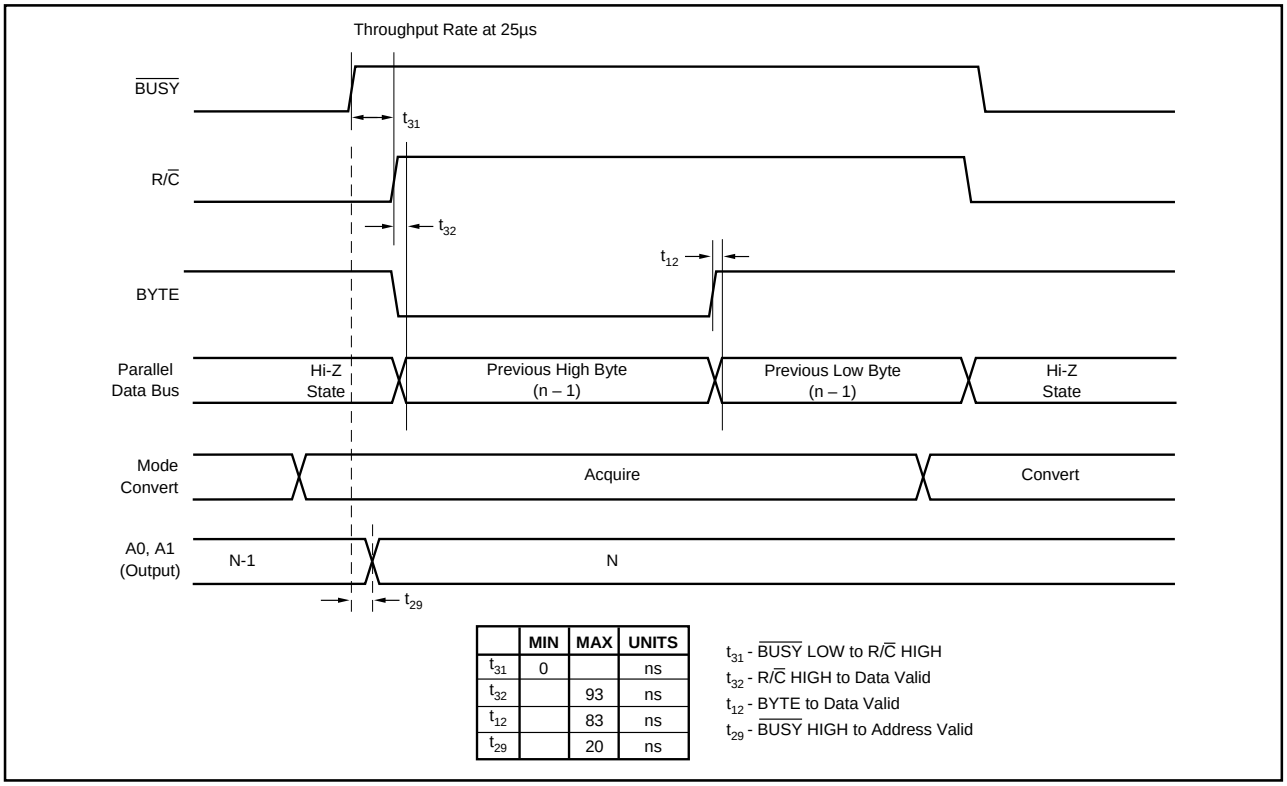
Figure 2 shows a circuit that can implement the continuous mode while these devices are in the parallel mode without

processor intervention. In this circuit, the ADS7824 (or ADS7825) is configured to operate in the continuous mode with CONTC HIGH, PAR/$\overline{SER}$ HIGH, and $\overline{CS}$ LOW. On the rising edge of $\overline{BUSY}$, R/$\overline{C}$ is triggered high through a one shot, SN74123. This one shot stays high as dictated by the values of the resistor and capacitor, R1 and C1 and then falls. In this manner, the parallel outputs of the ADS7824/25 are taken out of their high impedance mode and the data from the previous conversion is available on the output pins. In order to access both the HIGH Byte and LOW Byte of the converted data, the other half of the dual, SN74123 is used to toggle the BYTE pin of the converter. Refer to Figure 3 for the timing details of this circuit.

As is with the serial continuous mode, the input channel selection is done with either the PWRD function or the CONTC pin. If PWRD is cycled, the first channel that will be acquired will be channel 0, AIN_0. If CONTC is cycled, the register does not change and the current channel becomes the first in the sequence. When CONTC is high, A0 and A1 address inputs become outputs. When $\overline{BUSY}$ rises at the end of a conversion, A0 and A1 will output the address of the channel that will be converted next. Data will be valid for the previous channel after $\overline{BUSY}$ rises. The address lines are updated when $\overline{BUSY}$ rises. See Table III and Figure 3 for channel selection timing in the continuous, parallel conversion mode.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	BYTE	PWRD	OPERATION
0	0	↑	X	0	The end of conversion 'n' (when $\overline{BUSY}$ rises) increments the internal channel latches and outputs the channel address for conversion 'n + 1' on A0 and A1.
0	0	0	X	0	Conversion in process.
0	↓	1	X	0	Restarts continuous conversion process on next input channel.
0	1	1	1	0	Disables Hi-Z mode at the parallel outputs and puts the MSB byte on the output pins.
0	1	1	0	0	Disables Hi-Z mode at the parallel outputs and puts the LSB byte on the output pins.
X	X	X	X	1	All analog functions powered down. Conversion in process or initiated will yield meaningless data. Resets selected input channel for next conversion to AIN_0.

TABLE III. Truth Table for the Continuous Mode when the A/D Converter is in the Parallel Output Mode (PAR/$\overline{SER}$ = HIGH, CONT = HIGH, $\overline{CS}$ = LOW). A0 and A1 become outputs in this mode.



	MIN	MAX	UNITS
t_{31}	0		ns
t_{32}		93	ns
t_{12}		83	ns
t_{29}		20	ns

t_{31} - $\overline{BUSY}$ LOW to R/$\overline{C}$ HIGH
t_{32} - R/$\overline{C}$ HIGH to Data Valid
t_{12} - BYTE to Data Valid
t_{29} - $\overline{BUSY}$ HIGH to Address Valid

FIGURE 3. Timing Diagram for Circuit Shown in Figure 2. In this diagram the byte control is arbitrary and the low byte can be acquired before the high byte without any consequences on operation.

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