DLP5530S-Q1 Chipset Functional Safety Manual

User's Guide

Literature Number: DLPU094
July 2020

Contents

1 Introduction 4
2 Common Terms and Abbreviations 4
3 DLP5530S-Q1 Chipset Functional Safety Capability 5
4 Development Process for Management of Systematic Faults 6
4.1 TI New-Product Development Process 6
5 DLP5530S-Q1 Chipset Overview 6
5.1 Target Applications 7
5.2 DLP5530S-Q1 Chipset Functional Safety Concept 7
5.3 Functional Safety Constraints and Assumptions 9
6 Description of Device Blocks 9
7 DLP5530S-Q1 Management of Random Faults 11
7.1 Fault Reporting 11
7.2 Fault Handling 11
7.3 Description of Functional Safety Mechanisms 11
8 Recommendations for chipset integration and evaluation in a functional safety system 24
Appendix A Summary of Recommended Functional Safety Mechanism Usage 26

List of Figures

1 TI New-Product Development Process 6
2 DLP5530S-Q1 Block Diagram 7
3 DLP5530S-Q1 Video Path With Diagnostics 8
4 Illumination Control Architecture With Diagnostics 9
5 DLP5530S-Q1 Video Path with Diagnostics 12
6 DLP5530S-Q1 Video Path 13
7 Video Input BISTs 14
8 Video Processing BIST 15
9 Video Output BISTs 16
10 Illumination Control Architecture 18
11 LED Driver Architecture 18
12 Software and settings origin and destination 19
13 Illumination Control Architecture with Diagnostics 20

List of Tables

1 DLPC230S-Q1 Blocks 9
2 TPS99000S-Q1 Blocks 10
3 DLP5530S-Q1 Blocks 10
4 Recommended methods for testing BISTs 24
5 Legend of Functional Safety Mechanisms 26
6 Summary of Functional Safety Mechanisms 27

DLP5530S-Q1 Chipset Functional Safety Manual

1 Introduction

This document is a functional safety manual for the Texas Instruments DLP5530S-Q1 chipset. The chipset consists of three devices: DLP5530S-Q1 Digital Micromirror Device (DMD), the DLPC230S-Q1 controller for the DMD, and the TPS99000S-Q1 illumination controller. The specific orderable part numbers supported by this functional safety manual are as follows:

- DLP5530SAFYSQ1
- DLPC230STZDQQ1
- DLPC230STZDQRQ1
- TPS990STPZPQ1
- TPS990STPZPRQ1

This functional safety manual provides information needed by system developers to help in the creation of a functional safety system using the DLP5530S-Q1 chipset. This document includes:

- An overview of the chipset architecture
- An overview of the development process used to decrease the probability of systematic failures
- An overview of the functional safety architecture for management of random failures
- The details of architecture partitions and recommended functional safety mechanisms

The following information is documented in the **Functional Safety Analysis Report** and is not repeated in this document:

- Summary of failure rates (FIT) of the component
- Summary of functional safety metrics of the hardware component for targeted standards (for example IEC 61508, ISO 26262, and so forth
- Quantitative functional safety analysis (also known as FMEDA, Failure Modes, Effects, and Diagnostics Analysis) with detail of the different parts of the chipset, allowing for customized application of functional safety mechanisms. For the DLP5530S-Q1 chipset, TI will provide four total FMEDAs. One FMEDA for each component of the chipset, and one for the chipset.
- Assumptions used in the calculation of functional safety metrics

The user of this document should have a general familiarity with the DLP5530S-Q1 chipset. For more information, refer to the chipset data sheets (DLPC230S-Q1, TPS99000S-Q1, DLP5530S-Q1) and the DLPC230-Q1 Programmer's Guide for Display Applications. This document is intended to be used in conjunction with the pertinent data sheets, technical reference manuals, and other component documentation.

For information that is beyond the scope of the listed deliverables, contact your TI sales representative or go to http://www.ti.com.

2 Common Terms and Abbreviations

- **DMD:** Digital Micromirror Device
- **BIST:**Built In Self Test. A diagnostic feature of the chipset to check for errors in operation

3 DLP5530S-Q1 Chipset Functional Safety Capability

This section summarizes the chipset's functional safety capability.

This chipset:

- Is a quality managed (QM) device according to ISO 26262
- FIT rates and failure mode distributions are provided as part of the Functional Safety Analysis Report for customers to calculate random fault integrity metrics
- TI recommends that this component is integrated into the system through the strategy of "evaluation of hardware element" (ISO 26262-8:2018 clause 13)

NOTE: This component is still undergoing development and its functional safety assessment is not yet complete.

4 Development Process for Management of Systematic Faults

For functional safety development, it is necessary to manage both systematic and random faults. Texas Instruments follows a new-product development process for all of its components which helps to decrease the probability of systematic failures. This new-product development process is described in Section 4.1 .

4.1 TI New-Product Development Process

Texas Instruments has been developing components for automotive and industrial markets since 1996. Automotive markets have strong requirements regarding quality management and product reliability. The TI new-product development process features many elements necessary to manage systematic faults. Additionally, the documentation and reports for these components can be used to assist with compliance to a wide range of standards for customer's end applications including automotive and industrial systems (e.g ISO 26262-4, IEC 61508-2).

This component was developed using TI's new product development process which has been certified as compliant to ISO 9001 / IATF 16949 as assessed by Bureau Veritas (BV).

The standard development process breaks development into phases:

- Assess
- Plan
- Create
- Validate

Figure 1 shows the standard process.

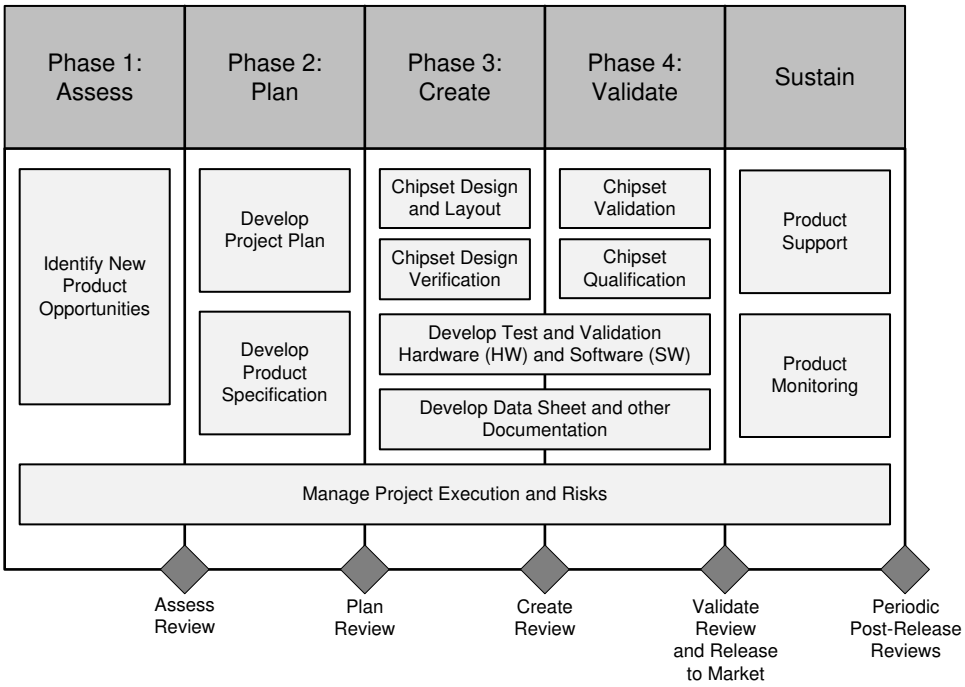

Figure 1. TI New-Product Development Process

5 DLP5530S-Q1 Chipset Overview

The DLP5530S-Q1 chipset consisting of the DLP5530S-Q1 automotive Digital Micromirror Device (DMD), DLPC230S-Q1 DMD controller, and TPS99000S-Q1 system management and illumination controller, provides the capability to achieve a high performance augmented reality Head-Up Display or a windshield cluster display. Figure 2 shows a block diagram for a Head-Up Display or Windshield Cluster using the DLP5530S-Q1 chipset.

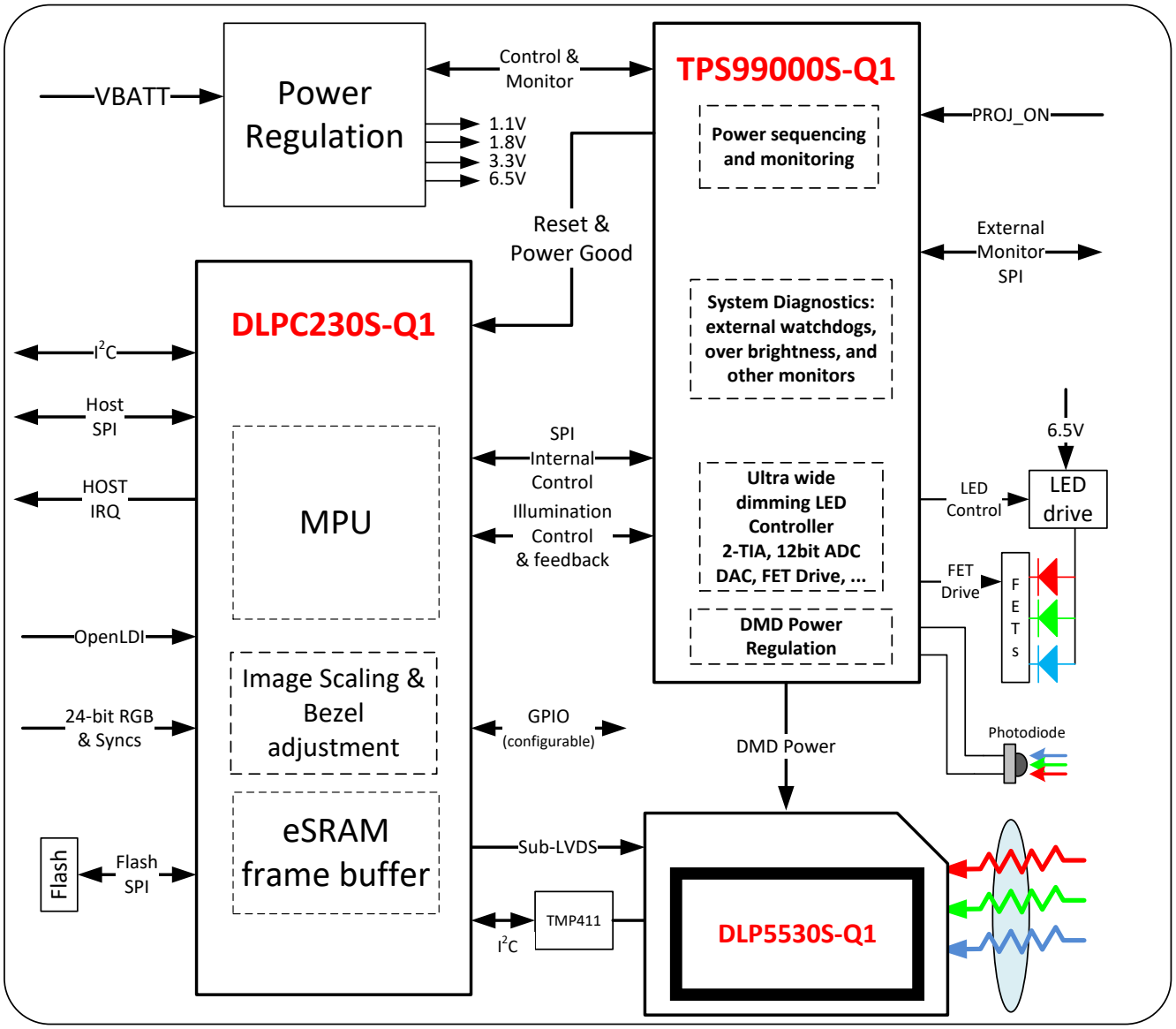

Figure 2. DLP5530S-Q1 Block Diagram

5.1 Target Applications

The DLP5530S-Q1 chipset is targeted for the following applications:

- Automotive Head-Up Display
- Automotive windshield cluster

5.2 DLP5530S-Q1 Chipset Functional Safety Concept

Typical applications for the DLP5530S-Q1 chipset include a HUD and Windshield Cluster. This section discusses some typical hazards in these applications and how this chipset can help minimize the risk of these hazards.

For risk minimization, this chipset includes many Built-In Self Tests (BISTs). These are monitoring and diagnostic functions that are implemented in the chipset to detect and act upon failure conditions. A general overview of BISTs with regards to typical hazards is provided below. For full implementation details, please refer to the DLPC230S-Q1 Programmer's Guide for Display Applications.

5.2.1 Typical Hazards

Well-known hazards in a HUD and Windshield Cluster include:

- Corruption of image content such that it prevents the driver from seeing obstacles or traffic on the road ahead
- Excessively bright LEDs that results in a very bright image that glares the driver

Note: The list of hazards above may not be exhaustive. The OEM and system integrator should consider any other risks involved.

5.2.2 Chipset Architecture

The architecture of the DLP5530S-Q1 helps minimize risk of hazards through independent monitoring and distributed responsibility. For example, the TPS99000S-Q1 independently monitors the DLPC230S-Q1 via watchdogs. Many Built-In Self Tests (BISTs) of the chipset also distribute the responsibility amongst the devices. For example, the TPS99000S-Q1 is responsible for taking ADC measurements, however, the DLPC230S-Q1 has the software to analyze the measurements and detect error conditions.

The architecture of this chipset makes it more robust against random faults.

5.2.3 Built-In Self Tests

The DLP5530S-Q1 chipset includes a wide variety of Built-In Self Tests (BISTs). These BISTs, are the mechanisms used to monitor and diagnose the chipset, and protect against the hazards described in Section 5.2.1. Figure 3 and Figure 4 give a brief overview of the BISTs in the DLP5530S-Q1 chipset for protecting against functional safety related faults. These BISTs are described in more detail in Section 7.3.

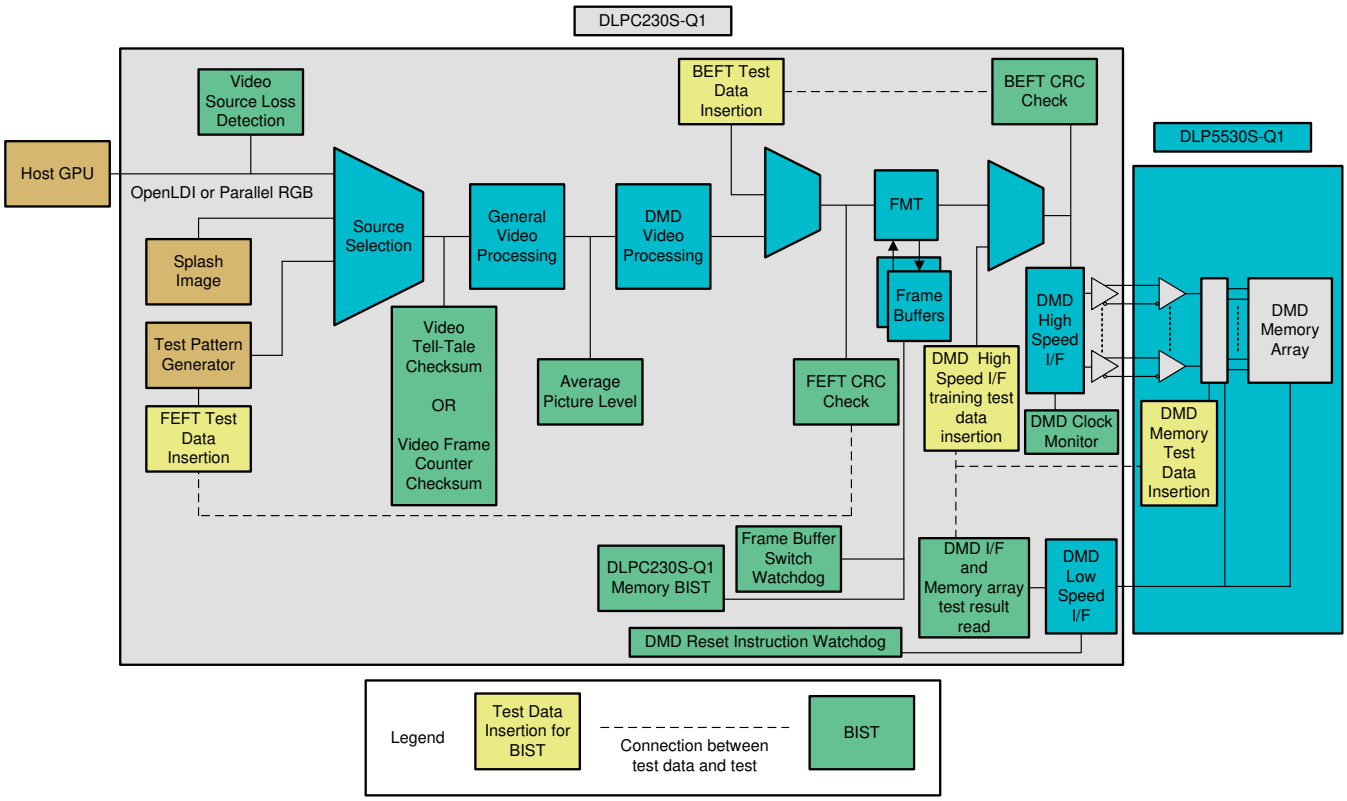

Figure 3. DLP5530S-Q1 Video Path With Diagnostics

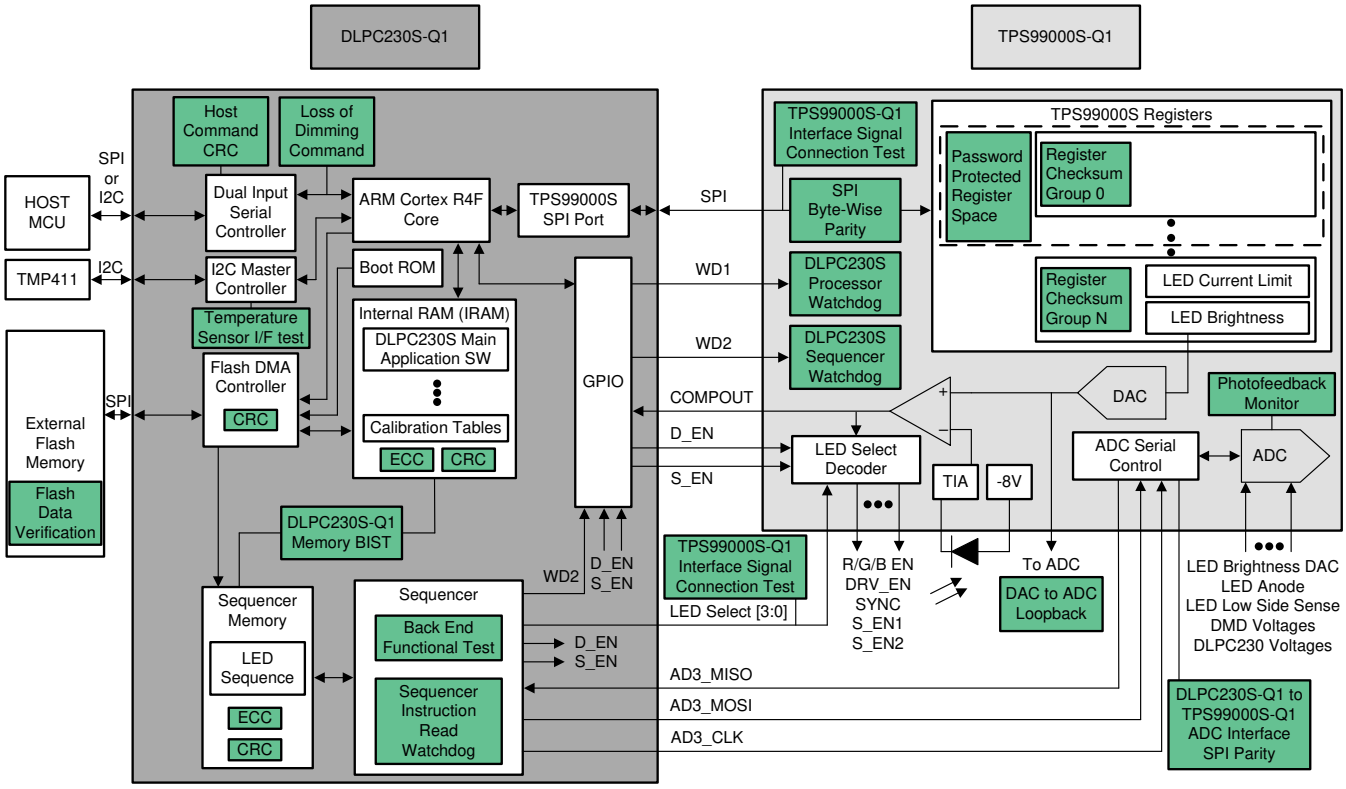

Figure 4. Illumination Control Architecture With Diagnostics

5.3 *Functional Safety Constraints and Assumptions*

In creating a functional safety concept and doing the functional safety analysis, TI generates a series of assumptions on system level design, and requirements. These assumptions (sometimes called Assumptions of Use) are listed below. Additional assumptions about the detailed implementation of safety mechanisms are separately located in Section 7.3.

The DLP5530S-Q1 Functional Safety Analysis was done under the following system assumptions:

- **[SA_1]** The system integrator shall follow all requirements in the latest component data sheets
- **[SA_2]** The system integrator shall enable all BISTs

During integration activities these assumptions of use and integration guidelines described for this component shall be considered. Use caution if one of the above functional safety assumptions on this component cannot be met, as some identified gaps may be unresolvable at the system level.

6 Description of Device Blocks

This section provides a brief overview of the various blocks of the three chipset components. The quantitative functional safety analysis is done according to these partitions. Partitions for each device are given in Table 1

Table 1. DLPC230S-Q1 Blocks

Block Name	Block Function
VGP	Video and Graphics Processor. Receives input video data and generates splash images or test patterns. Performs video processing functions such as scaling and color space conversion.
RTP	Real-Time Processor. ARM micro-processor core and related memories

Table 1. DLPC230S-Q1 Blocks (continued)

Block Name	Block Function
RSC	Real-Time System Control. Timing control for LEDs, DMD mirror transitions, and ADC measurements. Includes hardware processing blocks and associated memories.
FMT	Formatter and Universal Memory Controller. Converts data output from the VGP into single color images that are displayed on the DMD. Includes the SRAM frame buffers. Data is received from the VGP, processed, and stored into the frame buffer. Data is output from the frame buffer to the DMD based on instructions from the RSC.
SSF	Clock generation for various clock domains in the DLPC230S-Q1
DDI	DMD data interface. High speed interface for outputting data from DLPC230S-Q1 to DMD
FPD	OpenLDI input video port
RTP BROM	Boot ROM that initiates loading of software from external flash to internal RAM and performs boot tests

Table 2. TPS99000S-Q1 Blocks

Block Name	Block Function
AAC	ADC control including the TPS99000S-Q1 to DLPC230S-Q1 AD3 interface
CSR	Configuration status registers
DEG	Deglitching for signals
DTV	Data transfer validation. DLPC230S-Q1 to TPS99000S-Q1 SPI port and related functions.
ILM	Illumination control
PSC	Power state controller
SSF	Secondary SPI port for diagnostics
ROM	ROM used for storing device trim data

Table 3. DLP5530S-Q1 Blocks

Block Name	Block Function
SRAM	SRAM cells under micro-mirror layer. Data loaded into SRAM determines state of each mirror.
IO	High speed interface that receives the video data from the DLPC230S-Q1
SCTRL	Instruction decoder for data received over IO
Reset Ctrl	Mirror transition control
LSIF	Low speed interface for DMD configuration and mirror reset voltage control

7 DLP5530S-Q1 Management of Random Faults

For a functional safety critical development it is necessary to manage both systematic and random faults. The DLP5530S-Q1 chipset architecture includes many functional safety mechanisms, which can detect and respond to random faults when used correctly. This section of the document describes the architectural functional safety concept for the DLP5530S-Q1 chipset. The system integrator shall review the recommended functional safety mechanisms in the functional safety analysis report and the Failure Mode, Effects, and Diagnostics Analysis (FMEDA) in addition to this safety manual to determine the appropriate functional safety mechanisms to include in their system. The DLPC230S-Q1 Programmer's Guide for Display Applications is a useful document for finding more specific information about the implementation of these features.

7.1 Fault Reporting

The DLP5530S-Q1 has two major mechanisms for fault reporting—Error History and HOST_IRQ

7.1.1 Error History

The DLPC230S-Q1 stores an error history to indicate which errors have occurred in the system. The error history can be read by the host MCU via SPI or I2C. Full implementation details of the Error History, including error codes are described in the DLPC230S-Q1 Programmer's Guide For Display Applications.

7.1.2 HOST_IRQ

For more urgent error conditions, the DLPC230S-Q1 has the HOST_IRQ signal that can be used for interrupt driven programming of the host MCU. The DLPC230S-Q1 asserts this signal high to indicate to the host MCU that a serious system error has occurred. A serious system error is something that TI considers likely to corrupt the display image, and/or create a bright display image, and/or damage one or more chipset devices. This signal can be used to interrupt the host MCU to handle the urgent error.

7.2 Fault Handling

The DLPC230S-Q1 software implements two ways of error handling—error logging and emergency shutdown. All errors detected by the system are logged in the error history. However, for more critical errors, i.e. errors that will obviously lead to a bright image, corrupted image, or damaged devices, the DLPC230S-Q1 executes an emergency shutdown.

In emergency shutdown, DLPC230S-Q1 main application software performs the following actions:

- Disables LEDs
- Parks and powers down DMD
- Transitions software to Standby Mode
- Captures errors in error history
- Sets emergency shutdown bit in status
- Asserts HOST_IRQ

Full implementation details of emergency shutdown can be found in the DLPC230-Q1 Programmer's Guide For Display Applications.

7.3 Description of Functional Safety Mechanisms

The DLP5530S-Q1 chipset implements a many monitoring and diagnostics features. This section describes how these can be used to reduce the risk of two particular hazards encountered in a HUD or Windshield Cluster.

This document is not intended to provide implementation and configuration details of each mechanism. For such details, please see the DLPC230-Q1 Programmer's Guide for Display Applications.

This document focuses on the BISTs related to the hazards described in Section 5.2.1. However, the chipset contains additional BISTs. For an exhaustive list, please see the DLPC230S-Q1 Programmer's Guide for Display Applications.

7.3.1 Video path protection

In order to prevent against corrupted image, the DLP5530S-Q1 chipset includes many Built-In Self Tests (BISTs) that monitor the video path. The BISTs implemented in the chipset monitor and diagnose the input, the processing, and output of the video. An overview of the entire video path with the BISTs is shown in Figure 5 below. Further description of the video path and the BISTs is provided in the following sections.

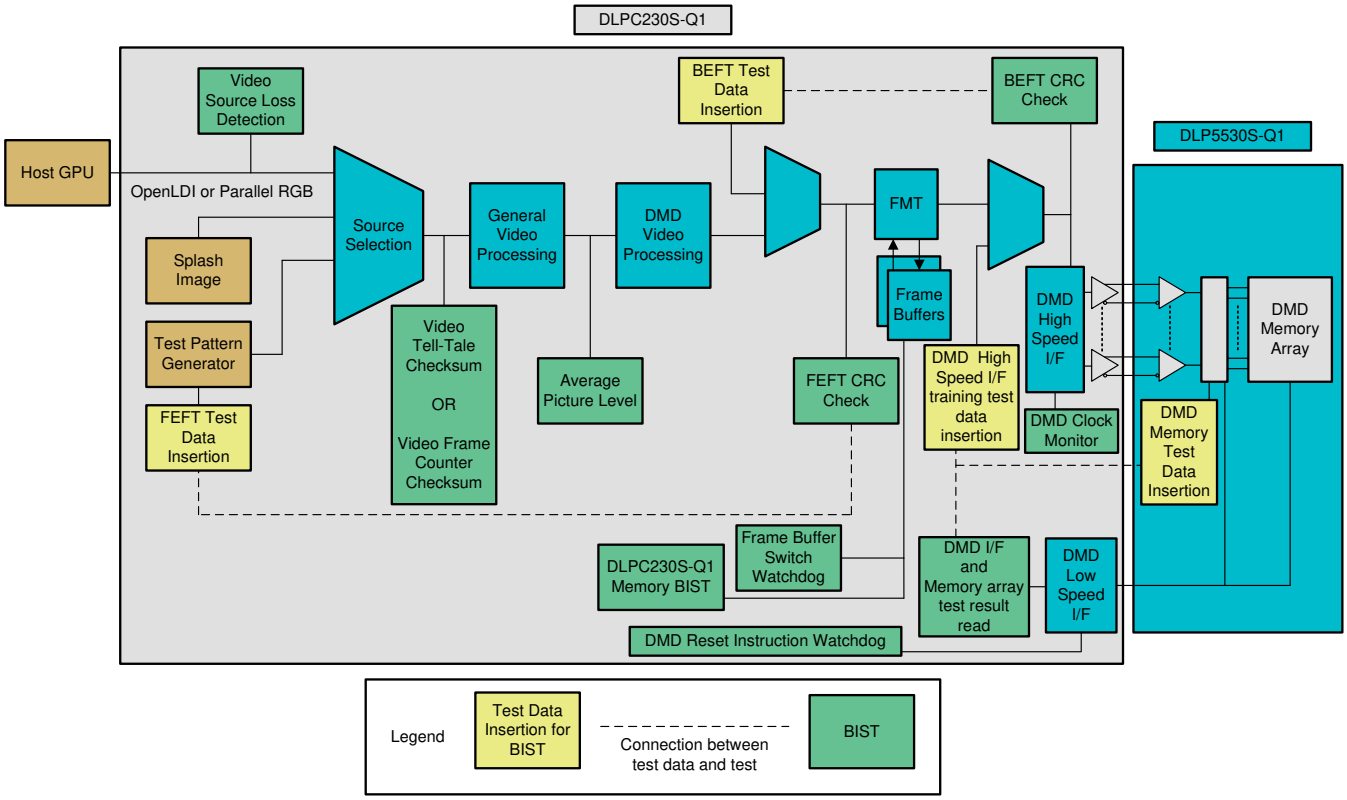

Figure 5. DLP5530S-Q1 Video Path with Diagnostics

7.3.1.1 Video Path

Figure 6 shows the video path of the DLP5530S-Q1.

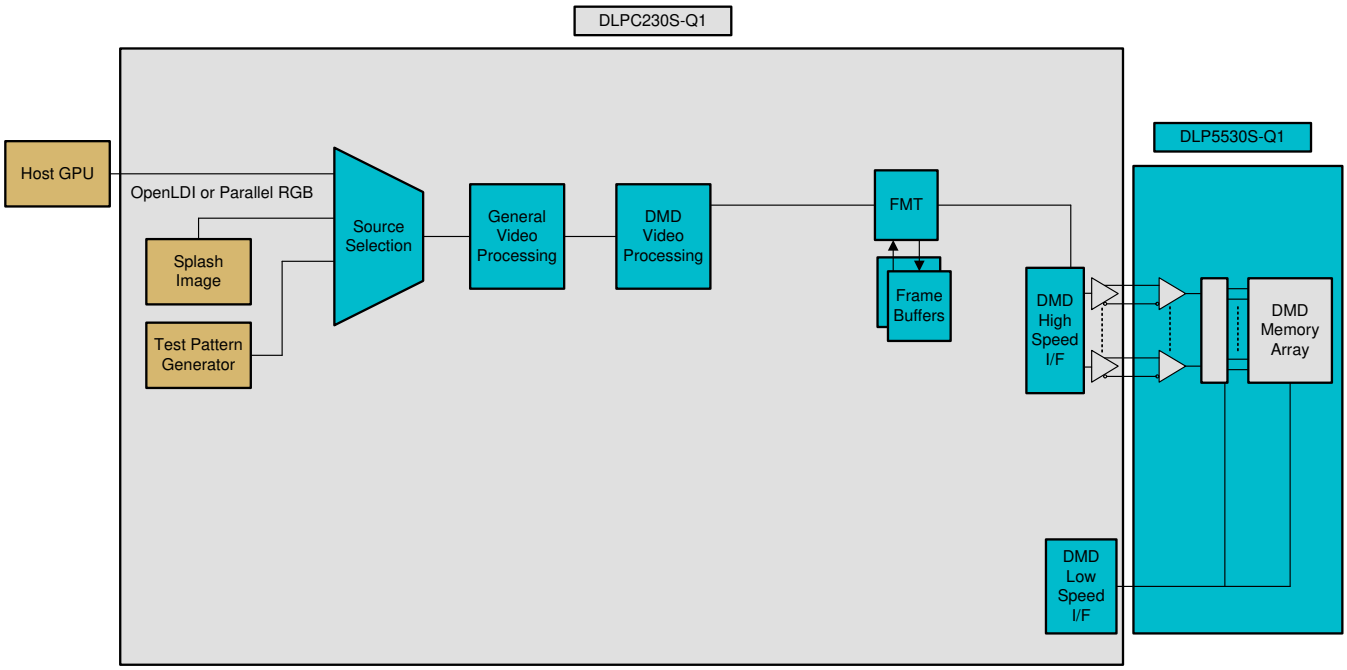

Figure 6. DLP5530S-Q1 Video Path

The DLPC230S-Q1 can use several display sources. Source video can come from a vehicle's GPU, either using OpenLDI or Parallel RGB, Internal Test Patterns, or Splash Images. The video source is selected by a host MCU.

After the input multiplexer, some general video processing is applied to the video. This processing includes scaling, and color space correction (for some splash images). Next, some DMD specific video processing is applied. This includes de-gamma correction, dithering, and finally, a conversion to single color "bit plane" data.

"Bit Planes" are sub-frames corresponding to single color codes. The DMD displays single color sub-frames and the human eye integrates them to form a full color image for that frame of the video. After conversion from standard video to bit planes the video is sent to the FMT block.

The FMT consists of some video processing logic and is connected to two frame buffers. The processing in the FMT and the use of the frame buffers is explained below:

- Performs flips, crops, and bezel adjustment of the video. This video is stored into one of the two frame buffers.
- Simultaneously, video from the other frame buffer is output to the DMD.
- The two frame buffers switch roles every frame.

The DMD High Speed Interface is used to load time multiplexed binary data into the DMD's Memory Array. This binary data determines the state of each DMD mirror during each "bit plane". A reset pulse transitions micro-mirrors from one "bit plane" to the next. The DLPC230S-Q1 utilizes a low speed interface that is used for configuration of DMD registers, generating the DMD mirror reset waveforms, and monitoring the DMD.

The DLP5530S-Q1 chipset contains overlapping BIST coverage of the various blocks involved in the video path. These BISTs cover the input, processing, and output of the video path. These BISTs are discussed in the following sections.

7.3.1.2 Video Input BISTs

Figure 7 gives an overview of BISTs used to monitor the video input.

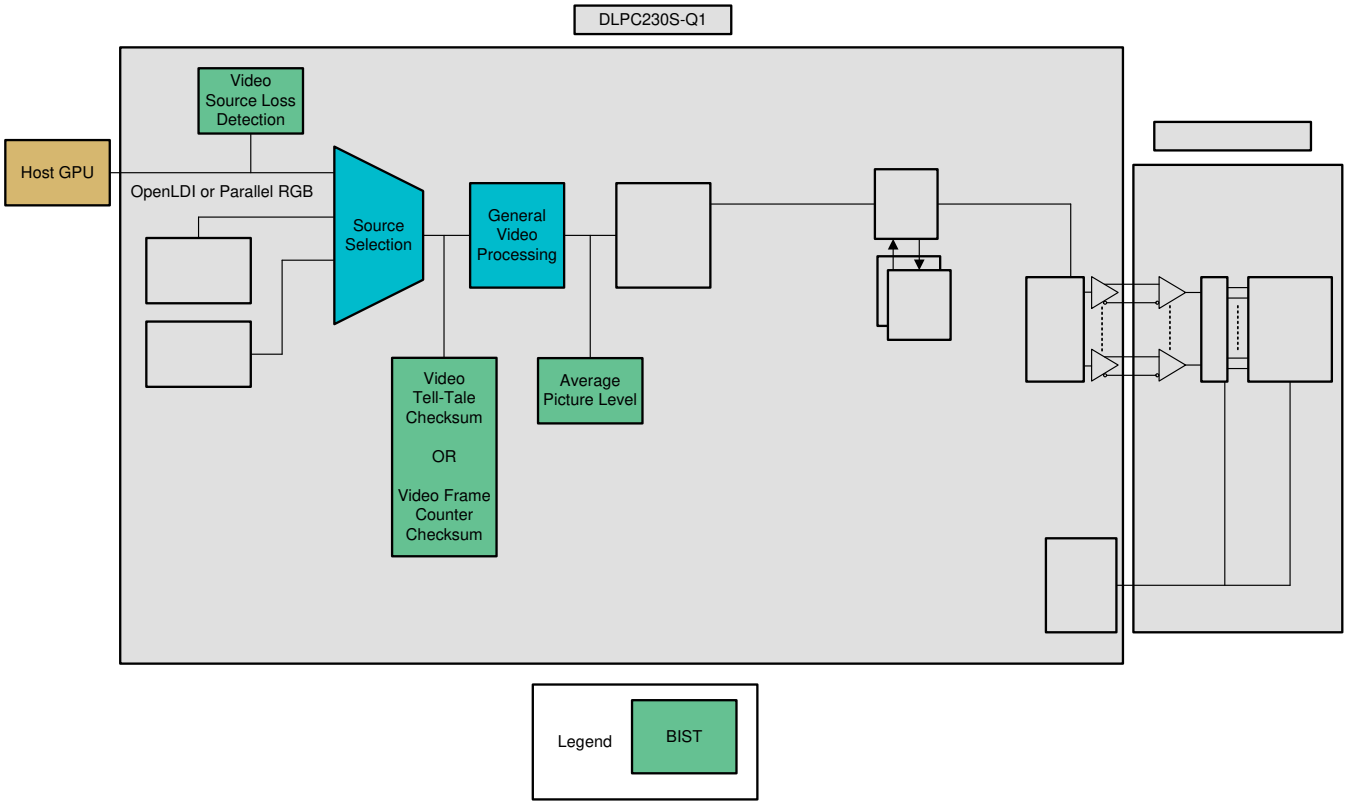

Figure 7. Video Input BISTs

- **[SM_1] Video Source Loss Detection:** Checks if the source of video to the DLPC230S-Q1 has disconnected. It checks the video parameters to make sure they are within acceptable ranges. These parameters are the pixel clock frequency, the VSYNC frequency, the number of active lines per frame, and number of active pixels per line. If the video source is invalid at the initial transition to display mode, no image will be displayed. The system will stay in standby mode. If the source becomes invalid after Display Mode operation, the system will transition to an alternate display image specified in the configuration options—either a test pattern or splash image. In some cases it is possible for the system to auto-recover after a source loss. Auto-recover and alternate source settings can be configured in flash.
- **[SM_2] Video Tell-Tale Checksum:** Checks the expected video from the host versus the video received by the DLPC230S-Q1. Host MCU provides a checksum for a region of the image, and the DLPC230S-Q1 calculates a checksum over the same region. If the two checksums don't match, the test fails. This checksum can be performed over any rectangular region of the video, including and up to the entire image. However, this test is designed to be used on static or slowly changing portions of the image. The test region of the checksum and the expected checksum can only be changed while the test is disabled. A minimum of two frames is required to disable the test, update the checksum region and/or value, and re-enable the test. The failure action is configurable in flash, but not during operation. Upon test failure, an error can be logged with no additional action, an error can be logged with a change to an alternate source, or an error can be logged and emergency shutdown can be executed. **This test cannot be used simultaneously with the Video Frame Counter Checksum.**
- **[SM_3] Video Frame Counter Checksum:** Checks the value of a counter embedded within the video data from the host. If the counter does not increment as expected, the test fails. A subsection of the image can be defined as the counter. The minimum and maximum expected value of this counter is also configurable. Once the counter reaches the maximum, it is expected to roll over and start from the minimum. The counter region can be as small as one pixel and as large as the entire image. HUD images typically have large amounts of unused area in the display area. It is recommended to embed the counter in one of these regions, such as a corner. If the area is sufficiently small, its pixel data can change without being noticeable by the viewer. The failure action is configurable in flash, but not during

operation. Upon test failure, an error can be logged with no additional action, an error can be logged with a change to an alternate source, or an error can be logged and emergency shutdown can be executed. **This test cannot be used simultaneously with the Video Tell-Tale Checksum**

- **[SM_4] Average Picture Level:** Checks the numerical average of the incoming pixel data. If the average level is higher than the host specified maximum, the test fails. The failure action is configurable during flash build, but not during operation. Upon test failure, only an error can be logged, or an error can be logged and emergency shutdown can be executed.

7.3.1.3 Video Processing BISTs

Figure 8 gives an overview of the BISTs used to monitor and diagnose the video processing blocks in the DLPC230S-Q1.

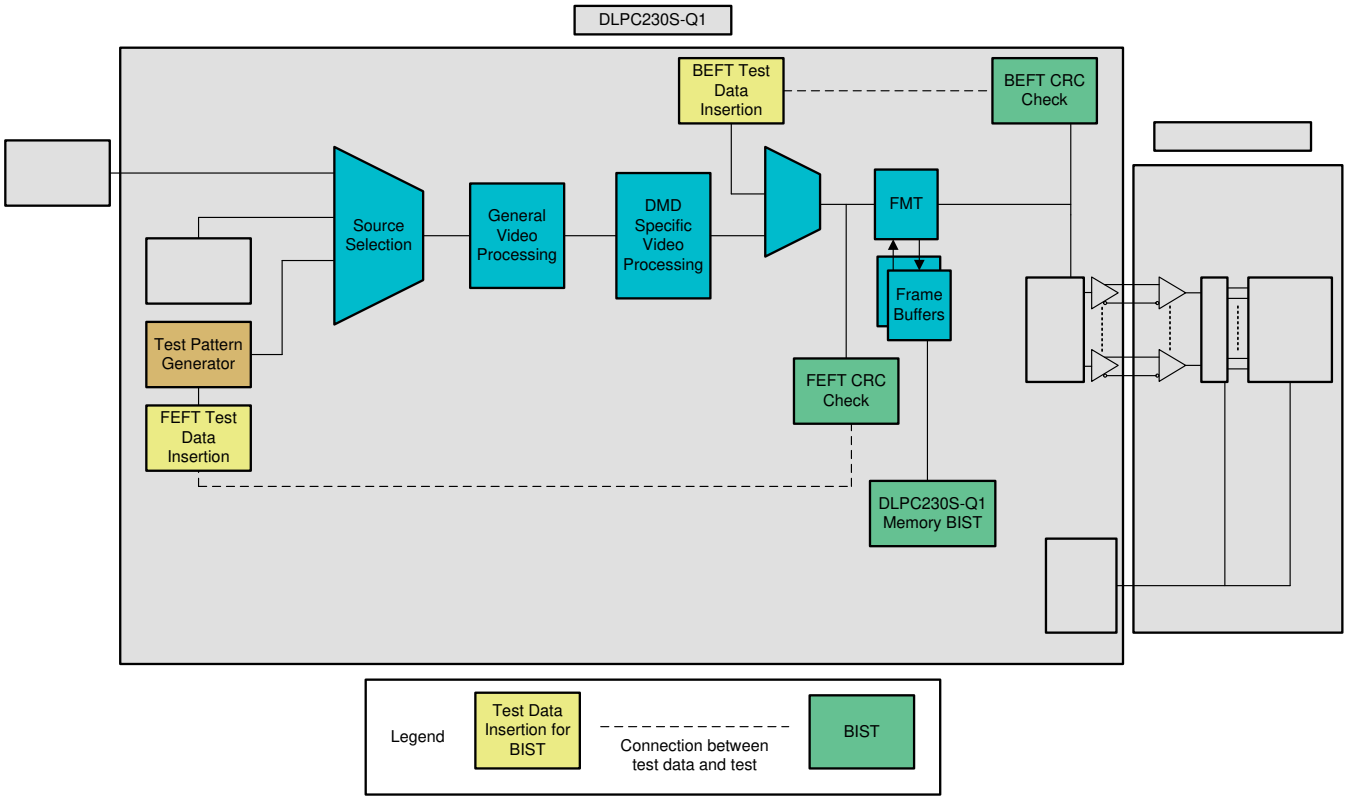

Figure 8. Video Processing BIST

- **[SM_5] Front-End Functional Test (FEFT):** Checks the video processing blocks in the DLPC230S-Q1 by inserting a test pattern data and performing a CRC check on the output of processing blocks. The test pattern is a 1920x608 horizontal ramp pattern with an overlaid random noise pattern. The size of the image is chosen in order to provide full coverage of the memory control. Two frames of ~120Hz data are tested. This provides a high source pixel clock frequency, in order to stress internal logic. A subset of the image is used for a CRC check. If the CRC after processing does not match the expected CRC, the test fails. This test can be configured to run at start-up, and it can be executed by command after the software is changed to Stand-by mode via host command. In case of test failure, software will not transition Display Mode even if it is commanded by the host. An error will also be logged.
- **[SM_6] Back-End Functional Test (BEFT):** Checks the DLPC230S-Q1 blocks responsible for outputting data from the frame buffers to the DMD driver. This checks functionality such as image flips, smooth image transition functions, and frame buffer swaps. Additionally, functionality related to the synchronization of the video with LEDs is tested. This will be discussed in more detail in Section 7.3.2. This test checks a 160x60 image with four configurations—no flip, East/West flip only, North/South flip only, and East/West plus North/South flip. The image size is small in order to increase test speed. The goal of this test is not to provide full coverage of the frame buffers, because that coverage is already

provided by other tests. A CRC check is performed on the image after formatting. If the resulting CRC does not match the expected value, the test fails. This test can be configured to run at start-up, and it can be executed by command after the software is changed to Stand-by mode via host command. In case of test failure, software will not transition to Display Mode even if it is commanded by the host. An error will also be logged.

- **[SM_7] DLPC230S-Q1 Memory BIST:** Checks functionality of internal memories such as the frame buffers, internal RAM, and sequence look up tables using a series of writes, delays, and reads. The frame buffer memory check is critical for diagnosing a corrupt video path. The SRAM frame buffers are tested using a series of instructions provided by the manufacturer of the SRAM cell. The instructions for executing the test are stored in external flash, but the test data is generated locally in the frame buffer. If the data read from the memory does not match the data written to the memory the test fails. This test can be configured to run at start-up, and it can be executed by command after the software is changed to Stand-by mode via host command. In case of test failure, software will not transition to Display Mode even if it is commanded by the host. An error will also be logged.

7.3.1.4 Video Output BISTs

Figure 9gives an overview of the BISTs used to monitor and diagnose the video output blocks in the DLP5530S-Q1 chipset.

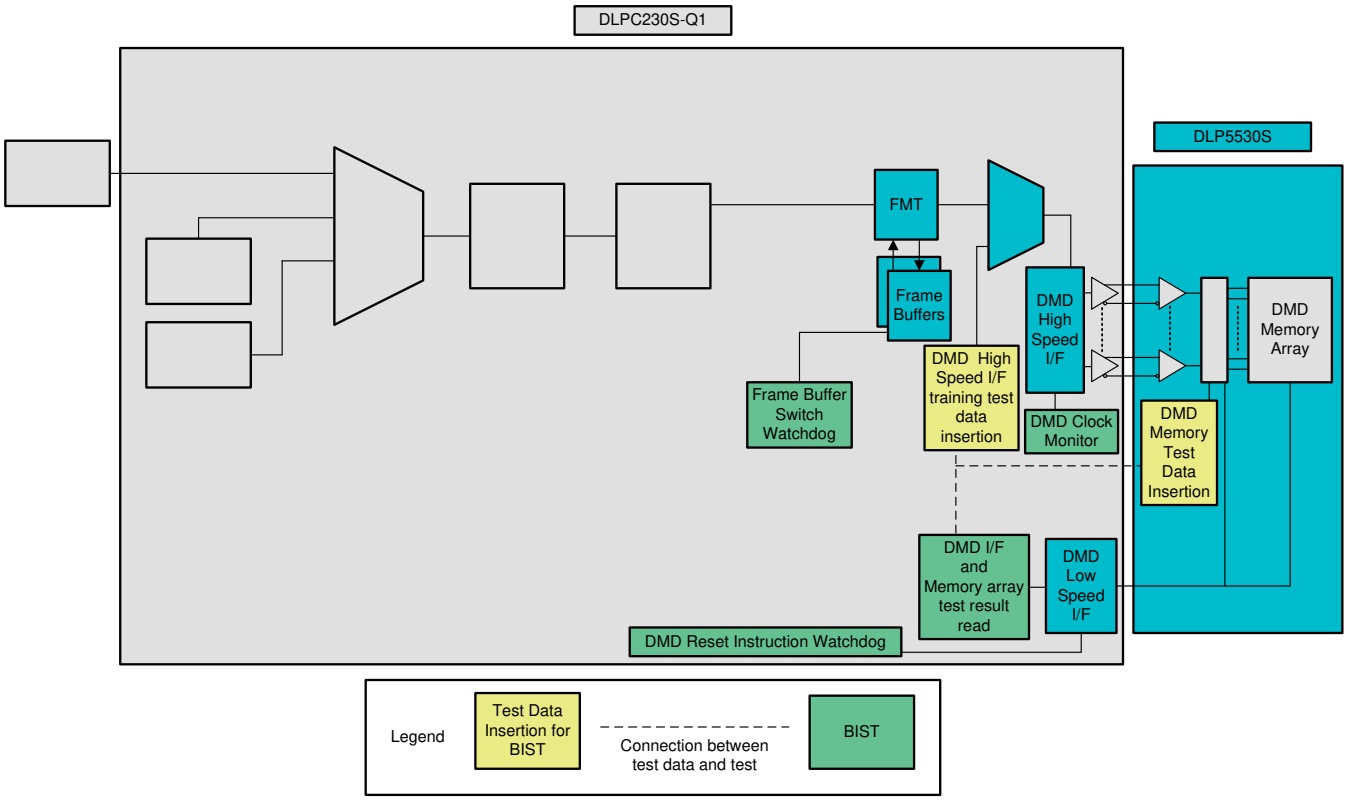

Figure 9. Video Output BISTs

- **[SM_8] Frame Buffer Swap Watchdog:** Checks that the frame buffers are switching roles each frame. Each frame, one buffer stores processed video, and the other buffer outputs data to the DMD. If the buffers don't switch each frame, the video will not update. The software of the DLPC230S-Q1 sets a timer for the buffer swap. When the buffer is successfully swapped, a signal from the frame buffer controller resets the timer. If the swap does not happen within the allocated time, the timer will expire. If the timer expires, the test fails. Upon failure, emergency shutdown will be executed and an error will be logged. This test is always active when an external video source or internal test pattern are being used. This test is not executed when a splash image is being displayed.
- **[SM_9] DMD High Speed Interface Training:** The DLPC230S-Q1 to DMD sub-LVDS interface can adjust the phase of each signal in order to optimize the position of the clock signal within the data eye.

This process compensates for variation in manufacturing, system temperature, and drive voltage. This process is called training. This training process can also detect faults in the DLPC230S-Q1 to DMD connection. The DMD low speed interface is used to configure the DMD for training and to read back the results of the training. This training is performed at start-up and continuously during display mode. A total of 8 frames is required to test all data pairs in the DLP5530S-Q1 chipset during display mode. If the test fails at start-up the system will stay in Stand-By mode, and an error will be logged. If failure happens during display mode, an error is logged. During display mode, failures may be transient. However, persistent errors can indicate a broken connection or another critical issue.

- **[SM_10] DMD Low Speed Interface Test:** Checks the DMD low speed interface by continuously writing a dedicated register and reading back the value. Reads and writes happen simultaneously with DMD High Speed Training Cycles. The DMD Low Speed Interface Test takes four total training cycles. A value is written in cycle 0, read back in cycle 1, the 1-s complement value is written in cycle 2, and another read is performed in cycle 3. This test is always executed during display mode. Upon failure, an error is logged.
- **[SM_11] DMD Memory Test:** Checks the DMD CMOS memory by writing data and confirming read back data. The DLPC230S-Q1 commands the DMD into a testing mode and the DMD writes known values into the memory cells below its pixels. The DMD then reads back the state of each memory cell and drives a signal to the DLPC230S-Q1 to indicate pass or fail for each column of the DMD memory. A column will be reported as a fail if one or more memory cells in that column reads an incorrect value. If a failure is detected in more than one column, the test fails. This test can be configured to run at start-up, and it can be executed by command after the software is changed to Stand-by mode via host command. In case of test failure, software will not transition Display Mode even if it is commanded by the host. An error will also be logged.
- **[SM_12] DMD Reset Instruction Watchdog:** Checks that the DMD has accepted command to update mirror positions. A reset command from the DLPC230S-Q1 tells the DMD to update mirror positions. If this command is not executed, mirrors will remain in their current position. Upon successfully receiving a reset command the DMD returns an acknowledge message. If this is not received by the DLPC230S-Q1 within an acceptable time, this test fails. Upon failure, emergency shutdown will be executed and an error will be logged. This test is always active when an image is being displayed.
- **[SM_13] DMD Clock Monitor:** The DLPC230S-Q1 clock generation block contains monitoring to ensure that the clock frequency of the DMD high speed interface is within the specified range.

7.3.2 Illumination Control Protection

The LEDs in the system should be properly controlled to prevent a bright image. In cases where proper control is not possible, the illumination should be turned off.

The DLP5530S-Q1 includes several features to monitoring the illumination control and turn off the LEDs in case of a fault.

7.3.2.1 Illumination Control Overview

Figure 10 and Figure 11 show the illumination control and LED driver architecture. Figure 12 shows the origin and destination of software, data, and settings.

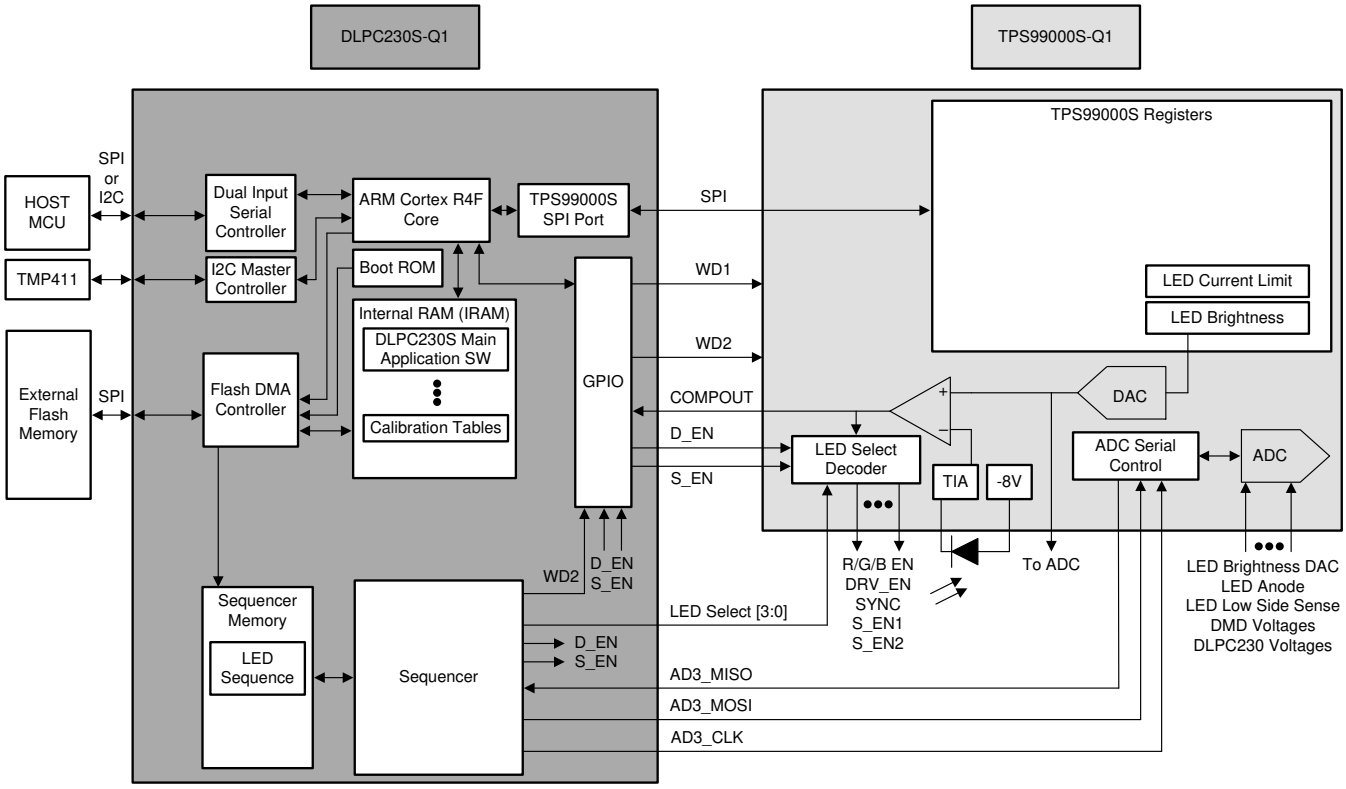

Figure 10. Illumination Control Architecture

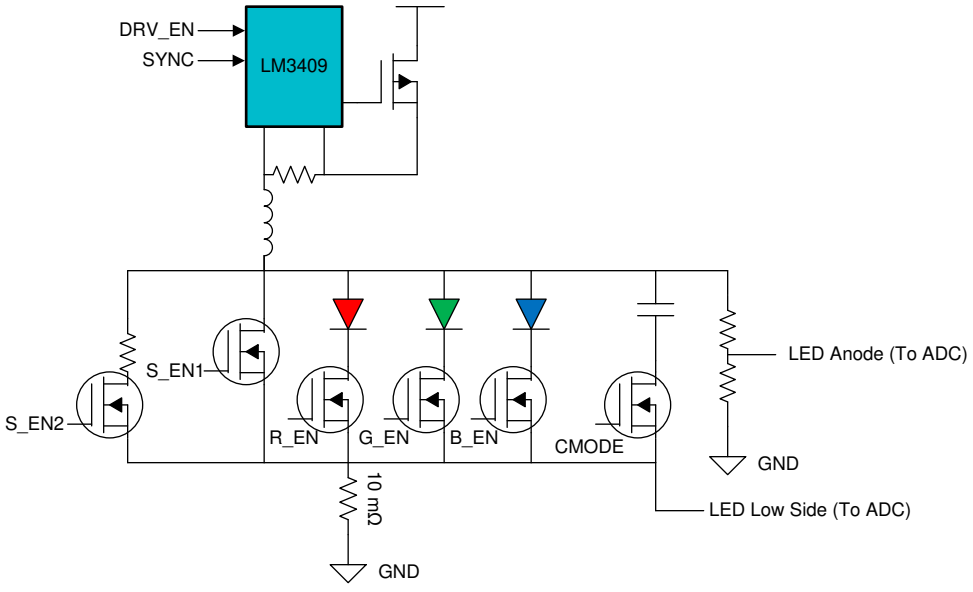

Figure 11. LED Driver Architecture

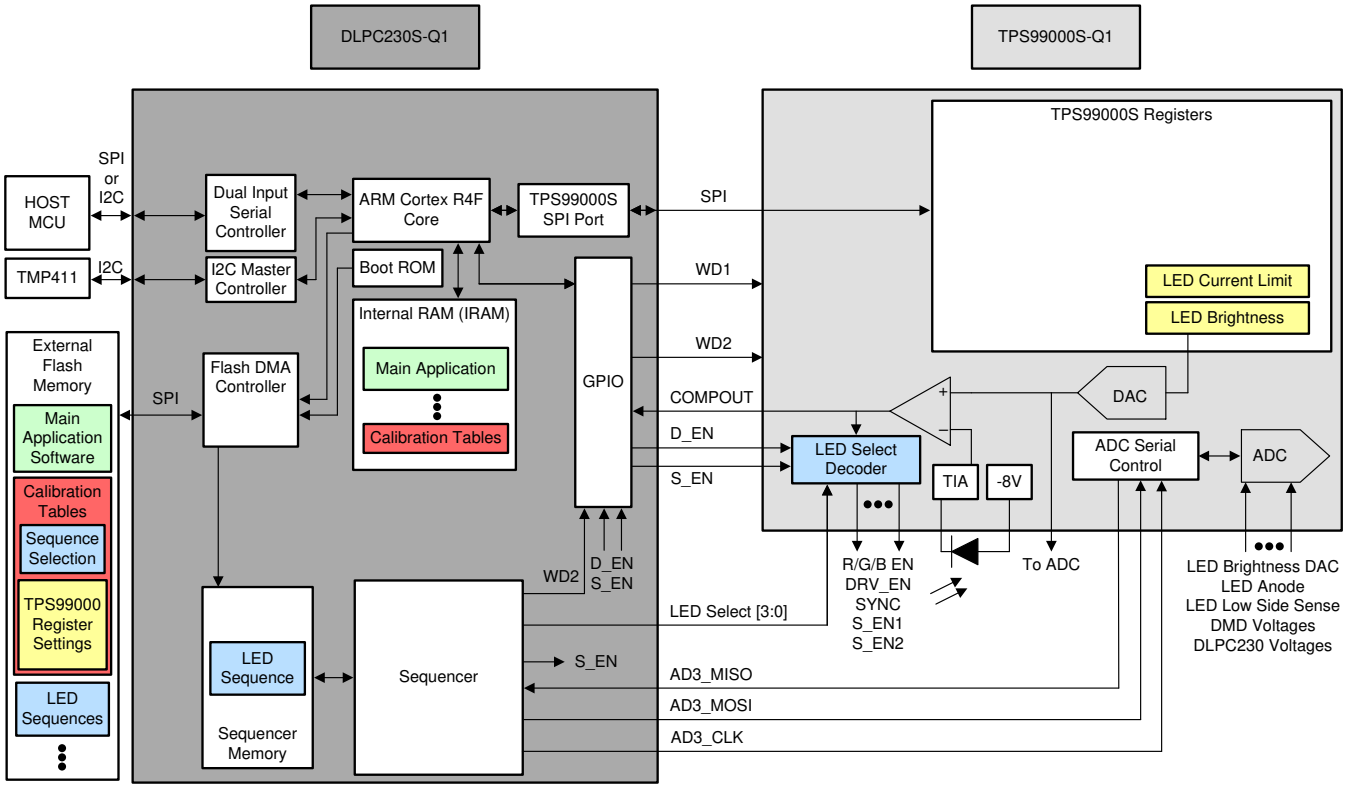

Figure 12. Software and settings origin and destination

As seen in Figure 10, Figure 11, and Figure 12:

- At start-up, the Boot ROM commands External Flash to load the Main Application Software and calibration data into the internal RAM (IRAM) of the DLPC230S-Q1. The ARM Core in the DLPC230S-Q1 executes the main application loaded in to the IRAM.
- The host MCU sends dimming commands periodically to the DLPC230S-Q1 to specify the brightness level of the system. At start-up, the calibration data provides a default dimming level.
- Based on the dimming level and calibration data, the DLPC230S-Q1 Software determines the correct LED sequence and TPS99000S-Q1 register settings. The LED sequence is the order and timing of LED pulses. TPS99000S-Q1 register settings determine the brightness of the LED pulses.
- The LED sequence determined by calibration data is requested to be loaded from external flash to the sequencer memory. The sequencer block uses the sequence loaded into its memory to send LED select signals to the TPS99000S-Q1. These signals control the enable and disable for individual LEDs.
- LED brightness is regulated to the level requested by the DLPC230S-Q1 via a feedback loop consisting of the TPS99000S-Q1, LM3409, the LEDs, and a photo-diode. The brightness target is set by the DLPC230S-Q1 into a DAC in the TPS99000S-Q1. LED brightness is measured by a photo-diode and trans-impedance amplifier (TIA) inside the TPS99000S-Q1. The target brightness and the measured brightness are compared by a comparator in the TPS99000S-Q1. The output of the comparator is used for hysteretic control of the LED light level.

7.3.2.2 *Illumination Control Monitoring and Diagnostics*

Figure 13 shows an overview of all of the monitoring and diagnostics BISTs included in the DLP5530S-Q1 Chipset.

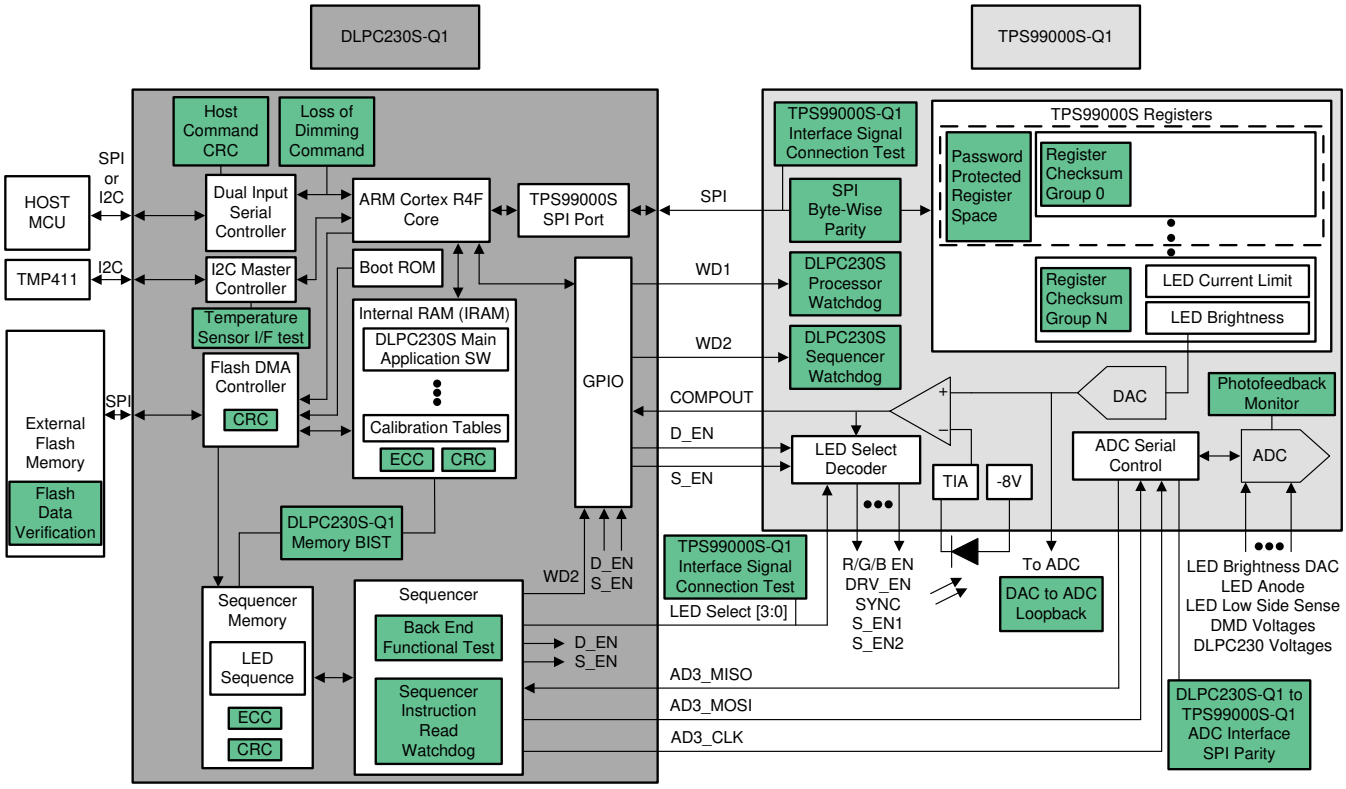

Figure 13. Illumination Control Architecture with Diagnostics

7.3.2.2.1 Communication Interface and Register Protection

The following methods are used to protect communication between ICs in the system and the data stored in critical registers.

- **[SM_14] Host Command CRC:** A CRC check on the incoming host commands to detect corrupted commands. Protects against incorrect dimming value being set due to a corrupted command
- **[SM_15] Loss Of Dimming Command Test:** Checks that dimming commands are regularly being received from the host. This enures that communication with the host has not been lost. If communication with the host is lost, and old dimming value may create an image that is too bright for the current driving conditions. The host can configure a timer within which the DLPC230S-Q1 should receive a dimming command. If the command is not received within this timing the test fails. A default value for the timer can also be configured in flash. Upon failure, emergency shutdown will be executed and an error will be logged.
- **[SM_16] TPS9000S-Q1 Interface Signal Connection Test:** Checks the SPI and the LED select interfaces between the DLPC230S-Q1 and TPS99000S-Q1. Checks SPI interface by writing to a dedicated register and reading back the value. Checks the LED select interface by sending LED select signals and reading back the LED select values from the TPS99000S-Q1 via SPI. This test can be configured to run at start-up, and it can be executed by command after the software is changed to Stand-by mode via host command. Upon failure, software will not transition Display Mode even if it is commanded by the host. An error will also be logged.
- **[SM_17] DLPC230S-Q1 to TPS99000S-Q1 SPI Byte-Wise Parity:** The DLPC230S-Q1 to TPS99000S-Q1 SPI interface implements a byte-wise parity for detecting command or data corruption. The DLPC230S-Q1 sends a parity bit with the payload for any read or write from the TPS99000S-Q1 registers. If the TPS99000S-Q1 detects a parity error it will indicate a parity error to the DLPC230S-Q1 via a status bit. Register writes to the TPS99000S-Q1 will not be performed if a parity error is detected. If the DLPC230S-Q1 detects three consecutive frames of parity error, it will not reset the DLPC230S-Q1 Processor Watchdog Timer (WD1). This will result in an emergency shutdown. An error code will also be logged.

- **[SM_18] DLPC230S-Q1 to TPS99000S-Q1 ADC Interface SPI Parity:** The DLPC230S-Q1 to TPS99000S-Q1 implements a parity check to ensure that ADC measurement commands and data are not corrupted. Parity is implemented on both the read command transaction and on the return data. Each command transaction from the DLPC230S-Q1 to TPS99000S-Q1 includes a start bit, the command id, the command id repeated, a parity bit, and a stop bit. The repeated command and data bytes must match and the parity bit must be correct. Additionally, the data returned from the TPS99000S-Q1 to DLPC230S-Q1 includes 12 data bits, 3 error bits, 12 data bits repeated, 3 error bits repeated, and 1 parity bit. The two copies of the 12-bit data, and the two copies of the 3-bit error codes must match. Additionally, the parity bit must be correct. If the TPS99000S-Q1 detects a parity error, it will indicate the error to the DLPC230S-Q1 via a status bit. If 3 consecutive errors are detected, the test fails. Upon failure, emergency shutdown will be executed and an error will be logged.
- **[SM_19] TPS99000S-Q1 Password Protected Register Space:** A portion of the TPS99000S-Q1 register space is protected by a password. The DLPC230S-Q1 unlocks this register space by writing the password before updating these registers. After updating these registers, the DLPC230S-Q1 locks this register space.
- **[SM_20] TPS99000S-Q1 Register Checksum:** The TPS99000S-Q1 implements a checksum on functionally grouped registers. This checksum is used to detect bit level changes occurring due to random events. When the DLPC230S-Q1 updates any TPS99000S-Q1 registers, it updates the checksum for that group. The TPS99000S-Q1 periodically calculates a checksum on each group of registers and compares it to the last checksum stored by the DLPC230S-Q1. If the TPS99000S-Q1 detects a checksum error, it sets a status bit that can be read by the DLPC230S-Q1 via SPI. If an error is detected, the DLPC230S-Q1 will attempt to re-write the registers and checksum up to three times. If the error persists after three attempts, an emergency shutdown will be executed and an error will be logged.

7.3.2.2.2 LED Control Feedback Loop Protection

The following methods are used to monitor and diagnose the control the LED control and feedback loop:

- **[SM_21] DAC to ADC Loopback Test:** Checks that the ADCs and DACs used to regulated LED brightness and current limit are functioning properly. Sets DAC levels and then measures the output of the DAC via ADC. If the ADC measurements do not match the expected DAC levels, the test fails. This test can be configured to run at start-up and it can be executed by command after the software is changed to Stand-by mode via host command. Upon failure, software will not transition to Display Mode even if it is commanded by the host. An error will also be logged.
- **[SM_22] Photo Feedback Monitor:** Checks the connection of the photodiode used to regulate LED brightness. The disconnection of the photodiode could result in a very bright image. The DLP5530S-Q1 chipset has two modes of operation—continuous mode for high brightness and discontinuous mode for mid and low brightness. In continuous mode, this test compares the output of the photodiode amplifier vs. the LED current. A high LED current and low photodiode reading on for all LEDs indicates that the photodiode is disconnected. In discontinuous mode, LED current measurements are not possible, so a different method is used. The COMPOUT signal indicates whether the photodiode measurement is below or above the target brightness level of the LEDs. If the photodiode measurement never reaches the target LED brightness for all LEDs in one frame, the photodiode is considered disconnected. To prevent false failures, the number of consecutive frames that the error must persist for it to be considered a real failure is configurable in flash. The number of frames can be increased for preventing false failures. However, the number of frames needed to indicate an error and respond to it should be less than the Fault Tolerant Time Interval (FTTI) specified by the OEM. Upon failure, emergency shutdown will be executed and an error will be logged. This test is always executed during display mode.
- **[SM_6] Back End Functional Test (BEFT):** Tests the sequencer block by executing a specialized LED sequence, but without turning on LEDs. Tests the sequencer block's ability to access and execute commands from sequencer memory. Makes sure that the sequencer can properly control LED illumination signals in continuous and discontinuous mode. This test can be configured to run at start-up, and it can be executed by command after the software is changed to Stand-by mode via host command. In case of test failure, software will not transition to Display Mode even if it is commanded by the host. An error will also be logged.

7.3.2.2.3 Data Load and Transfer Protection

The DLPC230S-Q1 contains several internal memories, such as the internal RAM and the sequencer memory. Data loaded into these memories comes from the external flash. The Flash Direct Memory Access (FDMA) block is used to facilitate the access and transport of data to the proper memories. In order to prevent or detect corruption of this data, the following features are implemented in the DLPC230S-Q1:

- **[SM_23] Flash Table Transport CRC:** The DLPC230S-Q1 performs two CRC checks on all data that is transported from flash to internal memories such as IRAM and sequencer memory. When the data is originally generated, a CRC is calculated and appended to each block. When data is loaded from flash to an internal memory, the embedded software reads the expected CRC value from flash. Next, the FDMA block calculates a CRC as the data is transferred. This CRC is compared to the expected CRC. Lastly, another CRC is calculated by the destination memory (IRAM, sequencer memory, etc.) hardware. If the CRCs do not match at any point, the data will be re-loaded and an error will be logged.
- **[SM_24] ECC:** The internal memories of the DLPC230S-Q1 implement ECC. The ECC can correct single-bit errors and detect, but not correct, multi-bit errors. In case of any errors, an error will be logged. In case of multi-bit errors an emergency shutdown will be executed.
- **[SM_25] DLPC230S-Q1 Memory BIST:** Checks functionality of internal memories such as the frame buffers, internal RAM, and sequence look up tables using a series of writes, delays, and reads. The frame buffer memory check is critical for diagnosing a corrupt video path. The SRAM frame buffers are tested using a series of instructions provided by the manufacturer of the SRAM cell. The instructions for executing the test are stored in external flash, but the test data is generated locally in the frame buffer. If the data read from the memory does not match the data written to the memory the test fails. This test can be configured to run at start-up, and it can be executed by command after the software is changed to Stand-by mode via host command. In case of test failure, software will not transition Display Mode even if it is commanded by the host. An error will also be logged.
- **[SM_26] Flash Data Verification:** Each block of flash data contains an expected CRC. The DLPC230S-Q1 software calculates the CRC of each block and compares it to the expected CRC stored in flash. If there is a mismatch, the test fails. This test is typically executed after programming flash data. A flash option determines if this test is executed at start-up. TI recommends enabling this option. This test can also be executed from standby mode. In case of failure, software will not transition Display Mode even if it is commanded by the host. An error will also be logged.
- **[SM_27] Periodic Refresh:** Memories in the DLPC230S-Q1 video path are periodically refreshed. For example, the frame buffers are reloaded every frame. The short reload period of these refreshes compared to the fault tolerant time interval means that the periodic refresh can be considered as a safety mechanism against transient errors in memories. Periodic refresh does not protect against permanent faults.
- **[SM_28] Boot ROM CRC:**The boot application runs a CRC on the boot ROM data and compares it to an expected value stored in the boot ROM memory. If the CRCs don't match the test fails. Upon failure, the failure stays in the boot application and does not proceed and logs an error.

7.3.2.2.4 Watchdogs and Clock Monitors

The following watchdogs are used to monitor that the various blocks of the DLPC230S-Q1 are properly operating. This is critical to ensuring that the LED brightness levels and timings are being properly controlled.

- **[SM_29] TPS99000S-Q1 Clock Ratio Monitor:** The TPS99000S-Q1 calculates a ratio between its internal clock and the external DLPC230S-Q1 clock input in order to validate proper frequency operation of the main DLPC230S-Q1 clock source. The DLPC230S-Q1 main application periodically reads this ratio. If the ratio is outside of the expected range, the test fails. Upon failure an error is logged
- **[SM_30] DLPC230S-Q1 Processor Watchdog (WD1):** The TPS99000S-Q1 monitors the DLPC230S-Q1 processor to make sure that it is continuously operating. The main application software periodically resets the watchdog timer within an allocated time window. If the watchdog signal is not received by the TPS99000S-Q1 during the time window, the test fails. Upon failure, the TPS99000S-Q1 will signal a park of the DMD and reset the chipset. The main application will read the reset cause from the TPS99000S-Q1 and assert HOST_IRQ during reset initialization.

- **[SM_31] DLPC230S-Q1 Sequencer Watchdog (WD2):** The TPS99000S-Q1 monitors the SEQ_START signal that is generated by the sequencer at the beginning of each frame. If the signal is not received within approximately 7 frames, the TPS99000S-Q1 determines that the sequencer is not functioning properly. The TPS99000S-Q1 alerts the DLPC230S-Q1. The DLPC230S-Q1 will attempt to disable and re-enable the sequencer 3 times. If it is unsuccessful after 3 tries, and emergency shutdown will be executed and an error will be logged.
- **[SM_32] Sequencer Instruction Read Watchdog:** During proper operation, the sequencer block constantly reads and executes instructions from the sequencer memory. The main application software sets a timer within which an instruction must be read from memory. The timer is reset every time an instruction is read. If an instruction is not read within the allocated time, the test fails. Upon failure, emergency shutdown will be executed and an error will be logged. This test is always active when an image is being displayed.
- **[SM_12] DMD Reset Instruction Watchdog:** Checks that the DMD has accepted command to update mirror positions. A reset command from the DLPC230S-Q1 tells the DMD to update mirror positions. If this command is not executed, mirrors will remain in their current position. Upon successfully receiving a reset command the DMD returns an acknowledge message. If this is not received by the DLPC230S-Q1 within an acceptable time, this test fails. Upon failure, emergency shutdown will be executed and an error will be logged. This test is always active when an image is being displayed.

7.3.2.2.5 Voltage Monitors

The following voltage monitors are used to make sure that the device operating voltages of the chipset are within an acceptable range

- **[SM_33] TPS99000S-Q1 DLPC230S-Q1 Real-Time Voltage Monitors:**: The TPS99000S-Q1 monitors the 1.1V, 1.8V, 3.3V, and VMAIN power supplies to the DLPC230S-Q1. These voltages are not generated by the TPS99000S-Q1. If any these voltages drop below the thresholds specified in the TPS99000S-Q1 datasheet, the TPS99000S-Q1 asserts the PARK_Z signal low. This initiates a hardware park routine within the DLPC230S-Q1, meaning no software is executed in order for this routine to execute. The hardware park routine disables LEDs and video output to the DMD. After the routine is completed, the TPS99000S-Q1 asserts RESET_Z low, which puts the DLPC230S-Q1 into reset.
- **[SM_34] TPS99000S-Q1 DMD Voltage Monitors:**The TPS99000S-Q1 generates and monitors the DMD VOFFSET, VBIAS, and VRESET voltages. Hardware monitors within the TPS99000S-Q1 detect if these voltages are outside the acceptable range and assert the PARK_Z signal low. This initiates a hardware park routine within the DLPC230S-Q1, meaning no software is executed in order for this routine to execute. The hardware park routine disables LEDs and video output to the DMD. After the routine is completed, the TPS99000S-Q1 asserts RESET_Z low, which puts the DLPC230S-Q1 into reset.
- **[SM_35] TPS99000S-Q1 Input Voltage Monitor:** The TPS99000S-Q1 monitors input voltages shown in the list below. If any of these voltages drops below the threshold, the TPS99000S-Q1 asserts PARK_Z signal low. This initiates a hardware park routine within the DLPC230S-Q1, meaning no software is executed in order for this routine to execute. The hardware park routine disables LEDs and video output to the DMD. After the routine is completed, the TPS99000S-Q1 asserts RESET_Z low, which puts the DLPC230S-Q1 into reset.
  - **3.3V Inputs:** AVDD, VDD_IO, DVDD
  - **6V Inputs:**VIN_DRST, VIN_LDOT_5V, VIN_LDOA_3P3V, VIN_LDOT_3P3V, DRVR_PWR
- **[SM_36] TPS99000S-Q1 Internally Generated Voltage Monitors:**The TPS99000S-Q1 generates and monitors several internally generated voltages (3V for ADCs and TIAs, and -8V for the photo-diode reverse biasing). Hardware monitors within the TPS99000S-Q1 detect if these voltages are outside the acceptable range and assert the PARK_Z signal low. This initiates a hardware park routine within the DLPC230S-Q1, meaning no software is executed in order for this routine to execute. The hardware park routine disables LEDs and video output to the DMD. After the routine is completed, the TPS99000S-Q1 asserts RESET_Z low, which puts the DLPC230S-Q1 into reset.
- **[SM_37] DLPC230S-Q1 DMD Voltage Monitor:** Every video frame the main application takes ADC measurements of the DMD voltages—VOFFSET, VBIAS, and VRESET. If these are not within the acceptable range, and error is logged and emergency shutdown is executed.
- **[SM_38] DLPC230S-Q1 System Voltage Monitor:** Every video frame the main application takes ADC

measurements of several system voltages. These include the DLPC230S-Q1 voltages (P1P1V, P1P8V, P3P3V), TPS99000S-Q1 voltages (DVDD, ADC_VREF, LDOT_M8, DRVR_PWR), and VMAIN. The thresholds for VMAIN are flash configurable. Upon failure, an error is logged.

8 Recommendations for chipset integration and evaluation in a functional safety system

In order to integrate and evaluate this chipset into an ISO 26262 certified system, TI recommends validating BIST functionality in-system. Recommended methods for testing each BIST are listed in Table 4. For cases that require batch command sets or special software builds to induce failures, please contact TI.

Table 4. Recommended methods for testing BISTs

BIST	Method to Induce Failure	Related HOST SPI Command
DLPC230S-Q1 Host Command CRC	Send SPI command to DLPC230S-Q1 with incorrect CRC	51h
Video Source Loss Detection	Remove video source	N/A
Video Tell-Tale Checksum	Use one of the following methods: 1. Modify source without changing expected checksum 2. Change expected checksum 3. Change checksum check region	2Bh / 2Ch
Video Frame Counter Checksum	Use one of the following methods: 1. Modify source to change frame counter 2. Change frame count check region	2Bh / 2Ch
Average Picture Level	1. Set input image to full white 2. Set APL level to 100	2Fh / 30h
Loss of Dimming Command	Enable test then do not send any dimming commands	33h / 34h
Photo Feedback Monitor	Disconnect photo-diode on system	N/A
DLPC230S-Q1 Processor Memory ECC	This failure can only be induced by TI. Please contact TI for more information.	N/A
Flash Table Transport CRC	Software build required to induce failure. Please contact TI	N/A
Frame Buffer Swap Watchdog	Batch command set required to induce failure. Please contact TI	N/A
Sequencer Instruction Read Watchdog	Batch command set required to induce failure. Please contact TI	N/A
DMD Reset Instruction Watchdog	Batch command set required to induce failure. Please contact TI	N/A
DLPC230S-Q1 System Voltage Monitor	Build and program flash with modified VMAIN threshold OR Adjust VMAIN with hardware until error is detected	N/A
DLPC230S-Q1 DMD Voltage Monitor	Software build required to induce failure. Please contact TI	N/A
DMD Clock Monitor	No method for inducing this error. TI performed validation on this test	
DMD High Speed Interface Training	Build and program flash image with incorrect pin mapping. Set system to display mode.	N/A
DMD Low Speed Interface Test	Software build required to induce failure. Please contact TI	N/A
TPS99000S-Q1 DLPC230S-Q1 Processor Watchdog (WD1)	Batch command set required to induce failure. Please contact TI	N/A
TPS99000S-Q1 DLPC230S-Q1 Sequencer Watchdog (WD2)	Batch command set required to induce failure. Please contact TI	N/A
TPS99000S-Q1 Clock Ratio Monitor	Software build required to induce failure. Please contact TI	N/A
TPS99000S-Q1 Register checksum	Batch command set required to induce failure. Please contact TI	N/A
DLPC230S-Q1 Front-End Functional Test	Software build required to induce failure. Please contact TI	N/A
DLPC230S-Q1 Back-End Functional Test	Software build required to induce failure. Please contact TI	N/A

Table 4. Recommended methods for testing BISTs (continued)

BIST	Method to Induce Failure	Related HOST SPI Command
DLPC230S-Q1 Memory BISTs	Software build required to induce failure. Please contact TI	N/A
TPS99000S-Q1 Signal Interface	Disconnect DLPC230S-Q1 to TPS99000S-Q1 SPI or LED Select Interface	N/A
DMD Memory Test	No method for inducing this error. TI performed validation on this test	N/A
Flash Data Verification	Software build required to induce failure. Please contact TI	N/A
DLPC230S-Q1 Boot ROM CRC	Software build required to induce failure. Please contact TI	N/A
DLPC230S-Q1 Flash Table CRC	Software build required to induce failure. Please contact TI	N/A
DLPC230S-Q1 Main App CRC	Software build required to induce failure. Please contact TI	N/A
DLPC230S-Q1 to TPS99000S-Q1 SPI Byte-Wise Parity	No method for inducing persistent parity error. TI performed software verification on this test	N/A
DLPC230S-Q1 to TPS99000S-Q1 ADC Interface SPI Parity	No method for inducing persistent parity error. TI performed software verification on this test	N/A
TPS99000S-Q1 password protected register space	No method for inducing this error	N/A
DAC to ADC loopback test		N/A

Summary of Recommended Functional Safety Mechanism Usage

Table 6 summarizes the monitoring and diagnostic features available in the chipset. Table 5 describes each column in Table 6. TI recommends the use of all mechanisms listed, unless one mechanism must be chosen instead of another. For example, the Video Tell-Tale Checksum and Video Frame Counter Checksum cannot be operated simultaneously so one must be selected.

Table 5. Legend of Functional Safety Mechanisms

Functional Safety Mechanism	Description
Safety Mechanism Name	The full name of this safety mechanism.
Safety Mechanism Operation Interval	The time interval at which the mechanism or test is re-executed after a pass
Test Execution Time	Time required for mechanism to definitively determine pass or fail condition.
Action on Detected Fault	The response that this safety mechanism takes when an error is detected.
Time to Report	Typical time required for safety mechanism to indicate a detected fault to the system or execute an emergency shutdown. Additional time may be required for host to read error condition from the chipset.

Table 6. Summary of Functional Safety Mechanisms

Safety Mechanism ID	Safety Mechanism Name	Safety Mechanism Operation Interval	Test Execution Time	Time to Report	Action on Detected Fault
SM_1	**Video Source Loss Detection**	1 Video Frame	1 video frame	TBD	Stay in standby or switch to alternate source
SM_2	**Video Tell-Tale Checksum**	1 Video Frame	1 video frame	TBD	Configurable: • No Action (Information only) • Log Error and Switch to Alternate Source • Emergency Shutdown and Log Error
SM_3	**Video Frame Counter Checksum**	1 Video Frame	1 video frame	TBD	Configurable: • No Action (Information only) • Log Error and Switch to Alternate Source • Emergency Shutdown and Log Error
SM_4	**Average Picture Level**	1 Video Frame	1 video frame	TBD	Configurable: • Log Error • Emergency Shutdown and Log Error
SM_5	**Front-End Functional Test**	1 Driving Cycle	33 ms	TBD	Stay in standby and log error
SM_6	**Back-End Functional Test**	1 Driving Cycle	16 ms	TBD	Stay in standby and log error
SM_7	**DLPC230S-Q1 Memory BIST**	1 Driving Cycle	47 ms	TBD	Stay in standby and log error
SM_8	**Frame Buffer Switch Watchdog**	1 Video Frame	9x video frame time	TBD	Emergency shutdown and Log Error
SM_9	**DMD High Speed Interface Training**	1 Video Frame	8x video frame time	TBD	Log Error
SM_10	**DMD Low Speed Interface Test**	1 Video Frame	1 video frame time	TBD	Log Error
SM_11	**DMD Memory Test**	1 Driving Cycle	21 ms	TBD	Stay in standby and log error
SM_12	**DMD Reset Instruction Watchdog**	1 DMD Mirror Transition Interval	9x video frame time	TBD	Emergency shutdown and log error
SM_13	**DMD Clock Monitor**				

Table 6. Summary of Functional Safety Mechanisms (continued)

Safety Mechanism ID	Safety Mechanism Name	Safety Mechanism Operation Interval	Test Execution Time	Time to Report	Action on Detected Fault
SM_14	**Host Command CRC**	1 Host SPI Command Transaction	1 SPI Command Time. Timing depends on SPI frequency	TBD	Log Error
SM_15	**Loss of Dimming Command Test**	Software Configurable	Software Configurable	TBD	Emergency shutdown and log error
SM_16	**TPS99000S-Q1 Interface Signal Connection Test**	1 Driving Cycle	3 ms	TBD	Stay in standby and log error
SM_17	**DLPC230S-Q1 to TPS99000S-Q1 SPI Byte-Wise Parity**	1 DLPC230S-Q1 to TPS99000S-Q1 command transaction	1.1 micro-seconds (4 SPI packet transactions at 30MHz; initial transaction + three re-tries)	TBD	Emergency Shutdown and Log Error
SM_18	**DLPC230S-Q1 to TPS99000S-Q1 ADC Interface SPI Parity**	1 DLPC230S-Q1 to TPS99000S-Q1 AD3 transaction	4.1 micro-seconds (4 transactions at 30MHz; initial transaction + three re-tries)	TBD	Emergency Shutdown and Log Error
SM_19	**TPS99000S-Q1 Password Protected Register Space**	1 DLPC230S-Q1 to TPS99000S-Q1 Register Write	4x video frame time	TBD	
SM_20	**TPS99000S-Q1 Register Checksum**	1 video frame	1 video frame to detect and correct 4 video frames to detect persistent error	TBD	Emergency Shutdown and Log Error
SM_21	**DAC to ADC Loopback Test**	1 Driving Cycle	27 ms	TBD	Stay in standby and log error
SM_22	**Photo Feedback Monitor**	1 Video Frame	Software Configurable	TBD	Depends on failure condition: • Emergency Shutdown and Log Error • Log Error
SM_23	**Flash Table Transport CRC**	Every Data Transfer from Flash	1 video frame	TBD	Re-load data and Log Error
SM_24	**DLPC230S-Q1 Memory ECC**	Continuous		TBD	• Correct Single-Bit Errors and Log Error • Emergency Shutdown and Log Error for multi-bit error
SM_25	**DLPC230S-Q1 Memory BIST**	1 Driving Cycle		TBD	Stay in standby and log error
SM_26	**Flash Data Verification**	1 Driving Cycle	42 micro-seconds / Kbyte of flash data	TBD	Stay in standby and log error

Table 6. Summary of Functional Safety Mechanisms (continued)

Safety Mechanism ID	Safety Mechanism Name	Safety Mechanism Operation Interval	Test Execution Time	Time to Report	Action on Detected Fault
SM_27	**Periodic Refresh**	1 Video Frame or less	N/A	N/A	N/A
SM_28	**Boot ROM CRC**	1 Driving Cycle			Stay in Boot and Log Error
SM_29	**TPS99000S-Q1 clock ratio monitor**	1 video frame time	1 video frame	TBD	Log Error
SM_30	**DLPC230S-Q1 Processor Watchdog (WD1)**	72 ms	128 ms	TBD	HOST_IRQ and system reset
SM_31	**DLPC230S-Q1 Sequencer Watchdog (WD2)**	1 video frame	7x video frame time	TBD	Emergency Shutdown and Log Error
SM_32	**Sequencer Instruction Read Watchdog**	Every sequencer instruction read, typically < 200 micro-seconds	9x video frame time	TBD	Emergency Shutdown and Log Error
SM_33	**TPS99000S-Q1 DLPC230S-Q1 Real-Time Voltage Monitors**	Continuous	52 micro-seconds	TBD	Emergency Shutdown
SM_34	**TPS99000S-Q1 DMD Voltage Monitors**	Continuous	52 micro-seconds	TBD	Emergency Shutdown
SM_35	**TPS99000S-Q1 Input Voltage Monitor**	Continuous	52 micro-seconds	TBD	Emergency Shutdown
SM_36	**TPS99000S-Q1 Internally Generated Voltage Monitors**	Continuous	Immediately	TBD	Emergency Shutdown
SM_37	**DLPC230S-Q1 DMD Voltage Monitor**	1 video frame	1 video frame	TBD	Emergency Shutdown and Log Error
SM_38	**DLPC230S-Q1 System Voltage Monitor**	1 video frame	1 video frame	TBD	Log Error

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