ULN2003LV 7 通道中继和电感负载灌电流驱动器

1 特性

- 7 通道高灌电流驱动器
- 支持高达 8V 的输出上拉电压
- 支持 3V 至 5V 的宽范围中继和电感线圈
- 0.4V（典型值）的低输出 VOL
  - 在 3.3V 的逻辑输入上，每通道具有 100mA（典型值）的电流吸收能力(1)
  - 在 5.0V 的逻辑输入上，每通道具有 140mA（典型值）的电流吸收能力(1)
- 与 3.3V 和 5.0V 微控制器和逻辑接口兼容
- 用于电感反冲保护的内部续流二极管
- 输入下拉电阻可实现三态输入驱动器
- 用来消除嘈杂环境中寄生运行的输入电阻电容 (RC) 缓冲器
- 低输入和输出泄漏电流
- 易于使用的并行接口
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求
  - 2kV 人体放电模式 (HBM)，500V 组件充电模式 (CDM)
- 采用 16 引脚小外形尺寸集成电路 (SOIC) 和薄型小外形尺寸 (TSSOP) 封装

(1) 总灌电流可能会受到内部结温、绝对最大电流等的限制 - 详细信息请参见电气规范部分。

2 应用

- 在多种电信、消费类、和工业应用中的中继和电感负载驱动器
- 照明灯和 LED 显示
- 逻辑电平转换器

3 说明

ULN2003LV 是一款针对 TI 生产的广受欢迎的 ULN2003 系列 7 通道达灵顿 (Darlington) 复合晶体管阵列的低压和低功耗升级产品。 ULN2003LV 下沉式驱动器特有 7 个低输出阻抗驱动器以支持低压中继和电感线圈应用。 低阻抗驱动器大大降低了片上功耗；对于典型 3V 中继，功率耗散低了多达 5 倍。 ULN2003LV 驱动器与相似封装内的 ULN2003 系列器件引脚到引脚兼容。

ULN2003LV 支持 3.3V 至 5V CMOS 逻辑输入接口，从而使得此器件与大范围的微控制器和其它逻辑接口兼容。 ULN2003LV 特有一个改进的输入接口，此接口可以大大降低取自外部驱动器的输入 DC 电流。 ULN2003LV 特有一个输入 RC 缓冲器，此缓冲器能够极大地改进此器件在嘈杂运行条件下的性能。 ULN2003LV 通道输入特有一个内部输入下拉电阻器从而可实现三态输入逻辑。 ULN2003LV 也可以支持其他逻辑输入电平，例如 TTL 和 1.8V，相关详细信息请参见*Application Information*部分。

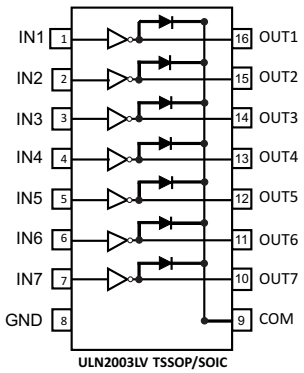
ULN2003LV 通过将几条相邻的并联通道相组合来提供增加电流吸收能力的灵活性。 在通常情况下，当所有 7 个通道并联时，ULN2003LV 能够支持高达 1.0A 的负载电流。 此外，ULN2003LV 还可用于各类需要灌电流驱动器的应用，例如驱动 LED 和逻辑电平转换。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ULN2003LVDR	SOIC (16)	3.90mm x 9.90mm
ULN2003LVPWR	TSSOP (16)	4.40mm x 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化功能图



目录

4 修订历史记录

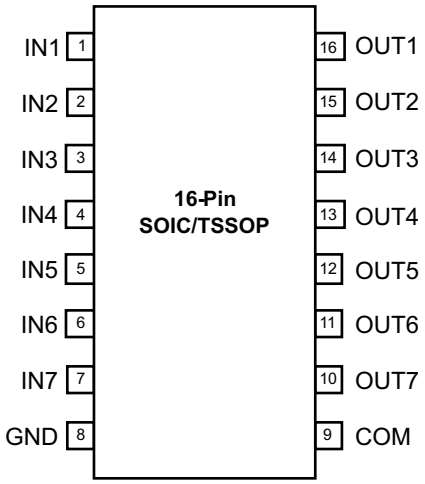
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2012) to Revision B **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1

5 Pin Configuration and Functions

D or PW Package
16-Pin SOIC or TSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN1	1	Input	Logic Input Pins IN1 through IN7
IN2	2	Input	
IN3	3	Input	
IN4	4	Input	
IN5	5	Input	
IN6	6	Input	
IN7	7	Input	
GND	8	Ground	Ground Reference Pin
COM	9	Output	Internal Free-Wheeling Diode Common Cathode Pin
OUT7	10	Output	Channel Output Pins OUT7 through OUT1
OUT6	11	Output	
OUT5	12	Output	
OUT4	13	Output	
OUT3	14	Output	
OUT2	15	Output	
OUT1	16	Output	

6 Specifications

6.1 Absolute Maximum Ratings

Specified at T_J = –40°C to 125°C unless otherwise noted.(1)

			MIN	MAX	UNIT
V_{IN}	Pins IN1- IN7 to GND voltage		–0.3	5.5	V
V_{OUT}	Pins OUT1 – OUT7 to GND voltage			8	V
V_{COM}	Pin COM to GND voltage			8	V
I_{GND}	Maximum GND-pin continuous current (T_J > +125°C)			700	mA
	Maximum GND-pin continuous current (T_J < +100°C)			1.0	A
P_D	Total device power dissipation at T_A = 85°C	16 Pin - SOIC		0.58	W
		16 Pin -TSSOP		0.45	W
T_A	Operating free-air ambient temperature		–40	85	°C
T_J	Operating virtual junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{OUT}	Channel off-state output pullup voltage			8	V
V_{COM}	COM pin voltage			8	V
$I_{OUT(ON)}$	Per channel continuous sink current	VINx = 3.3 V		100(1)	mA
		VINx = 5.0 V		140(1)	
T_J	Operating junction temperature		–40	125	ºC

(1) Refer to *Absolute Maximum Ratings* for T_J dependent absolute maximum GND-pin current

6.4 Thermal Information

THERMAL METRIC(1)		ULN2003LV		UNIT
		D (SOIC)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112	142	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69	74	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69	87	°C/W
ψ_{JT}	Junction-to-top characterization parameter	33	22	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69	87	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Specified over the recommended junction temperature range T_J = –40°C to 125°C unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUTS IN1 THROUGH IN7 PARAMETERS						
$V_{I(ON)}$	IN1–IN7 logic high input voltage	$V_{pull-up}$ = 3.3 V, R_{pullup} = 1 kΩ, I_{OUTX} = 3.2 mA	1.65			V
$V_{I(OFF)}$	IN1–IN7 logic low input voltage	V_{pullup} = 3.3 V, R_{pullup} = 1 kΩ, (I_{OUTX} = <5 µA)		0.4	0.6	V
$I_{I(ON)}$	IN1–IN7 ON state input current	V_{pullup} = 3.3 V, VIN_x = 3.3 V		12	25	µA
$I_{I(OFF)}$	IN1–IN7 OFF state input leakage	V_{pullup} = 3.3 V, VIN_x = 0 V			250	nA
OUTPUTS OUT1 THROUGH OUT7 PARAMETERS						
$V_{OL(VCE-SAT)}$	OUT1–OUT7 low-level output voltage	V_{INX} = 3.3 V, I_{OUTX} = 50 mA		0.17	0.24	V
		V_{INX} = 3.3 V, I_{OUTX} = 100 mA		0.36	0.49	
		V_{INX} = 5.0 V, I_{OUTX} = 100 mA		0.26	0.42	
		V_{INX} = 5.0 V, I_{OUTX} = 140 mA		0.40		
$I_{OUT(ON)}$	OUT1–OUT7 ON-state continuous current(1) (2) at V_{OUTX} = 0.4V	V_{INX} = 3.3 V, V_{OUTX} = 0.4 V	80	100		mA
		V_{INX} = 5.0 V, V_{OUTX} = 0.4 V	95	140		
$I_{OUT(OFF)(ICEX)}$	OUT1–OUT7 OFF-state leakage current	V_{INX} = 0 V, V_{OUTX} = V_{COM} = 8 V		0.17		µA
FREE-WHEELING DIODE PARAMETERS(3)(4)						
VF	Forward voltage drop	I_{F-peak} = 140 mA, VF = V_{OUTx} – V_{COM},		1.2		V
I_{F-peak}	Diode peak forward current			140		mA

(1) The typical continuous current rating is limited by V_{OL}= 0.4V. Whereas, absolute maximum operating continuous current may be limited by the Thermal Performance.parameters listed in the Dissipation Rating Table and other Reliability parameters listed in the Recommended Operating ConditionsTable.
(2) Refer to the *Absolute Maximum Ratings* table for T_J dependent absolute maximum GND-pin current.
(3) Not rated for continuous current operation – for higher reliability use an external freewheeling diode for inductive loads resulting in more than specified maximum free-wheeling. diode peak current across various temperature conditions
(4) Specified by design only.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	OUT1–OUT7 logic high propagation delay	V_{INX} = 3.3V, $V_{pull-up}$ = 3.3 V, $R_{pull-up}$ = 50 Ω		25		ns
		V_{INX} = 5.0V, $V_{pull-up}$ = 5 V, $R_{pull-up}$ = 1 kΩ		15		
t_{PLH}	OUT1–OUT7 logic low propagation delay	V_{INX} = 3.3V, $V_{pull-up}$ = 3.3 V, $R_{pull-up}$ = 50 Ω		45		ns
		V_{INX} = 5.0V, $V_{pull-up}$ = 5 V, $R_{pull-up}$ = 1kΩ		80		
R_{PD}	IN1–IN7 input pull-down Resistance		210	300	390	kΩ
ζ	IN1–IN7 Input filter time constant			9		ns
C_{OUT}	OUT1–OUT7 output capacitance	V_{INX} = 3.3 V, V_{OUTX} = 0.4 V		15		pF

(1) Rise and Fall propagation delays, t_{PHL} and t_{PLH}, are measured between 50% values of the input and the corresponding output signal amplitude transition.
(2) Specified by design only.

6.7 Dissipation Ratings

See (1)(2)

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$(3)	DERATING FACTOR ABOVE T_A = 25ºC	T_A < 25°C	T_A = 70°C	T_A = 85°C
High-K	16-Pin SOIC	69°C/W	112°C/W	8.88 mW/ºC	1.11 W	0.71 W	0.58 W
High-K	16-Pin TSSOP	74°C/W	142°C/W	7.11 mW/ºC	0.88 W	0.56 W	0.45 W

(1) Maximum dissipation values for retaining device junction temperature of 150°C
(2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance
(3) Operating at the absolute $T_{J\text{-}max}$ of 150°C can affect reliability– for higher reliability it is recommended to ensure T_J < 125°C

6.8 Typical Characteristics

T_A = +25ºC

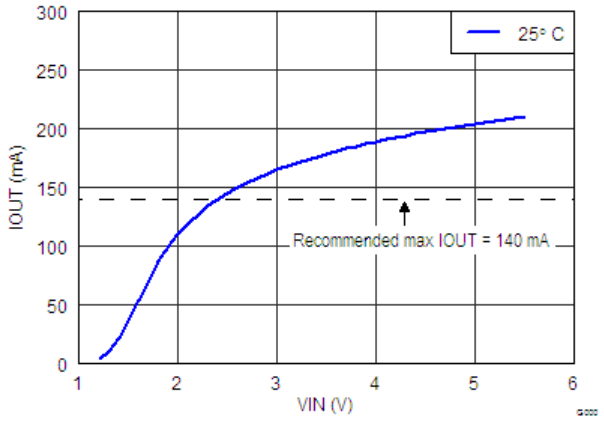


Figure 1. Load Current 1-Channel; VOL=0.4V

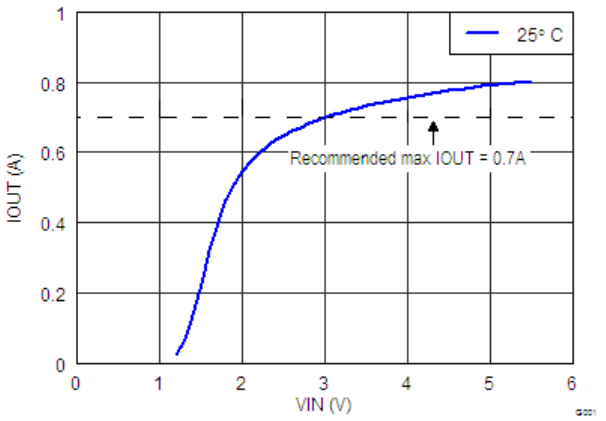


Figure 2. Load Current 7-Channels in Parallel; VOL=0.4V

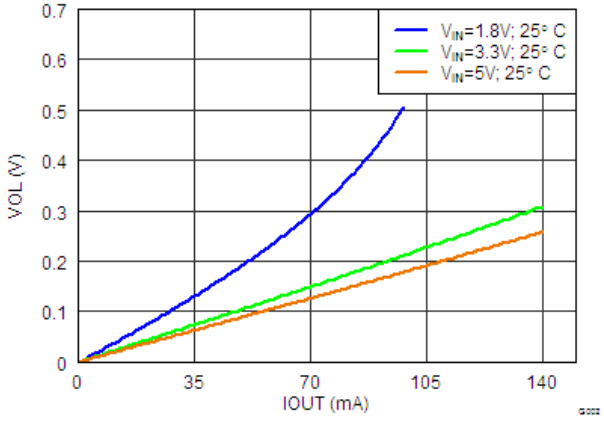


Figure 3. VOL versus IOUT VIN = 1.8V, 3.3V, 5.0V

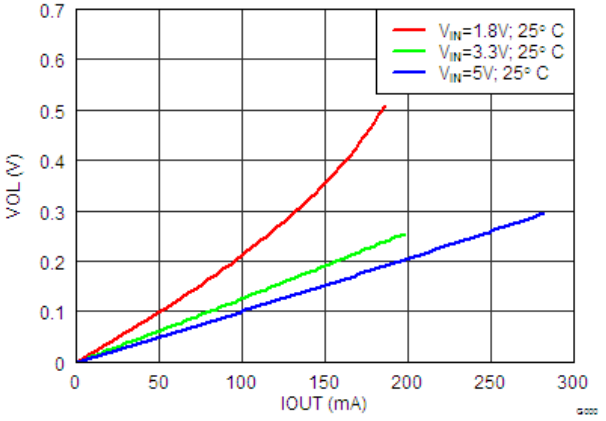


Figure 4. VOL versus IOUT 2-Channels in Parallel; VOL=0.4V

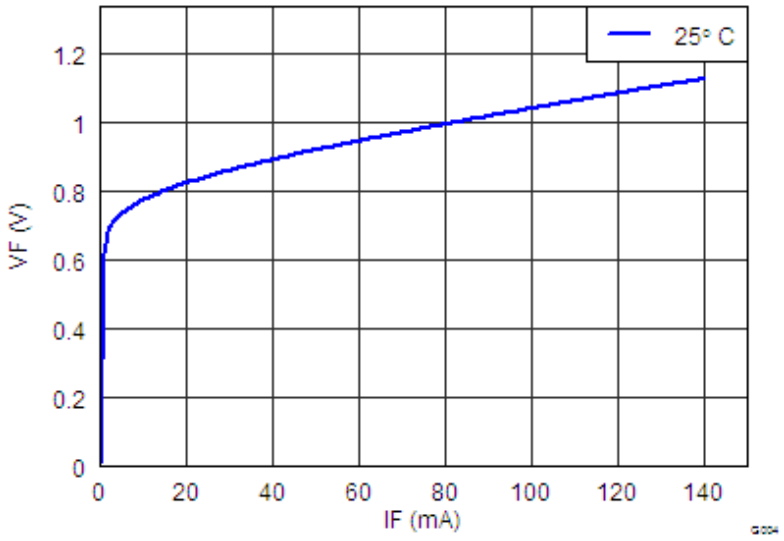


Figure 5. Freewheeling Diode VF vs IF

7 Detailed Description

7.1 Overview

ULN2003LV device is a seven-channel, low-side NMOS driver capable of driving 100-mA load with 3-V input drive voltage through each channel. This device can drive low voltage can drive low-voltage relays, LEDs or resistive loads. The ULN2003LV supports 3.3-V to 5-V CMOS logic input interface thus making it compatible to a wide range of micro-controllers and other logic interfaces. The ULN2003LV features an improved input interface that minimizes the input DC current drawn from the external drivers. The ULN2003LV features an input RC snubber that greatly improves its performance in noisy operating conditions. The ULN2003LV channel inputs feature an internal input pulldown resistor thus allowing input logic to be tri-stated. The ULN2003LV may also support other logic input levels, for example, TTL and 1.8 V.

7.2 Functional Block Diagram

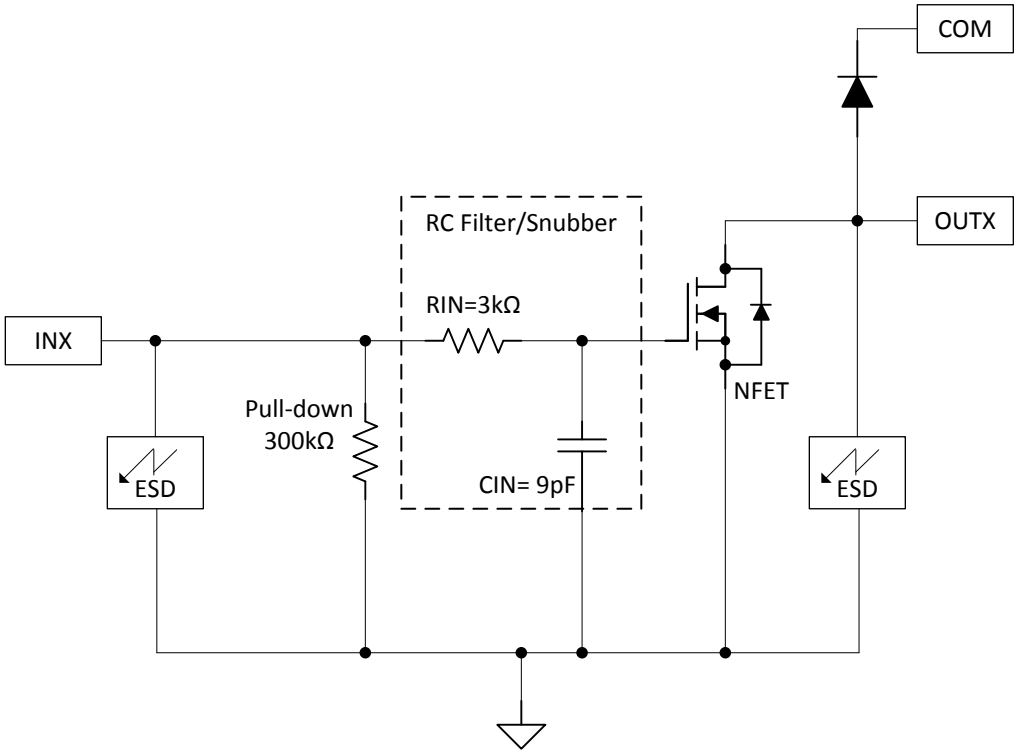


Figure 6. Channel Block Diagram

7.3 Feature Description

7.3.1 TTL and Other Logic Inputs

ULN2003LV input interface is specified for standard 3-V and 5-V CMOS logic interface. However, ULN2003LV input interface may support other logic input levels as well. Refer to Figure 1 and Figure 2 to establish VOL and the corresponding typical load current levels for various input voltage ranges. The *Application Information* section shows an implementation to drive 1.8-V relays using ULN2003LV.

7.3.2 Input RC Snubber

ULN2003LV features an input RC snubber that helps prevent spurious switching in noisy environment. Connect an external 1-kΩ to 5-kΩ resistor in series with the input to further enhance the noise tolerance of the ULN2003LV.

Feature Description (continued)

7.3.3 High-Impedance Input Drivers

ULN2003LV features a 300-kΩ input pulldown resistor. The presence of this resistor allows the input drivers to be tri-stated. When a high-impedance driver is connected to a channel input the ULN2003LV detects the channel input as a low-level input and remains in the OFF position. The input RC snubber helps improve noise tolerance when input drivers are in the high-impedance state.

7.4 Device Functional Modes

As shown in Figure 6, each output of the ULN2003LV features an internal free-wheeling diode connected in a common-cathode configuration at the COM pin. The ULN2003LV provides flexibility of increasing current sink capability through combining several adjacent channels in parallel. Under typical conditions the ULN2003LV can support up to 1.0 A of load current when all 7-channels are connected in parallel. The ULN2003LV can also be used in a variety of other applications requiring a sink drivers.

Table 1. ULN2003LV Function Table(1)

INPUT (IN1 – IN7)	OUTPUT (OUT1–OUT7)
L	Z
H	L
Z	Z

(1) L = Low-level (GND); H= High-level; Z= High-impedance

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The typical application of the ULN2003LV is a sink driver. The ULN2003LV provides a low-impedance path to GND for driving external peripherals or open-drain signals. If all 7 channels are tied together, the ULN2003 can sink up to 1 A of current in these applications

8.2 Typical Application

To use ULN2003LV as an open-collector or an open-drain inverting logic level shifter configure the device as shown in Figure 7. The ULN2003LV's each channel input and output logic levels can also be set independently. When using different channel input and output logic voltages connect the ULN2003LV COM pin to the maximum voltage.

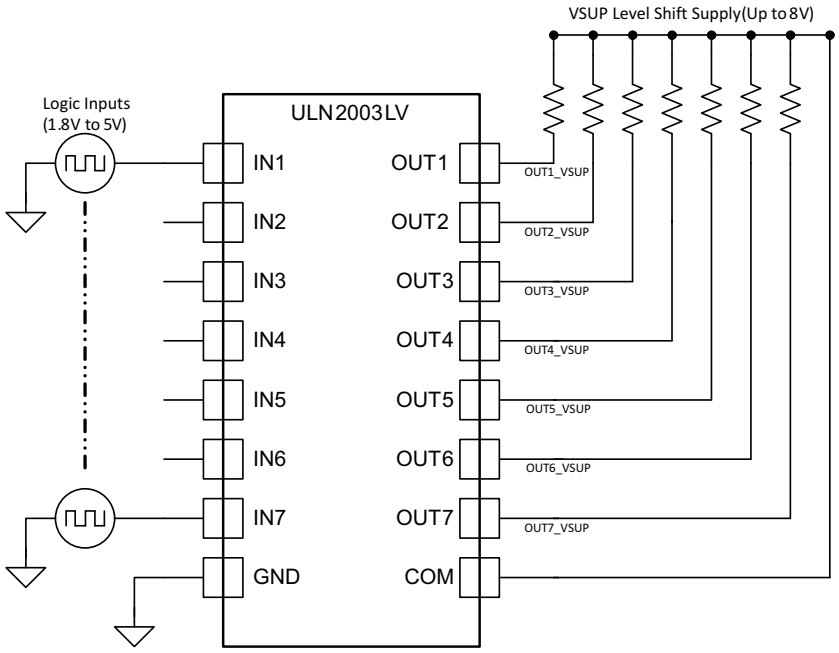


Figure 7. ULN2003LV as Inverting Logic Level Shifter

8.2.1 Design Requirements

ULN2003LV can be used in digital application requiring logic level shifting up to 8 V at the output side. Applications requiring a level shift operation from 1.8 V to 8 V. Since device pulls the output transistor low when input is high, this configuration is useful for applications requiring inverting logic with the level shifting operation.

8.2.2 Detailed Design Procedure

To operate in level shifting operation certain time aspects should be kept in mind. Depending on the pull up resistors at the output ULN2003LV exhibits different propagation delays. The choice of pull up resistor is dependent on the drive required at the output. The device can pull output to ground with the output transistor but to transition from low to high output resistor plays a critical role. If high drive at output is required a lower resistance can be calculated using Equation 1.

$$R_{Pullup} = OUT1\_VSUP / I_{Drive} \quad (1)$$

Typical Application (continued)

For example, a drive of 5 mA is required at the output for 1.8-V to 5-V translation application.

$$R_{Pullup} = OUT1\_VSUP / I_{Drive} = 5/0.005 = 1\ K \quad (2)$$

8.2.3 Application Curve

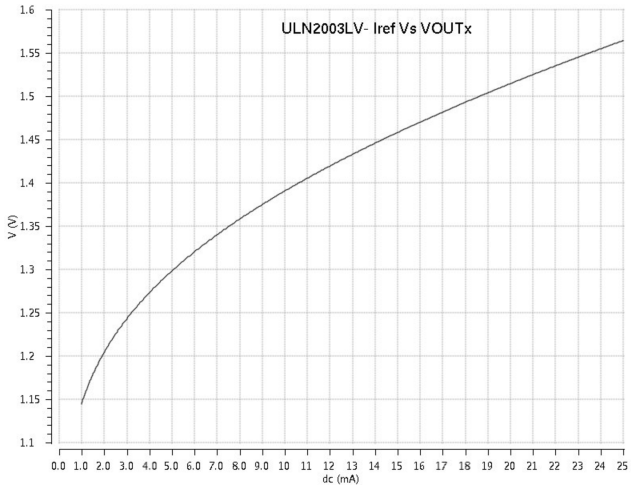


Figure 8. ULN2003LV Iref vs VOUTx

8.3 System Examples

8.3.1 Max Supply Selector

The Figure 9 implements a max supply selector along with a 4-channel logic level shifter using a single ULN20003LV. This setup configures ULN2003LV's channel clamp diodes OUT5 – OUT7 in a diode-OR configuration and thus the maximum supply among VSUP1, VSUP2 and VSUP3 becomes available at the COM pin. The maximum supply is then used as a pull-up voltage for level shifters. Limit the net GND pin current to less than 100mA DC to ensure reliability of the conducting diode. The unconnected inputs IN5-IN7 are pulled to GND potential through 300kΩ internal pull-down resistor.

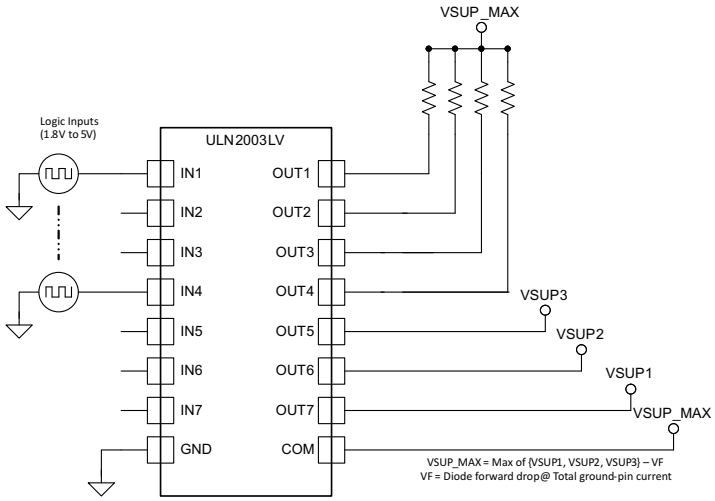


Figure 9. ULN2003LV as Max Supply Selector

System Examples (continued)

8.3.2 Constant Current Generation

When configured as per Figure 10 the ULN2003LV outputs OUT1-OUT6 act as independent constant current sources. The current flowing through the resistor R1 is copied on all other channels. To increase the current sourcing connect several output channels in parallel. To ensure best current copying set voltage drop across connected load such that VOUTx matches to VOUT7.

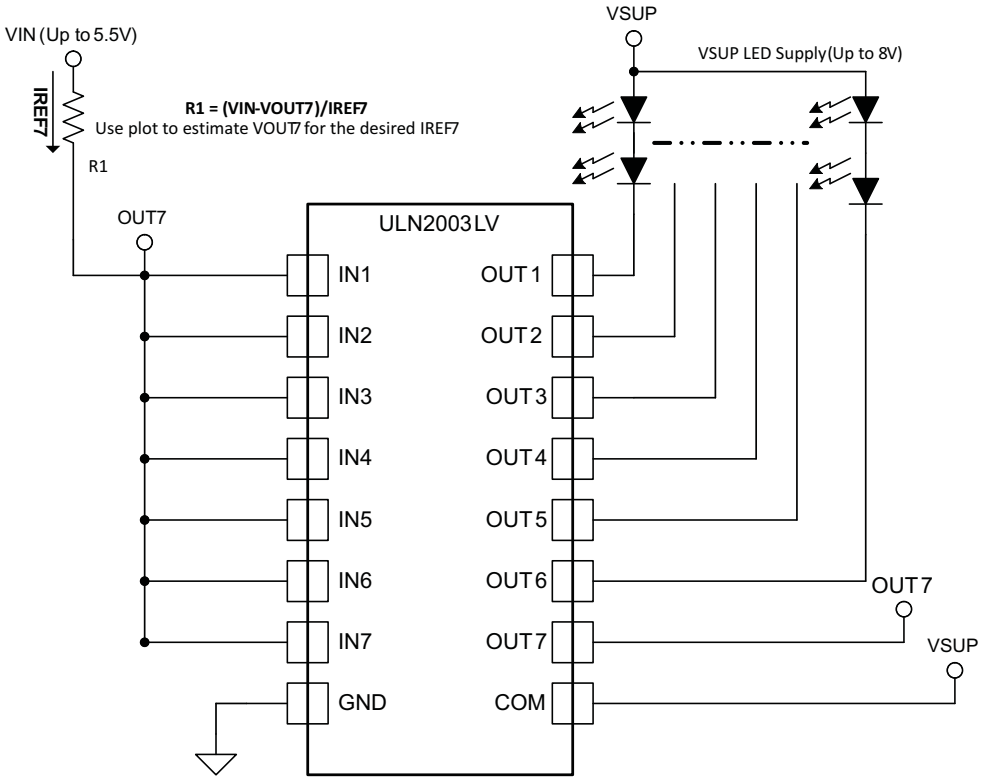


Figure 10. ULN2003LV as a Constant Current Driver

System Examples (continued)

8.3.3 Unipolar Stepper Motor Driver

The Figure 11 shows an implementation of ULN2003LV for driving a uniploar stepper motor. The unconnected input channels can be used for other functions. When an input pin is left open the internal 300kΩ pull down resistor pulls the respective input pin to GND potential. For higher noise immunity use an external short across an unconnected input and GND pins.

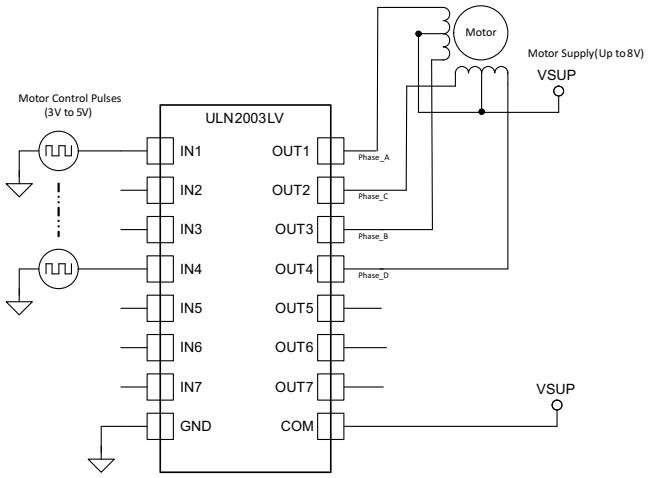


Figure 11. ULN2003LV as a Stepper Motor Driver

8.3.4 NOR Logic Driver

Figure 12 shows a NOR Logic driver implementation using ULN2003LV. The output channels sharing a common pull-up resistor implement a logic NOR of the respective channel inputs. The LEDs connected to outputs OUT5-OUT7 light up when any of the inputs IN5-IN7 is logic-high (> VIH).

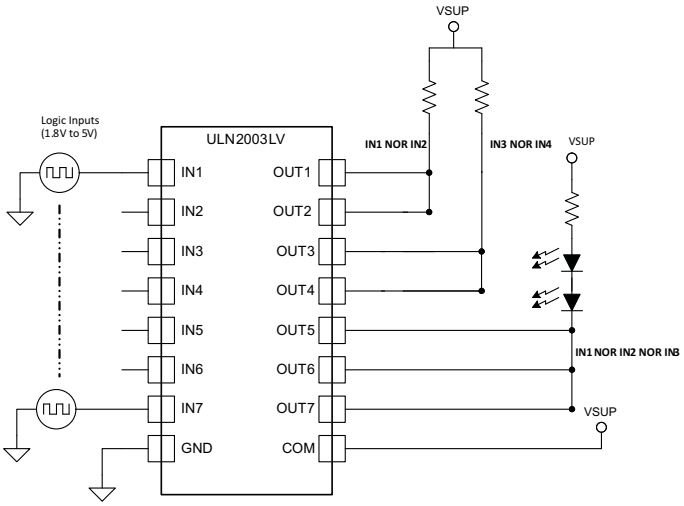


Figure 12. ULN2003LV as a NOR driver

System Examples (continued)

8.3.5 1.8-V Relay Driver

To drive lower voltage relays, like 1.8V, connect two or more adjacent channels in parallel as shown in Figure 13. Connecting several channels in parallel lowers the channel output resistance and thus minimizes VOL for a fixed current.

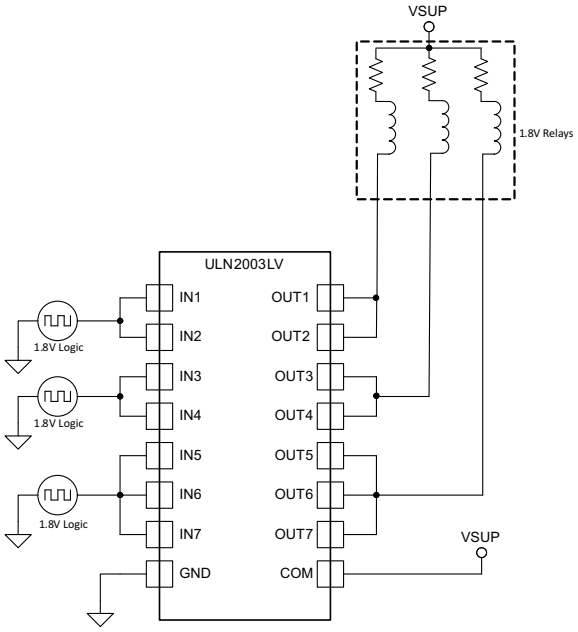


Figure 13. ULN2003LV Driving 1.8V Relays

9 Power Supply Recommendations

The COM pin is the power supply pin of this device to power the gate drive circuitry. Although not required but depending on the power supply, TI recommends to put a bypass capacitor of 100 nF across the Vcom pin and Gnd.

10 Layout

10.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive ULN2003LV. Take care to separate the input channels as much as possible, as to eliminate cross-talk. Thick traces are recommended for the output, in order to drive high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current. Since all of the channels currents return to a common ground, it is best to size that trace width to be very wide. Some applications require up to 1 A.

10.2 Layout Example

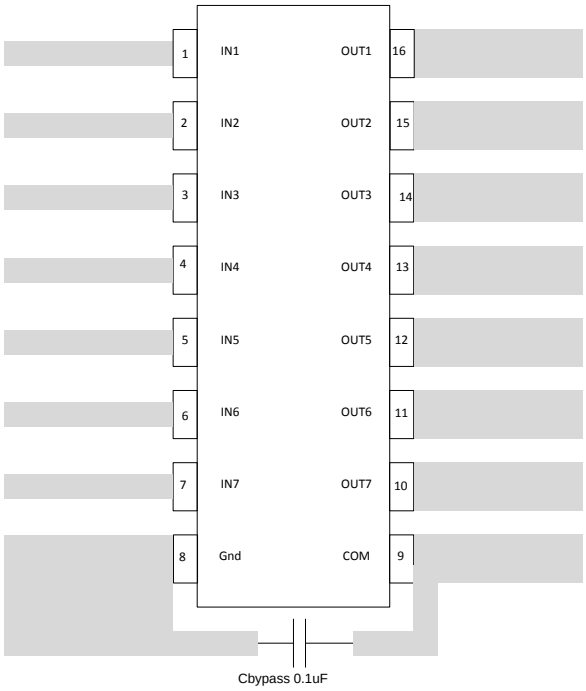


Figure 14. Layout Example Recommendation

10.3 On-Chip Power Dissipation

Use Equation 3 to calculate ULN2003LV on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \quad (3)$$

where

- N is the number of channels active together.
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}.

10.4 Thermal Considerations

TI recommends to limit ULN2003LV IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate the maximum allowable on-chip power dissipation for a target IC junction temperature:

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) \Big/ \theta_{JA} \quad (4)$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature.
- T_A is the operating ambient temperature.
- $R_{\theta JA}$ is the package junction to ambient thermal resistance.

10.4.1 Improving Package Thermal Performance

The package $R_{\theta JA}$ value under standard conditions on a High-K board is listed in the *Dissipation Ratings*. $R_{\theta JA}$ value depends on the PCB layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce $R_{\theta JA}$ and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

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11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ULN2003LVDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	UN2003LV
ULN2003LVDR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	UN2003LV
ULN2003LVPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	UN2003LV
ULN2003LVPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	UN2003LV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

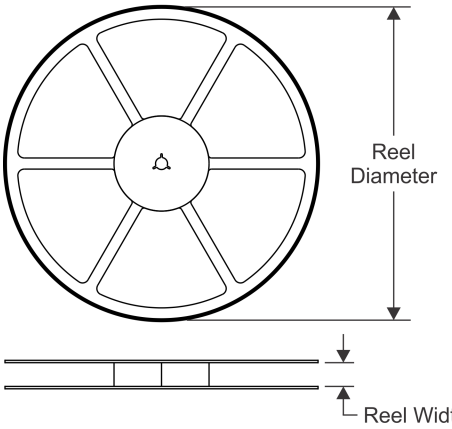
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

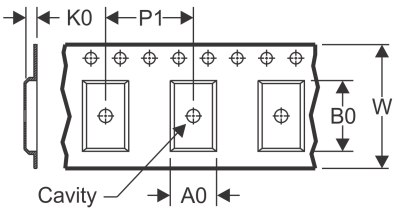
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

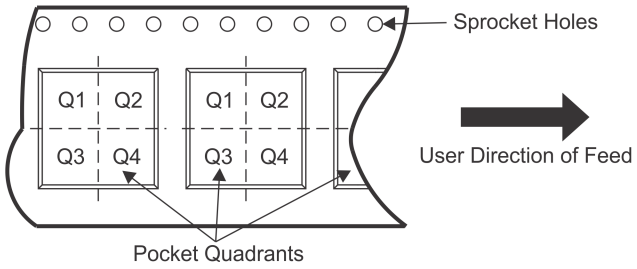


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

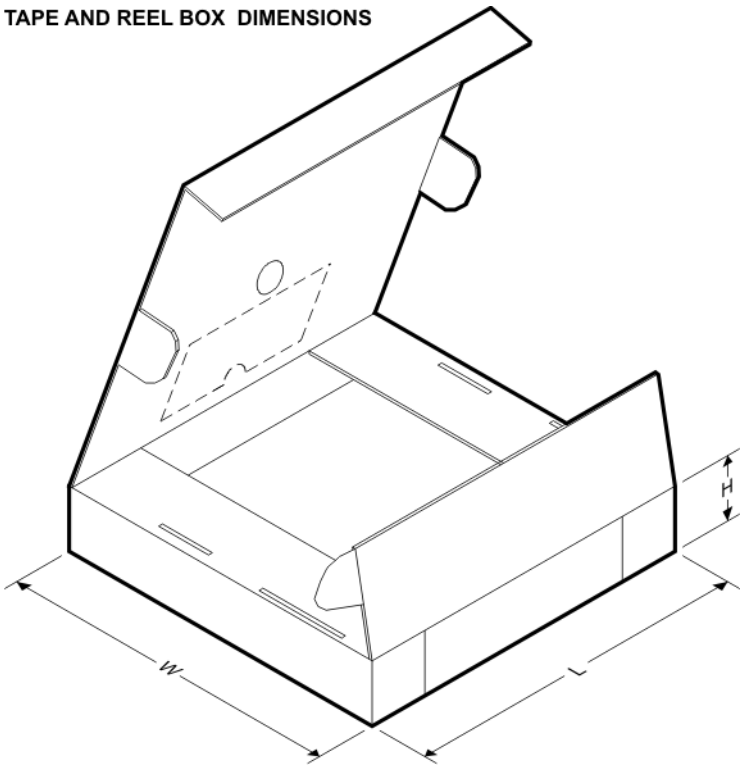
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2003LVDR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003LVPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

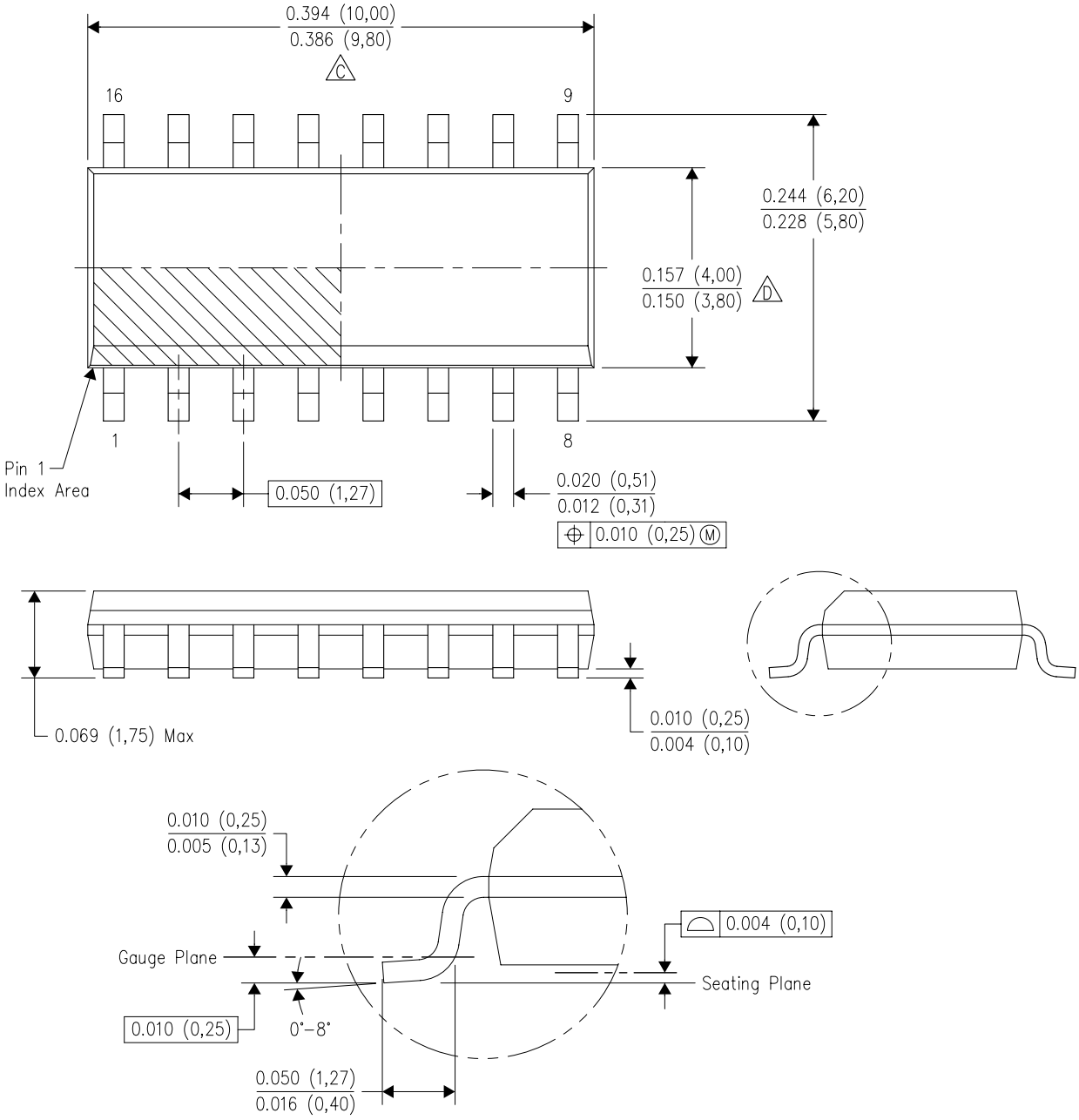
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2003LVDR	SOIC	D	16	2500	364.0	364.0	27.0
ULN2003LVPWR	TSSOP	PW	16	2000	364.0	364.0	27.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



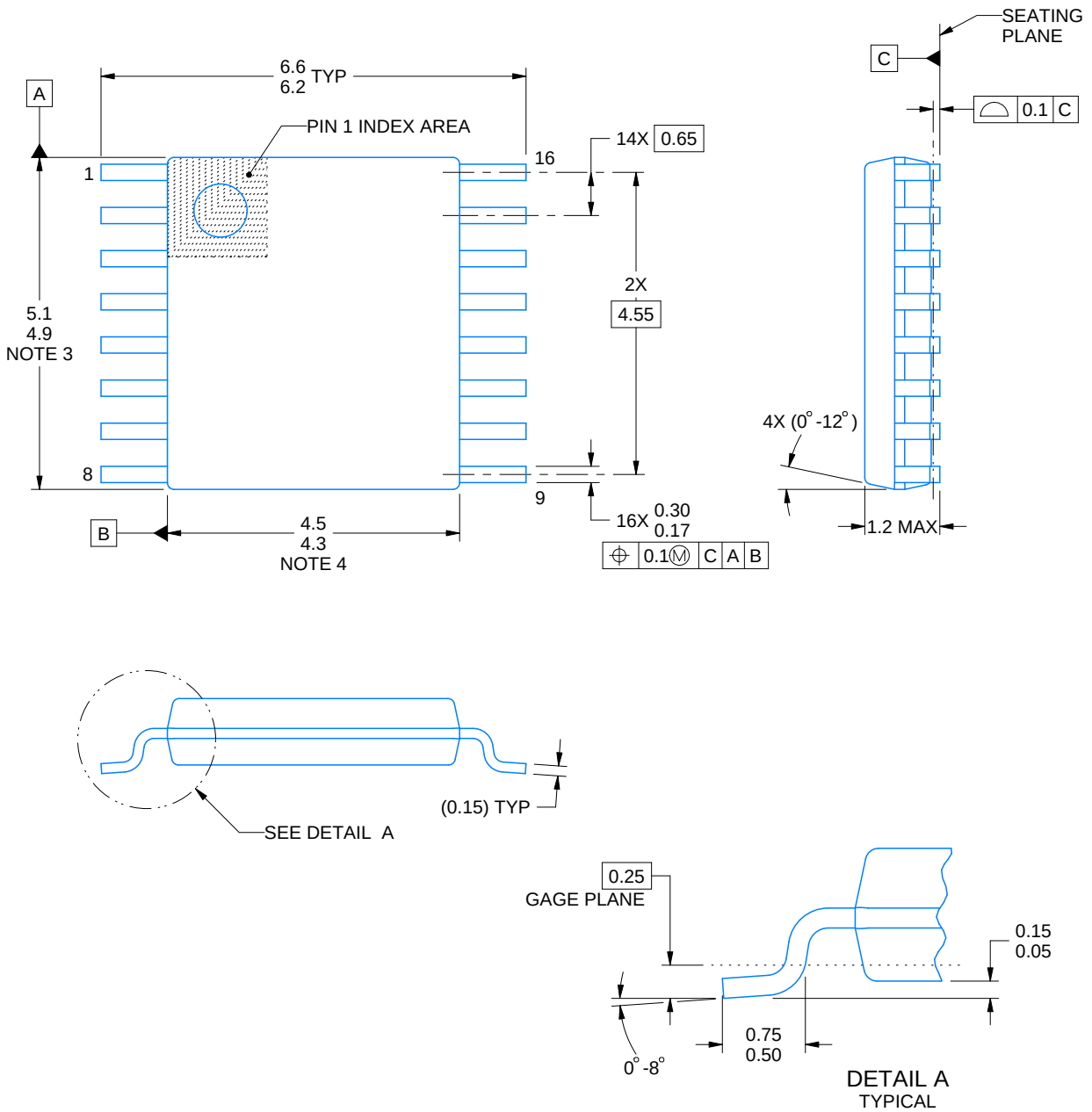
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

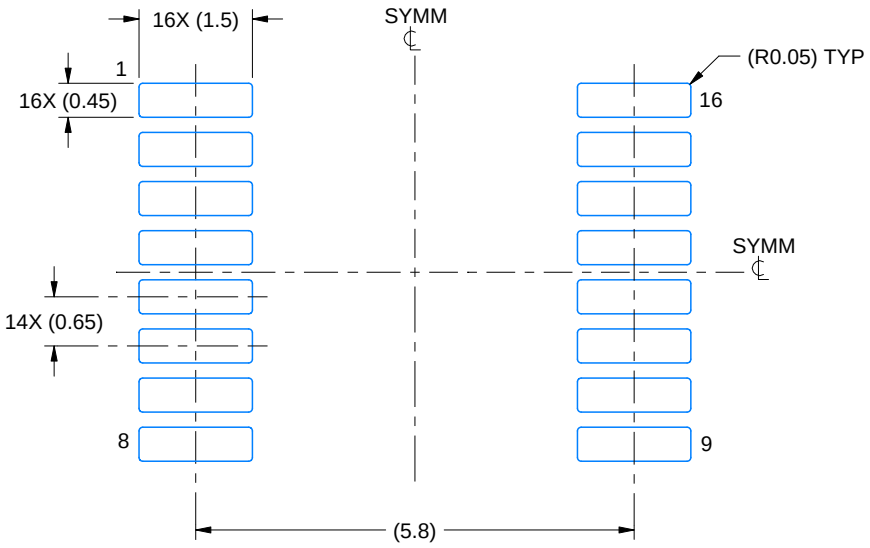
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



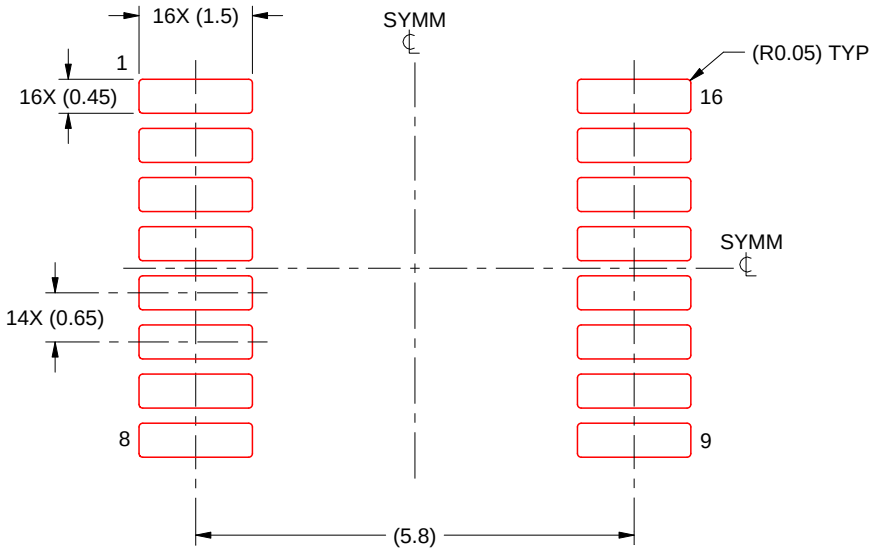
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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