UCC29950 CCM PFC 和 LLC 组合控制器

1 特性

- 高效功率因数校正 (PFC) 和半桥谐振逻辑链路控制 (LLC) 组合控制器
- 连续导通模式 (CCM) 升压功率因数校正
- 支持自偏置或辅助（外部）偏置工作模式
- 完全内部补偿的 PFC 环路
- 3 步轻松设计 PFC 级（设计电压反馈、电流反馈和功率级）
- 100kHz 固定 PFC 频率，具有抖动特性，可确保符合 EMI 标准
- 真正的输入功率限制，独立于线路电压
- 固定 LLC 频率工作范围为 70kHz 至 350kHz
- 死区变化范围为 LLC 半桥功率级的整个负载范围，可扩展零电压开关 (ZVS) 范围
- 三级 LLC 过流保护
- Hiccup 工作模式，可提供连续过载和短路保护
- 低待机功耗，由高压启动金属氧化物半导体场效应晶体管 (MOSFET) 和 X-Cap 放电功能共同实现
- 内置软启动和转换器排序功能，可简化设计
- 交流线路欠压保护，具有故障指示器
- PFC 总线过压和欠压保护
- 过温保护
- 用于扩展功率级的外部栅极驱动器
- 小外形尺寸集成电路 (SOIC)-16 封装

2 应用

- 离线交流-直流服务器电源（通过 80 PLUS® 铜牌/银牌/金牌认证）
- 工业 DIN 导轨和开放式电源
- 游戏机和打印机电源
- 高密度适配器
- 照明驱动器

3 说明

UCC29950 可为交流-直流转换器提供 LLC 转换器级和 CCM 升压功率因数校正 (PFC) 级，从而实现全部控制功能。 这款转换器经过了优化，非常便于使用。

凭借专有 CCM PFC 算法，系统能够获得高效率、更小的转换器尺寸以及高功率因数等诸多优势。 集成的 LLC 控制器可实现高效直流-直流转换级，利用软开关来降低电磁干扰 (EMI) 噪声。 这款组合控制器兼具 PFC 控制和 LLC 控制，使得控制算法能够充分利用来自两级的信息。

该控制器包含一个启动控制电路，此电路采用耗尽型 MOSFET 且内置器件电源管理功能，可最大程度降低外部元件需求，并且有助于降低系统实现成本。

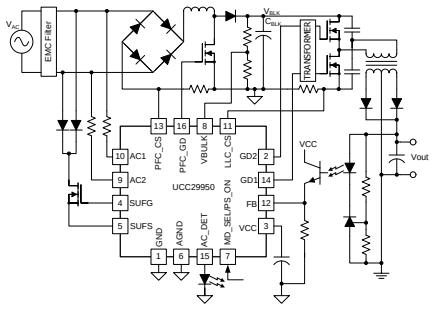
为进一步降低待机功耗，该控制器还集成了 X-Cap 放电电路。 UCC29950 实现了一整套系统保护功能，其中包括交流线路欠压保护、PFC 总线欠压 PFC 和 LLC、过流保护和热关断保护。

器件信息(1)

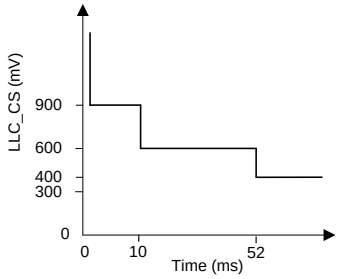
器件型号	封装	封装尺寸（标称值）
UCC29950	SOIC 16 引脚 (D)	9.90mm x 6.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



LLC 级过流保护曲线



目录

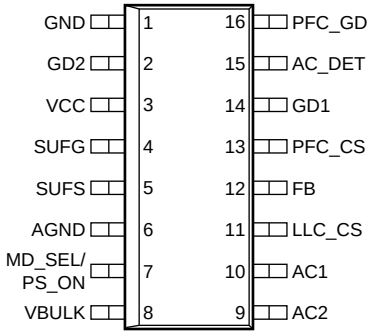
4 修订历史记录

Changes from Original (September 2014) to Revision A **Page**

- 已更改 销售状态从产品定制到产品目录。 1

5 Pin Configuration and Functions

SOIC (D)
16 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	-	Power ground. Connect all the gate driver pulsating current returns to this pin.
GD2	2	O	Gate drive output for LLC stage MOSFET. The typical peak current is 1-A source, 1.6-A sink (C_{LOAD} = 1 nF)
VCC	3	-	Bias supply input.
SUFG	4	O	Start-up MOSFET gate drive output. Leave open circuit if not used.
SUFS	5	I	Start-up MOSFET Source. Connect to VCC if not used.
AGND	6	-	Signal ground. Connect all device control signal returns to this ground.
MD_SEL/PS_ ON	7	I	Dual function pin: 1. Mode Select Function (MD_SEL): Select self bias or Aux bias mode of operation. 2. Power Supply On Function (PS_ON): Stop/start control of PFC and LLC stages, Aux Bias mode only.
VBULK	8	I	Voltage sense input for PFC stage output.
AC2	9	I	AC line voltage detection. Connect 9.3 MΩ between AC line and this pin.
AC1	10	I	AC line voltage detection. Connect 9.3 MΩ between AC line and this pin.
LLC_CS	11	I	Current sense input for the LLC stage.
FB	12	I	Feedback signal input for LLC stage.
PFC_CS	13	I	Current sense input for the PFC stage.
GD1	14	O	Gate drive output for LLC stage MOSFET. The typical peak current is 1-A source, 1.6-A sink (C_{LOAD} = 1 nF).
AC_DET	15	O	AC line voltage fail signal output, for system use.
PFC_GD	16	O	The typical peak current is 0.6-A source, 1.3-A sink (C_{LOAD} = 1 nF).

5.1 Detailed Pin Descriptions

5.1.1 VCC

The VCC pin is the power supply input terminal to the device. This pin should be decoupled with a 10-µF ceramic bypass capacitor in both Aux Bias and Self Bias Modes. An additional hold-up capacitor is needed at this pin if operating in Self Bias Mode.

5.1.2 MD_SEL/PS_ON

MD_SEL/PS_ON pin. This pin can be used to make the UCC29950 operate in Self Bias or Auxiliary Bias Mode. If MD_SEL/PS_ON pin is high during start up the controller enters Self Bias Mode. In this mode, the capacitor on the device's VCC rail is charged by an external depletion mode MOSFET connected at the SUFS and SUFG pins. Once the VCC rail reaches an appropriate operating voltage, the FET is turned off and the VCC rail is then supplied from an auxiliary winding on the LLC transformer. This avoids the standing or static losses incurred if a drop resistor from rectified AC line were used to charge the VCC rail during startup.

If the MD_SEL/PS_ON pin is held low for at least 10 ms during start up the UCC29950 enters Aux Bias Mode. Once this time has passed this pin may be used to turn on the PFC stage on its own or both the PFC and LLC stages according to the values given in the MD_SEL/PS_ON part of the Electrical Characteristics.

5.1.3 SUFG, SUFS

The SUFG and SUFS are the control pins for an external start-up depletion mode FET. The use of a switched device here eliminates the static power dissipation in a conventional resistive start-up approach where a drop resistor from the rectified AC line to VCC is typically used. As a result standby power consumption is reduced.

Connect the FET gate to SUFG and its source to SUFS. The drain of the FET is connected to the rectified AC voltage. SUFG and SUFS control the initial charging of the capacitor on the VCC rail during start-up in the Self-Bias mode of operation. In this mode SUFG tracks SUFS as C_{VCC} is charged and VCC rises. When VCC reaches $VCC_{SB(start)}$ (typically 16.2 V) SUFG goes low. This turns the start-up FET off and the PFC and LLC gate outputs start running. SUFG remains low unless VCC falls below $VCC_{SB\_UVLO(stop)}$ (typically 7.9 V) or an X-Cap discharge is required. If VCC falls below $VCC_{SB\_UVLO(stop)}$ then SUFG goes high to turn the start-up FET on and recharge C_{VCC} back up to VCC_{SB_START}.

SUFG and SUFS also provide an X-Cap discharge function in both Aux Bias and Self Bias Modes. This function is described fully in Active X-Cap Discharge.

If the UCC29950 is used in Aux Bias Mode then VCC is supplied by an external source and the external depletion mode FET is used only to provide the X-Cap discharge function. SUFG is at 0 V after a time $T_{MODE\_SEL\_READ}$ has elapsed during power up after C_{VCC} exceeds VCC_{START}. SUFG goes high whenever an X-Cap discharge is required. If the start up FET is not used and X-Cap discharge is not desired then SUFS should be connected to VCC and SUFG should be left open circuit.

5.1.4 GD1, GD2

GD1 and GD2 are the LLC gate drive outputs for the LLC half-bridge power MOSFETs. A gate drive transformer or other suitable device is required to generate a floating drive for the high-side MOSFET. The first and last LLC gate drive pulses are normally half width and appear on GD1 and GD2 respectively. If the LLC_OCP3 level is exceeded then the final pulse is of normal width. The typical peak current is 1-A source, 1.6-A sink (1-nF load).

Detailed Pin Descriptions (continued)

5.1.5 GND

GND is the power ground for the device. Connect all the gate-driver pulsating current returns to this pin.

5.1.6 AGND

AGND is the signal ground for device control signals. Connect all control signal returns to this pin.

5.1.7 LLC_CS

LLC_CS is the LLC stage current sense input. LLC_CS is used for LLC stage over-load protection. The load current is reflected to the primary side of the transformer where it is sensed using a resistor. The UCC29950 senses the LLC stage input current level and enters the over-current protection Shut-Down Mode when the current-sense signal exceeds the current and time thresholds described in LLC Three Level Over-Current Protection . The controller tries to resume operation at 1-s intervals.

5.1.8 FB

FB is the LLC stage control-loop feedback input. Connect the opto-coupler emitter to this pin. The FB pin is the input to the internal VCO. The VCO generates the switching frequency of the LLC converter. GD1 and GD2 stop switching if this pin is driven above $V_{FB\_LLC(off)}$ (typically 3.75 V) and resume operation when it falls below $V_{FB(max)}$ (typically 3.0 V). If this pin is held below $V_{FB(min)}$ (typically 200 mV) the GD1 and GD2 outputs runs at their minimum frequency.

5.1.9 PFC_GD

PFC_GD is the gate-driver output for a PFC MOSFET. Connect the PFC MOSFET gate through a resistor to control its switching speed. Because of the limited driving capability an external gate driver might be needed to support certain power MOSFET input capacitance conditions. The typical peak current is 0.6-A source, 1.3-A sink (C_{LOAD} = 1 nF).

5.1.10 PFC_CS

PFC_CS is the current sense input for the PFC stage. It is recommended to add a current-limiting resistor between the current-sense resistor and current-sense pin, to prevent damage during inrush conditions. A 1-kΩ resistor normally suffices. The UCC29950 implements a new hybrid average current-control method which controls the average current but uses the peak PFC_CS signal to terminate each switching cycle (see Hybrid PFC Control Loop). Correct PCB layout is important to ensure that the signal at this pin is an accurate representation of the current being controlled.

5.1.11 VBULK

The VBULK pin is used for PFC output-voltage sensing. Connect the sensing resistors to this pin. The upper resistor in the potential divider must be 30 MΩ and the lower resistor must be 73.3 kΩ. The high impedance reduces the static power dissipation.

5.1.12 AC1, AC2

AC1 and AC2 are the AC line voltage sensing inputs. The UCC29950 uses differential sensing for more accurate measurement of line voltage. These pins must be connected to the two line inputs via 9.3-MΩ resistors.

5.1.13 AC_DET

The AC_DET is a system-level signal which may be used for indication and system control. AC_DET goes high if the instantaneous AC voltage remains below the brownout level for longer than 32 ms. An opto-coupler can be used to send a signal to a system supervisor device so that appropriate action can be taken. In order to provide hold-up time to the system, the power stages continue to operate for 100 ms after AC_DET goes high. This behavior is shown in Figure 10, Figure 11 and Figure 12.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply Voltage	VCC	–0.3	20	V
Continuous Input Voltage Range	LLC_CS	–0.3	4.5	V
	FB, AC1, AC2, VBULK, MD_SEL/PS_ON	–0.3	VCC+0.3	V
	AC_DET	0	4.5	V
	SUFS	–0.3	20	V
	SUFG	–0.3	SUFS+0.3	V
	GD1, GD2, PFC_GD	–0.5	VCC+0.5	V
	PFC_CS	–1.3	4.5	V
Continuous Input Current Range	PFC_CS		±15	mA
T_{SOL}	Lead temperature (10 s)		260	°C
Operational Junction Temperature, T_J		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Storage Conditions

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–40	150	°C

6.3 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage range	11		18	V
V_{FB}	FB pin voltage range	0		VCC	V
V_{MD_SEL/PS_ON}	MD_SEL/PS_ON pin voltage range	0		VCC	V
RL1/RL2	Line sensing resistors		9.3		MΩ

6.5 Thermal Information

THERMAL METRIC(1)		UCC29950 SOIC (D) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.3	
ψ_{JT}	Junction-to-top characterization parameter	8.9	
ψ_{JB}	Junction-to-board characterization parameter	36.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

–40°C < T_J < 125°C(1), VCC = 12 V, all voltages are with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC Bias Supply (Self Bias Mode)						
I_{SUFS}	Charging current into V_{CC}	SUFS = 7.5 V, VCC = 4 V	–1	–2	–4	mA
$VCC_{SB(start)}$	In Self Bias mode, the controller will not start PFC and LLC gate drive outputs until the start up FET has charged the capacitance on the VCC pin above this level	MD_SEL/PS_ON = VCC at power-up (self bias mode)	15.0	16.2	17.4	V
$VCC_{SB\_UVLO(stop)}$	In Self Bias mode, VCC must be greater than this level to allow the controller to continue to output the PFC and LLC gate drives.	VCC falling Self Bias Mode	7.3	7.9	8.5	
VCC Bias Supply (Aux Bias Mode)						
VCC_{START}(2)	Controller logic starts at this VCC voltage	VCC rising	4.4	6	7.0	V
VCC_{STOP}(2)	Controller logic stops at this VCC voltage	VCC falling	3.7	5.0	5.8	
$VCC_{AB\_UVLO(start)}$	In Aux Bias Mode, VCC must be greater than this level to allow the controller to start the PFC and LLC gate drive outputs.	VCC rising MD_SEL/PS_ON = 0 V at power-up (Aux Bias Mode)	10.0	10.5	10.9	
$VCC_{AB\_UVLO(stop)}$	In Aux Bias Mode, VCC must be greater than this level to allow the controller to continue to output the PFC and LLC gate drives.	VCC falling Aux Bias Mode	9.1	9.6	10.0	
VCC Supply Current						
ICC_{ENABLE}	Device is Enabled and providing PFC & LLC gate drive outputs	GD1, GD2 at LLC_{FMAX}. PFC_GD at f_{PFC} (100 kHz nom). GD1, GD2 and PFC_GD pins unloaded.	7.5	8.0	18.3	mA
MD_SEL/PS_ON, Mode Select Function at Power Up						
V_{MODE_SELSB}	Minimum voltage on the MD_SEL/PS_ON pin that will select Self Bias mode on power up (see Device Functional Modes).		1.1	1.6	2.1	V
$T_{MODE\_SEL\_READ}$	After VCC pin exceeds VCC_{START}. This is the minimum time that the MD_SEL/PS_ON pin must remain below V_{MODE_SELSB} to ensure that Aux Bias Mode is selected (see Device Functional Modes).		10			ms
MD_SEL/PS_ON, Power Supply On Function, Aux Bias Mode Only						
$V_{PS\_ONPFC\_RUN}$	Minimum voltage on the MD_SEL/PS_ON pin that causes PFC stage to run(3)		20	25	33	%VCC
$V_{PS\_ONLLCPFC\_RUN}$	Minimum voltage on the MD_SEL/PS_ON pin that causes PFC and LLC stages to run(3)		66	75	85	%VCC
AC_DET						
$V_{OH\_TP\_LZ}$	AC_DET output high	$I_{(AC\_DET)}$ = –1 mA	2.5	3.1	4.1	V
V_{OL}	AC_DET output low	$I_{(AC\_DET)}$ = 1 mA	19	35	80	mV
$I_{O(max\_source)}$	AC_DET source current	V_{OUT} > 2.4 V			–1.6	mA
$I_{O(max\_sink)}$	AC_DET sink current	V_{OUT}< 0.5 V			6.0	mA

(1) The device has been characterized over the entire temperature range during development. Individual devices may enter temperature shutdown (T_{SD}) at T_J lower than 125°C.
(2) $VCC_{START}$is always greater than VCC_{STOP}.
(3) Threshold voltage will track VCC and is therefore specified as a percentage of VCC.

Electrical Characteristics (continued)

–40°C < T_J < 125°C(1), VCC = 12 V, all voltages are with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBULK, PFC OUTPUT VOLTAGE						
$V_{BULK(ovp)}$	PFC output overvoltage protection (auto recovery)		1.06	1.10	1.14	V
$V_{BULK(reg)}$	V_{BULK} regulation set-point		0.907	0.940	0.973	V
$V_{BULK(llc\_start)}$	LLC operation start threshold		0.70	0.73	0.77	V
$V_{BULK(llc\_stop)}$	LLC operation stop threshold		0.45	0.49	0.53	V
AC1, AC2, AC LINE SENSING FOR PFC						
R_{AC1}	AC1 pin resistance to AGND	AC1 pin	45	60	71	kΩ
R_{AC2}	AC2 pin resistance to AGND	AC2 pin	45	60	71	
$I_{AC(det)}$ (4)(5)	AC_DET is active HIGH when I_{AC} is below this level	Force current into AC1 or AC2 pins. Unused pin input at 0 V.	7.03	7.48	7.93	μA_{RMS}
$I_{AC(low\_falling)}$ (4)(5)	PFC stage stops 100 ms after I_{AC} is at or below this level	Force current into AC1 or AC2 pins. Unused pin input at 0 V.	7.03	7.48	7.93	
$I_{AC(low\_rising)}$ (4)(5)	PFC stage is allowed to start when I_{AC} is at or above this level	Force current into AC1 or AC2 pins. Unused pin input at 0 V.	8.04	8.55	9.1	
$I_{AC(high\_falling)}$ (4)(5)	PFC stage restarts if I_{AC} falls below this level. No soft-start	Force current into AC1 or AC2 pins. Unused pin input at 0 V.	30.7	32.0	33.3	
$I_{AC(high\_rising)}$ (4)(5)	PFC stage stops if I_{AC} is at or above this level	Force current into AC1 or AC2 pins. Unused pin input at 0 V.	31.8	33.1	34.4	
$I_{AC(halt)}$ (4)(5)	PFC and LLC stages stop if I_{AC} is at or above this level	Force current into AC1 or AC2 pins. Unused pin input at 0 V.	32.8	34.2	35.6	
PFC_CS, PFC CURRENT SENSE						
$V_{PFCCS(cav\_max)}$	Maximum voltage at PFC_CS pin, (ignoring signal ripple due to inductor ripple current) that determines maximum power delivered. Used to determine R_{CS_PFC}. (see PFC Stage Current Sensing Figure 13 and Figure 6)		–200	–225	–250	mV
$V_{PFCCS(max)}$	Maximum voltage at PFC_CS pin	VBULK pin = 800 mV, $\lvert V_{AC1} - V_{AC2} \rvert = V_{AC\_PEAK}$ (6)	–570	–800	–950	
PFC_GD, PFC GATE DRIVER						
$V_{HI(pfc\_2mA)}$	PFC_GD high level	$I_{O(PFC\_GD)}$ = –2 mA	11.5	11.8	12.0	V
$V_{HI(pfc\_75mA)}$	PFC_GD high level	$I_{O(PFC\_GD)}$ = –75 mA	8.5	9.5	10.5	
$R_{PFC(gd\_hi)}$	PFC_GD pull-up resistance	$I_{O(PFC\_GD)}$ = –50 mA		14	25	Ω
$R_{PFC(gd\_lo)}$	PFC_GD pull-down resistance	$I_{O(PFC\_GD)}$ = 75 mA		4.4	10	
$t_{R(pfc)}$	PFC_GD rise time	Capacitive load of 1.0 nF on PFC_GD pin, 20% to 80%		30	45	ns
$t_{F(pfc)}$	PFC_GD fall time	Capacitive load of 1.0 nF on PFC_GD pin, 20% to 80%		10	25	
f_{PFC}	Switching frequency	Includes dithering of ±2 kHz at nominal 333-Hz rate.	87	98	109	kHz

(4) These are specified at 25°C. The relative levels for these specifications track each other. The equivalent line voltages are given in Table 3, assuming a source impedance of 9.3 MΩ.
(5) This is the current into the AC1 or AC2 pins.
(6) Tested at peak of line voltage or 90° from zero crossing.

Electrical Characteristics (continued)

–40°C < T_J < 125°C(1), VCC = 12 V, all voltages are with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FB, LLC Control Loop Feedback						
$V_{FB(min)}$ (7)	Minimum voltage on FB pin where LLC frequency is modulated	Below V_{FB_MIN}, LLC frequency is LLC_{Fmin}	0.17	0.2	0.23	V
$V_{FB(max)}$ (7)	Maximum voltage on FB pin where LLC frequency is modulated	Between V_{FB_MAX}, and $V_{FB\_LLC\_OFF}$ LLC frequency is LLC_{Fmax}	2.90	3	3.10	
$V_{FB(llc\_off)}$ (7)	Voltage on FB pin above which LLC gate drive terminated	Once V_{FB} exceeds $V_{FB\_LLC\_OFF}$, V_{FB} must fall below V_{FB_MAX} to resume switching	3.62	3.75	3.88	
LLC_{FMIN} (7)	Minimum LLC switching frequency		63.7	70	74.8	kHz
LLC_{FMAX} (7)	Maximum LLC switching frequency		321	350	378	
$LLC_{T(dead)}$ (8)	Time for which GD1 and GD2 are both low during LLC operation at LLC_{FMIN}	LLC dead-time at minimum switching frequency.	224	300	388	ns
R_{FB}	Internal resistance from FB pin to AGND		45	60	71	kΩ
LLC_CS, LLC Current Sense						
$V_{CS(ocp3)}$ (9)	LLC Overcurrent threshold level three	If this level is exceeded the PFC and LLC stages will stop for $t_{LONG(fault)}$. Restart with a normal soft-start sequence	0.87	0.9	0.94	V
$V_{CS(llc\_max)}$	Voltage at LLC_CS pin at 100% of full load		0.27	0.30	0.33	
FAULT Section						
$t_{LONG(fault)}$	Recovery time after long fault		0.9	1.0	1.5	s
$t_{SHORT(fault)}$	Recovery time after short fault		90	100	150	ms
GD1, GD2, LLC GATE Drive Output						
$V_{GD(hi\_2mA)}$	GD1, GD2 output high level	$I_{O(GDx)}$ = –2 mA	11.5	11.8	12	V
$V_{GD(hi\_75mA)}$	GD1, GD2 output high level	$I_{O(GDx)}$ = –75 mA	9.3	10.1	10.9	
$R_{GD(hi)}$	GD1, GD2 gate driver pull-up resistance	$I_{O(GDx)}$ = –50 mA		5.8	10.5	Ω
$R_{GD(lo)}$	GD1, GD2 gate driver pull-down resistance	$I_{O(GDx)}$ = 75 mA		1.6	5	
$t_{r(llcgd)}$	LLC gate driver rise time	Capacitive load of 1 nF on GD1, GD2 pins		12	30	ns
$t_{f(llcgd)}$	LLC gate driver fall time	capacitive load of 1 nF on GD1, GD2 pins (20% to 80%)		11	25	
Thermal Shutdown						
T_{SD}	Thermal shutdown temperature				125	°C
T_{ST}	Start / restart temperature			113		

(7) Refer to Figure 1.
(8) Refer to Figure 2.
(9) Refer to Table 4 for other LLC Stage Over-Current Protection Levels.

6.7 Typical Characteristics

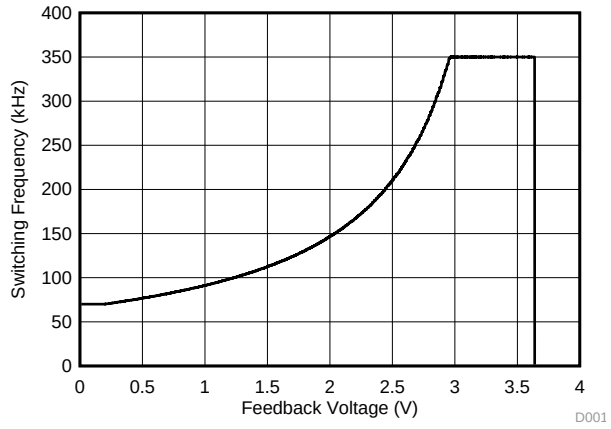


Figure 1. LLC Switching Frequency vs V_{FB}

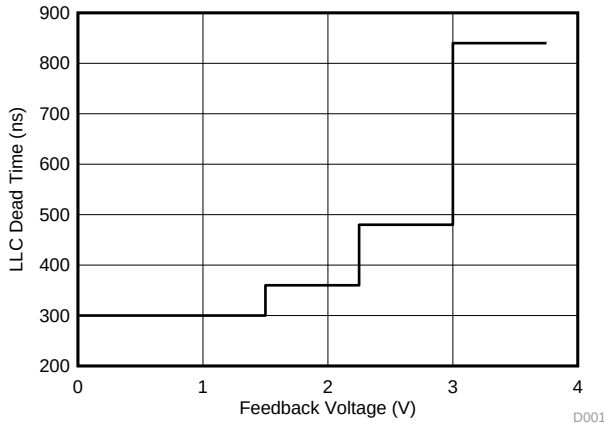


Figure 2. LLC Dead Time vs V_{FB}

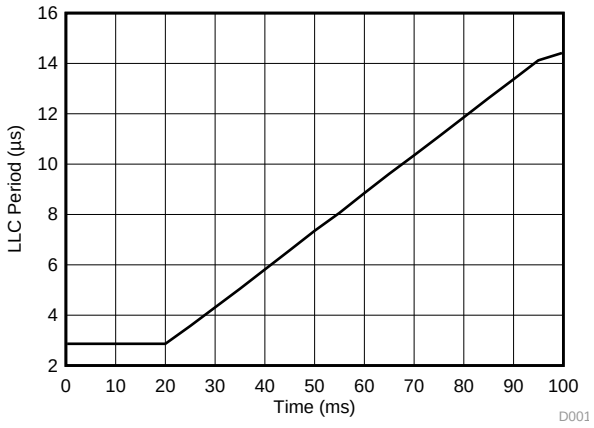


Figure 3. LLC Period vs Time During Soft-Start

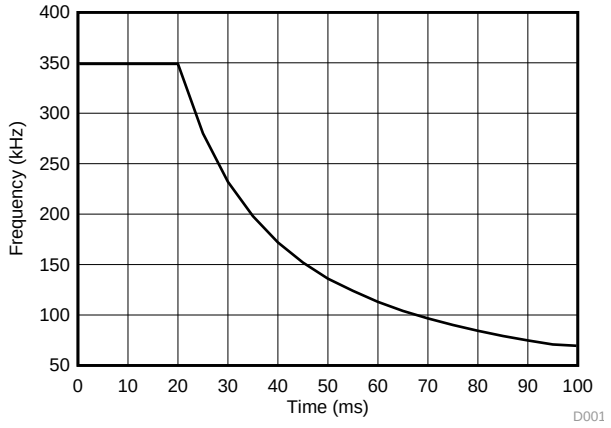


Figure 4. LLC Frequency vs Time During Soft-Start

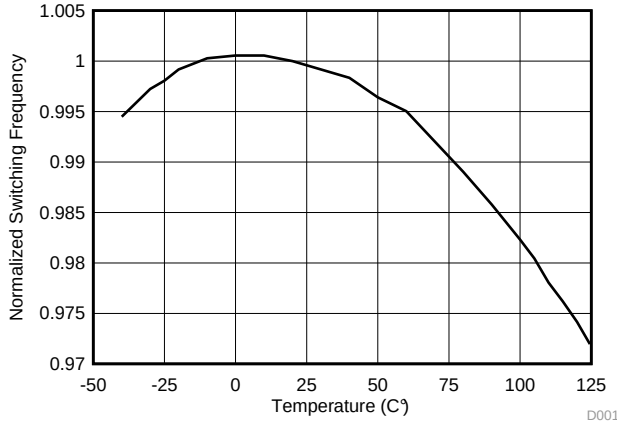


Figure 5. Switching Frequency vs Temperature (for PFC and LLC). Normalized to 1 at 20°C

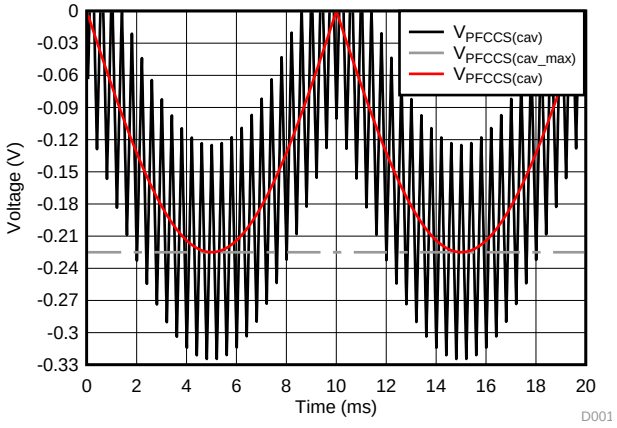


Figure 6. PFC_CS Signal (diagrammatic)

Typical Characteristics (continued)

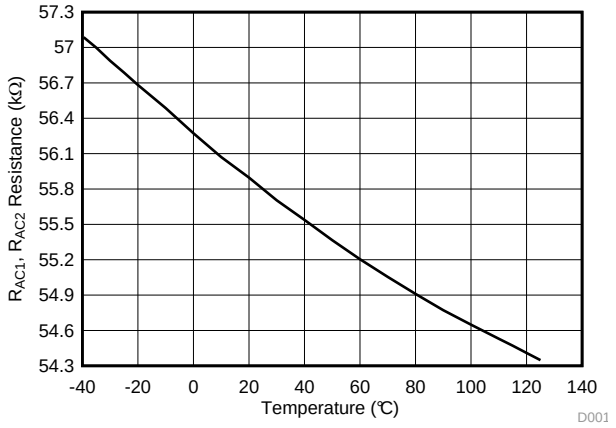


Figure 7. R_{AC1}, R_{AC2} Resistance vs Temperature

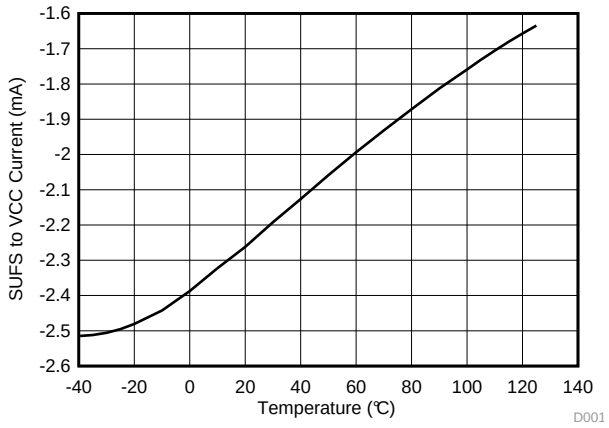


Figure 8. SUFS to VCC Current vs Temperature

7 Detailed Description

7.1 Overview

The UCC29950 combines all the functions necessary to control a Boost PFC and LLC power system. It is packaged in an SOIC-16 package. The SUFG and SUFS pins allow the system designer to use an external depletion mode MOSFET to provide start up power instead of using a dissipative resistor. The use of high-impedance voltage sensing networks further reduces standby power. The combo device uses information from both PFC and LLC stages to optimize the system efficiency, transient response and standby power. The controller can be operated with bias current supplied from a small external PSU (Aux Bias) or from a winding on the LLC transformer (Self Bias). In Aux Bias Mode, the MD_SEL/PS_ON pin allows the user to turn on the PFC stage alone or both PFC and LLC stages.

The UCC29950 has many protection features, these include:

- Bias Rail Under-Voltage Lockout
- Active X-Cap Discharge
- Line Under-Voltage Detection
- Line Over-Voltage Detection
- Line Brownout Detection
- Three Level Output Overcurrent Profile on LLC Stage
- PFC Stage Constant Input Power Limit
- PFC Stage Input Current Limit
- PFC Stage Second Current Limit
- PFC Stage Output Overvoltage Protection
- V_{BLK} Sensing Network Fault Detection
- V_{BLK} Over-Voltage Protection
- PFC and LLC Stage Soft-Start
- PFC Stage Frequency Dithering
- Thermal Shutdown

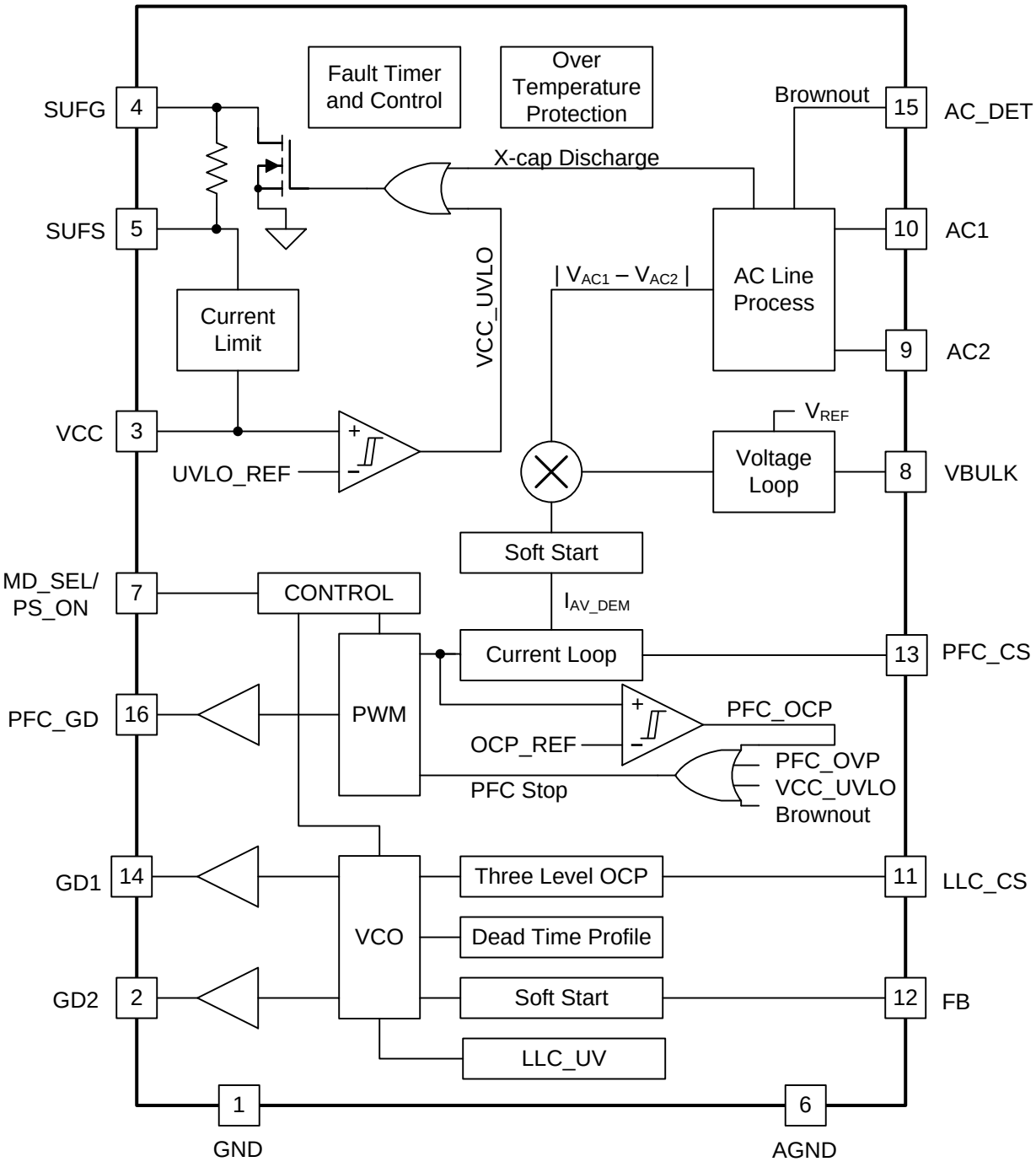
The UCC29950 implements an advanced control algorithm to control the PFC stage input current. This proprietary hybrid method combines both average and peak-mode control methods.

- Accurate control of the average current drawn from the line gives good THD.
- Peak inductor current information is used to terminate each PFC switching cycle.
- The algorithm is insensitive to variations in the peak-to-average current ratio.

The input current is accurately controlled so that it follows the correct sinusoidal shape and also gives inherent cycle-by-cycle protection against excess MOSFET current. A further advantage is that the control loop is insensitive to PFC inductor and bulk capacitor variations. The UCC29950 takes full advantage of this fact to implement internal compensation of the PFC stage. This simplifies the system designer's task and reduces the external component count. A sophisticated soft-start algorithm is used to achieve a constant soft-start ramp time over a wide range of bulk capacitor values and initial conditions.

An LLC stage is typically used to convert the PFC stage output to an isolated final voltage for system use. The UCC29950 provides all the primary-side functions needed to control such a second stage. The input to the FB pin is an isolated control signal from the output. This signal is fed into a voltage-to-frequency converter (VCO). The VCO inserts an appropriate dead time and the resulting signals are routed through some on-chip drivers connected to the GD1 and GD2 outputs. The dead time is shortest at low LLC frequencies and is increased automatically as frequency is increased. A three level Over-Current Protection (OCP) function stops the GD1 and GD2 signals if the current signal at the LLC_CS pin goes outside of a defined current vs time profile.

7.2 Functional Block Diagram



7.3 Feature Description

Table 1. UCC29950 Features and Benefits

Feature	Benefit
Self-Bias Mode allowing off-line operation	Eliminate cost of Auxiliary Flyback Bias supply in system
Control output for external high-voltage, depletion mode start-up MOSFET	Eliminates drop resistor from rectified AC line, reduces stand-by power
Integrated X-Cap discharge function using external start-up MOSFET	Eliminates bleed resistor across differential EMI filter capacitor, reduces stand-by power
PFC stage design in 3 easy steps - (i) design voltage feedback network, (ii) choose current sense feedback resistor, (iii) design power stage	Greatly simplifies design effort
Advanced control algorithm for PFC Stage	Good iTHD and insensitivity to inductor and bulk capacitor variations, Cycle by cycle PFC overcurrent protection
Internal compensation of PFC Stage Voltage and Current feedback loops	Reduces Component count, eliminates 2 design steps (voltage and current loop compensation)
Differential AC Line sensing with fixed 9.3M-ohm resistors	Accurate measurement of line conditions under no-load or start-up conditions for improved performance and protection - Eliminates 1 design step (AC line sensing)
PFC frequency dithering	Simplifies EMI filtering and eases EMI compliance
True input power limit, independent of line voltage	Limit set by choice of $R_{CS(pfc)}$ allowing designer greater flexibility compared to fixed limits that depending on AC line voltage
Zero Voltage Switching (ZVS) over a wide range of operating conditions	Reduced switching losses in the LLC converter power devices
Three Level over current protection for LLC and Hiccup mode of operation	Allows the power stage to ride through a short-term transient overload but reacts quickly to protect the power stage from heavy overload or output short-circuit events.

7.3.1 Sense Networks

The UCC29950 uses fixed scaling factors to measure the signals at its pins. The circuit position of the voltage sensing resistors is shown in Figure 9. The current sensing resistors are shown in Figure 13.

The resistors in the V_{BLK} sensing network, R_{TOP} and R_{BOT} in Figure 9 have been chosen to minimize the power dissipation and ensure correct operation over the expected tolerance bands. The impedance in this network may be reduced by choosing lower value resistors provided that the potential division ratio is unchanged or kept within the limits given below.

The nominal ratio is 30 MΩ/73.33 kΩ = 409.28. This has been chosen to give a nominal V_{BULK} regulation setpoint of 385 V. This voltage is the ideal operating point for the PFC. It prevents direct conduction into the bulk capacitor at high line and prevents false OVP tripping due to load transients - especially under high load conditions where the voltage ripple on the bulk capacitor is maximum. It is possible to change the nominal setpoint within the limits below.

If the ratio is increased above the nominal value then there is a risk of triggering a sense network fault condition at startup - as described in the next section. The maximum ratio is not an absolutely fixed value but is likely to be about 425 with a corresponding V_{BULK} regulation setpoint of 400 V. The minimum ratio is governed by the desire to avoid direct conduction into the bulk capacitor when operating at high line. V_{BULK} must be greater than 374 V to avoid this condition on a 264 VRMS line. The corresponding minimum ratio is about 395.

Table 2. Sensing Resistor Values

RESISTOR	DESCRIPTION	MIN	TYP	MAX	UNIT
R_{L1} and R_{L2}	1% tolerance parts are recommended. To meet voltage ratings, it may be necessary to split the resistance across more than one part.	9.21	9.30	9.40	MΩ
R_{TOP}	1% tolerance parts are recommended. To meet voltage ratings, it may be necessary to split the resistance across more than one part.	29.7	30.0	30.3	
R_{BOT}	1% tolerance parts are recommended. A parallel combination of a 75-kΩ and a 3.3-MΩ resistor gives a nominal 73.33 kΩ	72.50	73.33	74.07	kΩ
$R_{CS(pfc)}$	Value depends on system power level and is given by Equation 59		33		mΩ
$R_{CS(llc)}$	Value depends on system power level and is given by Equation 36		400		

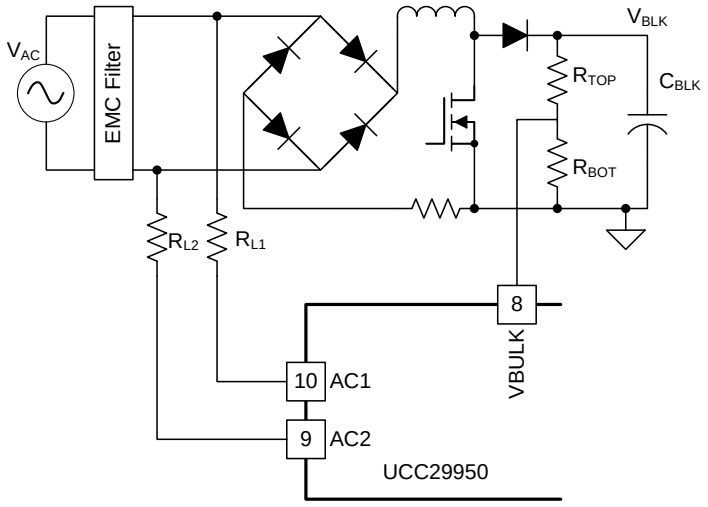


Figure 9. Voltage Sensing Network

7.3.2 Sense Network Fault Detection

In a boost converter, there is a direct conduction path from AC line to the bulk capacitor which ensures that it will be charged to peak of line even if the PFC stage controller is inactive. At start-up the UCC29950 measures AC line voltage and the voltage on the PFC bulk energy storage capacitor. If the UCC29950 measures V_{BLK} to be lower than V_{AC} it enters a latched fault condition. This feature prevents the PFC stage from running if the upper resistor in the voltage sensing network has gone open circuit. If the lower resistor has gone open circuit, then the UCC29950 detects this as an over-voltage event on the output and PFC switching will not start.

7.3.3 PFC Stage Soft-Start

The UCC29950 soft-start will typically charge the PFC boost capacitor within 50 ms to 100 ms of starting.

7.3.4 AC Line Voltage Sensing

The UCC29950 uses differential AC line sensing through its AC1 and AC2 pins. Differential sensing provides more accurate measurements than single ended sensing, especially at startup and under light load conditions. It also allows faster detection of AC line disconnection or failure.

Normal single ended sensing assumes that the diodes connected to the negative going AC line are forward biased and that a single measurement of the positive going AC line is a true representation of the input voltage. This is normally true but if there is no current being drawn, as is the case under no-load or start up conditions, then it is possible that all the diodes in the bridge are reverse biased. If this happens then a single ended measurement will overestimate the true AC line voltage. The differential AC line sensing used in the UCC29950 avoids these errors.

The external resistor value impedance for AC1 and AC2 is required to be 9.3 MΩ. This reduces the static power dissipation and provides the correct divider ratio in conjunction with the GAIN and OFFSET factors of the device, (see Equation 1).

These factors are set at the time the UCC29950 is tested. They are used to compensate for device to device variations in R_{AC1} and R_{AC2}.

$$VAC = |AC1 - AC2 - OFFSET| \times GAIN \quad (1)$$

AC1 and AC2 must be connected to the AC line side of the bridge rectifier through 9.3-MΩ resistors. The high impedance sensing network is effectively a current source which is why the levels in the electrical characteristics table are given in terms of currents rather than voltages. The equivalent voltages are given in Table 3.

The 9.3-MΩ resistors must be able to support the full voltage at peak of AC line and are conveniently made from three 3.09-MΩ resistors in series. It is recommended to minimize the length of track between the ACx pins and the lowest resistor in the chain.

Table 3. PFC AC Line Voltage Action Levels(1)

VOLTAGE		PARAMETER	MIN	TYP	MAX	UNIT
$V_{AC(det)}$	AC_DET will be active HIGH when VAC is below this level	$I_{AC(det)}$	65.5	70	74.5	V_{RMS}
$V_{AC(low\_falling)}$	PFC stage stops 100 ms after VAC is at or below this level	$I_{AC(low\_falling)}$	65.5	70	74.5	
$V_{AC(low\_rising)}$	PFC stage is allowed to start when VAC is at or above this level	$I_{AC(low\_rising)}$	75	80	85.2	
$V_{AC(high\_falling)}$	PFC stage restarts if VAC falls below this level	$I_{AC(high\_falling)}$	287	300	313	
$V_{AC(high\_rising)}$	PFC stage stops if VAC is at or above this level	$I_{AC(high\_rising)}$	297	310	323	
$V_{AC(halt)}$	PFC and LLC stages stop if VAC is at or above this level	$I_{AC(halt)}$	306	320	333	

(1) Based on parameter values in Electrical Characteristics table and calculated assuming 9.3 MΩ resistors in AC1 and AC2 lines. The relative levels of these action levels track each other.

7.3.5 V_{BLK} Sensing

V_{BLK} is sensed through a potential divider with a resistance of 30 MΩ between the VBULK pin and V_{BLK}. The bottom resistor in the potential divider is 73.3 kΩ. The 30 MΩ resistor has to support the full V_{BLK} voltage and it is normal to split this resistance into three separate parts of 10 MΩ each. As noted in Sense Network Fault Detection the UCC29950 will not start the power stages if it detects that V_{BLK} is less than peak of VAC. Because of the high impedance nature of the sensing network it is recommended to minimize the length of track between the VBULK pin and the lowest resistor in the sensing chain.

7.3.6 AC Input UVLO and Brownout Protection

The UCC29950 provides full brownout protection and will not react to single-cycle AC line dropouts. While the PFC stage is running the controller checks each AC line half-cycle. A valid AC line input is detected if the peak voltage during an AC line half-cycle is greater than the brownout level (equivalent to 70 V_{RMS}). The AC_DET output goes high if no valid AC line input is detected for a period greater than 32 ms and both the PFC and LLC stages stop operating 100 ms later.

NOTE

The LLC stage always stops immediately if VBULK falls below $V_{BULK(llc\_stop)}$.

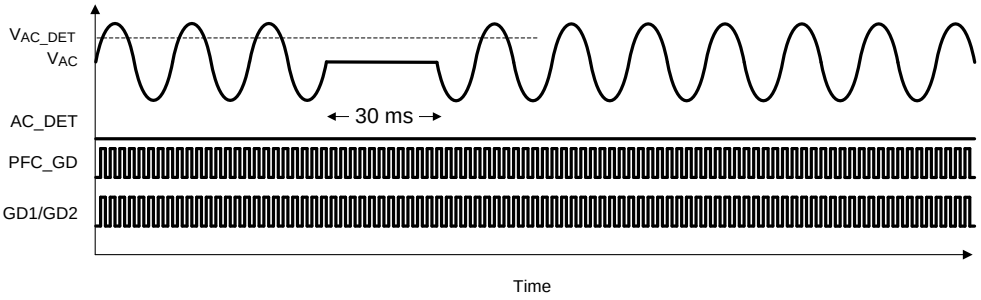


Figure 10. AC Line Dropout

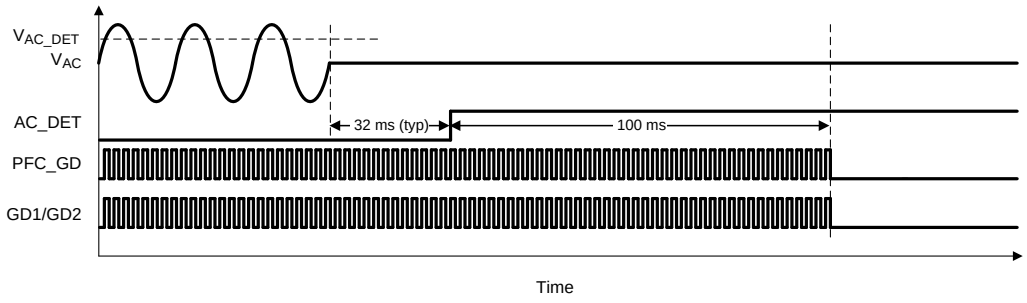


Figure 11. AC Line Disconnect

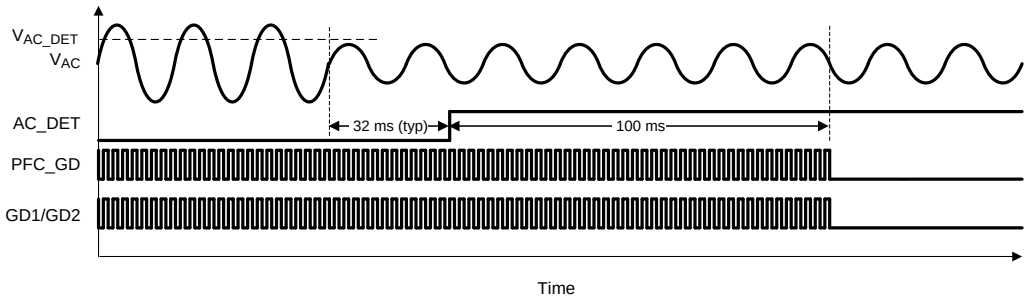


Figure 12. AC Line Brownout

7.3.7 Dither

The PFC stage switching frequency is stepped between three discrete frequencies at a rate of 333 Hz. The frequencies are spaced at nominal 2-kHz intervals. The dither rate is selected to avoid harmonics of the major AC line frequencies. Dither is effective in reducing the average EMI level and also reduces the quasi-peak levels but to a lesser extent.

7.3.8 Active X-Cap Discharge

If the Active X-Cap discharge function is to be used, the drain of the start-up FET must be connected to the AC side of the bridge rectifier, as shown in Figure 20. The X-Cap is discharged by bringing SUFG low to turn the start-up FET on. The discharge path is then through the startup FET, via the SUFS pin and into C_{VCC}.

NOTE

A Zener diode should be used to clamp VCC and prevent multiple X-Cap discharge events from over charging the capacitor. This Zener diode should be 18V rated device in Self-bias applications. A lower voltage Zener could be used in Aux bias applications, providing that the Zener voltage is greater than the normal operating VCC rail voltage.

When the AC line is removed the UCC29950 detects that the zero voltage crossings on V_{AC} have ceased. If the PFC stage is running at that time then the X-Cap is discharged through the switching action of the PFC stage and no further action is needed. If the PFC stage is not running at the time of disconnection, perhaps because MD_SEL/PS_ON is held low or VBULK is > $V_{BULK(reg)}$, then SUFG is set high if $VC_{X\text{-}Cap}$ (the voltage on the X-Cap) is greater than 42 V and the X-Cap is discharged. If $VC_{X\text{-}Cap}$ is < 42 V then it is regarded as being at a safe level, discharge is not needed and SUFG is not set high. The X-Cap is always discharged within the 1 s allowed by the safety standards but there may be up to 300 ms delay or latency in SUFG operation if the controller is operating in burst mode, for example at light loads. The UCC29950 makes the decision to set SUFG high based on the voltage on the X-Cap at the end of this latency period.

7.3.9 LLC Stage Soft Start

The LLC stage soft-start ramps the LLC gate drive frequency from min period ($1/LLC_{F(max)}$) to max period ($1/LLC_{F(min)}$) over a 100-ms interval. The ramp is terminated when the voltage at the FB pin is such that it would command a higher frequency than the ramp. The first pulse from the GD1 output is half width.

7.3.10 PFC Stage Current Sensing

The UCC29950 controls the average current in the PFC inductor. This means that the current sense signal at the PFC_CS pin must represent the inductor current during the full PFC switching cycle. That is when the MOSFET is ON and also when the MOSFET is OFF. This is achieved by putting the current sensing resistor, $R_{CS(pfc)}$, in the position shown in Figure 13 and Figure 34.

NOTE

The current sense signal, V_{CS_PFC}, is negative going, so the signal goes more negative as the inductor current increases.

The current sensing resistor is on the input current return path and inrush currents flow through it. These may generate large voltage drops on the current sense resistor. These voltages may be higher than the negative voltage rating on the PFC_CS pin. A resistor, recommended value = 1 kΩ, between the current sensing resistor and the PFC_CS pin is used to avoid over stressing the device. Signal diodes may be necessary to provide additional clamping. A small filter capacitor may be useful to further reduce the noise level at this pin but be careful that this part does not significantly attenuate the ripple component of the current sense signal. These components are shown in Figure 13.

The current drawn from the AC line is limited so that the peak voltage on the PFC_CS pin, ignoring PFC stage switching ripple, does not exceed –225 mV, $V_{TH(PFCCS(cav\_max))}$, as shown in Figure 6.

There is a second current limit point at $V_{PFCCS(max)}$ and the peak voltage at the PFC_CS pin should not be allowed to exceed this limit (–570 mV). The operation of this second current limit is explained later. The PFC current sense resistor ($R_{CS(pfc)}$) value needed can be calculated using Equation 59.

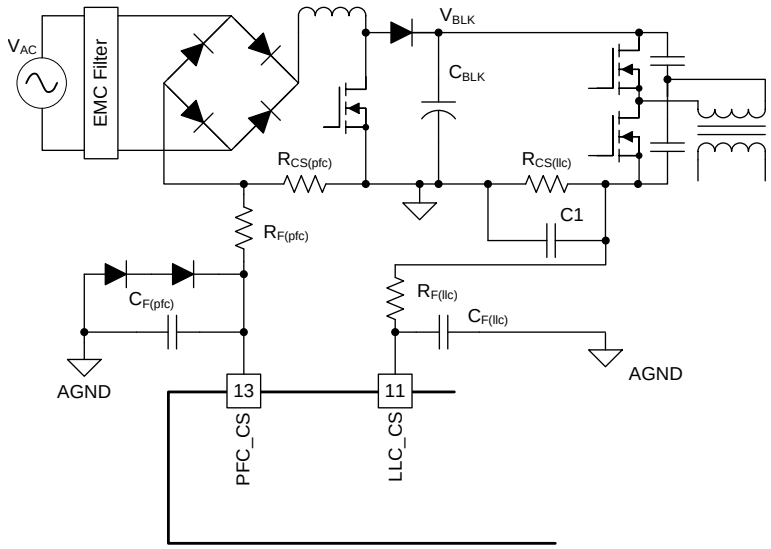


Figure 13. Current Sensing Connections

7.3.11 Input Power Limit

The UCC29950 has a true input power limit which limits the PFC stage power at a level which is independent of the AC line voltage. This is more useful than a simple fixed input current limit where the power would be limited at different levels depending on the AC line voltage. The power limit is set by the choice of $R_{CS(pfc)}$ according to Equation 59.

7.3.12 PFC Stage Soft Start

When the power system is first connected, the bulk capacitor charges to the peak value of the AC line voltage. The PFC stage soft-start process first calculates the current needed to charge the bulk capacitor from this initial stage to the regulation setpoint (VBULK at $V_{BULK(reg)}$) in a nominal 50 ms. This is an approximate calculation based on a bulk capacitance of 0.8-µF per watt and varies if a larger or smaller capacitor is used. The PFC stage is then started using this current limit value.

7.3.13 Hybrid PFC Control Loop

The UCC29950 controls a continuous-conduction mode PFC stage by using a novel method combining average current-mode control with peak-current sensing. Among other advantages, this method eliminates the peak-mode line current distortions due to a varying peak-to-average current ratio. The average current is used to control the average value of the PFC inductor current and the peak current is used to terminate each PWM cycle and provide high bandwidth, cycle-by-cycle current control or limiting. Good power factor is achieved by forcing the average input current to follow a demand signal that is derived from the AC line voltage.

Traditional current-mode control systems require resistor and capacitor compensation components to shape the system response. It is difficult to integrate these components into a semiconductor chip and external parts must be used. The UCC29950 avoids the need for external compensation networks by implementing the average portion of the control loop digitally. The entire outer-voltage control loop is digital and the required slow response is easily achieved without the need for external parts. This mixed signal approach uses digital methods for low-frequency compensation and analog op-amps and comparators for the actual PWM duty-cycle generation.

The input AC line voltage is sensed differentially through the AC1 and AC2 pins, as shown in Figure 14. Differential sensing allows more accurate measurement of the AC line voltage over the entire input power range, including no load, than single ended sensing. The output of the voltage loop is multiplied by the instantaneous line voltage, $|V_{AC1} - V_{AC2}|$, to give an average current demand signal, $I_{AV(dem)}$, for the current loop. The $I_{AV(dem)}$, the voltage loop and $|V_{AC1} - V_{AC2}|$ signals are all implemented digitally. The voltage loop provides correct compensation over the expected range of bulk capacitor values, based on a capacitance to power ratio between 0.5 µF W^{-1} and 2.4 µF W^{-1}. This eliminates the need for external compensation components and simplifies the design task.

The current-demand signal normally has a rectified sinusoidal shape. The current-loop output is used to program a duty cycle which is then sent to the PFC_GD pin through a driver. The minimum duty cycle is 0% at which point the PFG_GD output is kept low for the entire switching cycle. The maximum duty cycle for the PFC_GD output is at least 92%.

NOTE

The maximum duty cycle is imposed by the PWM block independently of the input from the current loop and does not depend on inputs from the current loop or elsewhere.

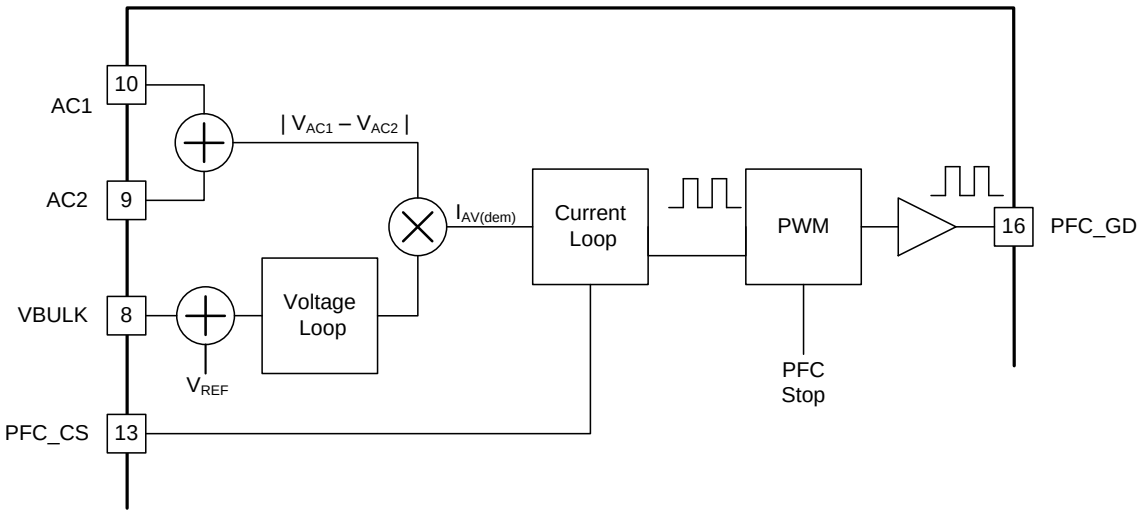


Figure 14. PFC Control Loop

The inner current loop uses a hybrid mixed signal control method as shown in Figure 15. The $I_{AV(dem)}$ signal (digital average current demand) is converted to an analog form and summed with the sensed current signal I_{CS} by the unity gain inverting amplifier, A1. The current sensed is the total inductor current which means that the sensing resistor must be placed in the negative return as shown in Figure 13. The $I_{AV(dem)}$ signal is positive going, greater $I_{AV(dem)}$ values commands larger currents. The signal at the PFC_CS pin is negative going so that larger currents give a more negative signal level. The action of the control loop is to keep the inverting and non-inverting inputs to A1 at the same level (450 mV). The output of the A1 amplifier contains both average and peak-inductor current information. The average level at the A1 amplifier output is extracted by the ADC and digital filter shown in the block called A2 in Figure 15. This average level is then subtracted from the fixed PWM ramp coming from the waveform generator. The result is converted into an analog signal by the DAC and sent to the inverting input of the fast analog PWM Comparator. The comparator ramp has an offset which is a function of the digital-filter output. This offset value moves up and down in response to changes at the A1 output. The comparator ramp at the inverting input is negative going and that at the non-inverting input is positive going. This increases the noise immunity of the comparator making an incorrect, early termination of the cycle is less likely.

If the $I_{AV(dem)}$ signal increases, for example in response to an AC line voltage or load change then the average output of the A1 amplifier initially decreases by the same amount. The PWM duty cycle, and inductor current, will then increase because as $V_{A1(out)}$ moves negative, it takes longer for the two signals at the comparator inputs to intersect and terminate the cycle. The digital-filter output also increases in response to the change in $V_{A1(out)}$ according to its frequency response characteristic and the average value of the comparator ramp moves negative. This tends to reduce the PWM duty cycle. Eventually, as the PFC inductor current increases the $V_{A1(out)}$ signal returns to its equilibrium point at 450 mV. The digital filter dynamically adjusts its output up or down so as to keep the average value of the comparator ramp at the level where $V_{A1(out)}$ is kept at 450 mV. The overall effect is that a unipolar sinusoidal demand signal is translated into a unipolar sinusoidal PFC inductor current.

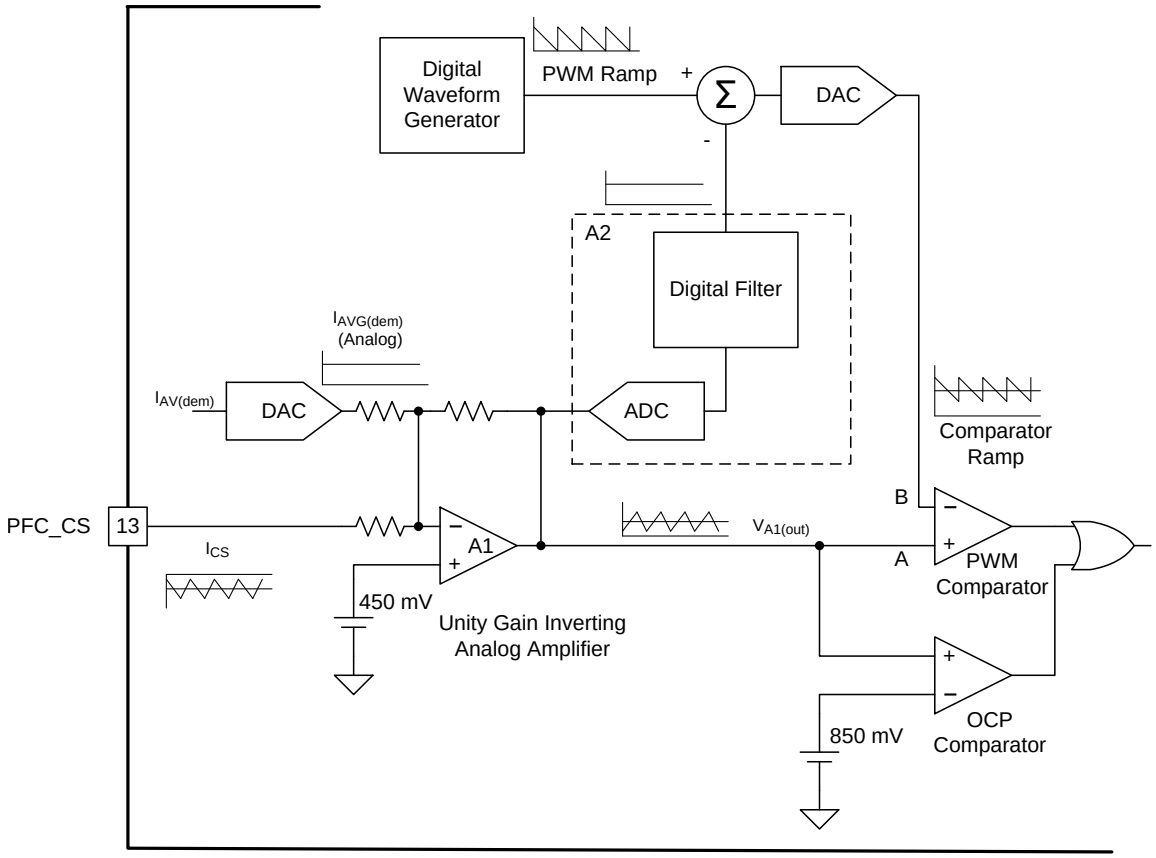


Figure 15. UCC29950 Hybrid Current-Mode Control

7.3.14 PFC Stage Second Current Limit

An individual PFC switching cycle is normally terminated by the PWM Comparator. If for some reason the PWM Comparator fails or has stopped operating then there is a second comparator monitoring the output of the A1 amplifier (OCP Comparator in Figure 15). The OCP comparator turns the PFC MOSFET off and provides an additional protection function for the devices in the power train.

If the output of A1 reaches 850 mV then the OCP comparator trips. Two actions follow:

1. The existing PWM cycle is terminated immediately.
2. Both the PFC and LLC stages shut down for 1 s followed by a re-start.

7.3.15 PFC Inductor and Bulk Capacitor Recommendations

The CCM Boost converter current-mode control loop is insensitive to PFC inductor value and can operate over a wide range of inductance values. The inductor value in a given application is a trade off between ripple current, physical size, losses, cost and several other parameters. For example, in Detailed Design Procedure for the PFC stage a value of 600 µH for a 300-W application is chosen.

The hybrid control loop has been designed to be stable for any bulk capacitance between 0.5 µF W^{-1} and 2.4 µF W^{-1}. For a 300-W application, this would allow the use of a bulk capacitance between 150 µF and 720 µF. These limits on PFC inductance and bulk capacitance are conservative.

7.3.16 PFC Stage Over Voltage Protection

In normal operation the PFC stage control loop in the UCC29950 regulates the PFC stage output voltage (V_{BLK}) such that the voltage at the VBULK pin is held at $V_{BULK(reg)}$. If the recommended sensing network is used then this corresponds to 385 V on the bulk capacitor. If the voltage at the VBULK pin exceeds $V_{BULK(ovp)}$ the PFC stage is stopped immediately. It restarts once VBULK falls back to the $V_{BULK(reg)}$ level. The OVP level corresponds to 450 V at the PFC bulk capacitor. This protects the PFC stage against over stresses due to rapid increases in V_{BLK}, occurring if an AC line surge event were to happen. The LLC stage continues to operate in order to load and discharge the bulk capacitor. The OVP response is immediate, of the order of 100 µs, and is more rapid than the response of the normal PFC voltage control loop.

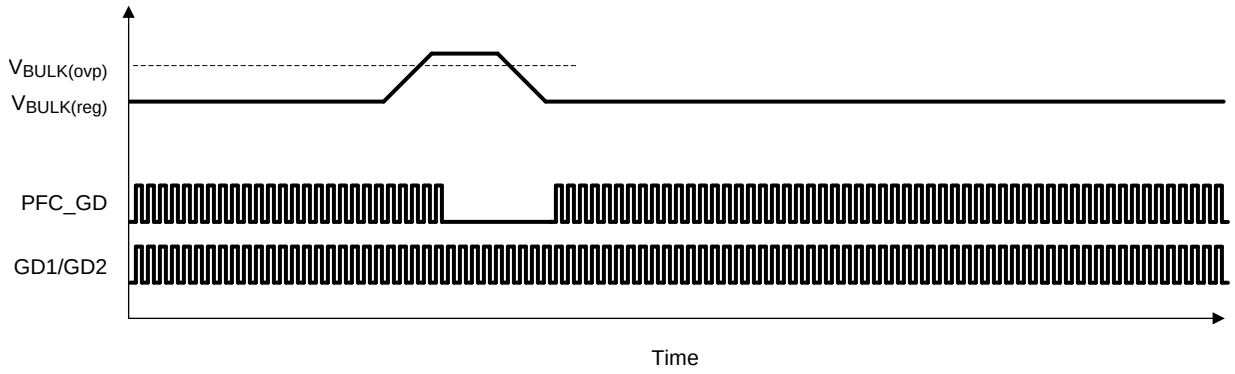


Figure 16. VBULK Over-Voltage Protection

7.3.17 LLC Stage Control

The UCC29950 has three pins dedicated to the control of an LLC power stage, the two gate drives GD1 and GD2, and the feedback pin, FB. If the controller is operating in Aux Bias Mode then the MD_SEL/PS_ON pin may also be used to turn the LLC stage on or off. The UCC29950 includes an on chip Voltage to Frequency Converter (VCO) which converts the voltage on the FB pin into a square wave at the desired frequency according to the graph in Figure 1. The basic response time of the voltage to frequency conversion process is typically less than 40 µs. This means that the overall response of the LLC power system is dominated by the other components in the loop, for example, the opto-coupler and error amplifier on the output , rather than by the UCC29950. Inverted and non-inverted versions of the square wave are produced and a dead time is added. The dead time added is a function of the frequency being generated according to the graph in Figure 2. The signal is then passed to the on-chip drivers connected at the GD1 and GD2 pins. The duty cycles of the GD1 and GD2 signals are highly symmetrical, typically they match to better than 0.1%.

The first and last LLC gate drive pulses are normally half width and appear on GD1 and GD2 respectively. The half width pulses reduce any DC flux in the transformer at start up or shutdown. If the LLC_OCP3 level is exceeded then the final pulse is of normal width.

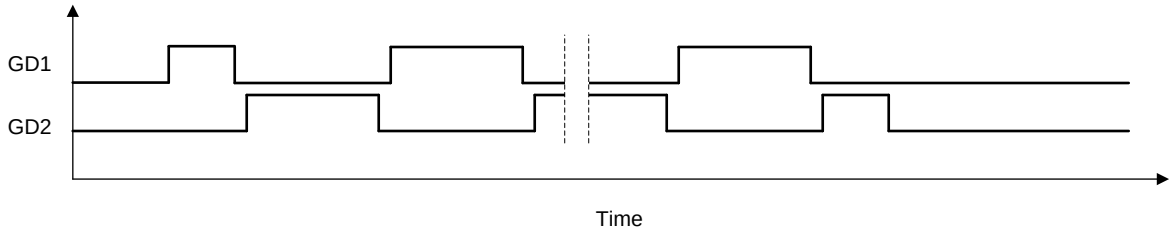


Figure 17. LLC GD1 and GD2 Start and Stop

7.3.18 Driver Output Stages and Characteristic

The output stage pull-up features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The function of the N-Channel MOSFET is to provide an increased sourcing current enabling fast turn-on, as it delivers the highest peak-source current during the Miller plateau region of the power-switch turn-on transition, when the power switch drain or collector voltage experiences high dV/dt. The N-Channel device can pull the driver output to within one threshold voltage drop of the V+ rail. The P-Channel device can pull the driver output all the way to V+.

The effective resistance of the UCC29950 pull-up stage during the turn-on instant is therefore lowest during the time when the highest current is needed. The pull-down structure in UCC29950 is composed of an N-Channel MOSFET which can pull the output all the way to GND.

The structure in Figure 18 is used in the output circuit of the low power driver used to output the AC_DET signal. It has the same pull up characteristics, but at an impedance level more suitable for driving a signal level load such as an optocoupler LED.

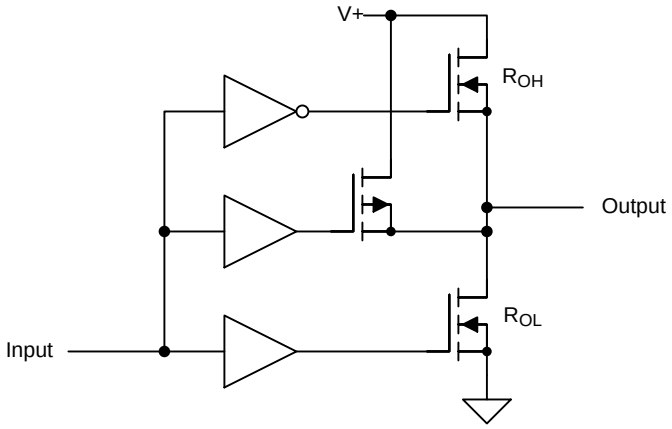


Figure 18. Driver Output Stage (simplified)

7.3.19 LLC Stage Dead Time Profile

The UCC29950 programs a dead time into the LLC gate drive outputs (GD1 and GD2) which follows the profile shown in Figure 2. The dead time is longest at high frequencies because the currents in the resonant tank circuit are less and so the stray capacitances at the switched node take longer to swing from one rail to the other. At low frequencies the opposite is true, the currents in the resonant tank are greater and the switched node swings more quickly.

7.3.20 LLC Stage Current Sensing

The UCC29950 uses primary-side current sensing to monitor the output current. This has the advantage that current limiting can be implemented without having to bring a current limit signal across the primary-to-secondary isolation barrier. Also, assuming that the output voltage of the LLC stage is lower than the input, the currents in the primary circuit are lower than those in the secondary. This allows a larger value of sensing resistor to be used without incurring excessive power dissipation. One side effect of sensing on the transformer primary is that the sensed current includes start up charging currents onto the LLC stage output capacitance. The three level OCP feature allows this charging current to flow without tripping a fault. Even if the current sensing were done on the secondary side and outboard of the LLC stage output capacitance there may still be additional, off-board capacitance whose charging current does flow in the sensing resistor.

7.3.21 LLC Three Level Over-Current Protection

The UCC29950 uses the LLC stage input current to represent the output current. The value of the LLC current sense resistor that should be used is given by Equation 36.

Three levels of overcurrent protection as shown in Figure 19, are provided to allow the UCC29950 to react in a flexible manner to an over current event. $V_{CS(ocp1)}$ and $V_{CS(ocp2)}$ faults are triggered after a short delay. $V_{CS(ocp3)}$ level faults are acted on immediately.

Table 4. LLC Stage Over-Current Protection Levels

OCP PARAMETER	DESCRIPTION	VALUE
$V_{CS(ocp1)}$	First overload detection level. If this threshold is exceeded for t_{OCP1} then both the PFC and LLC stages will shut-down. Restart with a normal soft-start sequence after $t_{LONG(fault)}$ (1 s typ).	133% of $V_{CS(llc\_max)}$. Typically 400 mV
t_{OCP1}		52 ms
$V_{CS(ocp2)}$	Second overload detection level. If this threshold is exceeded for t_{OCP2} then both the PFC and LLC stages will shut-down. Restart with a normal soft start sequence after $t_{LONG(fault)}$ (1 s typ).	200% of $V_{CS(llc\_max)}$. Typically 600 mV
t_{OCP2}		10 ms
$V_{CS(ocp3)}$	Third overload detection level. If this threshold is exceeded for t_{OCP3} then both the PFC and LLC stages will shut-down. Restart with a normal soft start sequence after $t_{LONG(fault)}$ (1 s typ).	300% of $V_{CS(llc\_max)}$. Typically 900 mV
t_{OCP3}	This is the time the UCC29950 takes to react to a level three overload voltage at the LLC_CS pin. Board level filtering can reduce the signal rise time at the pin and significantly increase the overall reaction time.	<5 µs

If any of these over-current protection events occurs the controller enters a hiccup mode of operation and it tries to restart the power stages at 1-s intervals. This graduated response allows the power stage to ride through a short-term transient overload but reacts quickly to protect the power stage from heavy overload or output short-circuit events.

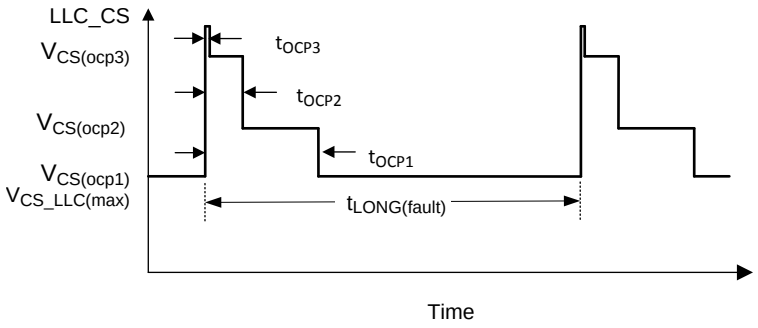


Figure 19. UCC29950 Output Over-Current Protection Profile

7.3.22 Over-Temperature Protection

If the UCC29950 junction reaches its T_{SD} (Thermal Shutdown Temperature) it stops both the PFC and LLC stages. The device then cools down to its T_{ST} (Start / Restart Temperature). It then initiates a full soft start of both stages, provided that the other conditions for start up are met. An over-temperature protection event is treated as a long fault with a 1-s recovery time. The thermal inertia in the device package normally prevents the junction temperature from falling to T_{ST} within 1 s so that this 1 s fault time is not apparent to the user.

7.3.23 Fault Timer and Control

Three types of faults are recognized by the UCC29950:

- Latching
- Long with Auto Recovery (1 s)
- Short with Auto Recovery (100 ms)

A latching shutdown is triggered by the following events. VCC must be cycled off and on to reset these faults:

- V_{BLK} < Peak of AC line. (This can happen only if there is a fault in the V_{BLK} sensing network or an open circuit in the path between the line input and C_{BLK}. This condition is evaluated each time the UCC29950 turns on. It is not evaluated during normal operation.)
- At start-up the UCC29950 performs a cyclic redundancy check on its internal memory. If the device fails this check it stops immediately and will not attempt to start the power stages.

A long fault is triggered by any of the following events:

- LLC stage Over Current Protection
- PFC Stage Second Current Limit
- X-Cap Discharge (This reduces average power dissipation in the high-voltage depletion mode MOSFET)
- Over Temperature Fault (Thermal inertia increases the recovery time)

A short fault is triggered by any of the following events:

- VCC Under Voltage
- VAC < $V_{AC(low\_falling)}$ (Brownout)
- VAC > $V_{AC(high\_rising)}$

7.4 Device Functional Modes

7.4.1 Mode Selection

The UCC29950 may be operated in one of two modes. In Aux Bias Mode VCC is supplied from an external source. A small, separate fly-back supply is normally used for this purpose. Aux Bias Mode allows the user to turn both the LLC and PFC stages off or to run only the PFC stage or to run both PFC and LLC stages together and to run the system at no load if desired. In Self Bias Mode the VCC rail is powered from a small auxiliary winding on the LLC transformer and ON/OFF control of the PFC and LLC stages is not possible in Self Bias Mode.

7.4.2 Start-Up in Aux Bias Mode

A small external PSU is used to supply VCC in Aux Bias Mode. A 12-V 50-mA supply is normally sufficient but this does depend on system level factors such as the gate-driver circuitry used, the load presented by the switching MOSFETs and other factors.

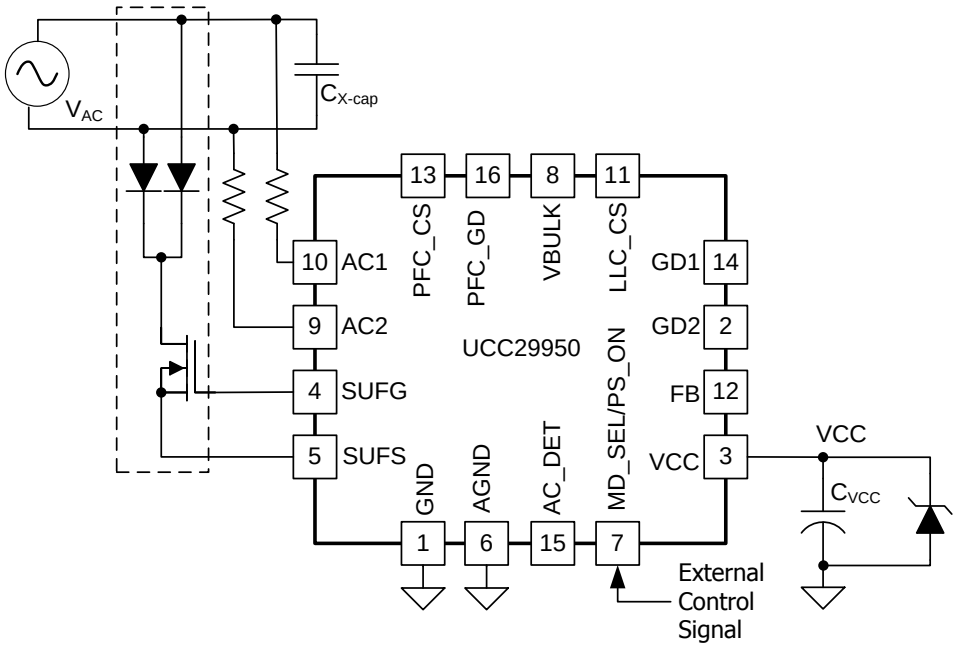


Figure 20. External Control Signal

Device Functional Modes (continued)

Aux Bias Mode is selected if the MD_SEL/PS_ON pin is kept lower than $V_{MODE(selsb)}$ for a time greater than $T_{MODE(sel\_read)}$ after VCC passes the VCC_{START} threshold. After this time has passed, the MD_SEL/PS_ON pin may be used to turn on the PFC stage alone by setting this pin to a voltage between the $V_{PS\_ONPFC\_RUN}$ and $V_{PS\_ONLLCPFC\_RUN}$ levels. The PFC and LLC stages may both be turned on by setting the MD_SEL/PS_ON pin to a voltage greater than $V_{PS\_ONLLCPFC\_RUN}$. Refer to the Electrical Characteristics table for the related tolerances on these thresholds.

The MD_SEL/PS_ON pin may be driven from an active source such as a comparator or digital output (with appropriate level shifting, provided by an optocoupler for example). A simple RC network may also be used if an active source is not available. Connect a capacitor from MD_SEL/PS_ON to AGND and a resistor from MD_SEL/PS_ON to VCC. The RC time constant should be chosen so that the voltage at the MD_SEL/PS_ON pin is less than V_{MODE_SELSB} 10 ms after VCC increases past $V_{CC(start)}$. Normally an RC time constant of 100ms will be satisfactory. The slow rise of the MD_SEL/PS_ON signal between the $V_{PS\_ONPFC\_RUN}$ and $V_{PS\_ONLLCPFC\_RUN}$ levels increases overall start-up time by a few 100 ms.

The normal sequence in a system is that V_{AC} is applied, MD_SEL/PS_ON is held low, VCC comes up and MD_SEL/PS_ON is then used to turn the PFC/LLC stages on as shown in Figure 21.

This sequence applies whether or not the X-Cap discharge function is being used.

Typical start-up times in Aux Bias Mode are in the range 150 ms to 250 ms after MD_SEL/PS_ON is brought high.

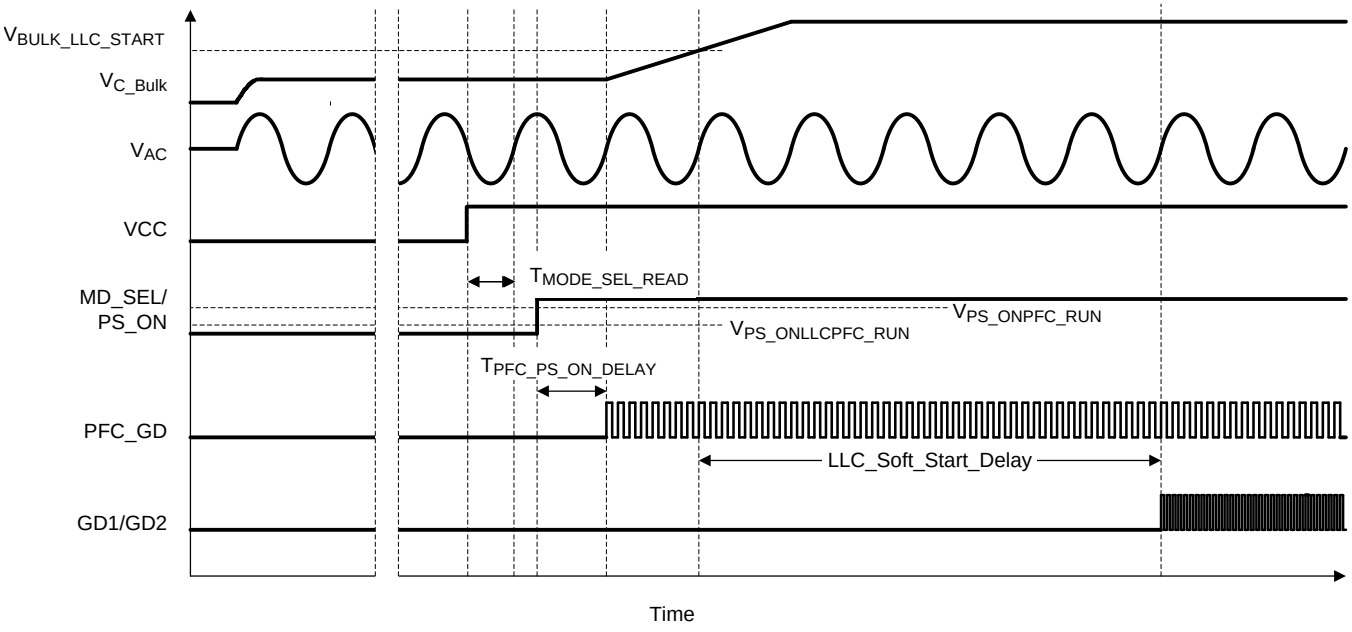


Figure 21. Typical Aux Bias Turn-On Sequence (both PFC and LLC stages are turned on simultaneously by pulling MD_SEL/PS_ON above $V_{PS\_ONLLCPFC\_RUN}$)

Device Functional Modes (continued)

7.4.3 Start-Up Operation in Self-Bias Mode

In Self Bias Mode, the MD_SEL/PS_ON pin should be tied to VCC as shown. The start-up FET is a normally on depletion mode device, a BSS126 for example. C_{VCC} is charged via the start-up FET and the internal current-limiting block. Initial charging of C_{VCC} happens automatically even though VCC is below VCC_{START}. When VCC reaches VCC_{START} the SUFG pin goes low, which turns the start-up FET off. If the MD_SEL/PS_ON pin is tied to VCC, the UCC29950 enters Self Bias Mode. SUFG goes high again to turn the start-up FET on again and allow C_{VCC} to charge further. When C_{VCC} has been charged to $VCC_{SB(start)}$ (typically 16.2 V) the start-up FET is turned off and providing that the current into the AC1 and AC2 pins is greater than $I_{AC(low\_rising)}$ and that the sensed V_{BLK} voltage is greater than peak of AC line the PFC stage is started. As noted earlier, an 18-V zener diode should be used to clamp the voltage on C_{VCC}. The switching operation of the PFC and LLC stage is maintained as long as C_{VCC} is above $VCC_{SB(stop)}$. Equation 2 allows the user to select the value of C_{VCC}.

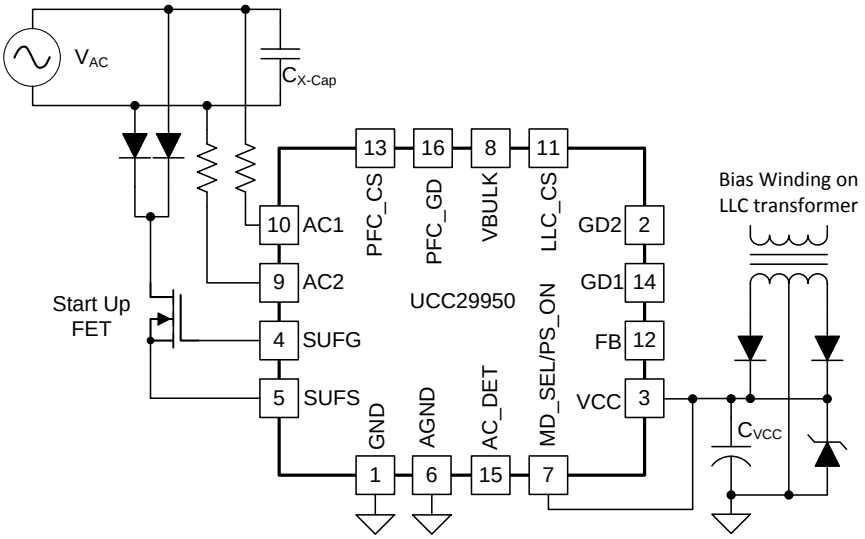


Figure 22. Self Bias Mode

Device Functional Modes (continued)

The start-up time in Self Bias Mode depends strongly on the current available for charging and on the capacitance on the VCC rail and. A first pass estimate of start-up time can be made using:

$$t_{SB(start)} \approx \frac{C_{VCC} \times VCC_{SB(start)}}{I_{SUFS}} + 200\ \text{ms} \quad (2)$$

For typical values, assuming C_{VCC} is 200 µF, t_{START} is therefore 1.8 s.

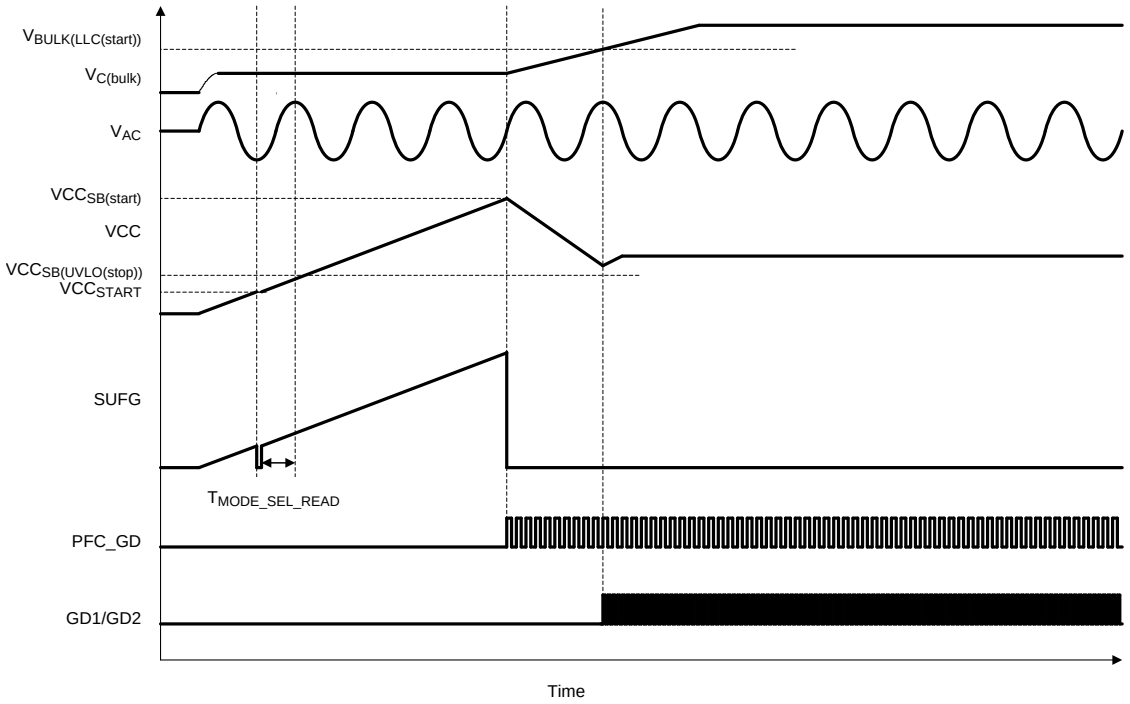


Figure 23. Typical Self Bias Turn-On Sequence

7.4.4 Bias Rail UVLO

The UCC29950 continuously monitors the voltage at its VCC pin. It stops both the PFC and LLC stages if VCC falls below $VCC_{AB(uvlo\_stop)}$ or $VCC_{SB(uvlo\_stop)}$, depending on whether it is operating in Aux Bias or Self Bias Modes respectively. In Aux Bias Mode, the device simply waits for VCC to recover to a voltage greater than $VCC_{AB(uvlo\_stop)}$. At which point it restarts. If it is operating in Self Bias Mode it sets SUFG HI to turn the start-up FET on. The current through the start-up FET then charges the capacitance on the VCC rail up to $VCC_{SB(start)}$ at which point the system tries to restart as described earlier.

7.4.5 LLC Stage MOSFET Drive

UCC29950 includes two high-power drivers that are capable of directly driving both MOSFETs in the half bridge LLC circuit through a suitable gate drive transformer as shown in Figure 24. Alternatively an external driver device, with its own high-side channel, can be used to interface between UCC29950 and half bridge MOSFETs as shown in Figure 25.

If a gate drive transformer is used then GD1 should be used to drive the high-side MOSFET and GD2 used to drive the low-side MOSFET. If a gate driver device is used then GD1 should be used to drive the low-side MOSFET and GD2 used to drive the high-side MOSFET. TI recommends the UCC22714 as a suitable gate driver device. The first and last LLC gate drive pulses are normally half width and appear on GD1 and GD2 respectively, see Figure 17.

Device Functional Modes (continued)

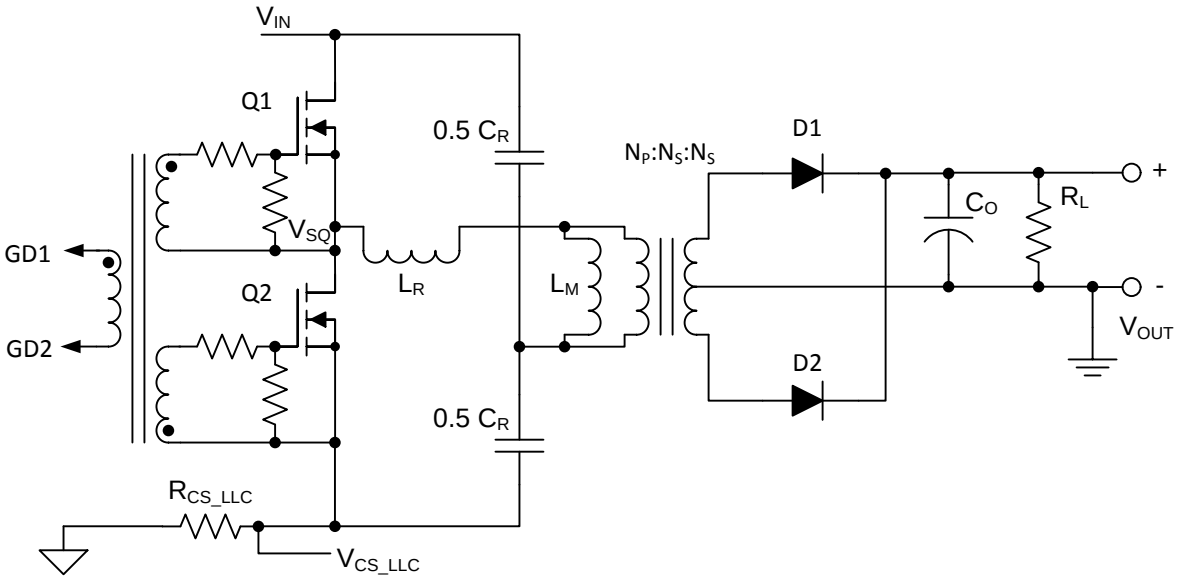


Figure 24. LLC MOSFET Gate Drive Using a Gate Drive Transformer (simplified)

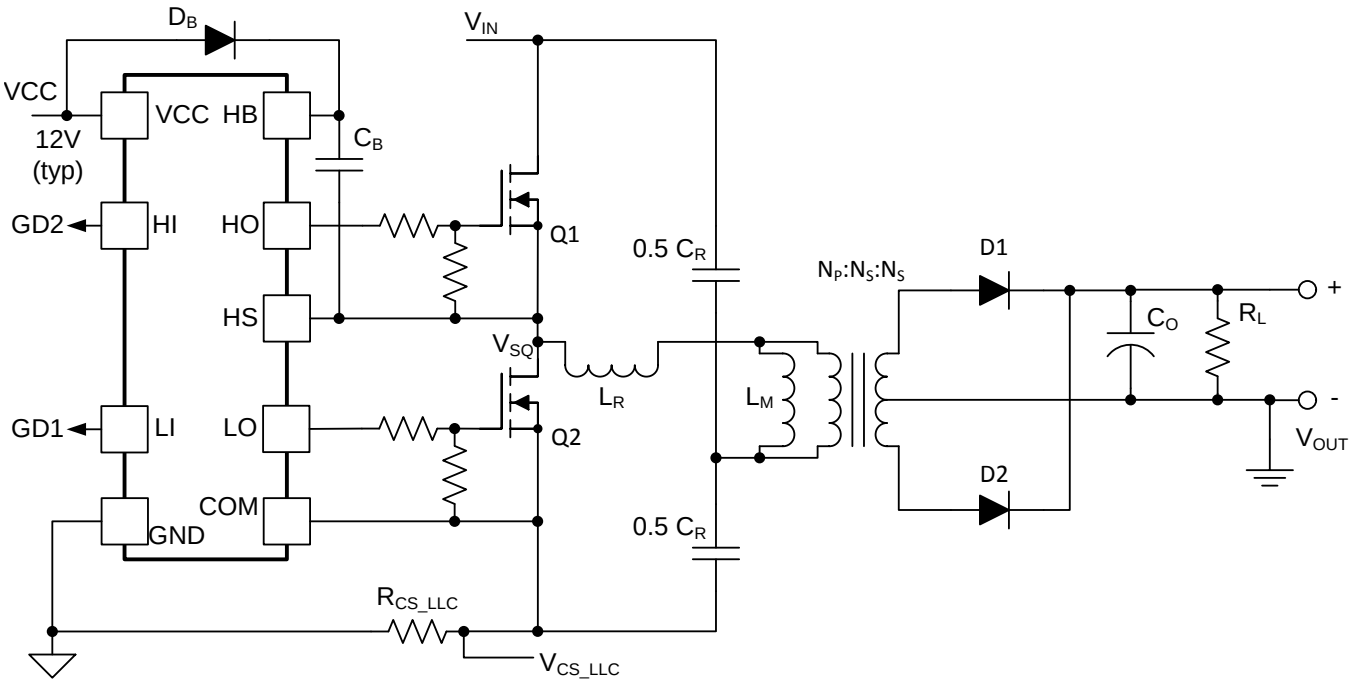


Figure 25. LLC MOSFET Gate Drive Using a Driver Device (simplified)

Device Functional Modes (continued)

7.4.6 Gate Drive Transformer

Gate driver transformers are robust and less susceptible to noise than gate drive devices but will also be larger than a solution using a gate driver device.

The GD1 and GD2 outputs from the UCC29950 are symmetrical, with 180˚ phase shift and a duty cycle less than 50%. If the gate drive transformer is driven as shown in Figure 24, then the waveform at its primary has no DC component. The gate-drive transformer must be able to support the maximum V sec product based on the GD1 and GD2 signal at LLC F_{MIN}. In steady state conditions, the duty cycles of GD1 and GD2 outputs are extremely well matched, typically within 0.1% of each other. When using a gate-drive transformer, the GD1 signal should be used to driver the high-side MOSFET and the GD2 signal used to drive the low-side MOSFET, as shown in Figure 24. The initial half-width pulse on GD1 and final half-width pulse on GD2 ensures that there is no DC flux imbalance on either the gate-drive transformer or in the main transformer see Figure 17.

The gate-drive transformer used to directly drive the LLC power MOSFETs should have a low common-mode capacitance. The common-mode current that flows from the upper-gate winding, back through the UCC29950 drivers, during bridge-switching transitions must return to the power circuit via the UCC29950 GND pin. Voltage disturbance on the GND pins during LLC bridge transitions may lead to audible interaction between the PFC and LLC power stages.

Placing a screen between the controller winding and gate-drive windings is one way to reduce the common-mode capacitance of the transformer. This screen should be connected to the source of the lower half-bridge MOSFET (Q2).

The gate-drive transformer should drive both the low-side and high-side MOSFETs as shown in Figure 24. This ensures that propagation delays through the transformer are matched and the symmetry of the dead time is maintained.

7.4.7 Gate Drive Device

A gate-driver device solution is less bulky than a gate-drive transformer and may be easier to design and layout. The capacitance from output to input is very low which means that interference from common-mode currents will not normally occur. In both Aux Bias and Self Bias Modes, the HO and LO outputs must make a clean transition between their active state (where they obey the HI and LI inputs) and their UVLO state (where they are latched low). Additionally, if operating in Aux Bias Mode it is very important to make sure that the UVLO level of the gate-driver device is less than that of the UCC29950 ($V_{CCAB\_UVLO(stop)}$). This ensures that the GD1 and GD2 signals are always passed on to the switching MOSFETs and that the UCC29950 maintains control of the LLC power train. It also ensures, if there is a UVLO condition on the bias rail, that the UCC29950 can enter and exit the UVLO condition correctly with a proper soft start during the recovery phase. In Self Bias Mode, it is not necessary that the driver UVLO is lower than that of the UCC29950, if the MOSFET gate drives stop for any reason then the bias always collapse to the UCC29950 $V_{CCSB\_UVLO(stop)}$ level, followed by a full restart as described in LLC Stage Soft Start.

High-side driver devices use a bootstrap capacitor, C_B in Figure 25, to supply the current to charge the gate of the high side MOSFET. This capacitor must first be charged to the driver high-side UVLO voltage before any HO pulses are delivered to the high-side MOSFET gate. C_B is charged during the first few LO pulses. Once the voltage across C_B reaches the high side driver UVLO level there is normally a short delay, 20 µs, before HO pulses appear. The current in the circuit during the first few switching cycles, when both high-side and low-side MOSFETs are being driven, will be higher than normal. The circuit designer must ensure that the LLC power-circuit components are rated for these stresses.

Device Functional Modes (continued)

7.4.8 Comparison

Users who employ a gate-drive transformer benefit from special features in UCC29950 to ensure a much smoother start-up transition of the LLC converter. This allows magnetics with a lower peak-current rating to be used safely. It is important to use a gate-drive transformer with a low common-mode capacitance.

If an external high-side driver is used then the smooth start-up feature is effectively disabled and the designer must ensure that the LLC magnetics are rated to cope with the resulting increased peak current during start-up.

Figure 26 compares the LLC resonant current waveform observed during the start-up transient. Both traces are triggered on GD1 output at the same point. The lower trace is observed when directly driving the LLC bridge MOSFETs via a gate drive transformer. The upper trace is observed when driving the LLC bridge MOSFETs via an external gate device driver. Vertical scale is 2 A/div. Horizontal scale is 10 µs/div.

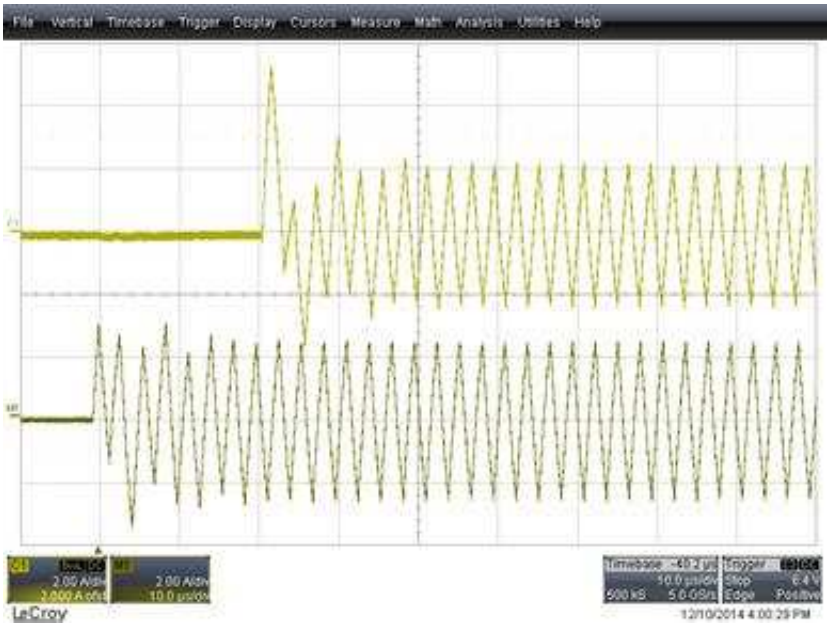


Figure 26. Typical LLC Transformer Primary Current During Startup

8 Application and Implementation

8.1 Application Information

The UCC29950 device is a highly-integrated combo controller. It is designed for applications requiring a CCM boost PFC input stage followed by an LLC output / isolation stage. The PFC loop is internally compensated and requires no external loop-compensation components. EMI filtering is simplified because the PFC stage operates at a fixed frequency with dither. A three level output overload protection current/time profile is included.

8.2 Typical Application

A typical application for this device would be in a 300-W, universal input isolated PSU with a 24-V (12.5-A) output.

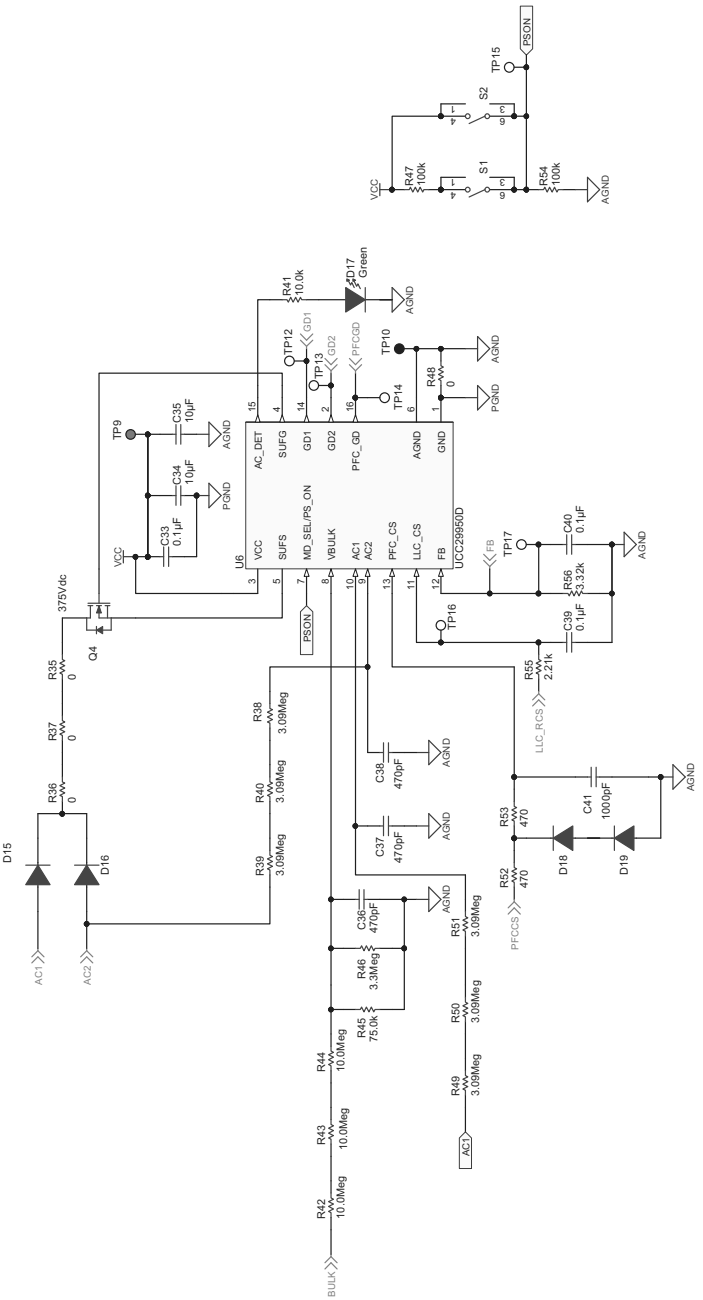


Figure 27. Controller Application

Typical Application (continued)

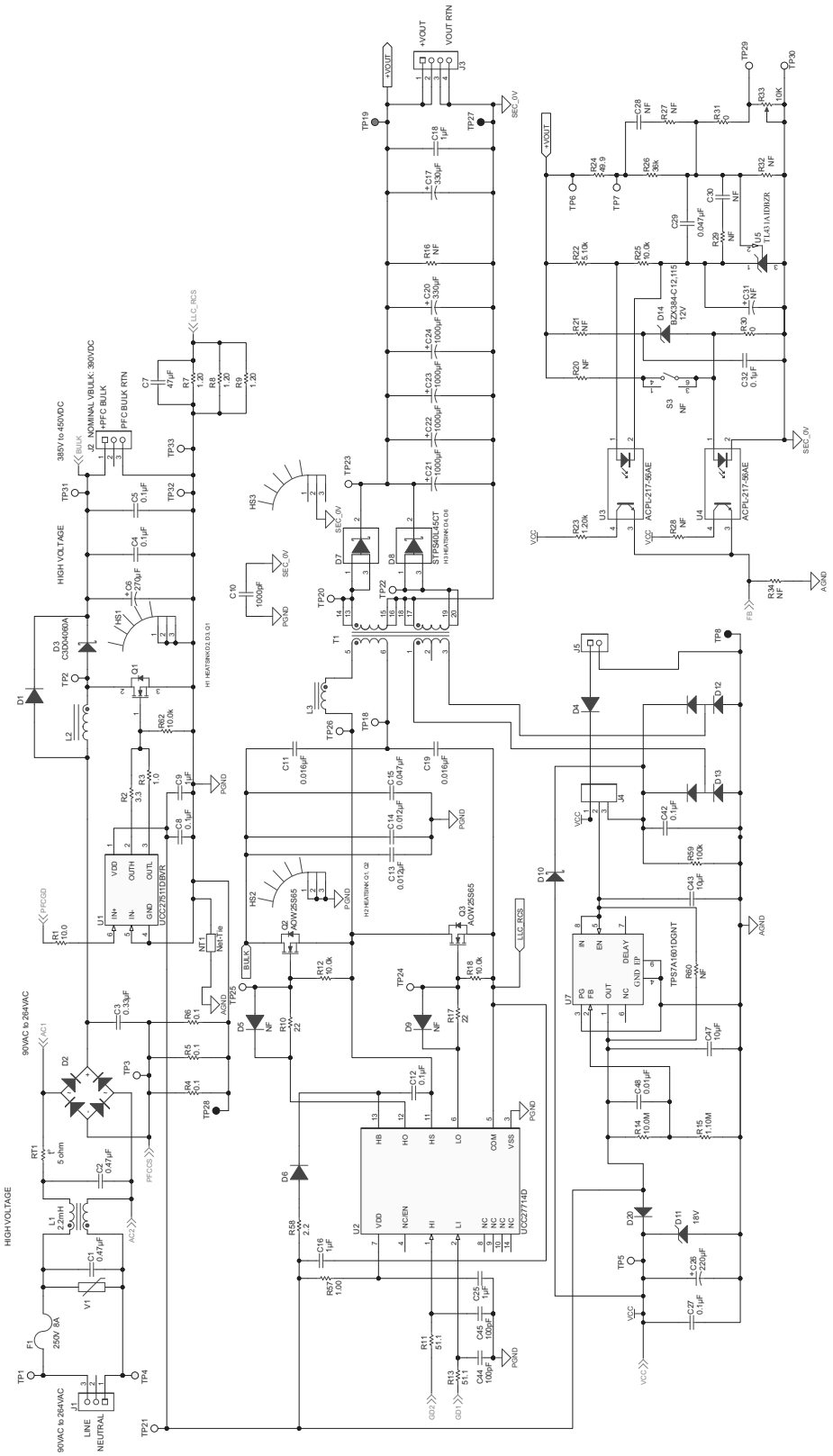


Figure 28. Power Stage Application

Typical Application (continued)

8.2.1 Design Requirements

The typical application should meet the following requirements:

Table 5. Typical Application Requirements

PARAMETER	REQUIREMENT	
V_{AC}	Input voltage	85 V_{AC} to 264 V_{AC}
f_{LINE}	Line frequency	47 Hz to 63 Hz
V_{BLK}	Nominal PFC stage output voltage	385 V
$V_{BLK(ripple)}$	Max V_{BLK} ripple (2 x Line Frequency)	30 V_{PP}
$V_{BLK(max)}$	Maximum PFC stage output voltage, V_{BLK} + ½ $V_{BLK(ripple)}$	400 V
$V_{BLK(min)}$	Minimum PFC stage output voltage, V_{BLK} – ½ $V_{BLK(ripple)}$	370 V
$V_{BLK(hu)}$	Minimum PFC stage output voltage at end of hold-up time	300 V
V_{OUT}	Output voltage	24 VDC
$V_{OUT(min)}$	Min output voltage	21.6 V (V_{OUT} – 10%)
$V_{OUT(max)}$	Max output voltage	26.4 V (V_{OUT} +10%)
I_{OUT}	Full load output current	12.5 A
$V_{OUT(pk\_pk)}$	Output voltage ripple	300 mV
P_{OUT}	Output power	300 W
η	Efficiency	90 %
P_F	Power factor	0.99
t_H	Hold-up time	20 ms
f_{PFC}	PFC stage switching frequency	98 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 LLC Stage

Start the design by deciding on the component values in the LLC power train and then move to the PFC stage.

The LLC stage design procedure outlined here follows the one given in the TI publication “Designing an LLC Resonant Half-Bridge Power Converter” which is available at http://www.ti.com/lit/ml/slup263/slup263.pdf. The document contains a full explanation of the origin of each of the equations used. The equations given below are based on the First Harmonic Approximation (FHA) method commonly used to analyze the LLC topology. This method gives a good starting point for any design, but a final design requires an iterative approach combining the FHA results, circuit simulation and hardware testing. An alternative design approach is given in TI Application Note, LLC Design for UCC29950, Texas Instruments Literature Number SLUA733.

One of the reasons that the LLC topology is so popular is that it can achieve Zero Voltage Switching (ZVS) over a wide range of operating conditions. ZVS is important because it reduces switching losses in the power devices. The schematic for a basic LLC is shown in Figure 29.

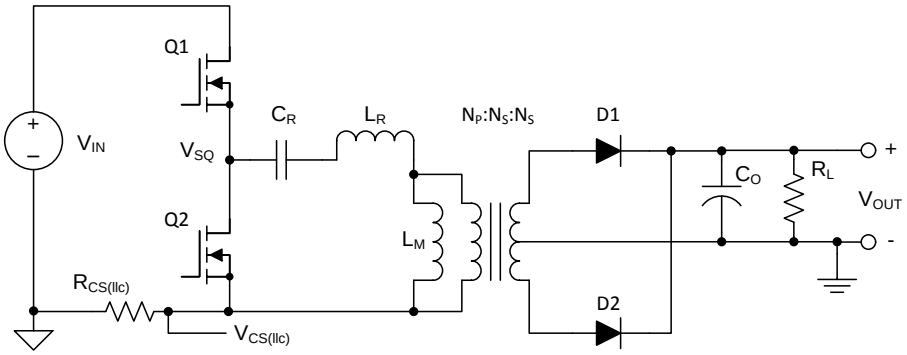


Figure 29. Basic LLC Schematic

In this system the input V_{IN} is the output of the PFC stage. V_{IN} is a DC voltage with some AC ripple at twice the line frequency. The two switches Q1 and Q2 are driven in anti-phase to generate a high-frequency square wave input signal V_{SQ} at the input to the resonant network formed by C_R, L_R and L_M. $R_{CS(llc)}$ is a current sensing resistor. Current flows in $R_{CS(llc)}$ only during the on time of Q1 in this single ended version of the LLC topology. This has two effects.

1. There is a significant voltage ripple on the current sense signal as Q1 and Q2 are switched.
2. Fault currents in Q2 are measured indirectly by their effect on currents in Q1.

The modified LLC topology shown in Figure 33 eliminates these disadvantages.

The resistor R_L loads this circuit through the transformer turns ratio and the peak gain is therefore a function of load, as shown in Figure 30. At no load, R_L is very high and its influence may be neglected and circuit has a resonance at:

$$f_p = \frac{1}{2\pi\sqrt{(L_R + L_M)C_R}} \tag{3}$$

At the other extreme, R_L is zero and it effectively shorts the transformer magnetizing inductance L_M. The resonant frequency under this condition is:

$$f_0 = \frac{1}{2\pi\sqrt{L_R C_R}} \tag{4}$$

This means that as the load changes from no load to short circuit the peak-gain frequency (f_{C0}) moves between these two values so that:

$$f_p \leq f_{C0} \leq f_0 \tag{5}$$

Output voltage regulation is achieved by changing the switching frequency of the LLC stage. If V_{IN} increases the LLC stage gain must reduce in order to keep V_{OUT} unchanged. The gain is reduced by increasing the switching frequency as can be seen in Figure 30. If V_{IN} reduces, then the gain must be increased and this is done by reducing the switching frequency. The frequency must remain above the resonant frequency f_{C0} to maintain zero voltage switching and to avoid control law reversal. This is especially important in a short circuit condition where the control loop would try to reduce the switching frequency and where simultaneously f_{C0} has increased to its maximum at f_0. Short circuit and overload protection are provided in the UCC29950 and are discussed in LLC Stage Over-Current Protection, Current Sense Resistor below.

8.2.2.2 LLC Switching Frequency

Selecting the nominal full-load switching frequency is relatively straightforward. Most EMI standards for conducted emissions have a lower limit at 150 kHz. If the fundamental switching frequency is lower than this then it does not appear in the EMI test scans which makes EMI filtering easier. Otherwise, if it is too low then the magnetic components are larger than necessary and the efficiency benefits of ZVS are reduced. A switching frequency of 120 kHz is a good compromise and is the one used in this design.

8.2.2.3 LLC Transformer Turns Ratio

The transformer turns ratio is given by the equation:

$$N = \frac{V_{IN}/2}{V_{OUT}} = \frac{385\,V/2}{24\,V} = 8.02 \Rightarrow 8 \quad (6)$$

V_{IN} is the voltage on the bulk capacitor. This is regulated at 385 V_{DC} if the resistor values suggested in Table 2 are used for the potential divider at the VBULK pin and ignoring diode forward voltage drops V_{OUT} is 24 V.

8.2.2.4 LLC Stage Equivalent Load Resistance

This is the effective load resistance reflected through the transformer turns ratio. Re is determined at the full load point.

$$R_E = \frac{8\,N^2}{\pi^2} R_L = 8 \times \frac{64}{9.87} \times \frac{24\,V}{12.5\,A} = 99.6\,\Omega \quad (7)$$

8.2.2.5 LLC Gain Range

These parameters set the gain range required of the LLC stage. It is assumed a 0.5-V drop in the rectifier diodes (V_f) and a further 0.5-V drop due to other losses (V_{LOSS}).

$$M_{G(min)} = N \frac{V_{OUT(min)}}{V_{IN(max)}/2} = 8 \times \frac{(21.6\,V + 0.5\,V)}{(400\,V)/2} = 0.88 \quad (8)$$

$$M_{G(max)} = N \frac{V_{OUT} + V_f + V_{LOSS}}{V_{BLK(hu)}/2} = 8 \times \frac{(24\,V + 0.5\,V + 0.5\,V)}{(300\,V)/2} = 1.33 \quad (9)$$

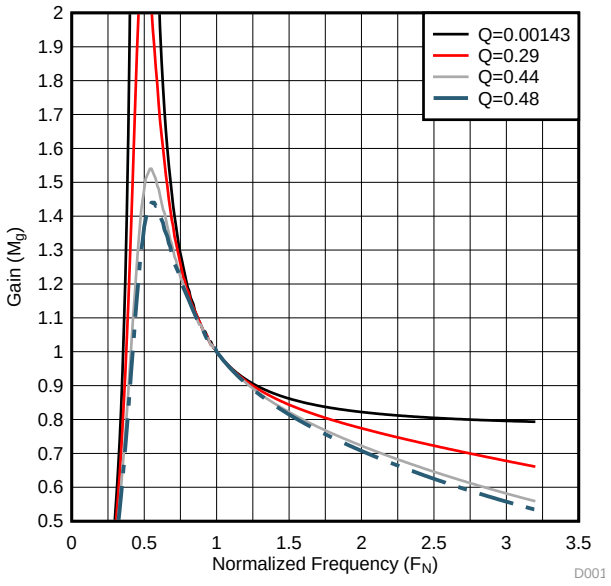


Figure 30. LLC Stage Gain Curve

8.2.2.6 Select L_N and Q_E

From Figure 31 and Figure 32 select suitable L_N and Q_E values to meet the M_{G_MIN} and M_{G_MAX} values from Equation 8 and Equation 9.

L_N is the primary inductance ratio and is given by:

$$L_N = \frac{L_M}{L_R} = 5.0 \tag{10}$$

Q_E is the quality factor of the resonant network.

$$Q_E = \frac{\sqrt{L_R/C_R}}{R_E} = 0.4 \tag{11}$$

Set L_N = 5.0 and Q_E = 0.40 for this application. The LLC peak gain curves below show a maximum which is greater than the maximum calculated by Equation 9.

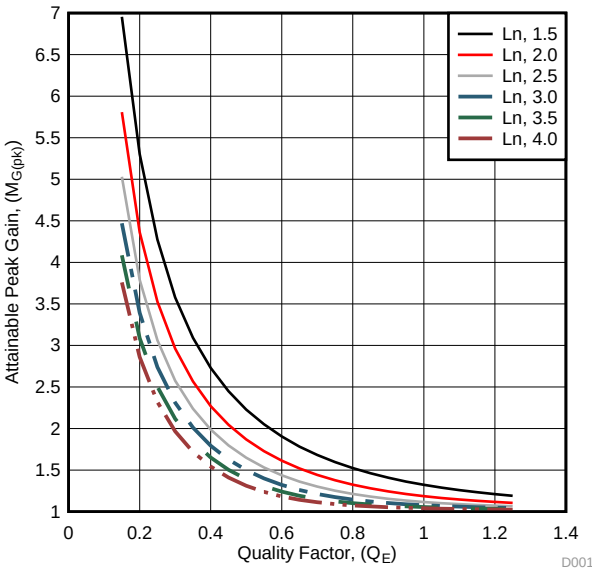


Figure 31. LLC Peak Gain Curves

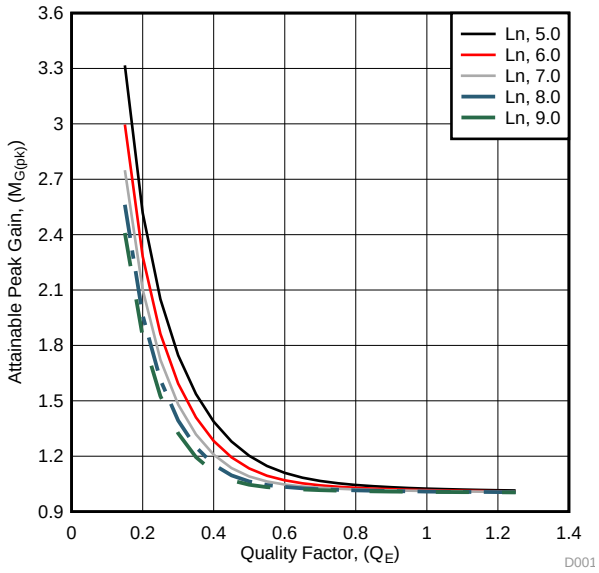


Figure 32. LLC Peak Gain Curves

8.2.2.7 LLC No-Load Gain

The gain required at no load is:

$$M_{G(\infty)} = \frac{L_N}{L_N + 1} = \frac{5.0}{5.0 + 1} = 0.83 \tag{12}$$

Figure 30 shows that the design can achieve a minimum gain of 0.8 at the maximum frequency of the UCC29950 (350 kHz or 2.9 times the normalized f_0 of 120 kHz).). If the gain is too high then the UCC29950 enters a burst mode of operation to keep the output voltage under control.

8.2.2.8 Parameters of the LLC Resonant Circuit

The value of the resonant capacitor is given by the equation:

$$C_R = \frac{1}{2\,\pi\,f_{SW}\,R_E\,Q_E} = \frac{1}{2\,\pi\,\times 120\,kHz\,\times\,99.6\,\Omega\,\times 0.4} = 33\,nF\;\Rightarrow 32\,nF \tag{13}$$

The resonant inductor is given by the equation:

$$L_R = \frac{1}{(2\,\pi\,f_{SW})^2\,C_R} = \frac{1}{(2\,\pi\,120\,kHz)^2\,\times\,32\,nF} = 55\,\mu H \tag{14}$$

Rearranging Equation 10 gives a value for L_M, the transformer magnetizing inductance:

$$L_M = L_N\,L_R = 5.0\,\times\,55\,\mu H = 275\,\mu H \tag{15}$$

8.2.2.9 Verify the LLC Resonant Circuit Design

The series resonant frequency is given by Equation 4.

$$f_0 = \frac{1}{2\pi\sqrt{L_R C_R}} = \frac{1}{2\pi\sqrt{55\ \mu H \times 32\ nF}} = 120\ kHz \tag{16}$$

The inductance ratio is given by:

$$L_N = \frac{L_M}{L_R} = \frac{275\ \mu H}{55\ \mu H} = 5.0 \tag{17}$$

The quality factor at full load is given by:

$$Q_E = \frac{\sqrt{L_R/C_R}}{R_E} = \frac{\sqrt{55\ \mu H/32\ nF}}{99.6\ \Omega} = 0.42 \tag{18}$$

This differs from the initial value of 0.45 because a rounded value for C_R is used here and in the calculation of L_R.

The difference is not significant.

Figure 30 has been normalized to the series resonant frequency which is 120 kHz in this example.

At the minimum gain condition with minimum output voltage and maximum input voltage ($M_{G(min)}$) the frequency is 1.6 times f_0 or $f_{SW(max)}$ = 192 kHz.

At the maximum gain condition with maximum output voltage and minimum input voltage ($M_{G(max)}$) the frequency is 0.6 times f_0 or $f_{SW(min)}$ = 72 kHz.

8.2.2.10 LLC Primary-Side Currents

The primary-side RMS load current is given by:

$$I_{OE} = \frac{\pi}{2\sqrt{2}} \times \frac{1}{N} \times I_O = \frac{\pi}{2\sqrt{2}} \times \frac{1}{8} \times 110\% \times 12.5\ A = 1.91\ A \tag{19}$$

The RMS magnetizing current at minimum switching frequency is:

$$I_M = \frac{2\sqrt{2}}{\pi}\frac{NV_{OUT}}{\omega L_M} = \frac{2\sqrt{2}}{\pi}\frac{8 \times 24}{2\pi \times 72\ kHz \times 275\ \mu H} = 1.4\ A \tag{20}$$

The total current in the resonant circuit is then given by:

$$I_R = I_{WP} = I_{CR} = \sqrt{I_M^2 + I_{OE}^2} = \sqrt{(1.91\ A)^2 + (1.4\ A)^2} = 2.4\ A \tag{21}$$

This current also flows in the transformer primary winding (I_{WP}) and the resonant capacitor (I_{CR}).

8.2.2.11 LLC Secondary-Side Currents

The total secondary-side RMS current is the current referred from the primary side (I_{OE}) to the secondary side.

$$I_{OE(S)} = N\, I_{OE} = 8 \times 1.91\ A = 15.3\ A \tag{22}$$

The design uses a centre tapped secondary so that this current is shared equally between the two windings. The current in each winding is then:

$$I_{WS} = \frac{\sqrt{2}\, I_{OE(S)}}{2} = \frac{\sqrt{2} \times 15.3\ A}{2} = 10.8\ A \tag{23}$$

And the half-wave average current in the secondary windings is:

$$I_{SAV} = \frac{\sqrt{2}\, I_{OE(S)}}{\pi} = \frac{\sqrt{2} \times 15.3\ A}{\pi} = 6.89\ A \tag{24}$$

8.2.2.12 LLC Transformer

The transformer can be built or purchased according to these specifications:

- Turns Ratio (N): 8
- Primary Magnetizing Inductance: L_M = 275 µH
- Primary Terminal Voltage: 450 V_{AC}
- Primary Winding Rated Current: I_{WP} = 2.4 A
- Secondary Terminal Voltage: 56 V_{AC}
- Secondary Winding Rated Current: I_{WS} = 10.8 A
- No Load Operating Frequency: $f_{SW(max)}$ = 192 kHz
- Full Load Operating Frequency: $f_{SW(min)}$ = 72 kHz
- Reinforced Insulation Barrier from Primary-to-Secondary to IEC60950

The minimum operating frequency during normal operation is that calculated above but during shutdown the LLC can operate at at LLC_{FMIN} .The magnetic components in the resonant circuit, the transformer and resonant inductor, should be rated to operate at this lower frequency.

8.2.2.13 LLC Resonant Inductor

The AC voltage across the resonant inductor is given by its impedance times the current:

$$V_{L_R} = \omega L_R \; I_R = 2\pi \times 72\ kHz \times 55\ \mu H \times 2.4\ A = 59.6\ V \Rightarrow 60\ V \tag{25}$$

As with the transformer, the resonant inductor can be built or specified according to these specifications:

- Inductance: L_R = 55 µH
- Rated Current: I_R = 2.4 A
- Terminal AC Voltage: V_{LR} = 60 V
- Frequency Range: 72 kHz to 192 kHz.

The minimum operating frequency during normal operation is that calculated above but during shutdown the LLC can operate at at LLC_{FMIN}.The magnetic components in the resonant circuit, the transformer and resonant inductor, should be rated to operate at this lower frequency.

8.2.2.14 Combining the LLC Resonant Inductor and Transformer

All physical transformers have a certain amount of leakage inductance. This inductance appears in series with the magnetizing inductance. It degrades the performance of most topologies so designers usually try to minimize it. In the LLC topology however, the leakage inductance appears in the same position as the Resonant Inductor L_R in Figure 29. This means that it is possible to design the transformer so that its leakage inductance replaces the separate resonant inductor.

The Advantages:

- Fewer Magnetic Components
- Simpler PCB
- Lower Cost

The disadvantage to the transformer must be designed to have a relatively large and well controlled amount of leakage inductance. The resonant inductance in the design above is about 20% of the total L_R + L_M. This is a high ratio and careful control of the winding geometry and layering is needed to keep the leakage inductance within acceptable limits.

The design procedure given above is valid irrespective of whether a design uses a separate resonant inductor and transformer or uses a single high-leakage transformer.

8.2.2.15 LLC Resonant Capacitor

This capacitor carries the full-primary current at a high frequency. A low dissipation factor part is needed to prevent overheating in the part.

The AC voltage across the resonant capacitor is given by its impedance times the current.

$$V_{CR} = \frac{I_{CR}}{\omega C_R} = \frac{2.4\ A}{2\pi \times 72\ kHz \times 32\ nF} = 166\ V \tag{26}$$

$$V_{CR(rms)} = \sqrt{\left(\frac{V_{IN(max)}}{2}\right)^2 + V_{CR}^2} = \sqrt{\left(\frac{400\ V}{2}\right)^2 + 166\ V^2} = 260\ V \tag{27}$$

And the corresponding peak voltage:

$$V_{CR(peak)} = \frac{V_{IN(max)}}{2} + \sqrt{2} V_{CR} = \frac{400\ V}{2} + \sqrt{2} \times 260\ V = 434\ V \tag{28}$$

The part selected must meet these specifications:

- Rated Current: I_{CR} = 2.4 A
- AC Voltage: $V_{CR(peak)}$ = 434 V

8.2.2.16 LLC Stage with Split Resonant Capacitor

It is possible to split the resonant capacitor in Figure 29 into two separate parts as shown below. The two circuits are topologically equivalent but there are some differences in circuit stresses. The calculation of the resonant circuit components is the same and the values of L_R, L_M and C_R are unchanged. The two resonant capacitors are each half the value of C_R.

The major advantages are:

- The current stresses in the capacitors are halved because the resonant current is shared between the two parts.
- The currents during the conduction times of both Q1 and Q2 flow in the current sensing resistor.

The main disadvantage is two parts are needed.

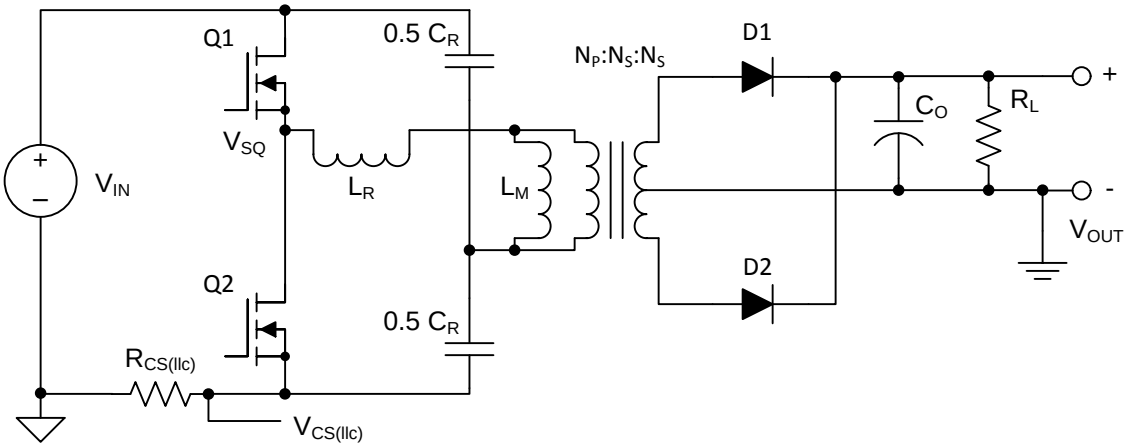


Figure 33. Basic LLC Schematic with Split Resonant Capacitor

8.2.2.17 LLC Primary-Side MOSFETs

V_{IN} appears across the MOSFET which is not conducting. The voltage rating must then be:

$$V_{Q1(peak)} = V_{Q2(peak)} = V_{IN} = 400\,V \Rightarrow 500\,V \quad (29)$$

This is a minimum rating and a 650-V rated part would be a better choice to allow margin for line-surge tests.

In the steady state, each MOSFET carries half of the resonant current. Start-up currents can be significantly higher so we set the RMS current rating to 110 % of the resonant current.

$$I_{Q1(rms)} = I_{Q2(rms)} = 110\%\, I_R = 1.1 \times 2.4A = 2.65\,A \quad (30)$$

8.2.2.18 LLC Output Rectifier Diodes

The voltage rating for the output diodes is given by:

$$V_{DB} = \frac{V_{IN(max)}}{N} = \frac{400\,V}{8} = 50\,V \Rightarrow 62\,V \quad (31)$$

The current rating for the output diodes is given by:

$$I_{SAV} = \frac{\sqrt{2}\ I_{OE(S)}}{\pi} = \frac{\sqrt{2}\ \times 15.3\,A}{\pi} = 6.9\,A \quad (32)$$

8.2.2.19 LLC Stage Output Capacitors

The LLC converter topology does not require an output filter although a small second stage filter inductor may be useful in reducing peak-to-peak output noise.

Assuming that the output capacitors carry the rectifier's full wave output current then the capacitor ripple current rating is:

$$I_{RECT} = I_{SW} = \frac{\pi}{2\sqrt{2}} I_{OUT} = \frac{\pi}{2\sqrt{2}} \times 12.5\ A = 13.9\ A \tag{33}$$

The capacitor's RMS current rating at 120 kHz is:

$$I_{C(out)} = \sqrt{(\frac{\pi}{2\sqrt{2}} I_{OUT})^2 - {I_{OUT}}^2} = \sqrt{\frac{\pi^2}{8} - 1} \times I_{OUT} = 0.483 \times 12.5\ A = 6.04\ A \tag{34}$$

Solid Aluminum capacitors with conductive polymer technology have high ripple-current ratings and are a good choice here. The ripple-current rating for a single capacitor may not be sufficient so multiple capacitors are often connected in parallel.

The ripple voltage at the output of the LLC stage is a function of the amount of AC current that flows in the capacitors. To estimate this voltage, we assume that all the current, including the DC current in the load, flows in the filter capacitors.

$$ESR_{MAX} = \frac{V_{OUT(pk-pk)}}{I_{RECT(pk)}} = \frac{V_{OUT(pk-pk)}}{2\,\frac{\pi}{4}\,I_{OUT}} = \frac{300\ mV}{2\,\frac{\pi}{4} \times 12.5\ A} = 15.3\ m\Omega \tag{35}$$

The capacitor specifications are:

- Voltage Rating: 30 V
- Ripple Current Rating: 6.04 A at 120 kHz
- ESR: < 15 mΩ

8.2.2.20 LLC Stage Over-Current Protection, Current Sense Resistor

This resistor shown in Figure 29 and Figure 33 senses the LLC stage input current. This current contains a significant component at the switching frequency in additional to a DC component. Only the DC component is proportional to the load current. This means that the signal should be filtered before it is applied to the LLC_CS pin of the UCC29950. The degree of filtering is a compromise between response time and accuracy. A recommended schematic is shown in Figure 13. An RC filter with a pole at about 1 kHz is used to filter the signal. An additional capacitor, C1, across the current sense resistor provides a higher frequency pole at approximately 10 kHz.

The LLC current sensing resistor is selected so that the LLC_CS signal is at 90% of the OCP1 level (400 mV x 0.9 = 360 mV) when the converter is operating at full load and nominal input and output conditions. The resistor value is then given by:

$$R_{CS(llc)} = \frac{V_{CS(llc\_fl)} V_{BLK(min)}}{\frac{1}{\eta} P_{OUT}} = \frac{0.36\ V \times 370\ V}{110\% \times 300\ W} = 403\ m\Omega \Rightarrow 400\ m\Omega \tag{36}$$

Where $V_{BLK(min)}$ is the voltage at the bottom of the line ripple on C_{BLK}.

Assuming there is no ripple current in the current sensing resistor, the full load power dissipated in this resistor is given by:

$$P_{R_{CS(LLC)}} = \frac{V_{CS(llc\_fl)}^2}{R_{CS(llc)}} = \frac{0.36\ V^2}{400\ m\Omega} = 324\ mW \tag{37}$$

The resistor should be able to dissipate the power due to an overload which is just lower than the OCP_1 threshold.

$$P_{R_C(llc\_max)} = \frac{V_{CS(OCP1)}^2}{R_{CS(LLC)}} = \frac{0.4\ V^2}{400\ m\Omega} = 400\ mW \tag{38}$$

8.2.2.21 Detailed Design Procedure for the PFC stage

The boost topology operated in Continuous Conduction Mode (CCM) is a popular choice for a Power Factor Correction (PFC) stage because it has lower component stresses than other topologies. This becomes more important at higher power levels.

The schematic for a basic PFC is shown in Figure 34. The basic schematics for the three boost PFC circuits, Discontinuous Conduction Mode (DCM), Transition Mode (TM) and CCM, are the same. The differences relate to whether or not the inductor current is allowed to go to zero for part of the PWM cycle (DCM) and whether the PFC frequency is held constant or used as a control variable (TM)

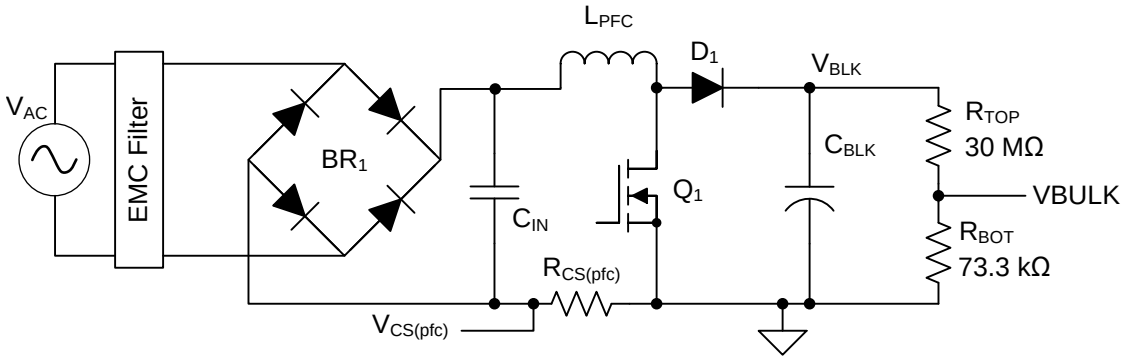


Figure 34. Basic PFC Schematic

8.2.2.22 PFC Stage Output Current Calculation

The first step is to determine the maximum load current on the PFC stage, allowing for an overload to 110 % of maximum load power.

$$I_{OUT(pfc)} = \frac{110\%\ P_{OUT}}{V_{BLK(min)}} = \frac{1.1\ \times 300\ W}{370\ V} = 0.9\ A \tag{39}$$

8.2.2.23 Line Current Calculation

Next determine the maximum RMS input-line current, allowing for an overload to 110% of maximum load power.

$$I_{LINE(RMS(max))} = \frac{110\%\ P_{OUT}}{\eta\ V_{AC(min)}} = \frac{1.1\ \times 300\ W}{0.9\ \times 85\ V} = 4.31\ A \tag{40}$$

The peak line current is:

$$I_{LINE(PEAK(max))} = \sqrt{2}\ I_{LINE(RMS(max))} = \sqrt{2} \times 4.07\ A = 6.1\ A \tag{41}$$

The average line current is given by:

$$I_{LINE(AVG(max))} = \frac{2\ I_{LINE(PEAK(max))}}{\pi} = \frac{2 \times 6.1\ A}{\pi} = 3.88\ A \tag{42}$$

8.2.2.24 Bridge Rectifier

A typical bridge rectifier has a forward voltage drop V_{F_BR} of 0.95 V. The power loss in the bridge rectifier can be calculated from:

$$P_{BR} = 2\ V_{F(BR)}\ I_{LINE(AVG(max))} = 2\ \times 0.95\ V\ \times 3.88\ A = 7.37\ W \tag{43}$$

The bridge rectifier must be rated to carry the full-line current ($I_{LINE(avg\_max)}$). The voltage rating of the bridge should be at least 600 V. The bridge rectifier also carries the full inrush current as the bulk capacitor (C_{BLK}) charges when the line is connected. The amplitude and duration of this current is difficult to determine in advance because it depends on many unknown parameters.

8.2.2.25 PFC Boost Inductor

The boost inductor is usually chosen so that the peak-to-peak amplitude of the switching frequency ripple current, $I_{HFR(pfc)}$, is between 20% and 40% of the average current at peak of line. This design example uses I_{HFR_PFC} = 30%. Numerically this is, (from Equation 41)

$$I_{HFR(pfc)} = 0.30\ I_{LINE(PEAK(max))} = 0.30 \times 6.1\ A = 1.83\ A \tag{44}$$

The minimum boost inductor value is calculated from a worst case duty cycle of 50%.

$$L_{PFC} \geq \frac{V_{BLK}\ D(1-D)}{f_{PFC}\ I_{HFR_{PFC}}} = \frac{385\ V \times 0.5 \times (1-0.5)}{98\ kHz \times 1.83\ A} = 536\ \mu H \Rightarrow 550\ \mu H \tag{45}$$

The boost inductor must be able to support a maximum current of:

$$I_{L(peak)} = I_{LINE(peak(max))} + \frac{I_{HFR(pfc)}}{2} = 6.1\ A + \frac{1.83\ A}{2} = 7.0 A \tag{46}$$

The boost inductor specifications are:

- L_{PFC} = 550 µH
- Current = 7 A

8.2.2.26 PFC Input Capacitor

The purpose of the input capacitor is to provide a local, low-impedance source for the high-frequency ripple currents which flow in the PFC inductor. The allowed voltage ripple on C_{IN} is ΔV_{IN}.

$$\Delta V_{IN} = 5\% \sqrt{2}\ V_{AC(min)} = 5\% \times \sqrt{2} \times 85\ V = 6.0\ V \tag{47}$$

$$C_{IN} = \frac{I_{HFR(pfc)}}{8\ f_{PFC}\ \Delta V_{IN}} = \frac{1.83\ A}{8 \times 98\ kHz \times 6.0\ V} = 390\ nF \Rightarrow 470\ nF \tag{48}$$

An X2 film capacitor is normally chosen for this application.

8.2.2.27 PFC Stage MOSFET

The main specifications for the PFC stage MOSFET are:

- B_{VDSS}, Drain Source Breakdown Voltage, ≥ 650 V
- $R_{DS(on)}$, On State Drain Source Resistance, 460 mΩ (125 °C)
- C_{OSS}, Output Capacitance, 87 pF
- t_r, device rise time, 30 ns
- t_f device fall time, 34 ns

The losses in the device are calculated below. These calculations are approximations because the losses are dependent on parameters which are not well controlled. For example the $R_{DS(on)}$ of a MOSFET can vary by a factor of 2 from 25°C to 125°C. Therefore several iterations may be needed to choose an optimum device for an application different to the one discussed.

The conduction losses are estimated by:

$$P_{Q1(cond)} = \left(\frac{P_{OUT(max)}}{\sqrt{2}V_{AC(min)}}\sqrt{2 - \frac{16\sqrt{2}V_{AC(min)}}{3\pi V_{BLK}}}\right)^2 R_{DS(on)} \tag{49}$$

Numerically:

$$P_{Q1(cond)} = \left(\frac{300\ W}{\sqrt{2} \times 85\ V}\sqrt{2 - \frac{16\sqrt{2} \times 85\ V}{3\pi \times 385\ V}}\right)^2 \times 0.46\ \Omega = 4.21\ W \tag{50}$$

The switching losses in the MOSFET are estimated by:

$$P_{Q1(sw)} = \frac{1}{2} f_{PFC} \left(V_{BLK} I_{LINE(RMS(max))} \left(t_r + t_f\right) + C_{OSS} V_{BLK}^2\right) \tag{51}$$

Numerically:

$$P_{Q1(sw)} = \frac{1}{2} \times 98\ kHz \times (385\ V \times 4.31\ A \times (30\ ns + 34\ ns) + 87\ pF \times 385\ V^2) = 5.84\ W \tag{52}$$

$$P_{Q1} = P_{Q1(cond)} + P_{Q1(sw)} = 4.21\ W + 5.84\ W = 10.05\ W \tag{53}$$

8.2.2.28 PFC Boost Diode

Reverse recovery losses can be significant in a CCM boost converter so a silicon carbide diode is chosen here because it has no reverse recovery charge, Q_{RR}, and therefore zero reverse recovery losses. The disadvantage is that the cost is higher than that of Silicon ultra fast diodes. The losses are estimated as follows:

$$P_{D1} = V_f I_{OUT} = 1.5\ V \times 0.9\ A = 1.35\ W \tag{54}$$

8.2.2.29 Bulk Capacitor

The value of the bulk capacitor is determined by three factors.

1. To ensure loop stability, the capacitance must be between 0.5 µF W^{-1} and 2.4 µF W^{-1} (see PFC Inductor and Bulk Capacitor Recommendations). For this 300-W application a bulk capacitance in the range 150 µF to 720 µF is allowed.
2. It must be large enough to provide the required hold-up time.
3. It must be large enough to keep the ripple at twice line frequency within the required limits.

The UCC29950 continues to run the LLC stage until the voltage at the VBULK pin has fallen below $V_{BULK(llc\_stop)}$ (0.49 V). This corresponds to a V_{BLK} of 200 V if the specified values for R_{BOT} and R_{TOP} are used. From Equation 55 it can be see that the LLC stage will not have enough gain to maintain V_{OUT} with such a low input voltage. The minimum voltage at which the LLC stage regulates is determined from Equation 55 which is a rearrangement of Equation 10. $M_{G(max)}$ is found from Figure 31 which gives a maximum gain of the LLC stage of 1.33.

$$V_{IN(min)} = N \frac{2\,V_{OUT}}{M_{G(max)}} = 8 \times \frac{2 \times 24\,V}{1.33} = 288\,V \Rightarrow 300\,V \tag{55}$$

The value of the capacitor is then given by:

$$C_{BLK} \geq \frac{2\,P_{OUT}\,t_H}{V_{BLK(min)}^2 - V_{BLK_{HU}}^2} = \frac{2 \times 300\,W \times 20\,ms}{370^2 - 300^2} = 255\,\mu F \Rightarrow 270\,\mu F \tag{56}$$

270 µF for 300 W is equal to 0.9 µF W^{-1} which lies within the allowed range for loop stability.

The peak-to-peak ripple voltage at twice line frequency on C_{BLK} is calculated as follows:

$$V_{BLK(ripple)} = \frac{I_{OUT(pfc)}}{\pi\,2\,f_{LINE(min)}C_{BLK}} = \frac{0.9\,A}{\pi \times 2 \times 47\,Hz \times 270\,\mu F} = 11.3\,V \tag{57}$$

The result of this calculation, 11.3 V, is significantly better than the specification, 30 V. This is because the size of the bulk capacitor is determined by the hold-up time rather than by the peak-to-peak line ripple specification.

The ripple current flowing in the bulk capacitor depends on the duty cycle which varies over the line cycle and also as a function of the RMS value of the line voltage. This makes a precise calculation difficult however Equation 58 gives a good approximation.

$$I_{C_{BLK\_R}} = I_{OUT(pfc)}\sqrt{\frac{D}{1-D}} \approx 0.9\,A \times \sqrt{\frac{0.5}{1-0.5}} \approx 0.9\,A \tag{58}$$

8.2.2.30 PFC Stage Current Sense Resistor

The current sense resistor is selected so that:

$$R_{CS(pfc)} = V_{PFCCS\,(cav\_max)}\,V_{AC(min)}\,\frac{\eta}{\sqrt{2}\,125\%\,P_{OUT}} \tag{59}$$

Numerically this is:

$$R_{CS(pfc)} = 225\,mV \times 85\,V\,\frac{90\%}{\sqrt{2}\,125\%\,P_{OUT}} = 33\,m\Omega \tag{60}$$

8.2.3 Application Curves

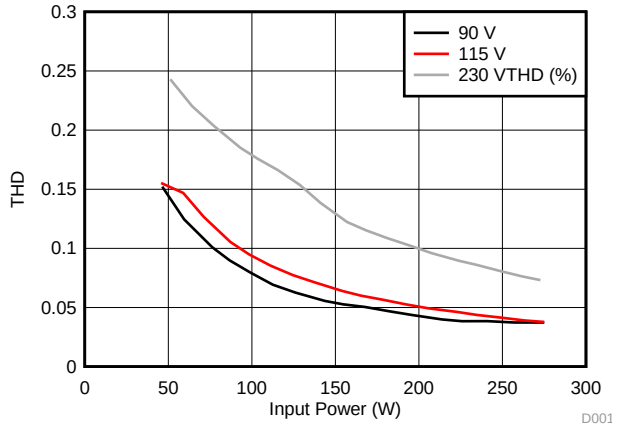


Figure 35. Typical THD vs. Input Power

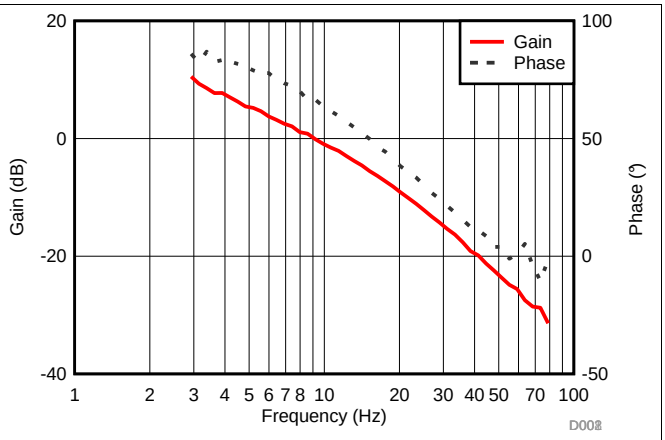


Figure 36. PFC Loop Gain/Phase at 300 W, 115 V

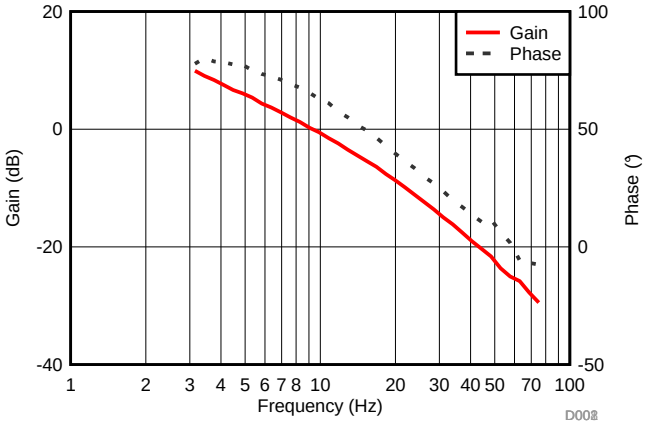


Figure 37. PFC Loop Gain/Phase at 300 W, 230 V

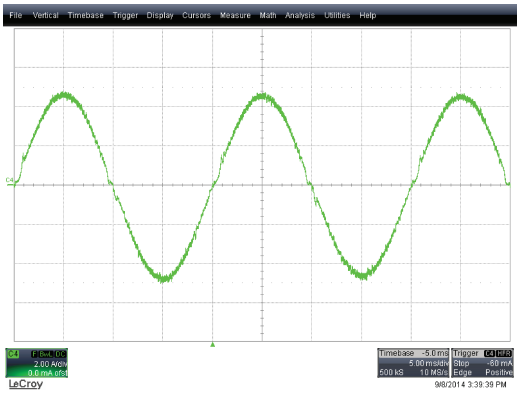


Figure 38.

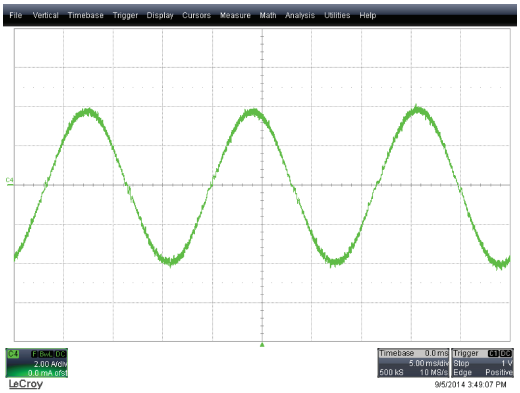


Figure 39. Line Current 115 V

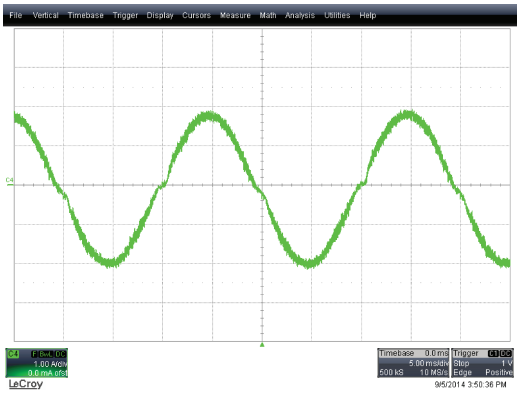


Figure 40. Line Current 230 V

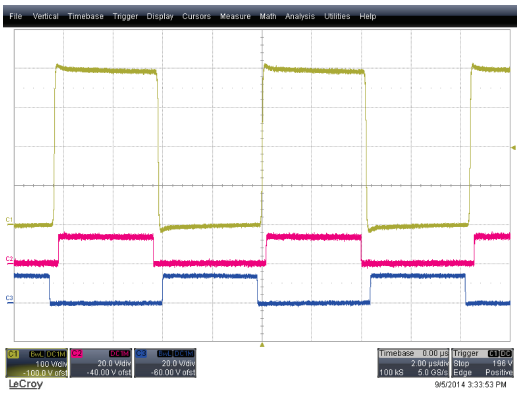


Figure 41. LLC Stage Switching
(C1: VSQ, C2: GD1, C3: GD2 See Figure 33)

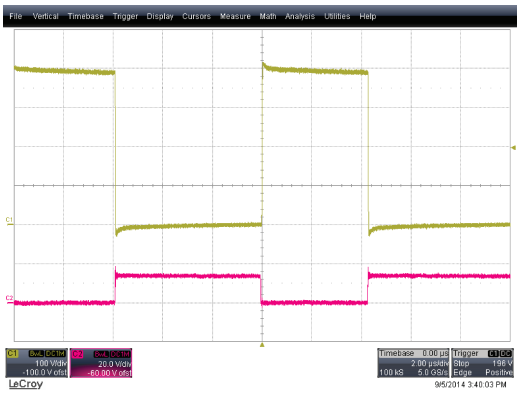


Figure 42. PFC Stage Switching (C1: V_{DS}, C2: PFC_GD See Figure 34)

8.3 Do's and Don'ts

Don’t probe the SUFG pin unless absolutely necessary. A normal X10 Oscilloscope probe can significantly load the very high output impedance of this pin .

Pay careful attention to grounding and to the routing of the sensing signals at PFC_CS, LLC_CS, VBULK, AC1 and AC2 pins.

The UCC29950 uses low value PFC current sense resistors, 38 mΩ in the example above. Careful attention to layout is needed to avoid significant errors in the PFC current and power limit points. Use Kelvin connections to the resistors.

9 Power Supply Recommendations

The UCC29950 should be operated from a VCC rail which is within the limits given in the VCC Bias Supply section of the Electrical Characteristics table. To avoid the possibility that the device might stop switching, VCC must not be allowed to fall into the UVLO range. In order to minimize power dissipation in the device, VCC should not be unnecessarily high. Keeping VCC at 12 V is a good compromise between these competing constraints. The gate drive outputs from the UCC29950 deliver large current pulses into their loads. This indicates the need for a low ESR decoupling capacitor to be connected as directly as possible between the VCC and PGND terminals. Ceramic capacitors with a stable dielectric characteristic over temperature, such as X7R, are recommended. Avoid capacitors which have a large drop in capacitance with applied DC voltage bias and use a part that has a low voltage co-efficient of capacitance. The recommended decoupling capacitance is 10 µF, X7R, with at least a 25-V rating.

Operation in Self Bias Mode requires an additional, larger, energy storage capacitor. The value required depends on the details of the application but typically this part is between 100 µF and 300 µF. This energy storage capacitor does not require low ESR and it does not need to be placed close to the UCC29950. A 25-V rated aluminum electrolytic capacitor is a good choice.

10 Layout

10.1 Layout Guidelines

In order to increase the reliability and robustness of the design, it is recommended that the following layout guidelines be met.

10.1.1 GND Pin

- This pin is the power ground connection and should be used as the return connection for the driver pins PFC_GD, GD1 and GD2.
- GND and AGND must be connected at a star point close to the pins on the controller
- If possible use a ground plane to minimize noise pickup.

10.1.2 GD1, GD2 Pins

- The GD1 and GD2 gate drive pins can be used to directly drive the primary winding of a gate-drive transformer or a high voltage gate driver device. The tracks connected to these pins carry high dv/dt signals. Minimize noise pickup by routing them as far away as possible from tracks connected to the device inputs, AC1, AC2, VBULK, FB, PFC_CS and LLC_CS.

10.1.3 VCC Pin

- The VCC pin must be decoupled to GND and AGND by two 10-µF 1206 ceramic capacitors placed close to the pins. In addition it is recommended that an additional 0.1-µF ceramic capacitor 0603 be placed in parallel between the VCC and AGND pin.

10.1.4 SUFG Pin

- The SUFG is a high-impedance pin and can only be connected to the gate of the external depletion mode MOSFET when the external high-voltage start-up feature is required. If the application does not require the external high-voltage start-up circuit then the SUFG pin should be left open circuit.

10.1.5 SUFS Pin

- The SUFS connects to the source of an external depletion mode MOSFET, if this feature in not required, SUFS should be connected to the VCC rail.

10.1.6 AGND Pin

- As with all PWM controllers, the effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return. Place all decoupling and filter capacitors as close as possible to the device pins with short traces. The AGND pin is used as the return connection for the low-power signaling and sensitive signal traces, AC1, AC2, VBULK, FB, MD_SEL/PS_ON and AC DET. It is also used as local decoupling return for PFC_CS and LLC_CS. It is connected to the GND pin at a star point close to the device.

10.1.7 MD_SEL/PS_ON Pin

- This pin is not especially sensitive but minimize coupling to tracks carrying high dv/dt signals.

10.1.8 VBULK Pin

- The VBULK sense chain is connected to the high-voltage rail on the PFC stage. Typically the top resistive element of the sense chain is split into two or three separate resistors to reduce the voltage stress on each device and permit the use of standard low-cost resistors, such as 1206 sized SMT devices, in the sense chain. Sufficient PCB spacing must be given between the high-voltage connections to the low voltage and GND nets. The VBULK is a high-impedance connection and should be shielded by a ground plane from any high-voltage switching nets. The copper area connecting the VBULK pin to the lower resistor/filter capacitor and the last resistor in the high-side divider chain should be kept to a minimum to reduce parasitic capacitance to any nearby switching nets. The bottom resistor in the divider network and filter capacitor must be placed close to the VBULK pin.

Layout Guidelines (continued)

10.1.9 AC1, AC2 Pins

- The AC1 and AC2 are connected to the AC input lines by resistive divider chains. These divider chains are normally formed using several discrete resistors in series. The AC1 and AC2 are high-impedance pins and care must be taken to route the resistor divider components away from high voltage switching nets. Ideally the connections should be shielded by ground planes. Sufficient PCB spacing must be given between the high-voltage connections and any low-voltage nets. A filter capacitor, 470 pF, must be placed in close proximity to the pins on the controller to decouple any high-frequency noise picked up on the AC1 and AC2 sense-chain connections.

10.1.10 LLC_CS

- The LLC_CS pin should be decoupled by an external RC filter placed close to the pin. Suitable values are a 2.2-kΩ resistor and 0.1-µF ceramic capacitor.

10.1.11 FB

- The FB signal is a low-power, high-impedance signal from the LLC regulation circuit. The PCB tracks from the opto-coupler should be tracked to minimize the loop area by running the VÌ feed track and FB signal from the opto-coupler in parallel. It is also recommended to provide screening for these traces with ground plane(s).

10.1.12 PFC_CS

- The PFC_CS requires an external resistor, recommended value of 1 kΩ, between the current sensing resistor and the PFC_CS pin to avoid overstressing the device during inrush. A small filter capacitor (1 nF) may be useful to further reduce the noise level at this pin. These components should be placed close to PFC_CS pin.
- The PFC_CS resistor is a low resistance part. Be careful that the connections to this resistor connect directly to the part terminals to avoid adding extra parasitic resistance. Be especially careful of the connection to the ground side of this resistor.

10.1.13 AC_DET

- The AC_DET is a signal output. This is a low-voltage signal trace and must be kept clear of any high-voltage switching nodes.

10.1.14 PFC_GD

- The track connected to the PFC_GD pin carries high dv/dt signal. Minimize noise pickup by routing the trace to this pin as far away as possible from tracks connected to the device inputs – AC1, AC2, VBULK, FB, PFC_CS and LLC_CS

10.2 Layout Example

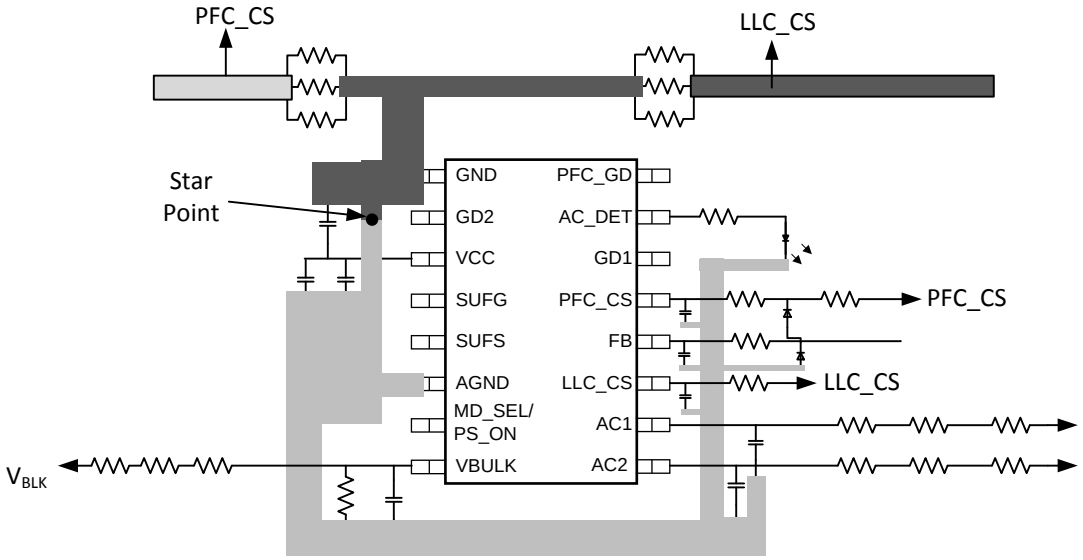


Figure 43.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

1. *《采用数字辅助模拟器件实现峰值电流模式控制与平均电流模式控制相结合》*；Seamus O'Driscoll，德州仪器 (TI) 和 David A. Grant，德州仪器；2014 IEEE 电力电子技术及应用国际会议暨展示会 (APEC 2014)，PP76
2. TI 应用手册*《UCC29950 的 LLC 设计》*（德州仪器 (TI) 文献编号：SLUA733）

11.2 商标

is a registered trademark of ~ECOVA, INC..
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC29950D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC29950
UCC29950D.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC29950
UCC29950DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC29950
UCC29950DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC29950

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

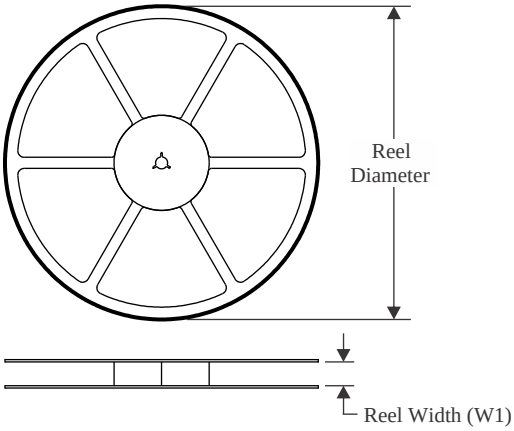
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

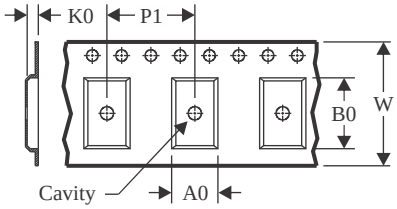
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

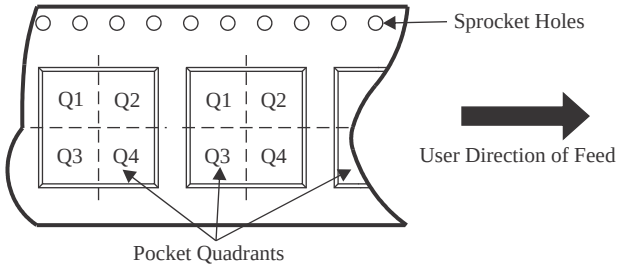


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

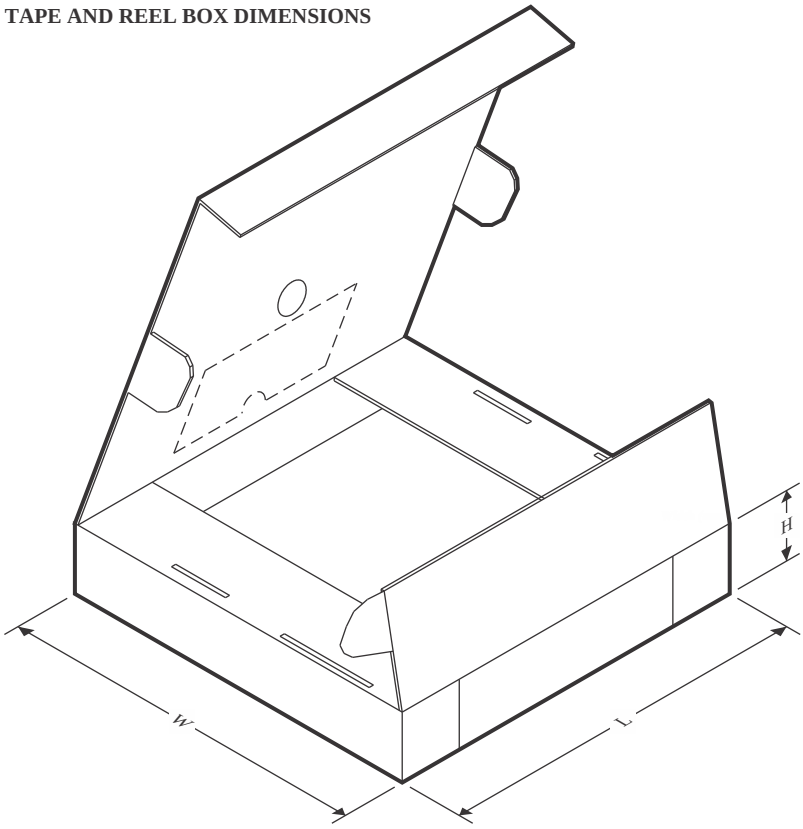
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC29950DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

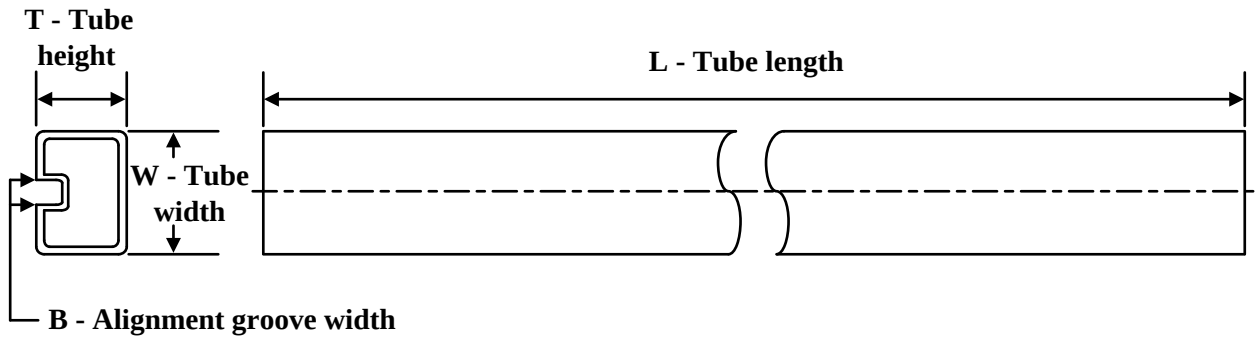
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC29950DR	SOIC	D	16	2500	353.0	353.0	32.0

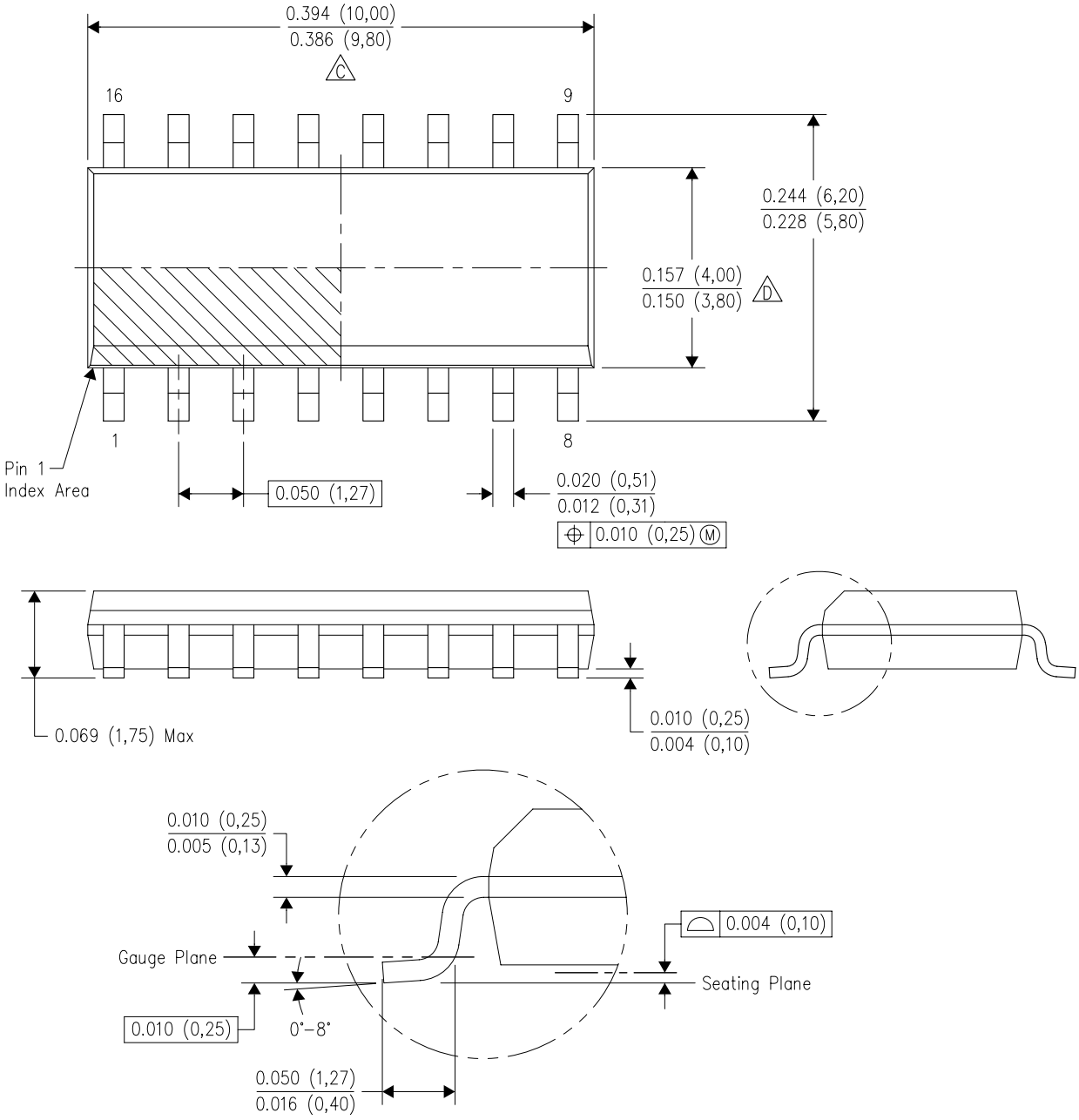
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC29950D	D	SOIC	16	40	507	8	3940	4.32
UCC29950D.A	D	SOIC	16	40	507	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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