UCC28C50-Q1, UCC28C51-Q1, UCC28C52-Q1, UCC28C53-Q1, UCC28C54-Q1, UCC28C55-Q1, UCC28C56H-Q1, UCC28C56L-Q1, UCC28C57H-Q1, UCC28C57L-Q1, UCC28C58-Q1, UCC28C59-Q1
ZHCSQ75C – JUNE 2022 – REVISED MARCH 2023

UCC28C5x-Q1 适用于 Si 和 SiC MOSFET 的汽车类低功耗、电流模式、高性能 PWM 控制器

1 特性

- 支持 Si 和 SiC MOSFET 应用的欠压锁定选项
- 30V VDD 绝对最大电压
- 1MHz 最大固定频率工作
- 50 µ A 启动电流，最大值 75 µ A
- 低工作电流：1.3mA (f_{OSC} = 52kHz)
- 高工作 T_J：150°C (最大值)
- 35ns 快速逐周期过流限制
- 峰值驱动电流为 ±1A
- 轨到轨输出：
  - 25ns 上升时间
  - 20ns 下降时间
- 精度为 ±1% 的 2.5V 误差放大器基准
- 与 UCC28C4x-Q1 引脚对引脚兼容的可直接替代产品
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 具有符合 AEC-Q100 标准的下列特性
  - 器件温度等级 1：-40°C 至 125°C
  - 器件 HBM 分类等级 2：±2kV
  - 器件 CDM 分类等级 C4B：750 V

2 应用

- 牵引逆变器高压转低压备用电源
- OBC 和直流/直流转换器隔离式偏置电源
- HVAC 压缩机高压隔离式电源
- 交流和直流 EV 充电设备中的单端直流转换器

3 说明

UCC28C5x-Q1 系列器件为高性能电流模式 PWM 控制器，可用于驱动各种应用中的 Si 和 SiC MOSFET。UCC28C5x-Q1 系列是 UCC28C4x-Q1 的更高效、更稳健的版本。

除持续支持 Si MOSFET 的现有 UVLO 阈值 (UCC28C50-55-Q1) 外，UCC28C5x-Q1 系列还具有可确保 SiC MOSFET 可靠运行的新 UVLO 阈值 (UCC28C56-59-Q1)。

VDD 绝对最大额定电压从 20V 增加至 30V，便于以理想方式驱动 20Vgs、18Vgs 或 15Vgs SiC MOSFET 的栅极，同时可无需使用外部 LDO。

器件性能改进

参数	UCC28C4x-Q1	UCC28C5x-Q1
52kHz 时的电源电流	2.3mA	1.3mA
启动电流 (上限值)	100µA	75µA
VDD 绝对上限值	20V	30V
基准电压精度	±2%	±1%
Si FET 的 UVLO 和 D_{MAX}	6 个选项	6 个选项
SiC FET 的 UVLO 和 D_{MAX}	none	6 个选项

1. 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

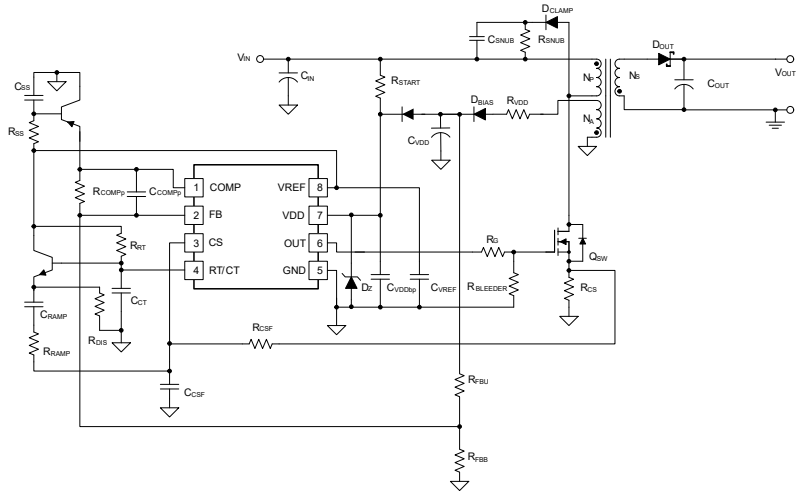


图 3-1. 典型汽车应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (February 2023) to Revision C (March 2023)	Page
• UCC28C58-Q1 器件的初始发行版	1
• Updated Available Options Table	3
• Added Link to Technical Support	48

Changes from Revision A (October 2022) to Revision B (February 2023)	Page
• UCC28C55-Q1、UCC28C56L-Q1、UCC28C57L-Q1 和 UCC28C57H-Q1 器件的初始发行版	1

Changes from Revision * (June 2022) to Revision A (October 2022)	Page
• UCC28C59-Q1 器件的初始发行版	1
• Updated Available Options Table	3
• Updated Electrical Characteristics section	7
• Updated Typical Characteristics section	9
• Updated Application Information section	26

5 Device Comparison Table

UVLO			MAXIMUM DUTY CYCLE	TEMPERATURE (T_A)
TURN ON AT 14.5 V TURN OFF AT 9 V SUITABLE FOR OFF-LINE APPLICATIONS	TURN ON AT 8.4 V TURN OFF AT 7.6 V SUITABLE FOR DC/DC APPLICATIONS	TURN ON AT 7 V TURN OFF AT 6.6 V SUITABLE FOR BATTERY APPLICATIONS		
UCC28C52QDRQ1	UCC28C53QDRQ1	UCC28C50QDRQ1	100%	–40°C to 125°C
UCC28C54QDRQ1	UCC28C55QDRQ1	UCC28C51QDRQ1	50%	

UVLO			MAXIMUM DUTY CYCLE	TEMPERATURE (T_A)
TURN ON AT 18.8 V TURN OFF AT 15.5V Suitable for HV applications using GEN-I SiC MOSFET	TURN ON AT 18.8 V TURN OFF AT 14.5V Suitable for HV applications using GEN-II SiC MOSFET	TURN ON AT 16 V TURN OFF AT 12.5V Suitable for HV applications using GEN-III SiC MOSFET		
UCC28C56HQDRQ1	UCC28C56LQDRQ1	UCC28C58QDRQ1	100%	–40°C to 125°C
UCC28C57HQDRQ1	UCC28C57LQDRQ1	UCC28C59QDRQ1	50%	

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28C50-Q1, UCC28C51-Q1, UCC28C52-Q1	SOIC (8)	4.90 mm × 3.91 mm
UCC28C53-Q1, UCC28C54-Q1, UCC28C55-Q1		
UCC28C56H-Q1, UCC28C56L-Q1		
UCC28C57H-Q1, UCC28C57L-Q1		
UCC28C58-Q1, UCC28C59-Q1		

6 Pin Configuration and Functions

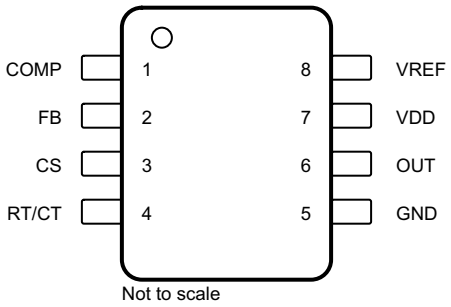


图 6-1. D Package 8-Pin SOIC Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	1	O	This pin provides the output of the error amplifier for compensation. In addition, the COMP pin is frequently used as a control port, by utilizing a secondary-side error amplifier to send an error signal across the secondary-primary isolation boundary through an opto-isolator. The error amplifier is internally current limited so the user can command zero duty cycle by externally forcing COMP to GND.
CS	3	I	Primary-side current sense pin. The current sense pin is the noninverting input to the PWM comparator. Connect to current sensing resistor. This signal is compared to a signal proportional to the error amplifier output voltage. The PWM uses this to terminate the OUT switch conduction. A voltage ramp can be applied to this pin to run the device with a voltage mode control configuration.
FB	2	I	This pin is the inverting input to the error amplifier. FB is used to control the power converter voltage-feedback loop for stability. The noninverting input to the error amplifier is internally trimmed to 2.5 V ±1%.
GND	5	—	Ground return pin for the output driver stage and the logic level controller section.
OUT	6	O	The output of the on-chip drive stage. OUT is intended to directly drive a MOSFET. The OUT pin in the UCC28C50-Q1, UCC28C52-Q1, UCC28C53-Q1, UCC28C56H/L-Q1, and UCC28C58-Q1 is the same frequency as the oscillator, and can operate near 100% duty cycle. In the UCC28C51-Q1, UCC28C54-Q1, UCC28C55-Q1, UCC28C57H/L-Q1, and UCC28C59-Q1, the frequency of OUT is one-half that of the oscillator due to an internal T flipflop. This limits the maximum duty cycle to < 50%. Peak currents of up to 1 A are sourced and sunk by this pin. OUT is actively held low when VDD is below the turn-on threshold.
RT/CT	4	I/O	Fixed frequency oscillator set point. Connect timing resistor (R_{RT}) to VREF and timing capacitor (C_{CT}) to GND from this pin to set the switching frequency. For best performance, keep the timing capacitor lead to the device GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions. The switching frequency (fSW) of the UCC28C50-Q1, UCC28C52-Q1, UCC28C53-Q1, UCC28C56H/L and UCC28C58 gate drive is equal to fOSC; the switching frequency of the UCC28C51-Q1, UCC28C54-Q1, UCC28C55-Q1, UCC28C57H/L-Q1, and UCC28C59-Q1 is equal to half of the f_{OSC}.
VDD	7	I	Analog controller bias input that provides power to the device. Total VDD current is the sum of the quiescent VDD current and the average OUT current. A bypass capacitor, typically 0.1 µF, connected directly to GND with minimal trace length, is required on this pin. Additional capacitance at least 10 times greater than the gate capacitance of the main switching FET used in the design and 10 times greater than the capacitance on the VREF pin are also required on VDD.
VREF	8	O	5-V reference voltage. VREF is used to provide charging current to the oscillator timing capacitor through the timing resistor. It is important for reference stability that VREF is bypassed to GND with a ceramic capacitor connected as close to the pin as possible. A minimum value of 0.1 µF ceramic is required. Additional VREF bypassing is required for external loads on VREF. No external voltage higher than specified VREF is allowed to superimposed to VREF pin Since VREF is an ouput.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Input voltage	VDD		30	V
Input current	I_{VDD}		30	mA
Output drive current (peak)			±1	A
Output energy (capacitive load), E_{OUT}			5	µJ
Analog input voltage	COMP, CS, FB, RT/CT	–0.3	6.3	V
Output driver voltage	OUT	–0.3	30	
Reference voltage	VREF		7	
Error amplifier output sink current	COMP		10	mA
Total power dissipation at T_A = 25°C	D package		72.3	°C/W
Lead temperature (soldering, 10 s), T_{LEAD}			300	°C
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under 节 7.3. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND pin. Currents are positive into and negative out of the specified terminals.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 节 7.2	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{VDD}	Input voltage			28	V
V_{OUT}	Output driver voltage			28	V
I_{OUT}	Average output driver current(1)			200	mA
$I_{OUT(VREF)}$	Reference output current(1)			– 20	mA
T_J	Operating junction temperature(1)	UCC28C5x-Q1	– 40	150	°C
T_A	Operating ambient temperature(1)	UCC28C5x-Q1	– 40	125	°C

(1) TI recommends against operating the device under conditions beyond those specified in this table for extended periods of time.

7.4 Thermal Information

THERMAL METRIC(1)		UCC28C5x-Q1	UNIT
		D (SOIC) 8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor anddevicePackage Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{VDD} = 20 V [1](for UCC28C56H/L-Q1, UCC28C57H/L-Q1 and UCC28C58/9-Q1), V_{VDD} = 15 V[1] (for the rest), R_{RT} = 10 kΩ, C_{CT} = 3.3 nF, C_{VDD} = 0.1 µF and no load on the outputs, T_J = –40°C to 150°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{VREF}	VREF voltage, initial accuracy	I_{OUT} = 1 mA	4.95	5	5.05	V
	Line regulation	V_{VDD} = 12 V to 25 V		0.2	20	mV
	Load regulation	1 mA to 20 mA		3	25	mV
	Temperature stability	See [2]		0.2	0.4	mV/°C
	Total output variation	See [2]	4.82		5.18	V
	VREF noise voltage	10 Hz to 10 kHz, T_J = 25°C, see [2]		50		µV
	Long term stability	1000 hours, T_J = 150°C, see [2]		5	25	mV
I_{VREF}	Output short circuit (source current)		30	45	55	mA
OSCILLATOR						
f_{OSC}	Initial accuracy	T_J = 25°C, see [3]	50.5	53	55	kHz
		T_J = Full Range, see [3]	50.5		57	kHz
	Voltage stability	12 V ≤ V_{VDD} ≤ 25 V		0.2%	1%	
	Temperature stability	$T_{J(MIN)}$ to $T_{J(MAX)}$, see [2]		1%	2.5%	
	Amplitude	RT/CT pin peak-to-peak voltage		1.9		V
	Discharge current	T_J = 25°C, $V_{RT/CT}$ = 2 V, see [4]	7.7	8.4	9	mA
		T_J = Full Range, $V_{RT/CT}$ = 2 V, see [4]	7.2	8.4	9.5	
ERROR AMPLIFIER						
V_{FB}	Feedback input voltage, initial accuracy	T_J = 25°C, V_{COMP} = 2.5 V	2.475	2.5	2.525	V
	Feedback input voltage, total variation	T_J = Full Range, V_{COMP} = 2.5 V	2.45	2.5	2.55	V
I_{FB}	Input bias current	V_{FB} = 5 V, (sourcing current)		0.1	2	µA
A_{VOL}	Open-loop voltage gain	2 V ≤ V_{OUT} ≤ 4 V	65	90		dB
	Unity gain bandwidth	See [2]	1	1.5		MHz
PSRR	Power supply rejection ratio	12 V ≤ V_{VDD} ≤ 25 V	60			dB
	Output sink current	V_{FB} = 2.7 V, V_{COMP} = 1.1 V	2	14		mA
	Output source current	V_{FB} = 2.3 V, V_{COMP} = 5 V, (sourcing current)	0.5	1		mA
VOH	High-level COMP voltage	V_{FB} = 2.7 V, R_{COMP} = 15 kΩ COMP to GND	V_{REF} – 0.2			V
VOL	Low-level COMP voltage	V_{FB} = 2.7 V, R_{COMP} = 15 kΩ COMP to VREF		0.1	1.1	V
CURRENT SENSE						
A_{CS}	Gain	T_J = 25°C, See [5]	2.85	3	3.15	V/V
		T_J = Full Range, See [5]	2.75	3	3.15	V/V
V_{CS}	Maximum input signal	V_{FB} < 2.4 V	0.9	1	1.1	V
PSRR	Power supply rejection ratio	V_{VDD} = 12 V to 25 V[2] [5]		70		dB
I_{CS}	Input bias current (source current)			0.1	2	µA
t_D	CS to output delay			35	70	ns
	COMP to CS offset	V_{CS} = 0 V		1.15		V
OUTPUT						
$V_{OUT(low)}$	$R_{DS(on)}$ pulldown	I_{SINK} = 200 mA		5.5	15	Ω
$V_{OUT(high)}$	$R_{DS(on)}$ pullup	I_{SOURCE} = 200 mA		10	25	Ω
t_{RISE}	Rise tIme	T_J = 25°C, C_{OUT} = 1 nF		25	50	ns
t_{FALL}	Fall tIme	T_J = 25°C, C_{OUT} = 1 nF		20	40	ns

V_{VDD} = 20 V (1)(for UCC28C56H/L-Q1, UCC28C57H/L-Q1 and UCC28C58/9-Q1), V_{VDD} = 15 V(1) (for the rest), R_{RT} = 10 kΩ, C_{CT} = 3.3 nF, C_{VDD} = 0.1 µF and no load on the outputs, T_J = –40°C to 150°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT						
VDD_{ON}	Start threshold(6)	UCC28C52-Q1, UCC28C54-Q1	13.5	14.5	15.5	V
		UCC28C53-Q1, UCC28C55-Q1	7.8	8.4	9	
		UCC28C50-Q1, UCC28C51-Q1	6.5	7	7.5	
		UCC28C56H-Q1, UCC28C57H-Q1	17.6	18.8	20	
		UCC28C56L-Q1, UCC28C57L-Q1	17.6	18.8	20	
		UCC28C58-Q1, UCC28C59-Q1	14.8	16	17.2	
VDD_{OFF}	Minimum operating voltage (6)	UCC28C52-Q1, UCC28C54-Q1	8	9	10	V
		UCC28C53-Q1, UCC28C55-Q1	7	7.6	8.2	
		UCC28C50-Q1, UCC28C51-Q1	6.1	6.6	7.1	
		UCC28C56H-Q1, UCC28C57H-Q1	15	15.5	16	
		UCC28C56L-Q1, UCC28C57L-Q1	13.95	14.5	15	
		UCC28C58-Q1, UCC28C59-Q1	12	12.5	13	
VDD_{Hyst}	VDD_{ON} - VDD_{OFF} (6)	UCC28C52-Q1, UCC28C54-Q1	5.4	5.5		V
		UCC28C53-Q1, UCC28C55-Q1	0.8	0.9		
		UCC28C51-Q1, UCC28C50-Q1	0.4	0.5		
		UCC28C56H-Q1, UCC28C57H-Q1	2.6	3.3		
		UCC28C56L-Q1, UCC28C57L-Q1	3.65	4.3		
		UCC28C58-Q1, UCC28C59-Q1	2.8	3.5		
PWM						
D_{MAX}	Maximum duty cycle	UCC28C52-Q1, UCC28C53-Q1, UCC28C50-Q1, V_{FB} < 2.4 V	94%	96%		
		UCC28C56H-Q1, UCC28C56L-Q1, UCC28C58-Q1, V_{FB} < 2.4 V				
		UCC28C54-Q1, UCC28C55-Q1, UCC28C51-Q1, V_{FB} < 2.4 V	47%	48%		
		UCC28C57H-Q1, UCC28C57L-Q1, UCC28C59-Q1, V_{FB} < 2.4 V				
D_{MIN}	Minimum duty cycle	V_{FB} > 2.6 V			0%	
CURRENT SUPPLY						
$I_{START-UP}$	Start-up current	V_{VDD} = VDD_{ON} – 0.5 V		50	75	µA
I_{VDD}	Operating supply current	V_{FB} = V_{CS} = 0 V		1.3	2	mA

(1) Adjust V_{VDD} above the start threshold before setting at 20 V for UCC28C56H/L-Q1, UCC28C57H/L-Q1 and UCC28C58/9-Q1, and 15.5 V for the rest family.
(2) Ensured by design. Not production tested.
(3) Output frequencies of the UCC28C51-Q1, UCC28C54-Q1, UCC28C55-Q1, UCC28C57H/L-Q1, and the UCC28C59-Q1 are half the oscillator frequency.
(4) Oscillator discharge current is measured with R_{RT} = 10 kΩ to VREF.
(5) Parameter measured at trip point of latch with V_{FB} = 0 V. Gain is defined as $A_{CS} = \Delta V_{COMP} / \Delta V_{CS}$, 0 V ≤ V_{CS} ≤ 900 mV.
(6) VDD_{ON}, VDD_{OFF}, and V_{REF} are tracking each other in the same direction, e.g., min VDD_{OFF} is due to min VDD_{ON}.

7.6 Typical Characteristics

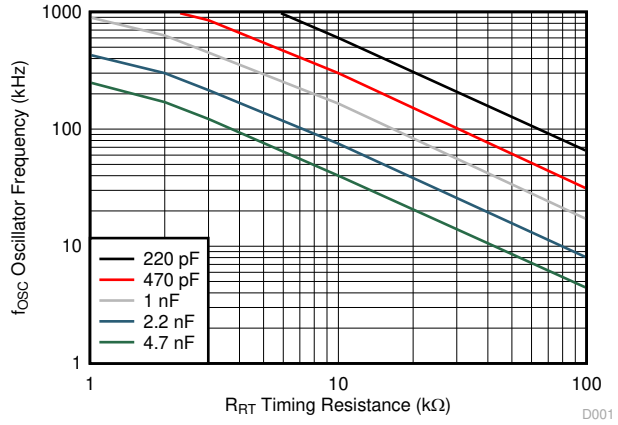
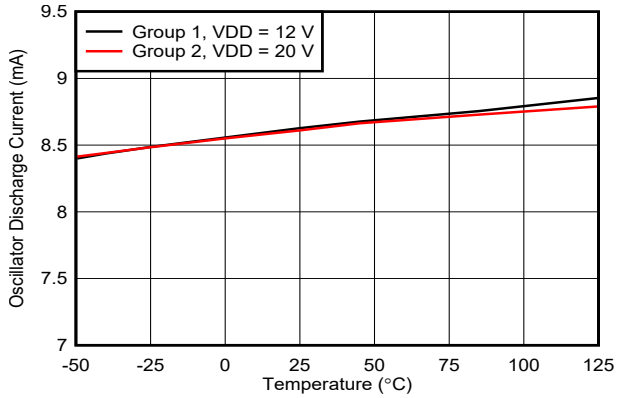


图 7-1. Oscillator Frequency vs Timing Resistance and Capacitance



Group 1: UCC28C50-Q1 to UCC28C55-Q1
Group 2: UCC28C56H-Q1 to UCC28C59-Q1

图 7-2. Oscillator Discharge Current vs Temperature

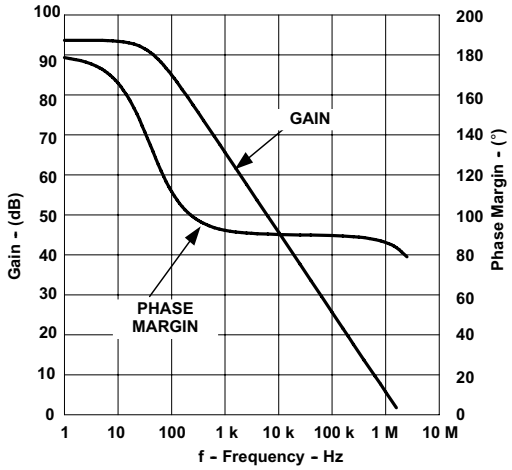
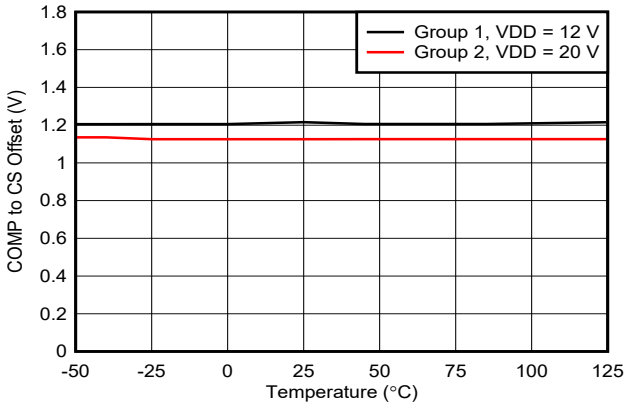


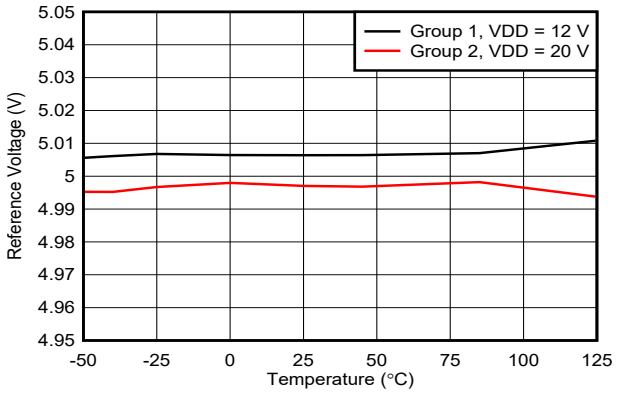
图 7-3. Error Amplifier Frequency Response



V_{CS} = 0

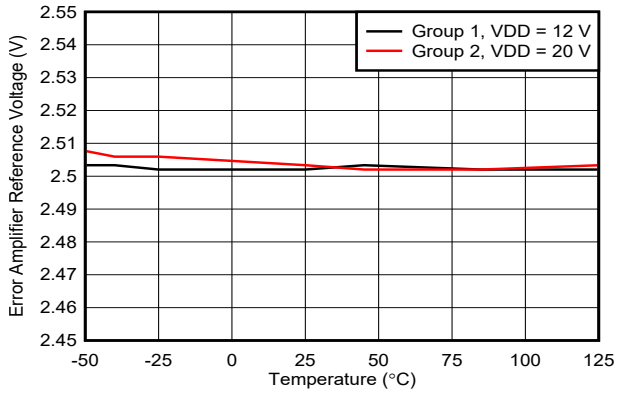
Group 1: UCC28C50-Q1 to UCC28C55-Q1
Group 2: UCC28C56H-Q1 to UCC28C59-Q1

图 7-4. COMP to CS Offset Voltage vs Temperature



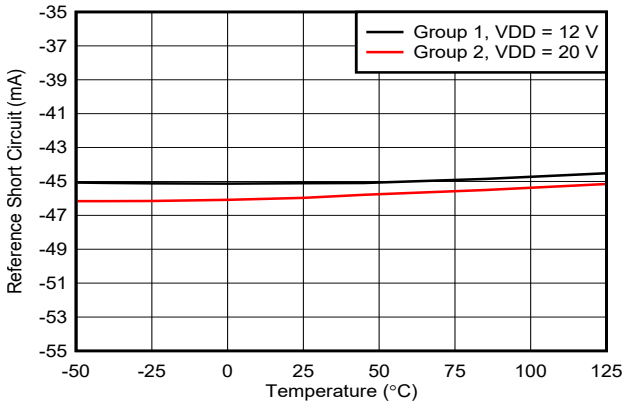
Group 1: UCC28C50-Q1 to UCC28C55-Q1
Group 2: UCC28C56H-Q1 to UCC28C59-Q1

图 7-5. Reference Voltage vs Temperature



Group 1: UCC28C50-Q1 to UCC28C55-Q1
Group 2: UCC28C56H-Q1 to UCC28C59-Q1

图 7-6. Error Amplifier Reference Voltage vs Temperature



Group 1: UCC28C50-Q1 to UCC28C55-Q1
Group 2: UCC28C56H-Q1 to UCC28C59-Q1

图 7-7. Reference Short-Circuit Current vs Temperature

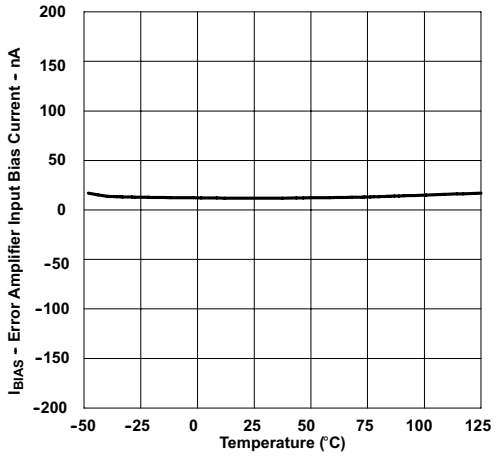
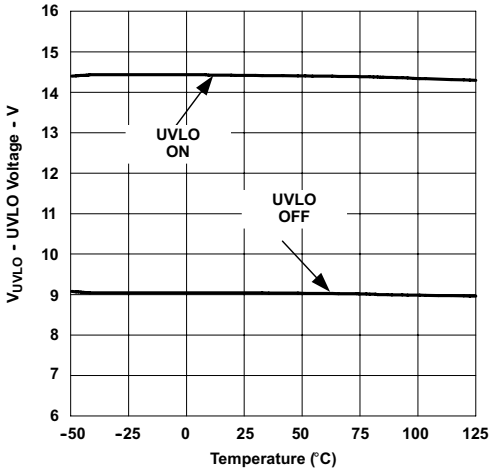
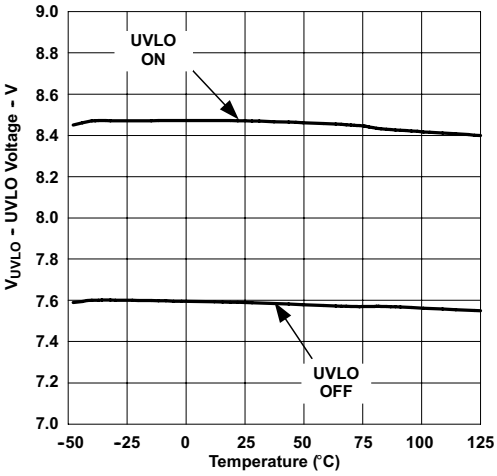


图 7-8. Error Amplifier Input Bias Current vs Temperature



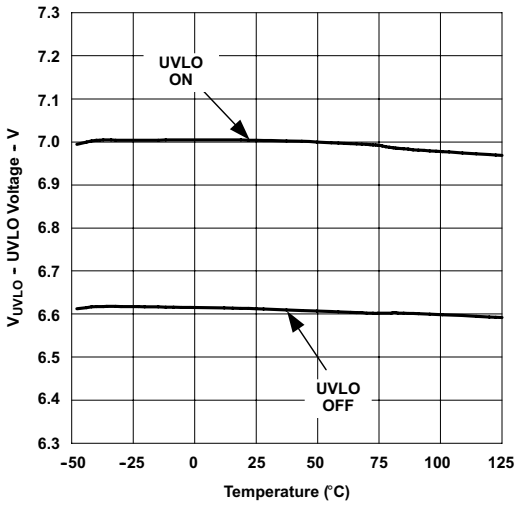
UCC28C52-Q1 and UCC28C54-Q1

图 7-9. Undervoltage Lockout vs Temperature



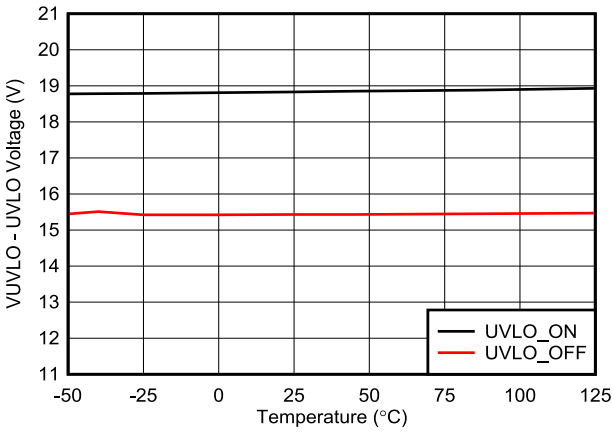
UCC28C53-Q1 and UCC28C55-Q1

图 7-10. Undervoltage Lockout vs Temperature



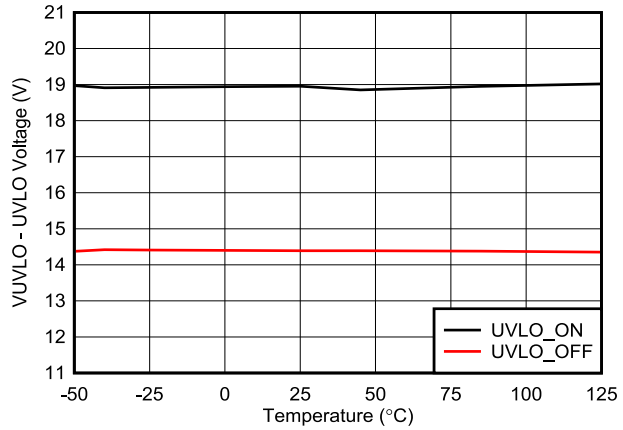
UCC28C50-Q1 and UCC28C51-Q1

图 7-11. Undervoltage Lockout vs Temperature



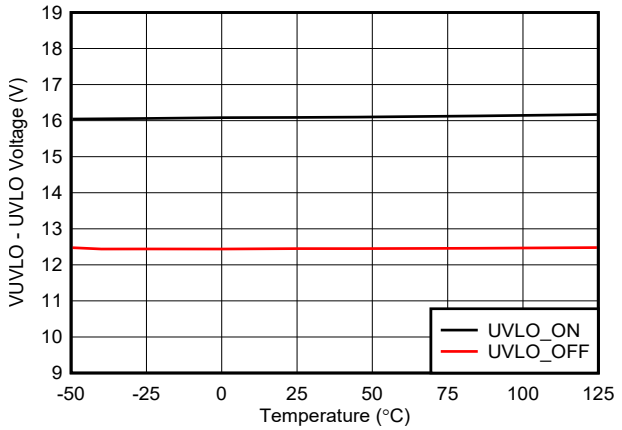
UCC28C56H-Q1 and UCC28C57H-Q1

图 7-12. Undervoltage Lockout vs Temperature



UCC28C56L-Q1 and UCC28C57L-Q1

图 7-13. Undervoltage Lockout vs Temperature



UCC28C58-Q1 and UCC28C59-Q1

图 7-14. Undervoltage Lockout vs Temperature

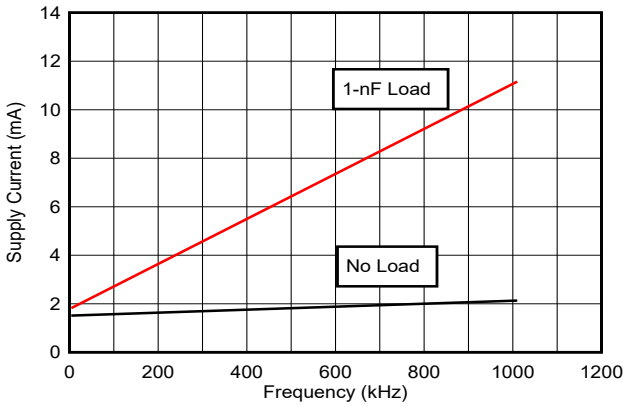
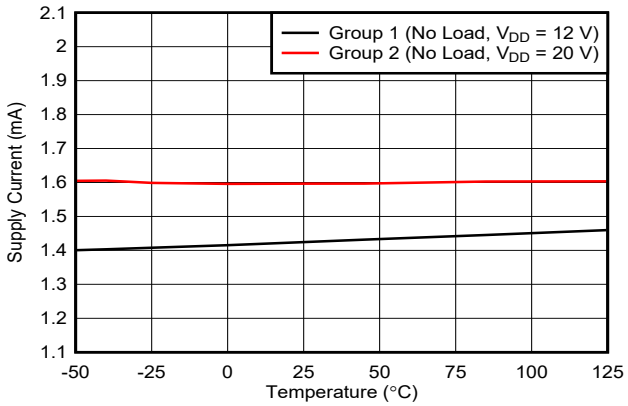


图 7-15. Supply Current vs Oscillator Frequency



Group 1: UCC28C50-Q1 to UCC28C55-Q1
Group 2: UCC28C56H-Q1 to UCC28C59-Q1

图 7-16. Supply Current vs Temperature

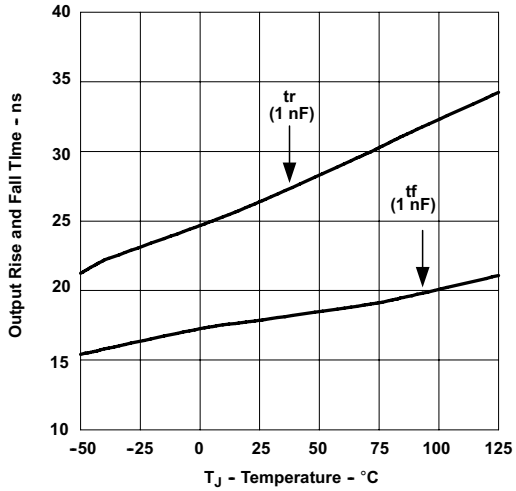


图 7-17. Output Rise Time and Fall Time vs Temperature

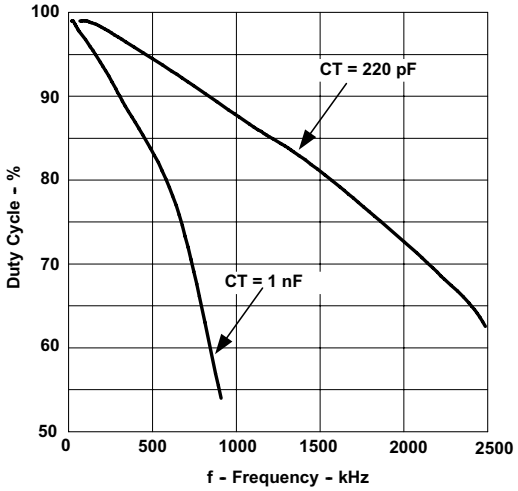
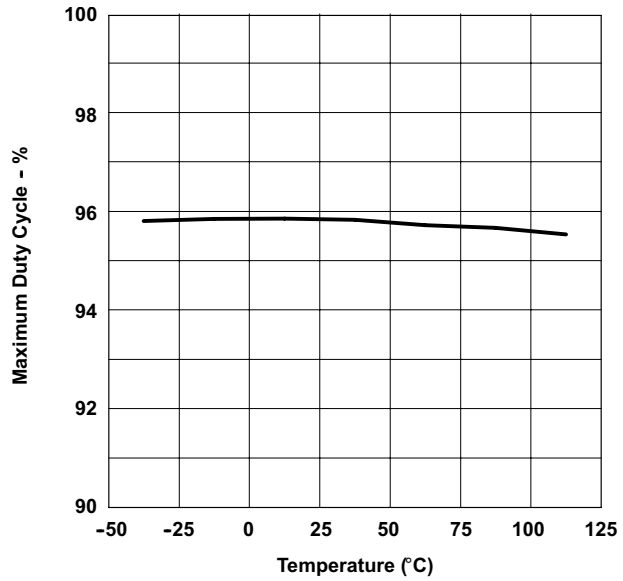
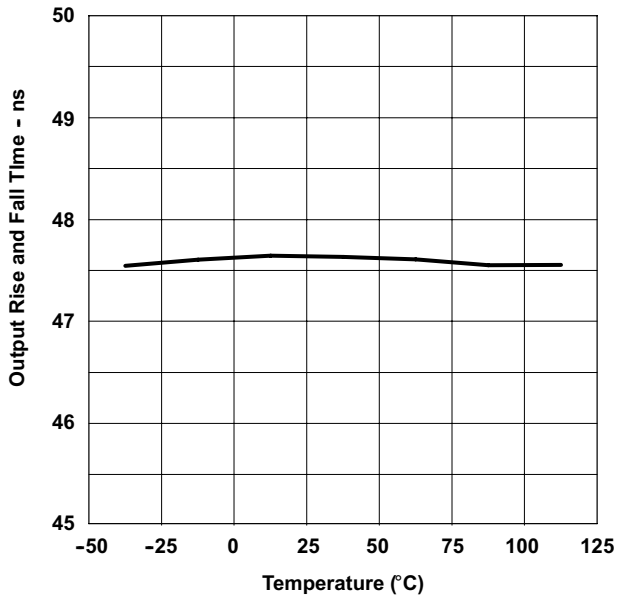


图 7-18. Maximum Duty Cycle vs Oscillator Frequency



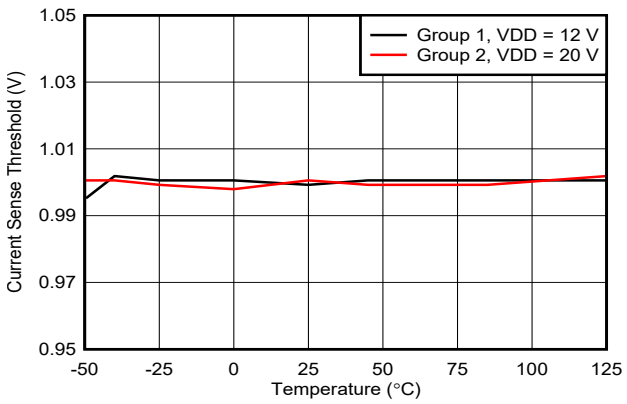
UCC28C50-Q1, UCC28C52-Q1, UCC28C53-Q1, UCC28C56H/L-Q1, and UCC28C58-Q1

图 7-19. Maximum Duty Cycle vs Temperature



UCC28C51-Q1, UCC28C54-Q1, UCC28C55-Q1, UCC28C57H/L-Q1, and UCC28C59-Q1

图 7-20. Maximum Duty Cycle vs Temperature



Group 1: UCC28C50-Q1 to UCC28C55-Q1

Group 2: UCC28C56H-Q1 to UCC28C59-Q1

图 7-21. Current Sense Threshold Voltage vs Temperature

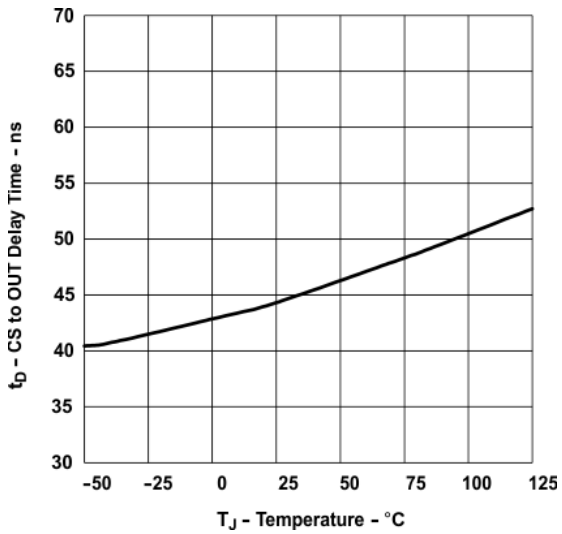


图 7-22. Current Sense to Output Delay Time vs Temperature

8 Detailed Description

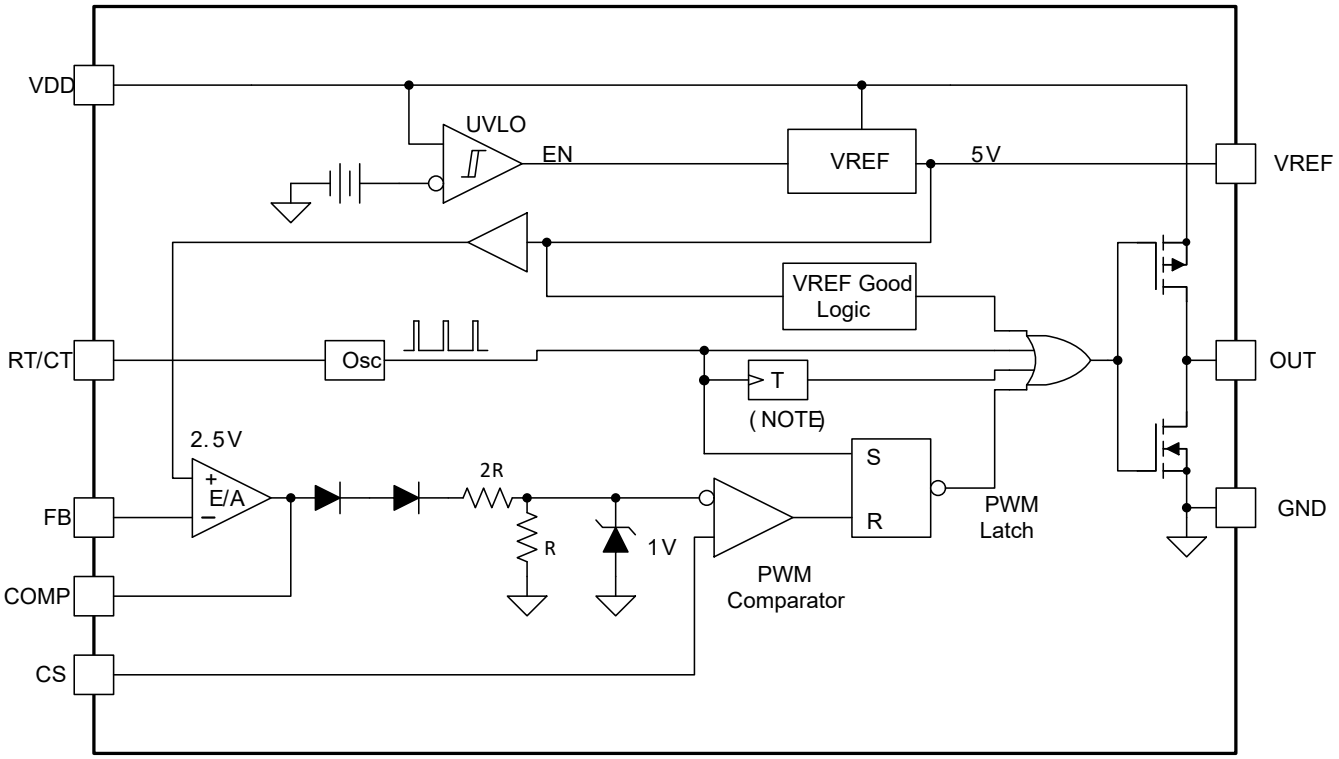
8.1 Overview

The UCC28C5x-Q1 series of control integrated circuits provide the features necessary to implement AC-DC or DC-to-DC fixed-frequency current-mode control schemes with a minimum number of external components. Protection circuitry includes undervoltage lockout (UVLO) and current limiting. Internally implemented circuits include a start-up current of less than 75 µA, a precision reference trimmed for accuracy at the error amplifier input, logic to ensure latched operation, a pulse-width modulation (PWM) comparator that also provides current-limit control, and an output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the OFF state. The oscillator contains a trimmed discharge current that enables accurate programming of the maximum duty cycle and dead time limit, making this device suitable for high-speed applications.

Major differences between members of this series are the UVLO thresholds, acceptable ambient temperature range, and maximum duty cycle and frequency. Typical UVLO thresholds of 14.5 V (ON) and 9 V (OFF) on the UCC28C52-Q1 and UCC28C54-Q1 devices make them ideally suited to off-line AC-DC applications. The corresponding typical thresholds for the UCC28C53-Q1 and UCC28C55-Q1 devices are 8.4-V (ON) and 7.6-V (OFF), making them ideal for use with regulated input voltages used in DC-DC applications. The UCC28C50-Q1 and UCC28C51-Q1 feature a start-up threshold of 7 V and a turnoff threshold of 6.6 V (OFF), which makes them suitable for battery- powered applications. The UCC28C56H/L-Q1, UCC28C57H/L-Q1, UCC28C58-Q1 and UCC28C59-Q1 operate with higher start-up thresholds for them suitably to work with SiC MOSFETs which often being used in high-voltage and high-power traction inverter applications. The UCC28C56H-Q1 and UCC28C57H-Q1 are with a start-up threshold 18.8-V (ON) and 15.5-V (OFF). The UCC28C56L-Q1 and UCC28C57L-Q1 are with a start-up threshold 18.8-V (ON) and 14.5-V (OFF). The UCC28C58-Q1 and UCC28C59-Q1 are with a start-up threshold 16-V (ON) and 12.5-V (OFF). The UCC28C50-Q1, UCC28C52-Q1, UCC28C53-Q1, UCC28C56H/L-Q1 and UCC28C58-Q1 devices operate to duty cycles approaching 100%. The UCC28C51-Q1, UCC28C54-Q1, UCC28C55-Q1, UCC28C57H/L-Q1 and UCC28C59-Q1 obtain a duty cycle from 0% to 50% by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle. The UCC28C5x series is specified for operation from –40°C to 125°C. The switching frequency (fSW) of the UCC28C50-Q1, UCC28C52-Q1, UCC28C53-Q1, UCC28C56H/L-Q1 and UCC28C58-Q1 gate drive is equal to fOSC; the switching frequency of the UCC28C51-Q1, UCC28C54-Q1, UCC28C55-Q1, UCC28C57H/L-Q1 and UCC28C59-Q1 is equal to half of the f_{OSC}.

The UCC28C5x-Q1 series are an enhanced replacement with pin-to-pin compatibility to the BiCMOS UCC28C4x- Q1 families. The new series offers improved performance when compared to older bipolar devices and other competitive BiCMOS devices with similar functionality. These improvements generally consist of tighter specification limits that are a subset of the older product ratings, maintaining drop-in capability. In new designs, these improvements can reduce the component count or enhance circuit performance when compared to the previously available devices.

8.2 Functional Block Diagram



Toggle flip-flop used only in UCC28C51-Q1, UCC28C54-Q1, UCC8C55-Q1, UCC28C57H/L-Q1, and UCC28C59-Q1

8.3 Feature Description

The BiCMOS design allows operation at high frequencies that were not feasible in the predecessor bipolar devices. First, the output stage has been redesigned to drive the external power switch in approximately half the time of the earlier devices. Second, the internal oscillator is more robust, with less variation as frequency increases. This faster oscillator makes this device suitable for high speed applications and the trimmed discharge current enables precise programming of the maximum duty cycle and dead-time limit. In addition, the current sense to output delay is kept the same 45 ns (typical) as the UCC28C4x-Q1. Such a delay time in the current sense results in superior overload protection at the power switch. The reduced start-up current of this device minimizes steady state power dissipation in the startup resistor, and the low operating current maximizes efficiency while running, increasing the total circuit efficiency, whether operating off-line, DC input, or battery operated circuits. These features combine to provide a device capable of reliable, high-frequency operation.

表 8-1. Key Parameters

PARAMETER	UCC28C4x-Q1	UCC28C5x-Q1
Supply current at 52 kHz	2.3 mA	1.3 mA
Start-up current	100 µA	75 µA
V_{DD} absolute maximum	20 V	30 V
Reference voltage accuracy	± 2%	± 1%
UVLO and D_{MAX} for Si MOSFET	6 options	6 options
UVLO and D_{MAX} for SiC MOSFET	no options	6 options

8.3.1 Detailed Pin Description

8.3.1.1 COMP

The error amplifier in the UCC28C5x-Q1 family has a unity-gain bandwidth about 1 MHz. The COMP terminal can both source and sink current. The error amplifier is internally current-limited, so that one can command zero duty cycle by externally forcing COMP to GND.

8.3.1.2 FB

FB is the inverting input of the error amplifier. The noninverting input to the error amplifier is internally trimmed to 2.5 V ± 1%. FB is used to control the power converter voltage-feedback loop for stability. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

8.3.1.3 CS

The UCC28C5x-Q1 current sense input connects directly to the PWM comparator. Connect CS to the MOSFET source current sense resistor. The PWM uses this signal to terminate the OUT switch conduction. A voltage ramp can be applied to this pin to run the device with a voltage mode control configuration or to add slope compensation. To prevent false triggering due to leading edge noises, an RC current sense filter may be required. The gain of the current sense amplifier is typically 3 V/V.

8.3.1.4 RT/CT

RT/CT is the oscillator timing pin. For fixed frequency operation, set the timing capacitor charging current by connecting a resistor from VREF to RT/CT. Set the frequency by connecting timing capacitor from RT/CT to GND. For the best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The UCC28C5x-Q1’s oscillator allows for operation to 1 MHz. The device uses an external resistor to set the charging current for the external capacitor, which determines the oscillator frequency. TI recommends timing resistor values from 1 kΩ to 100 kΩ and timing capacitor values from 220 pF to 4.7 nF. The UCC28C5x-Q1 oscillator is true to the curves of the original bipolar devices at lower frequencies, yet extends the frequency programmability range to at least 1 MHz. This allows the device to offer pin-to-pin capability where required, yet capable of extending the operational range to the higher frequencies. See 图 7-1 for component values for setting the oscillator frequency.

8.3.1.5 GND

GND is the signal and power returning ground. TI recommends separating the signal return path and the high current gate driver path so that the signal is not affected by the switching current.

8.3.1.6 OUT

The high-current output stage of the UCC28C5x-Q1 to drive the external power switch has been kept the same as the earlier devices UCC28C4x-Q1. To drive a power MOSFET directly, the totem-pole OUT driver sinks or source up to 1 A peak of current. The OUT of the UCC28C50-Q1, UCC28C52-Q1, UCC28C53-Q1, UCC28C56H/L-Q1 and UCC28C58-Q1 devices switch at the same frequency as the oscillator and can operate near 100% duty cycle. In the UCC28C51-Q1, UCC28C54-Q1, and UCC28C55-Q1, UCC28C57H/L-Q1 and UCC28C59-Q1, the switching frequency of OUT is one-half that of the oscillator due to an internal T flip-flop. This limits the maximum duty cycle in the UCC28C51-Q1, UCC28C54-Q1, UCC28C55-Q1, UCC28C57H/L-Q1 and UCC28C59-Q1 to < 50%.

The UCC28C5x-Q1 family houses unique totem pole drivers exhibiting a 10-Ω impedance to the upper rail and a 5.5-Ω impedance to ground, typically. This reduced impedance on the low-side switch helps minimize turn-off losses at the power MOSFET, whereas the higher turn-on impedance of the high-side is intended to better match the reverse recovery characteristics of many high-speed output rectifiers. Transition times, rising and falling edges, are typically 25 nanoseconds and 20 nanoseconds, respectively, for a 10% to 90% change in voltage.

A low impedance MOS structure in parallel with a bipolar transistor, or BiCMOS construction, comprises the totem-pole output structure. This more efficient utilization of silicon delivers the high peak current required along with sharp transitions and full rail-to-rail voltage swings. Furthermore, the output stage is self-biasing, active low during under-voltage lockout type. With no VDD supply voltage present, the output actively pulls low if an attempt is made to pull the output high. This condition frequently occurs at initial power-up with a power MOSFET as the driver load.

8.3.1.7 VDD

VDD is the power input connection for this device. In normal operation, power VDD through a current limiting resistor. The absolute maximum supply voltage is 30 V, extended from 20 V of UCC28C5x-Q1 to facilitate more designs and applications. The 30-V voltage, including any transients that may be present, cannot be exceeded, device damage is likely if otherwise. Hence UCC28C5x devices match the predecessor bipolar devices, which could survive up to 30 V on the input bias pin. But still, no internal clamp is included in the device, the VDD pin must be protected from external sources which could exceed the 30 V level. If containing the start-up and bootstrap supply voltage from the auxiliary winding N_A below 30 V under all line and load conditions can not be achieved, use a zener protection diode from VDD to GND. Depending on the impedance and arrangement of the bootstrap supply, this may require adding a resistor, R_{VDD}, in series with the auxiliary winding to limit the current into the zener as shown in 图 8-1. Insure that over all tolerances and temperatures, the minimum zener voltage is higher than the highest UVLO upper turn-on threshold. To ensure against noise related problems, filter VDD with a ceramic bypass capacitor to GND. The VDD pin must be decoupled as close to the GND pin as possible.

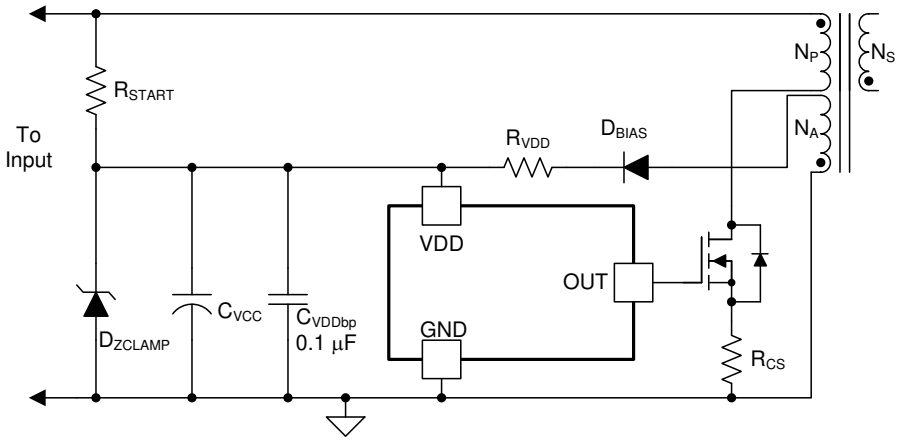


图 8-1. VDD Protection

Although nominal VDD operating current is only 1.3 mA, the total supply current is higher, depending on the OUT current. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from 方程式 1.

$$I_{OUT} = Q_g \times f_{SW} \quad (1)$$

8.3.1.8 VREF

VREF is the voltage reference for the error amplifier and also for many other internal circuits in the device. The 5-V reference tolerance is ±1% for the UCC28C5x-Q1 family. The high-speed switching logic uses VREF as the logic power supply. The reference voltage is divided down internally to 2.5 V ±1% and connected to the error amplifier's noninverting input for accurate output voltage regulation. The reference voltage sets the internal bias currents and thresholds for functions such as the oscillator upper and lower thresholds along with the overcurrent limiting threshold. The output short-circuit current is 55 mA (maximum). To avoid device over-heating and damage, do not pull VREF to ground as a means to terminate switching. For reference stability and to prevent noise problems with high-speed switching transients, bypass VREF to GND with a ceramic capacitor close to thedevicepackage. A minimum of 0.1-µF ceramic capacitor is required. Additional VREF bypassing is required for external loads on the reference. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

8.3.2 Undervoltage Lockout

Six sets of UVLO thresholds are available with turn-on and turnoff thresholds of: (14.5 V and 9 V), (8.4 V and 7.6 V), (7 V and 6.6 V), (18.8 V and 15.5 V), (18.8 V and 14.5V) and (16 V and 12.5V), respectively. The first set is primarily intended for off-line and 48-V distributed power applications, where the wider hysteresis allows for lower frequency operation and longer soft-starting time of the converter. The second set of UVLO option is ideal for high frequency DC-DC converters typically running from a 12-VDC input. The third set is for battery powered and portable applications. The fourth to sixth UVLO sets are to drive SiC MOSFETs in High Voltage applications. 表 8-2 shows the maximum duty cycle and UVLO thresholds by device.

表 8-2. UVLO Options

MAXIMUM DUTY CYCLE	UVLO ON	UVLO OFF	PART NUMBER
100%	14.5 V	9 V	UCC28C52-Q1
100%	8.4 V	7.6 V	UCC28C53-Q1
100%	7 V	6.6 V	UCC28C50-Q1
100%	18.8 V	15.5 V	UCC28C56H-Q1
100%	18.8 V	14.5 V	UCC28C56L-Q1
100%	16 V	12.5 V	UCC28C58-Q1
50%	14.5 V	9 V	UCC28C54-Q1
50%	8.4 V	7.6 V	UCC28C55-Q1
50%	7 V	6.6 V	UCC28C51-Q1
50%	18.8 V	15.5 V	UCC28C57H-Q1
50%	18.8 V	14.5 V	UCC28C57L-Q1
50%	16 V	12.5 V	UCC28C59-Q1

During UVLO the device draws less than 75 µA of supply current. Once crossing the turn-on threshold the device supply current increases to a maximum of 2 mA, typically 1.3 mA. This low start-up current allows the power supply designer to optimize the selection of the start-up resistor value to provide a more efficient design. In applications where low component cost overrides maximum efficiency, the low run current of 1.3 mA (typical) allows the control device to run directly through the single resistor to (+) rail, rather than requiring a bootstrap winding on the power transformer, along with a rectifier. The start and run resistor for this case must also pass enough current to allow driving the primary switching MOSFET, which may be a few milliamps in small devices.

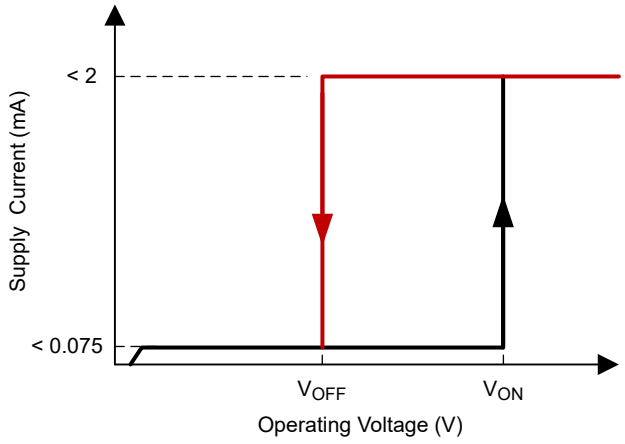


图 8-2. UVLO ON and OFF Profile

8.3.3 ±1% Internal Reference Voltage

The BiCMOS internal reference of 2.5 V has an enhanced design, and uses production trim to allow initial accuracy of ±1% at room temperature and ±2% over the full temperature range. This can be used to eliminate an external reference in applications that do not require the extreme accuracy afforded by the additional device. This is useful for non-isolated DC-DC applications, where the control device is referenced to the same common as the output. It is also applicable in off-line designs that regulate on the primary side of the isolation boundary by looking at a primary bias winding, or from a winding on the output inductor of a buck-derived circuit.

8.3.4 Current Sense and Overcurrent Limit

An external series resistor (R_{CS}) senses the current and converts this current into a voltage that becomes the input to the CS pin. The CS pin is the noninverting input to the PWM comparator. The CS input is compared to a signal proportional to the error amplifier output voltage; the gain of the current sense amplifier is typically 3 V/V. The peak I_{SENSE} current is determined using 方程式 2

$$I_{SENSE} = \frac{V_{CS}}{R_{CS}} \tag{2}$$

The typical value for V_{CS} is 1 V. A small RC filter (R_{CSF} and C_{CSF}) may be required to suppress switch transients caused by the reverse recovery of a secondary side diode or equivalent capacitive loading in addition to parasitic circuit impedances. The time constant of this filter should be considerably less than the switching period of the converter.

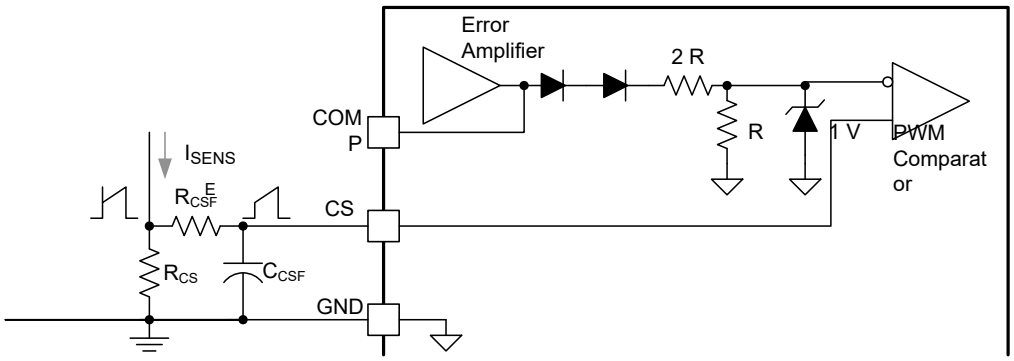


图 8-3. Current-Sense Circuit Schematic

Cycle-by-cycle pulse width modulation performed at the PWM comparator essentially compares the error amplifier output to the current sense input. This is not a direct volt-to-volt comparison, as the error amplifier output network incorporates two diodes in series with a resistive divider network before connecting to the PWM comparator. The two-diode drop adds an offset voltage that enables zero duty cycle to be achieved with a low amplifier output. The 2R/R resistive divider facilitates the use of a wider error amplifier output swing that can be more symmetrically centered on the 2.5-V noninverting input voltage.

The 1-V zener diode associated with the PWM comparator’s input from the error amplifier is not an actual diode in the device’s design, but an indication that the maximum current sense input amplitude is 1 V (typical). When this threshold is reached, regardless of the error amplifier output voltage, cycle-by-cycle current limiting occurs, and the output pulse width is terminated within 35 ns (typical). The minimum value for this current limit threshold is 0.9 V with a 1.1-V maximum. In addition to the tolerance of this parameter, the accuracy of the current sense resistor, or current sense circuitry, must be taken into account. It is advised to factor in the worst case of primary and secondary currents when sizing the ratings and worst-case conditions in all power semiconductors and magnetic components.

8.3.5 Reduced-Discharge Current Variation

The UCC28C5x-Q1 oscillator design incorporates a trimmed discharge current to accurately program maximum duty cycle and operating frequency. In its basic operation, a timing capacitor (C_{CT}) is charged by a current source, formed by the timing resistor (R_{RT}) connected to the device's reference voltage (VREF). The oscillator design incorporates comparators to monitor the amplitude of the timing capacitor's voltage. The exponentially shaped waveform charges up to a specific amplitude representing the oscillator's upper threshold of 2.5 V. Once reached, an internal current sink to ground is turned on and the capacitor begins discharging. This discharge continues until the oscillator's lower threshold has reached 0.7 V at which point the current sink is turned off. Next, the timing capacitor starts charging again and a new switching cycle begins.

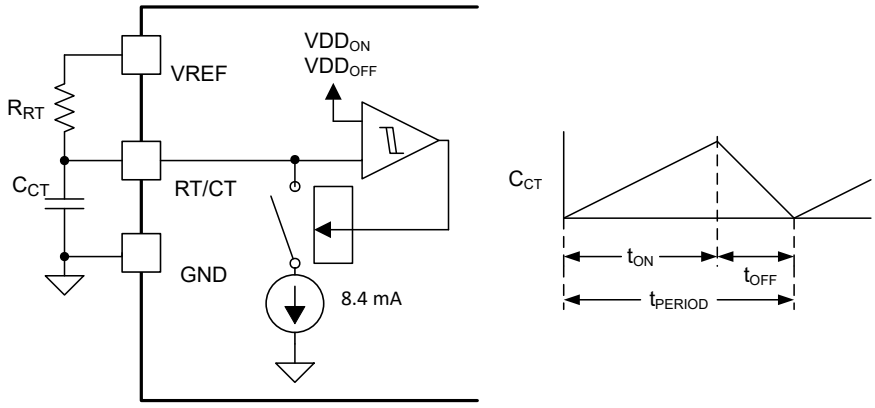


图 8-4. Oscillator Circuit

While the device is discharging the timing capacitor, resistor R_{RT} is also still trying to charge C_{CT}. It is the exact ratio of these two currents, the discharging versus the charging current, which specifies the maximum duty cycle. During the discharge time of C_{CT}, the device's output is always off. This represents an ensured minimum off time of the switch, commonly referred to as dead-time. To program an accurate maximum duty cycle, use the information provided in 图 7-18 for maximum duty cycle versus oscillator frequency. Any number of maximum duty cycles can be programmed for a given frequency by adjusting the values of R_{RT} and C_{CT}. Once R_{RT} is selected, the oscillator timing capacitor can be found using the curves in 图 7-1. However, because resistors are available in more precise increments, typically 1%, and capacitors are only available in 5% accuracy, it might be more practical to select the closest capacitor value first and then calculate the timing resistor value next.

8.3.6 Oscillator Synchronization

Synchronization is best achieved by forcing the timing capacitor voltage above the oscillator's internal upper threshold. A small resistor is placed in series with C_{CT} to GND. This resistor serves as the input for the sync pulse which raises the C_{CT} voltage above the oscillator’ s internal upper threshold. The PWM is allowed to run at the frequency set by R_{RT} and C_{CT} until the sync pulse appears. This scheme offers several advantages including having the local ramp available for slope compensation. The UCC28C5x-Q1 oscillator must be set to a lower frequency than the sync pulse stream, typically 20 percent with a 0.5-V pulse applied across the resistor.

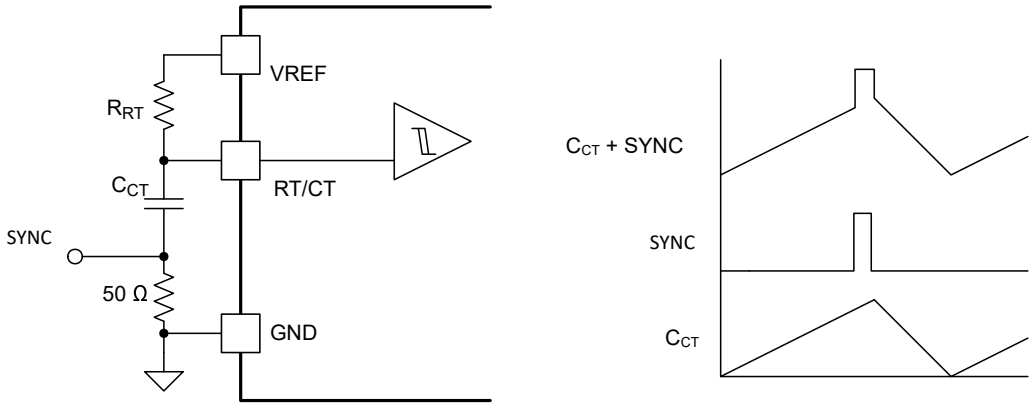


图 8-5. Oscillator Synchronization Circuit

8.3.7 Soft Start

Soft start is the technique to gradually power up the converter in a well-controlled fashion by slowly increasing the effective duty cycle starting at zero and gradually rising. Following start-up of the PWM, the error amplifier inverting input is low, commanding the error amplifier’s output to go high. The output stage of the amplifier can source 1 mA typically, which is enough to drive most high impedance compensation networks, but not enough for driving large loads quickly. Soft start is achieved by charging a fairly large value, >1-µF, capacitor (C_{SS}) connected to the error amplifier output through a PNP transistor as shown in 图 8-6

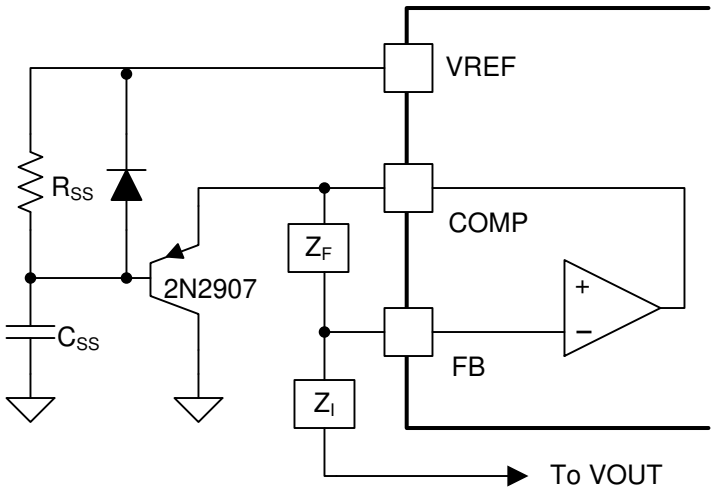


图 8-6. Soft-Start Implementation

The limited charging current of the amplifier into the capacitor translates into a dv/dt limitation on the error amplifier output. This directly corresponds to some maximum rate of change of primary current in a current mode controlled system as one of the PWM comparator’s inputs gradually rises. The values of R_{SS} and C_{SS} must be selected to bring the COMP pin up at a controlled rate, limiting the peak current supplied by the power stage. After the soft-start interval is complete, the capacitor continues to charge to VREF, effectively removing the PNP transistor from the circuit consideration. Soft start performs a different, frequently preferred function in current mode controlled systems than it does in voltage mode control. In current mode, soft start controls the rising of the peak switch current. In voltage mode control, soft start gradually widens the duty cycle, regardless of the primary current or rate of ramp-up.

The purpose of the resistor R_{SS} and diode is to take the soft-start capacitor out of the error amplifier’s path during normal operation, once soft start is complete and the capacitor is fully charged. The optional diode in parallel with the resistor forces a soft start each time the PWM goes through UVLO condition that forces VREF to go low. Without the diode, the capacitor remains charged during a brief loss of supply or brown-out, and no soft start is enabled upon re-application of VDD.

8.3.8 Enable and Disable

There are a few ways to enable or disable the UCC28C5x-Q1 devices, depending on which type of restart is required. The two basic techniques use external transistors to either pull the error amplifier output low (< 2 V_{BE}) or pull the current sense input high (> 1.1 V). Application of the disable signal causes the output of the PWM comparator to be high. The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or CS pin is removed. Another choice for restart without a soft start is to pull the current sense input above the cycle-by-cycle current limiting threshold. A logic level P-channel FET from the reference voltage to the current sense input can be used.

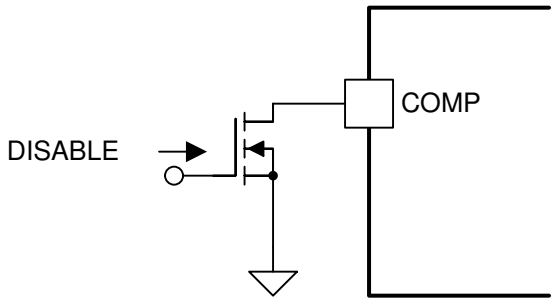


图 8-7. Disable Circuit

8.3.9 Slope Compensation

With current mode control, slope compensation is required to stabilize the overall loop with duty cycles exceeding 50%. Although not required, slope compensation also improves stability in applications using below a 50% maximum duty cycle. Slope compensation is introduced by injecting a portion of the oscillator waveform to the actual sensed primary current. The two signals are summed together at the current sense input (CS) connection at the filter capacitor. To minimize loading on the oscillator, it is best to buffer the timing capacitor waveform with a small transistor whose collector is connected to the reference voltage.

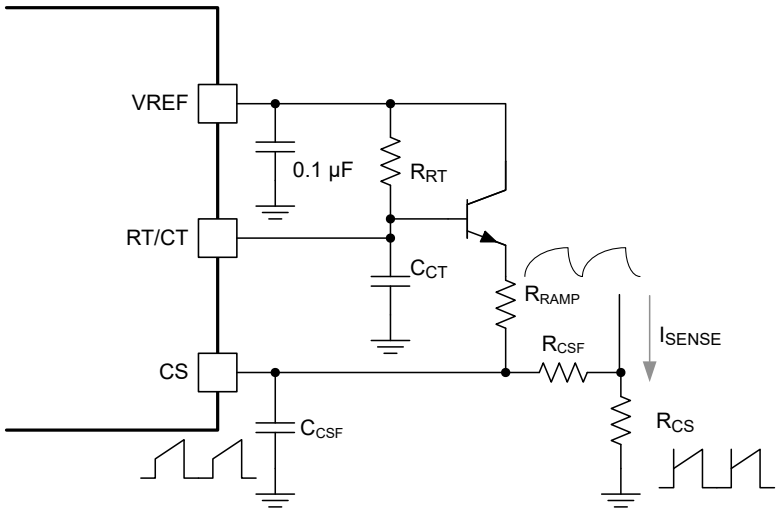


图 8-8. Slope Compensation Circuit

8.3.10 Voltage Mode

In certain applications, voltage mode control may be a preferred control strategy for a variety of reasons. Voltage mode control is easily executable with any current mode controller, especially the UCC28C5x-Q1 family members. Implementation requires generating a 0-V to 0.9-V sawtooth shaped signal to input to the current sense pin (CS) which is also one input to the PWM comparator. This is compared to the divided down error amplifier output voltage at the other input of the PWM comparator. As the error amplifier output is varied, it intersects the sawtooth waveform at different points in time, thereby generating different pulse widths. This is a straightforward method of linearly generating a pulse whose width is proportional to the error voltage.

Implementation of voltage mode control is possible by using a fraction of the oscillator timing capacitor (C_{CT}) waveform. This can be divided down and fed to the current sense pin as shown in 图 8-9. The oscillator timing components must be selected to approximate as close to a linear sawtooth waveform as possible. Although exponentially charged, large values of timing resistance and small values of timing capacitance help approximate a more linear shaped waveform. A small transistor is used to buffer the oscillator timing components from the loading of the resistive divider network.

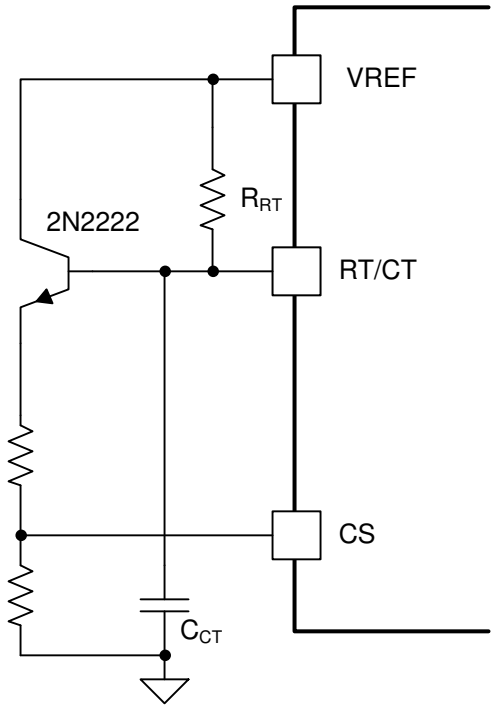


图 8-9. Current Mode PWM Used as a Voltage Mode PWM

8.4 Device Functional Modes

8.4.1 Normal Operation

During normal operating mode, the controller can be used in peak current mode or voltage mode control. When the converter is operating in peak current mode, the controller regulates the converter's peak current and duty cycle. When used in voltage mode control, the controller regulates the power converter's duty cycle. The regulation of the system's peak current and duty cycle can be achieved with the use of the integrated error amplifier and external feedback circuitry.

8.4.2 UVLO Mode

During the system start-up, VDD voltage starts to rise from 0 V. Before the VDD voltage reaches its corresponding turnon threshold, thedeviceis operating in UVLO mode. In this mode, the VREF pin voltage is not generated. When VDD is above 1 V and below the turnon threshold, the VREF pin is actively pulled low. This way, VREF can be used as a logic signal to indicate UVLO mode. If the bias voltage to VDD drops below the UVLO-OFF threshold, the PWM switching stops and VREF returns to 0 V. The device can be restarted by applying a voltage greater than the UVLO-ON threshold to the VDD pin.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The UCC28C5x-Q1 controllers are peak current mode pulse width modulators. These controllers have an integrated error amplifier and can be used in isolated or nonisolated power supply designs. There is an on-chip gate driver capable of delivering 1 A of peak current. This is a high-speed PWM capable of operating at switching frequencies up to 1 MHz. 图 9-1 shows a typical high-voltage input application with UCC28C56H-Q1.

9.2 Typical Application

A typical application for the UCC28C56H-Q1 in an 800-V_{TYP} flyback converter utilizing a single 1700-V SiC MOSFET is shown in 图 9-1. The UCC28C56H-Q1 uses an inner current control loop that contains a small current sense resistor which senses the primary inductor current ramp. This current sense resistor transforms the inductor current waveform to a voltage signal that is input to the PWM comparator. This inner loop determines the response to input voltage changes. An outer voltage control loop involves comparing a portion of the output voltage to a reference voltage at the input to an error amplifier. The bandwidth of the outer voltage control loop determines the response to load changes.

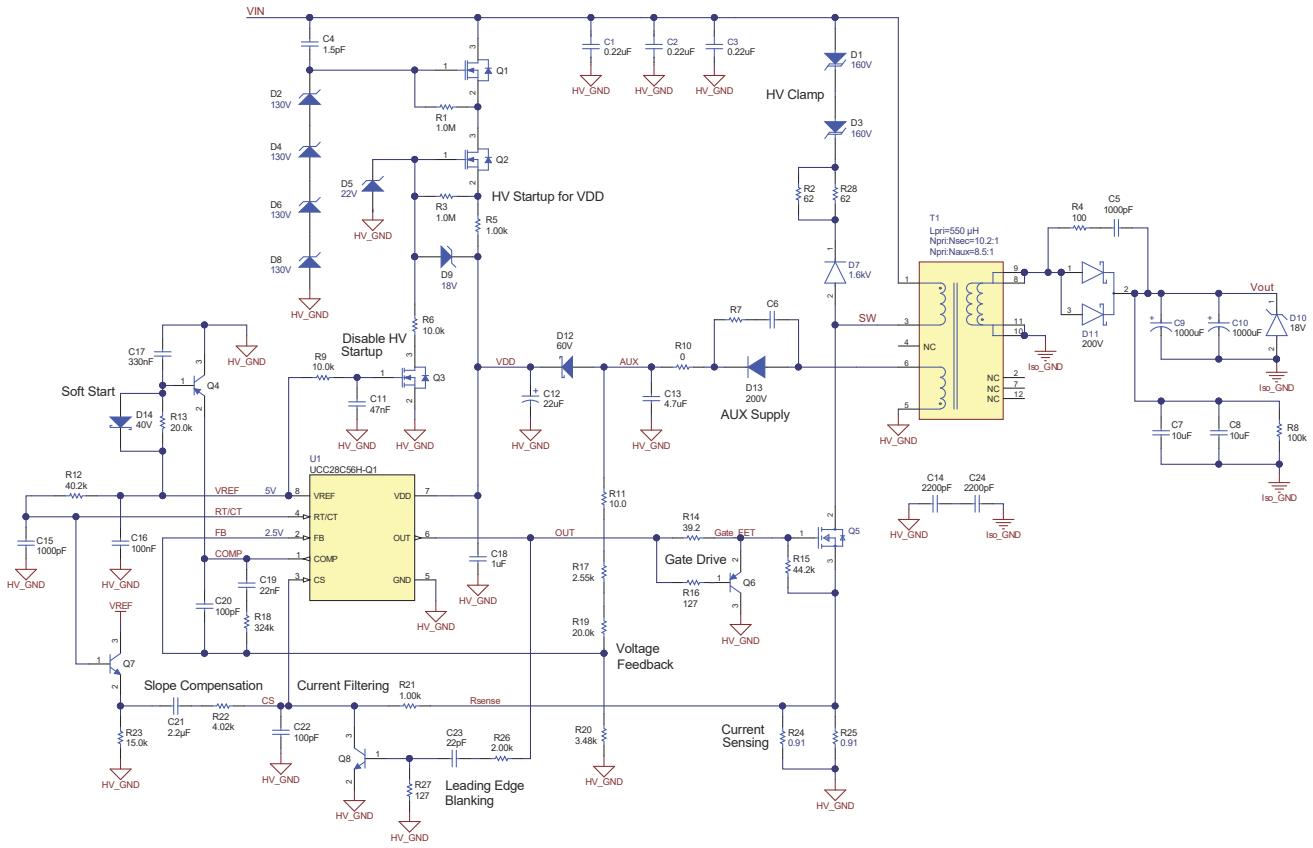


图 9-1. Typical Flyback Application Schematic

9.2.1 Design Requirements

表 9-1 shows a typical set of performance requirements for a high-voltage flyback converter capable of delivering 15 V output from a 40 V to 1000 V DC input. From 125 V to 1000 V input, the converter can deliver 40 W. From 40 V to 125 V input, the converter is derated to deliver 20 W. To minimize the transformer size and reduce losses, the power stage is designed such that it operates in discontinuous conduction mode (DCM) at high input voltage and very near transition mode at low input voltage. In DCM mode (i.e. relatively high input voltage) the magnetizing current is reset to zero before the start of the next PWM cycle. Compared to continuous conduction mode (CCM), DCM provides the advantage of very low turn-on switching losses, even at high V_{IN}, because the current always starts from 0A. Also, in DCM mode, the output rectifier current decays to zero before the next switching event. Therefore, DCM eliminates the reverse recovery losses of the output rectifier, unlike CCM.

The peak power of the converter is designed to support 48 W, 120 % higher than the nominal 40 W.

表 9-1. Design Parameters

PARAMETER		OPERATING CONDITIONS	MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage		40	800	1000	V_{DC}
V_{OUT}	Output Voltage	0.2 A ⩽ I_{OUT} ⩽ I_{OUT_FL}	14	15	16	V_{DC}
I_{OUT_FL}	Full-Load Output Current	125 V ⩽ V_{IN} ⩽ 1000 V			2.7	A
		40 V ⩽ V_{IN} < 125 V			1.3	A
f_{SW}	Switching Frequency			42.5		kHz
D_{VIN_MIN}	Duty Cycle at V_{IN_MIN}			80		%
V_{RIPPLE}	Output Voltage Ripple				0.5	V_{PP}

9.2.2 Detailed Design Procedure

This procedure outlines the steps to design a discontinuous current mode (DCM) flyback converter utilizing the UCC28C56H-Q1. However, it could be adopted for any of the controllers in the UCC28C5x family and other input/output voltages. See 图 9-1 for component reference designators referred to in the design procedure.

9.2.2.1 Primary-to-Secondary Turns Ratio of the Flyback Transformer (NPS)

To start, we need to estimate the forward voltage (V_F) of the output Schottky diode and the on-time of the MOSFET (t_{ON_EST})

$$V_F = 0.5V \tag{3}$$

$$t_{ON\_EST} = \frac{D_{VIN\_MIN}}{f_{SW}} = \frac{0.80}{42.5\ kHz} = 18.8\ \mu s \tag{4}$$

Next, estimate the transformer primary-to-secondary turns ratio

$$N_{PS} = \frac{V_{IN\_MIN} \times t_{ON\_EST}}{\left(\frac{1}{f_{SW}} - t_{ON\_EST}\right) \times \left(V_{OUT} + V_F\right)} = \frac{40\ V \times 18.8\ \mu s}{\left(\frac{1}{42.5\ kHz} - 18.8\ \mu s\right) \times \left(15\ V + 0.5\ V\right)} = 10.3 \tag{5}$$

Calculate the reverse withstand voltage of output rectifier diode during t_{ON_EST}

$$V_{SEC\_REV} = V_{OUT} + \frac{V_{IN\_MAX}}{N_{PS}} = 15\ V + \frac{1000\ V}{10.3} = 112\ V \tag{6}$$

Calculate the (expected) drain-to-source voltage of the MOSFET during the off time

$$V_{DS\_OFF} = V_{IN\_MAX} + (V_{OUT} + V_F) \times N_{PS} = 1000\,V + (15\,V + 0.5\,V) \times 10.3 = 1160\,V \quad (7)$$

The switching MOSFET and output rectifier generally experience voltage ringing due to transformer leakage and parasitic capacitance. Based on V_{SEC_REV}, a 200V-rated Schottky diode is chosen, so the secondary RC snubber can damp the voltage spike and ringing with reduced snubber power loss. Based on V_{DS_OFF}, a 1.7kV-rated SiC MOSFET is chosen, so a higher breakdown voltage of the primary TVS diode clamping circuit can clamp the switching voltage stress caused by the transformer leakage with reduced clamping power loss. If V_{DS_OFF} is too high, the turns ratio can be reduced by decreasing D_{VIN_MIN}, but V_{SEC_REV} will increase. Deciding which component voltage is more critical and iterate again if necessary.

9.2.2.2 Primary Magnetizing Inductance of the Flyback Transformer (LM)

Calculate the maximum primary magnetizing inductance (L_{M_CRIT}) to maintain DCM operation at full load and minimum input voltage using the following equation

$$L_{M\_CRIT} = \frac{V_{IN\_MIN} \times D_{VIN\_MIN} \times (1 - D_{VIN\_MIN}) \times N_{PS}}{2 \times f_{SW} \times I_{OUT}} = \frac{40\,V \times 0.80 \times (1 - 0.80) \times 10.3}{2 \times 42.5\,kHz \times 1.3\,A} = 597\,\mu H \quad (8)$$

To account for the inductance variance, a typical L_M of 550 µH is used in the following calculation. P_{O_MAX} occurs when the CS-pin voltage reaches at 1 V. P_{O_MAX} determines the maximum output power of the flyback converter, set 120% larger than the full-load output power of 40 W. Then, the maximum peak magnetizing current (I_{M_MAX}) can be calculated as

$$I_{M\_MAX} = \sqrt{\frac{2 \times P_{O\_MAX}}{L_M \times f_{SW} \times \eta}} = \sqrt{\frac{2 \times (40\,W \times 120\,\%)}{550\,\mu H \times 42.5\,kHz \times 0.85}} = 2.2\,A \quad (9)$$

9.2.2.3 Number of Turns of the Flyback Transformer Windings

The turns number of primary winding (N_P) and the cross-section area of transformer core (A_E) is chosen to ensure the maximum flux density (B_{MAX}) of transformer core is lower than the saturation flux density (B_{SAT}) at highest core temperature. In this example, the EFD30 core size with A_E of 0.69 cm^2 is used.

$$N_P = \frac{L_M \times I_{M\_MAX}}{B_{MAX} \times A_E} = \frac{550\,\mu H \times 2.2\,A}{0.34\,T \times 0.69\,cm^2} \approx 51\,turns \quad (10)$$

The number of turns of the secondary winding (N_S) can be calculated with N_{PS}, calculated previously. N_S and N_P are adjusted to the nearest suitable integers. Therefore, the new N_{PS} is changed from 10.3 to 10.2 for practical integer turns.

$$N_S = \frac{N_P}{N_{PS}} = \frac{51}{10.2} = 5\,turns \quad (11)$$

The turns number of auxiliary winding (N_{AUX}) needs to consider the targeted rectified auxiliary winding voltage (V_{AUX}) and the forward voltage of the rectifier diode (V_{F_DAUX}), since V_{AUX} determines the gate driver voltage on the SiC MOSFET which strongly affects its optimal R_{DS_ON}.

$$N_{AUX} = \frac{(V_{AUX} + V_{F\_DAUX}) \times N_S}{(V_{OUT} + V_F)} = \frac{(18\,V + 0.5\,V) \times 5}{(15\,V + 0.5\,V)} \approx 6\,turns \quad (12)$$

9.2.2.4 Current Sense Resistors (R24, R25) and Current Limiting

An external series resistor (R_{CS}) senses the current and converts this current into a voltage that becomes the input to the CS pin. The CS pin is the noninverting input to the PWM comparator. The CS input is compared to a signal proportional to the error amplifier output voltage. Calculate the current sense resistor based on the 2.2-A peak magnetizing current at P_{O_MAX} of 48 W.

$$R_{CS} = \frac{V_{CS\_MAX}}{I_{M\_MAX}} = \frac{1\,V}{2.2\,A} = 0.455\,\Omega \tag{13}$$

For any input voltage, if the output is shorted to ground or the output voltage ramps up quickly during soft-start, the controller duty cycle can easily reach the maximum duty cycle (D_{MAX}), so the power rating of the R_{CS} resistor(s) must maintain adequate design margin to support those transient events.

$$I_{PRI\_RMS\_MAX} = I_{M\_MAX} \times \sqrt{\frac{D_{MAX}}{3}} = 1.24\,A \tag{14}$$

$$P_{RCS} = {I_{RMS\_MAX}}^2 \times R_{CS} = 0.7\,W \tag{15}$$

The applications schematic shows two 0.91-Ω resistors that are 2010 size in parallel, R24 and R25, for a combined resistance of 0.455 Ω. Each can handle 0.55 W at 105°C ambient and 1 W below 70°C ambient. For a traction inverter at 105°C ambient, the two paralleled resistors can handle the worst case and offer enough margin from resistor mismatch.

9.2.2.5 Primary Clamp Circuit (D7, D1, D3, R2, R28) to Limit Voltage Stress

At turn-off a high voltage spike appears on the MOSFET due to the transformer’s leakage inductance. This voltage spike can exceed the MOSFETs maximum V_{DS} rating, leading to failure of the device. Therefore, a clamping circuit is required. There are two types of clamping circuits: the RCD clamp and the diode-zener (or TVS) clamp. The TVS clamp provides better light-load efficiency and lower input power at no load than the RCD clamp because the TVS may not activated at lighter output load. The RCD clamp offers additional damping of parasitic ringing and improved EMI. The TVS diode clamp is used in this design example. The series resistor (R_{CLAMP}), R2 // R8 in the schematic, creates a snubber effect for the TVS diode clamp for improved EMI, but the voltage stress on V_{DS} is increased.

The total clamping voltage (V_{CLAMP}) is designed to meet the 90% derating of the primary MOSFET at V_{IN_MAX}. V_{CLAMP} also needs to be higher than the reflected voltage on primary to limit the clamping loss. Two TVS diodes, D1 and D3, are connected in series to share the high clamping loss at full load. In the schematic, each 160-V clamp diode exhibits about 200 V at peak current, so the equivalent V_{CLAMP} is around 400V.

The maximum and minimum clamp voltages can be calculated with the following equations.

$$V_{CLAMP\_MAX} < V_{DS\_MAX} \times 90\% - V_{IN_{MAX}} - I_{M\_MAX} \times R_{CLAMP} = 1.7\,kV \times 0.9 - 1\,kV - 2.2\,A \times 31\,\Omega = 461\,V \tag{16}$$

$$V_{CLAMP\_MIN} > (V_{OUT} + V_F) \times N_{PS} = (15\,V + 0.5\,V) \times 10.2 = 158\,V \tag{17}$$

The voltage rating of the series rectifier diode (D7) needs to be higher than 1.4 kV, which is the summation of 1000 V_{IN_MAX} and 400 V_{CLAMP}, so a 1.6 kV device is chosen assuming 90% derating. Instead of an ultra-fast type, the slow-recovery P/N junction diode should be considered, so that the reverse recovery could help to damp the high-frequency ringing after clamping and also recycle partial leakage energy to secondary side for increased converter efficiency.

9.2.2.6 Primary-Side Current Stress and Input Capacitor Selection

The input capacitors must be rated for the maximum input voltage, limit the input voltage ripple, and support the required RMS current. The primary peak current (I_{M_VIN}) and duty cycle (D_{VIN}) at any input voltage (V_{IN}) can be derived with the following equations

$$I_{M\_VIN} = \sqrt{\frac{2 \times P_O}{L_M \times f_{SW} \times \eta}} \tag{18}$$

$$D_{VIN} = \frac{I_M \times L_M}{V_{IN}} f_{SW} \tag{19}$$

The minimum input capacitance (C_{IN_MIN}) and RMS current (I_{CIN_RMS}) they must support can be estimated with the following

$$C_{IN\_MIN} = \frac{I_M \times D_{VIN}}{2 \times f_{SW} \times V_{IN\_RIPPLE}} \tag{20}$$

$$I_{CIN\_RMS} = \sqrt{\frac{I_M{}^2 \times D_{VIN}}{3} - \left(\frac{P_O}{V_{IN} \times \eta}\right)^2} \tag{21}$$

Assuming 30% input voltage ripple for both 20 W at 40-V and 40 W at 125-V, the required minimum input capacitance is calculated for each case based on the above equations. C_{IN_MIN} at 40-V input is 1.15 µF, while C_{IN_MIN} at 125-V input is only 0.24 µF.

Low voltage operation requires almost 5x more input capacitance to produce the same percentage of input voltage ripple. If the input of auxiliary power supply is tapped to the input of the system power converters, such as the back-up power supply of traction inverters, the input capacitance of the power converters may be sufficient to meet the C_{IN_MIN} requirement at 40-V input. Therefore, the design example only parallels 2-3 high-voltage film capacitors near the regulator for high frequency decoupling.

9.2.2.7 Secondary-Side Current Stress and Output Capacitor Selection

Similar to the input capacitors, the output capacitors must limit the voltage ripple and support an RMS current. However, for DCM operation, the high peak secondary current results in a relatively substantial RMS current in the output capacitors, usually requiring multiple capacitors in parallel.

First, estimate the maximum ESR of the output capacitors (R_{ESR_MAX}) based on the output ripple requirement and highest secondary peak current at full load (I_{SEC_PEAK}). When an electrolytic capacitor is used, the output ripple magnitude is mainly determined by the ESR ripple. Paralleling the two output capacitors, C9 and C10, reduces the total ESR less than R_{ESR_MAX}.

$$I_{SEC\_PEAK} = N_{PS}\sqrt{\frac{2 \times 40\ W}{L_M \times f_{SW} \times \eta}} = 20.5\ A \tag{22}$$

$$R_{ESR\_MAX} = \frac{V_{OUT\_RIPPLE}}{I_{SEC\_PEAK}} = \frac{0.5\ V}{20.5\ A} = 24\ m\Omega \tag{23}$$

Next, calculate the minimum required output capacitance to meet the output voltage ripple requirement assuming full-load and 90% of R_{ESR_MAX}

$$C_{OUT} \geq \frac{I_{OUT} \times (1 - D_{VIN})}{(V_{OUT\_RIPPLE} - I_{SEC\_PEAK} \times 90\% \times R_{ESR\_MAX}) \times f_{SW}} = 1196\ \mu F \tag{24}$$

Finally, calculate the RMS current the output capacitors must withstand at full load (I_{COUT_RMS}), considering the demagnetizing time (i.e. duty cycle (D_{DEMAG})) during DCM operation. Note that paralleling two or more output capacitors, C9 and C10, shares the total RMS current and also reduces the power loss contributed by the ESR.

$$D_{DEMAG} = \frac{I_{M\_FL} \times L_M}{(V_{OUT} + V_F) \times N_{PS}} \times f_{SW} = 0.297 \quad (25)$$

$$I_{COUT\_RMS} = \sqrt{\frac{{I_{SEC\_PEAK}}^2 \times D_{DEMAG}}{3} - {I_{OUT}}^2} = 6.45\ A \quad (26)$$

9.2.2.8 VDD Capacitors (C12, C18)

During high-voltage (HV) startup from V_{IN}, capacitor C12 must hold the VDD voltage above the UVLO turn-off threshold until the AUX voltage rises high enough to forward bias D12. If the value of C12 is not high enough the VDD voltage will decay below the UVLO turn-off threshold and the converter will prematurely stop switching. The controller will continuously cycle on-and-off as the VDD voltage transitions between UVLO turn-on and UVLO turn-off. One of the most common issues seen with new designs is the VDD capacitor value is too low and “there's no output voltage” or "it's not starting" is reported.

First, estimate a total HV soft start time, t_{SS}. This estimate must include: (1) time for the COMP voltage to rise from 0 V to the PWM switching threshold (COMP to CS offset, 1.15 V_{TYP}), and (2) time for the AUX voltage (on C13) to rise from 0 V until it forward biases D12. Typical values are 1-2 ms for the COMP rise time and 10-14 ms for the AUX rise time. Calculate the VDD capacitor value with the following equation

$$C_{VDD} > \frac{\left(I_{VDD\_MAX} + 1.25 \times f_{SW} \times Q_{GATE}\right) \times t_{SS}}{\left(VDD_{ON} - VDD_{OFF}\right)} \quad (27)$$

Using I_{VDD_MAX} = 2 mA, f_{SW} = 42.5 kHz, Q_{GATE} = 11 nC, t_{SS} = 14 ms (2ms + 12ms),

VDD_{ON} = 17.6 V, and VDD_{OFF} = 14.5 V results in

$$C_{VDD} > 11.7\ \mu F \quad (28)$$

Allowing ±20% initial capacitor tolerance and another 20% for endurance (life, temperature, etc.) means the VDD bulk capacitor must be at least 19.5 µF. Select the next higher standard capacitor value, 22 µF. This capacitor should be rated to at least the ABS MAX voltage of the VDD pin, 30 V.

The electrolytic bulk capacitor (C12) should be located relatively close to the VDD pin. On the other hand, the high-frequency bypass capacitor, C18, must be a ceramic type and be physically placed and grounded as close as possible to the VDD pin. A 1.0 µF, X7R capacitor is recommended for the high-frequency decoupling. To offset the effects of DC-bias, this capacitor must be rated to about 2x the expected VDD voltage (⩾35V)

9.2.2.9 Gate Drive Network (R14, R16, Q6)

When the primary MOSFET turns on in DCM operation, its current starts from 0A and ramps up to a peak value each PWM cycle. Therefore, to reduce gate drive losses and increase overall efficiency, it is desirable to turn the MOSFET on relatively slowly when its current (and losses) are low. On the other hand, when the current ramps up to its peak the MOSFET must be turned off quickly to limit its losses, which also helps increase efficiency. R14 is the gate driver resistor controlling the turn-on time of the MOSFET (Q5). The optional PNP pull-down transistor (Q6) is used to turn the MOSFET off as quickly as possible, when the MOSFET is far away from the controller gate driver pin.

The selection of R14 resistor value must be done in conjunction with EMI compliance testing and efficiency testing. Using a larger resistor value for R14 slows down the turn-on of the MOSFET. A slower switching speed reduces EMI but also increases the switching loss. A tradeoff between switching loss and EMI performance must be carefully performed. For this design, efficiency was measured for a range of values for R14. Efficiency peaked with a value of 39-Ω for R14.

9.2.2.10 VREF Capacitor (C18)

The precision 5-V internal reference performs several important functions. The reference voltage is divided down internally to 2.5 V and connected to the error amplifier's noninverting input for accurate output voltage regulation. Other duties of the reference voltage are to set internal bias currents and thresholds for functions such as the VDD Start and Stop thresholds, and the oscillator upper and lower voltage thresholds. Therefore, the reference voltage must be bypassed with a ceramic capacitor. A 1.0-µF, 25-V ceramic capacitor was selected for this converter. Placement of this capacitor on the physical printed-circuit board layout must be as close as possible to the respective VREF and GND pins.

9.2.2.11 RT/CT Components (R12, C15)

The internal oscillator uses a timing capacitor (C15) and a timing resistor (R12) to program the oscillator frequency. The operating frequency can be programmed based the curves in Figure 7-1, where the timing resistor is found once the timing capacitor is selected. It is best for the timing capacitor to have a flat temperature coefficient, typical of most COG or NPO type capacitors. For this converter, 40.2 kΩ and 1000 pF were selected for R12 and C15 to operate at 42.5-kHz switching.

9.2.2.12 HV Start-Up Circuitry for VDD (Q1, Q2, D2, D4, D6, D8, R5)

The HV Startup circuit utilizes two 600-V depletion mode MOSFETs (Q1, Q2). The depletion mode MOSFET conducts when no gate voltage is applied and begins to turn off as the V_{GS} voltage becomes more and more negative. It is completely off when V_{GS} is below the turn-off threshold. The characteristics of the depletion mode FET make it well suited to implementing a current source for high-voltage startup. It is difficult to find a low-cost and small-size depletion MOSFET with 1.2-kV rating, but there are wide variety of selection in 600-V to 800-V domain. Therefore, the stacked depletion MOSFET configuration with the proposed gate clamp circuit will evenly distribute the voltage stress from the 1-kV input voltage.

First, let's look at the operation of Q1. Notice the four 130-V Zener diodes; D2, D4, D6 and D8. Their combined Zener voltage is 520 V. Next, think of R1 as a pull-up resistor to V_{IN} that simply provides current to the Zener diodes. With that in mind, it's obvious that these diodes will be off if V_{IN} < 520 V. Now, as V_{IN} rises above 520 V, the voltage at the source of Q1 will be clamped slightly above 520 V, let's say 521 V. In effect Q1 is biased such that the maximum voltage presented to Q2 is limited to 521 V. The V_{DS} voltage of Q1 is V_{IN} – 520 V. At 1000 V_{IN}, the V_{DS} of Q2 will be 521 V and V_{DS} of Q1 will be 479 V.

Next, let's look at the operation of Q2. For now, let's say D5 is a 22-V "safety" clamp to limit the maximum value of VDD in the event Q3 does not turn on. So, for normal operation it's practical to assume D5 is off. When VDD < V_{DD_ON}, Q3 is also off because the controller has not been powered up yet and VREF = 0 V. R3 is a pull-up resistor (similar to R1 for Q1) that biases D9 on in the forward direction during HV startup. The majority of current flows from the source of Q2 through R5 and charges the 22-µF capacitor on VDD (C12). We can use KVL around the loop formed by R3, D9, and R5 and solve for the current through R5.

$$I_{R5} = \frac{\left(V_{F(D9)} + V_{GS}\right)}{R5} \tag{29}$$

Typical values for V_{F_D9} and V_{GS}=V_{TH_Q2} are 0.3 V and 1.0 V, respectively. With this information we can solve for I_{R5}

$$I_{R5} = \frac{(0.3V + 1.0V)}{1k\Omega} = 1.3\ mA \tag{30}$$

Notice this current does not depend on V_{IN} so it will be constant over the entire range of V_{IN}.

If a soft start time requirement is provided ($t_{SS,MAX}$) the maximum value of R5 ($R5_{MAX}$) can be calculated.

$$R5_{MAX} = \frac{\left(V_{TH\_Q2} + V_{F\_D9}\right)}{\frac{C_{VDD} \times VDD_{ON}}{t_{SS,MAX}} + I_{SU\_UCC28C5x}} \tag{31}$$

Q3 functions as a simple switch controlled by VREF from the controller to shut down the HV startup circuit. When Q3 turns on zener diode D9 is reverse biased and clamps the V_{GS} voltage of Q2 to about –18 V. Shutting down the HV startup circuit when it is not needed reduces power and improves efficiency.

This HV startup circuit is presented in detail and compared to traditional NPN-based HV startup circuit in “High-Density 40W Auxiliary Power Supply Utilizing a SiC MOSFET for 800-V Traction Inverters”, SLUAAL3.

9.2.2.13 Desensitization to CS-pin Noise by RC Filtering, Leading-Edge Blanking, and Slope Compensation

High-voltage and fast switching leads to a high dv/dt switching node, which generates a fair amount of noise. During PCB layout, the switching node must be kept away from quiet areas, such as the current sense circuitry, voltage feedback circuitry, and loop compensation components to reduce noise coupling.

It’s common knowledge that each time the MOSFET turns on a spike appears on the current sense resistor for a very short time. This spike can cause the MOSFET to turn off early if precautions are not taken. Figure 9 shows several important sub-circuits required for reliable operation. First, and most important, R21 and C22 form a low pass filter between the (noisy) R_{SENSE} node and the CS pin. The low pass filter can attenuate most of the noise spike but too much filtering will delay the current information too. Second, Q6 and the components connected to its base are leading-edge blanking. This AC-coupled transistor pulls down on the CS voltage each time the MOSFET is turned on. The amount of leading-edge blanking is determined by C23, R26, and R27.

At duty cycles above 50 %, current mode control has a subharmonic oscillation phenomenon unless slope compensation is added. In Figure 9, R22 injects a small amount of voltage ramp to the CS pin. The voltage ramp for slope compensation is formed by passing the RT/CT voltage through an emitter-follower formed by Q7 and R23. The emitter follower buffers the RT/CT circuit so the switching frequency will not be changed. C21 ac-couples the output of the emitter follower to the CS pin (via R22). AC-coupling the slope compensation ramp is preferred because it avoids adding a DC bias at the CS pin, which would effectively reduce the current limit threshold. Lastly, C21 should be large enough to pass the slope compensation ramp. Making C21 too small results in a transient negative voltage at the CS pin when the RT/CT waveform resets, making very small on-times of the MOSFET impossible. The extra benefit of the slope-compensation signal is to create more noise margin to the leading-edge spike on CS pin from prematurely turning off primary MOSFET.

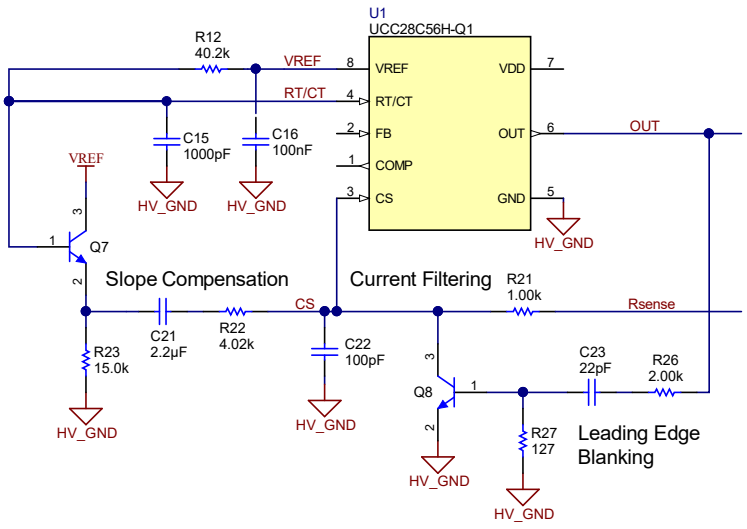


图 9-2. Figure TBD: Current Filtering, Leading-Edge Blanking, and Slope Compensation

9.2.2.14 Voltage Feedback Compensation

Feedback compensation, also called closed-loop control, can reduce or eliminate steady state error, reduce the sensitivity of the system to parametric changes, change the gain or phase of a system over some desired frequency range, reduce the effects of small signal load disturbances and noise on system performance, and create a stable system from an unstable system. A peak current mode flyback uses an outer voltage feedback loop to stabilize the converter. To adequately compensate the voltage loop, the open-loop parameters of the power stage must be determined.

9.2.2.14.1 Power Stage Gain, Poles, and Zeroes

The typical power stage of the DCM flyback has a single zero and a single pole. The zero is created by the ESR of the output capacitors and the output capacitance. The pole is created by the load resistance and the output capacitance. When the load changes the pole shifts in frequency as 1/RLOAD. The power stage will introduce the most phase loss when the load is relatively low and RLOAD is high. Therefore, it is best to stabilize the system and check the stability margins at low VIN, high VIN, light-load, and maximum load.

Start by calculating the location of the power-stage zero

$$f_{ZERO} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR_{COUT}} = \frac{1}{2 \times \pi \times 2000\mu F \times 16.5m\Omega} = 4.8\ kHz \tag{32}$$

Next, calculate the pole location with about 120 % of maximum load, 3.24 A load (R_{LOAD} = 4.6 Ω)

$$f_{POLE} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}} = \frac{1}{2 \times \pi \times 2000\mu F \times 4.6\Omega} = 17\ Hz \tag{33}$$

In this application, the feedback voltage is formed from an auxiliary winding. This feedback path contains a 22-µF capacitor (C12) and a 4.7-µF capacitor (C13) that introduce another (atypical) low frequency pole. The pole is formed by the total capacitance (C12+C13) and the equivalent load current of the regulator. The equivalent load of the regulator is the sum of the operating supply current (IVDD, 1.3 mATYP) and the gate drive current to the MOSFET (Q_G x f_{SW}, 11 nC x 42.5 kHz = 0.47 mA). The VDD voltage is typically 18.6 V, so the equivalent resistance can be modelled as 18.6 V / 1.77 mA = 10.5 kΩ.

The following figure shows the frequency response of the plant characteristic (a.k.a. COMP-to-output response). It compares the DCM flyback both with and without the pole formed by AUX components, 22 µF + 4.7 µF / 10.5 kΩ. Notice the response with the AUX components is ~15dB lower with an additional 45 deg of phase loss at 1.0 kHz.

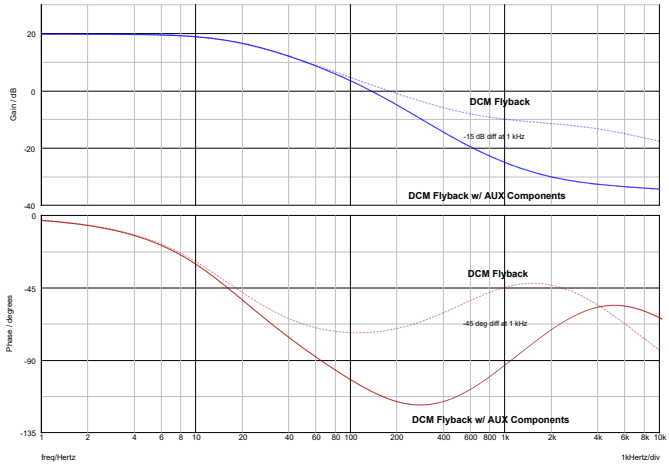


图 9-3. Comparison of DCM Flyback Plant with and without AUX Components

9.2.2.14.2 Compensation Components

To compensate a peak-current-mode controller it’ s very common to use a Type-II compensator. The Type-II compensator introduces a pole at DC, a relatively low frequency zero ($f_{Z,COMP}$), and a higher frequency pole ($f_{P,COMP}$). The pole at DC forces the system to have high gain at very low frequency and zero stead-state error.

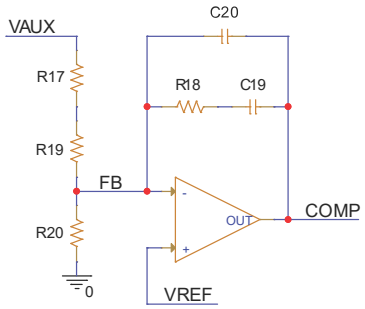


图 9-4. Type-II Compensation with an Error Amplifier

The low frequency zero is formed by R18 and C19

$$f_{Z,COMP} = \frac{1}{2 \times \pi \times C19 \times R18} \tag{34}$$

The higher frequency pole is formed by R18 and C20

$$f_{P,COMP} = \frac{1}{2 \times \pi \times C20 \times R18} \tag{35}$$

The mid-frequency gain of the compensator is given by

$$G_{COMP} = \frac{R18}{(R17 + R19)} \tag{36}$$

First, select a crossover frequency, 625 Hz. Then, use the frequency response of the plant (control-to-output) at low input voltage to determine how much gain the compensator must add to increase the crossover to the desired bandwidth. In 图 9-5 the plant is measured to be -23.3 dB at 625 Hz. Therefore, the error amplifier must have a mid-frequency gain of 14.6 V/V.

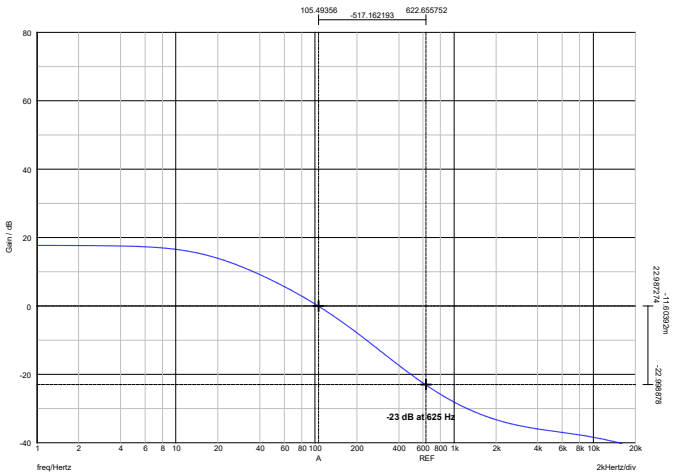


图 9-5. Measuring the plant gain at the desired crossover frequency: -23 dB at 625 Hz

Choose (R17+R19) = 22.5 kΩ, and solve for R18

$$R18 = G_{COMP} \times (R17 + R19) = 14.6\,V/V \times 22.5k\Omega = 328k\Omega \quad (37)$$

Select a standard value for R18, like 324 kΩ.

Now that we know R18, it’s fairly straightforward to set $f_{Z,COMP}$ = f_{POLE} and solve for C19

$$f_{Z,COMP} = f_{POLE} = \frac{1}{2 \times \pi \times C19 \times 324k\Omega} = 17\,Hz \quad (38)$$

$$C19 = 28nF \quad (39)$$

Likewise, set $f_{P,COMP}$ = f_{ZERO} and solve the following for C20

$$f_{P,COMP} = f_{ZERO} = \frac{1}{2 \times \pi \times C20 \times 324k\Omega} = 4.8\,kHz \quad (40)$$

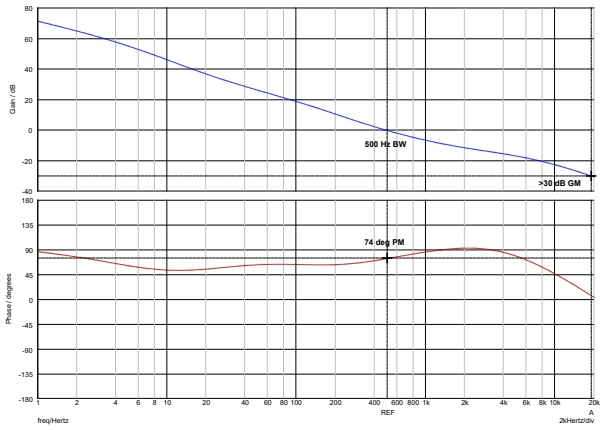
$$C20 = 102pF \quad (41)$$

Finally, choose standard capacitor values, C19 = 22 nF and C20 = 100 pF. Notice that a slightly lower value was used for C19 than calculated. This was done to have a faster “reset” time during after a load transient response. If the complete loop is found to have too little phase margin then C19 can be increased at the cost of slower reset time.

9.2.2.14.3 Bode Plots and Stability Margins

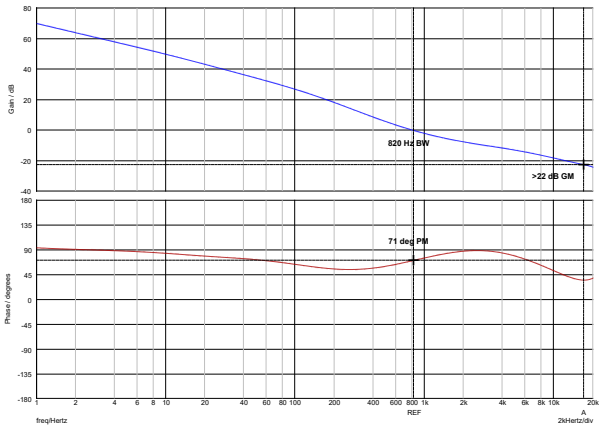
It’s important to simulate (or measure) the stability margins at low V_{IN} and high V_{IN} at both light load and heavy load. 图 9-6 to 图 9-9 show the simulated bandwidth, gain margin, and phase margin for this design at 40 V_{IN} and 800 V_{IN} at both light load and full load. The phase margin is always above 55 deg and the gain margin is >20 dB.

9.2.2.14.4 Stability Measurements



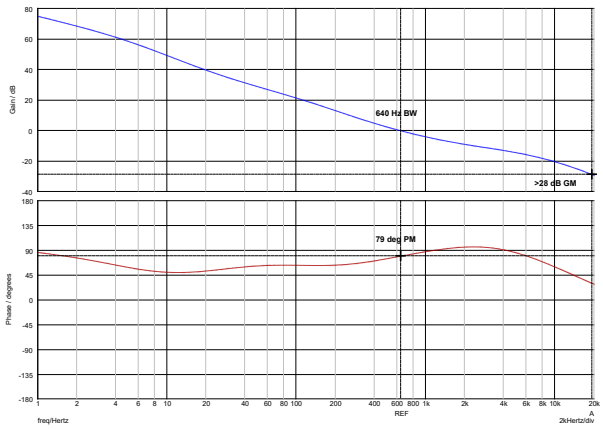
500 Hz Bandwidth
Phase Margin = 74 deg
Gain Margin > 30 dB

图 9-6. 40 V_{IN}, Light Load (500 mA)



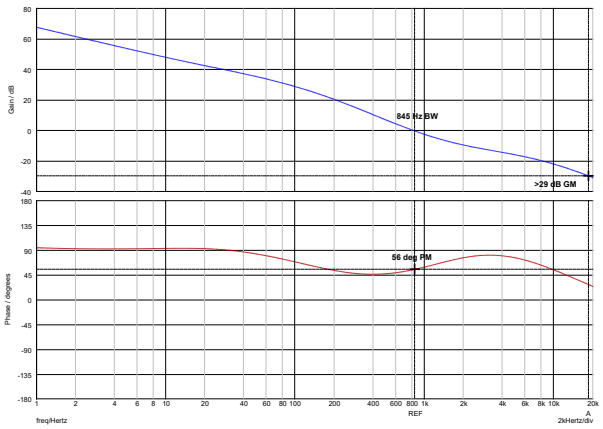
820 Hz Bandwidth
Phase Margin = 71 deg
Gain Margin > 22 dB

图 9-7. 40 V_{IN}, Maximum Load (1.33 A)



640 Hz Bandwidth
Phase Margin = 79 deg
Gain Margin > 28 dB

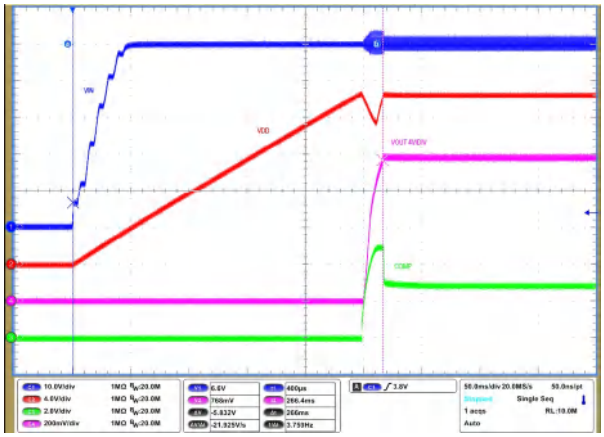
图 9-8. 800 V_{IN}, Light Load (500 mA)



845 Hz Bandwidth
Phase Margin = 56 deg
Gain Margin > 29 dB

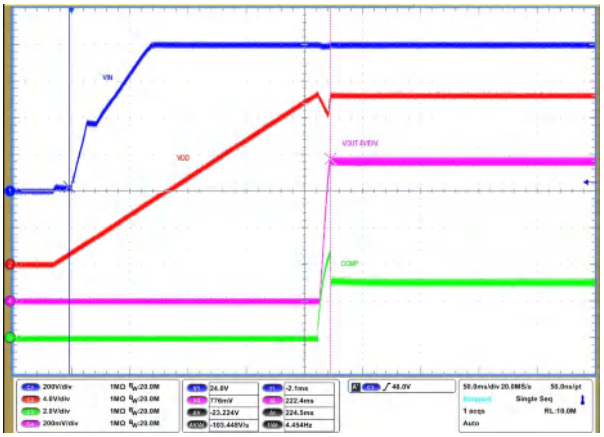
图 9-9. 800 V_{IN}, Maximum Load (2.7 A)

9.2.3 Application Curves



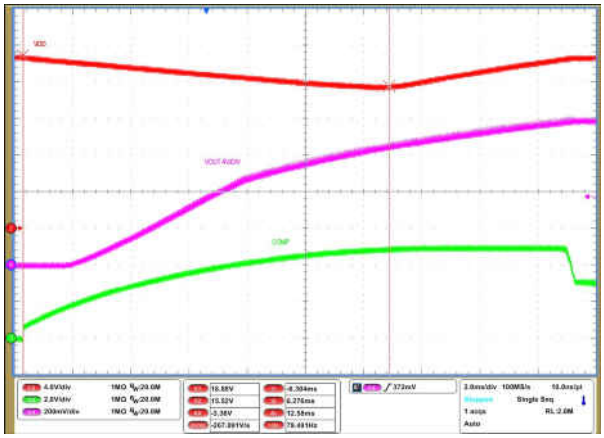
V_{IN} applied to V_{OUT} ready in 266 ms
CH1: V_{IN} at 10 V/DIV
CH2: VDD at 4 V/DIV
CH3: COMP at 2 V/DIV
CH4: VOUT at 4 V/DIV via differential probe

图 9-10. HV Startup at 50 V_{IN}, 20 W



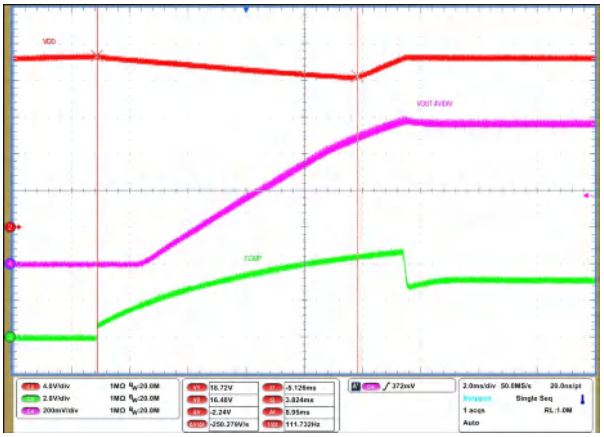
V_{IN} applied to V_{OUT} ready in 224 ms
CH1: V_{IN} at 200 V/DIV
CH2: VDD at 4 V/DIV
CH3: COMP at 2 V/DIV
CH4: VOUT at 4 V/DIV via differential probe

图 9-11. HV Startup at 800 V_{IN}, 40 W



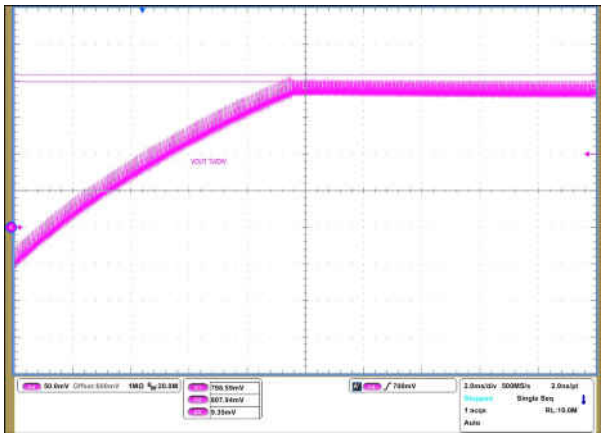
V_{DD} capacitor hold-up time = 12.6 ms
V_{OUT} rise time = 17.2 ms
CH2: VDD at 4 V/DIV
CH3: COMP at 2V/DIV
CH4: V_{OUT} at 4 V/DIV via differential probe

图 9-12. V_{OUT} Soft Starting at 50 V_{IN}, 20 W



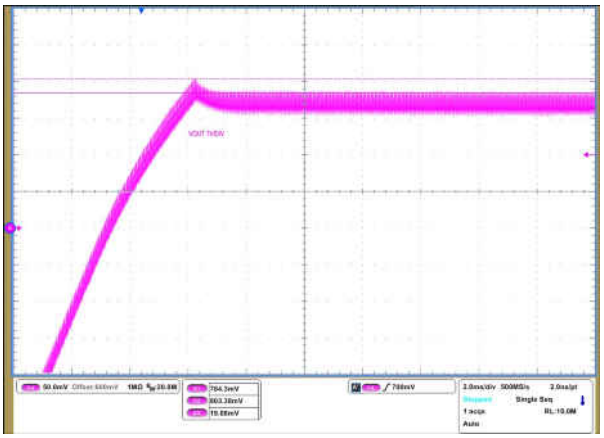
V_{DD} capacitor hold-up time = 8.9 ms
V_{OUT} rise time = 9.1 ms
CH2: VDD at 4 V/DIV
CH3: COMP at 2V/DIV
CH4: V_{OUT} at 4 V/DIV via differential probe

图 9-13. V_{OUT} Soft Starting at 800 V_{IN}, 40 W



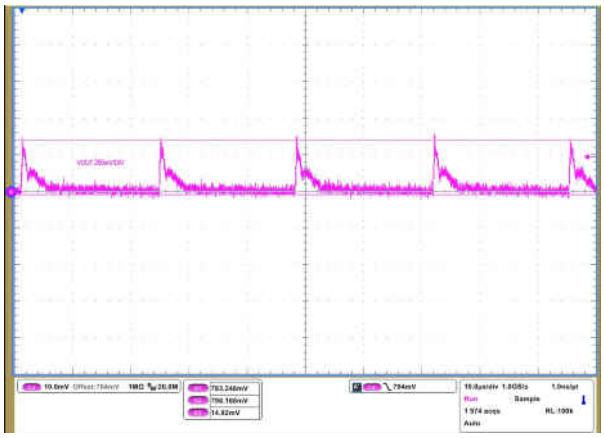
Soft Start Overshoot = 1.2 %
CH4: V_{OUT} at 1 V/DIV via differential probe

图 9-14. V_{OUT} Overshoot at 50 V_{IN}, 20W



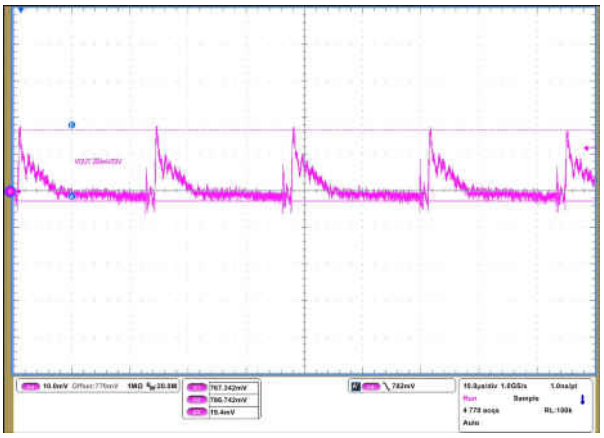
Soft Start Overshoot = 2.4 %
CH4: V_{OUT} at 1 V/DIV via differential probe

图 9-15. V_{OUT} Overshoot at 800 V_{IN}, 40 W



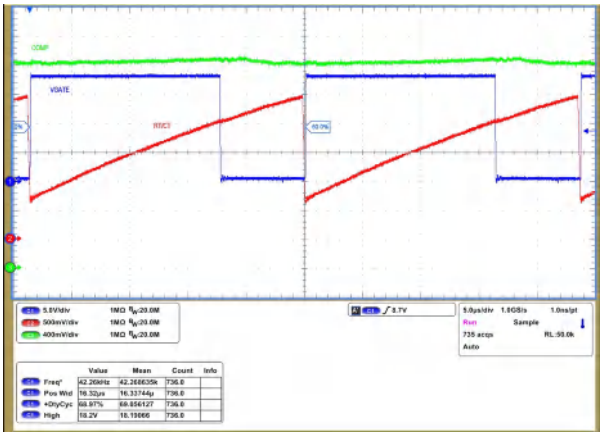
Output Voltage Ripple = 298 mV_{PP}
CH4: V_{OUT} at 200 mV/DIV via differential probe

图 9-16. Output Voltage Ripple at 50 V_{IN}, 20W



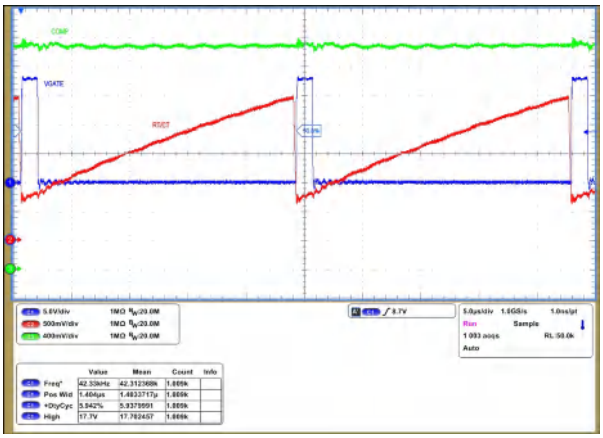
Output Voltage Ripple = 388 mV_{PP}
CH4: V_{OUT} at 200 mV/DIV via differential probe

图 9-17. Output Voltage Ripple at 800 V_{IN}, 40 W



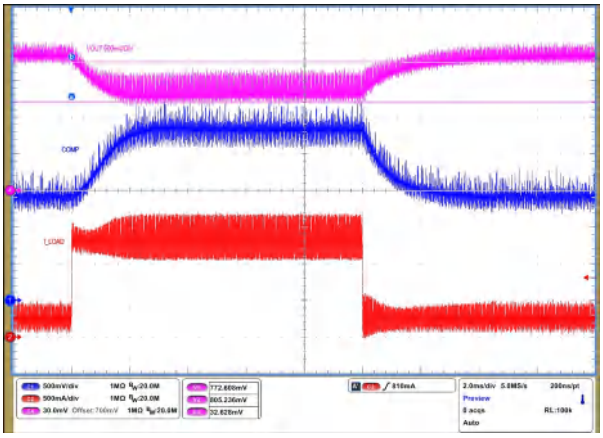
f_{SW} = 42.6 kHz, t_{ON} = 16.3 us, Duty Cycle = 69 %
CH1: VGATE at 5 V/DIV
CH2: RT/CT at 500 mV/DIV
CH3: COMP at 400 mV/DIV

图 9-18. PWM Switching at 50 V_{IN}, 20 W



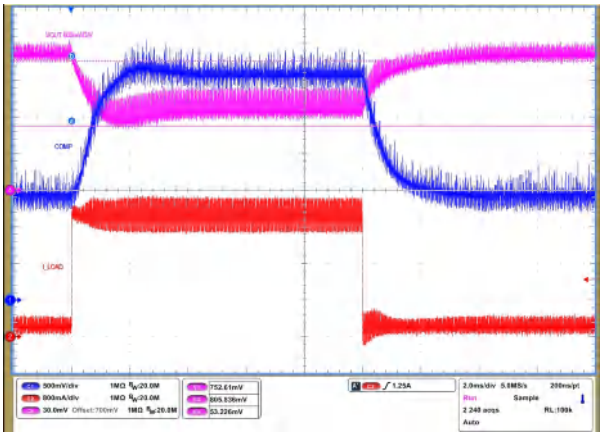
f_{SW} = 42.3 kHz, t_{ON} = 1.4 us, Duty Cycle = 5.9 %
CH1: VGATE at 5 V/DIV
CH2: RT/CT at 500 mV/DIV
CH3: COMP at 400 mV/DIV

图 9-19. PWM Switching at 800 V_{IN}, 40 W



250 mA to 1.3 A to 250 mA
V_{MAX} = 16.1 V, V_{MIN} = 15.4 V, dV = 0.7 V
CH1: COMP at 50 mV/DIV
CH2: I_LOAD at 500 mA/DIV
CH4: V_{OUT} at 600 mV/DIV via differential probe

图 9-20. Load Transient at 800 V_{IN}, 1 A Step Change



250 mA to 2.7 A to 250 mA
V_{MAX} = 16.1 V, V_{MIN} = 15.1V, dV = 1.0 V
CH1: COMP at 50 mV/DIV
CH2: I_LOAD at 800 mA/DIV
CH4: V_{OUT} at 600 mV/DIV via differential probe

图 9-21. Load Transient at 800 V_{IN}, 2.5 A Step

9.3 PCB Layout Recommendations

In general, try to keep all high current loop areas as small as possible. Keep all traces with high current and high frequency away from other traces in the design. If necessary, high frequency/high current traces should be perpendicular to signal traces, not parallel to them. Shielding signal traces with ground planes can help reduce noise pick up. Always consider appropriate clearances between the high-voltage connections and any low voltage nets.

In order to increase the reliability and robustness of the design TI recommends the following PCB layout guidelines.

9.3.1 PCB Layout Routing Examples

1) The power ground should not disturb (i.e. mix with) the signal ground. The signal ground includes the small R’s and C’s around the controller (for COMP, FB, RT/CT, CS) and the controller ground pin. The power ground includes the input capacitors, current sense resistors, return for the Y-capacitor, and gate drive return via the PNP transistor Q6.

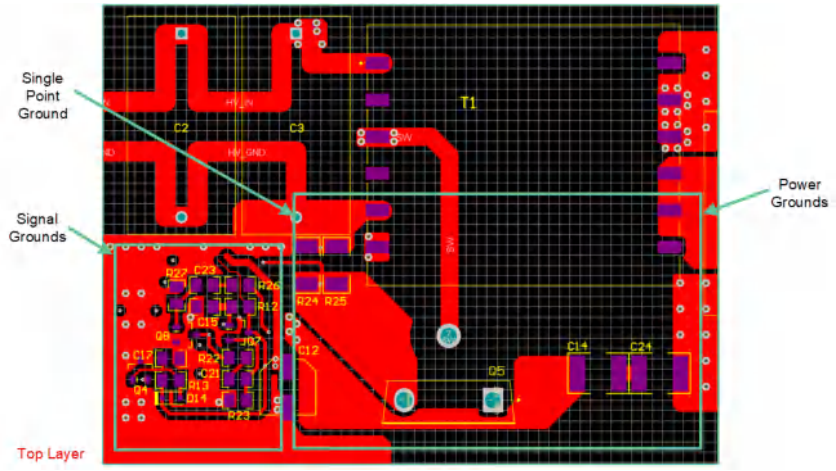


图 9-22. Top Layer: Signal Grounds, Power Grounds, and their Connection to a Single-Point Ground

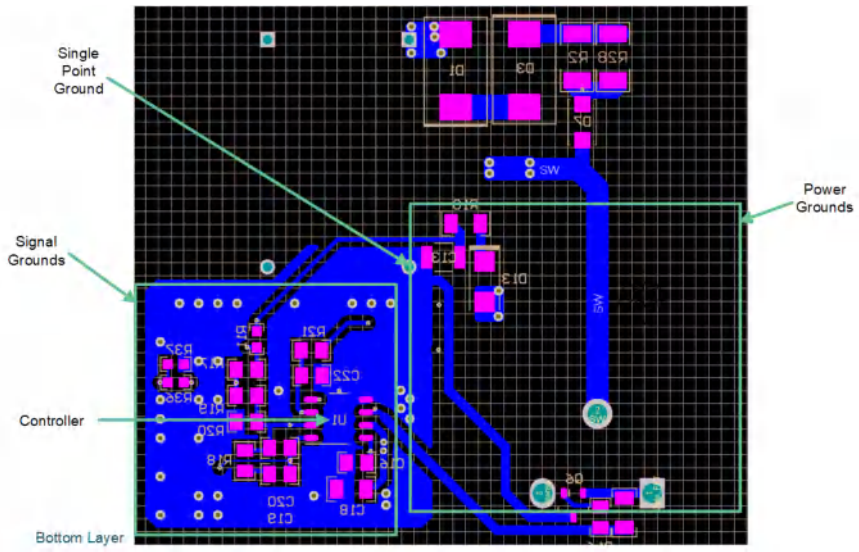


图 9-23. Bottom Layer: Signal Grounds, Power Grounds, and their Connection to a Single-Point Ground

2) The primary-side power loop must be minimized. Use relatively wide traces. This loop includes the input capacitors (C2, C3), transformer primary winding (T1 pins 1, 3), switching MOSFET (Q5), and sense resistors (R24, R25). Do not use vias in this path.

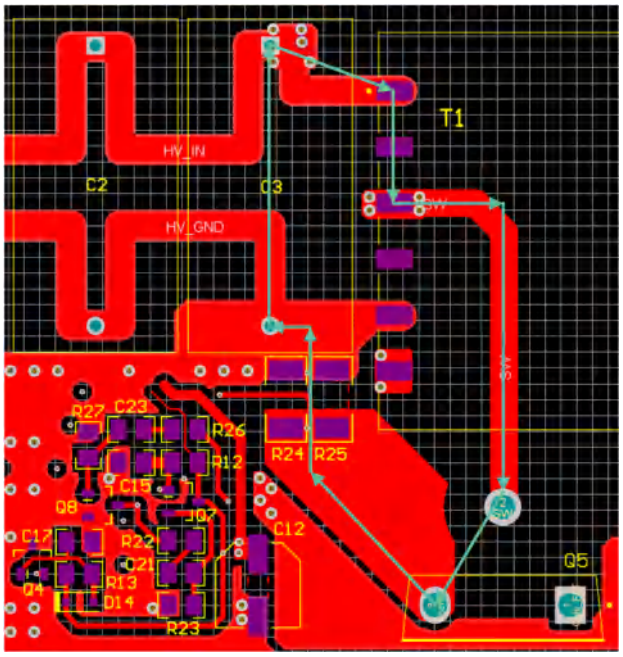


图 9-24. Primary-Side Power Loop Routing

3) The secondary-side power loop should be minimized. Use copper pours or very wide traces. This loop includes the output capacitors (C9, C10), transformer secondary winding (T1 pins 8/9, 10/11), and output rectifier diode (D11). If interconnection between layers is required use multiple vias to handle the high peak currents.

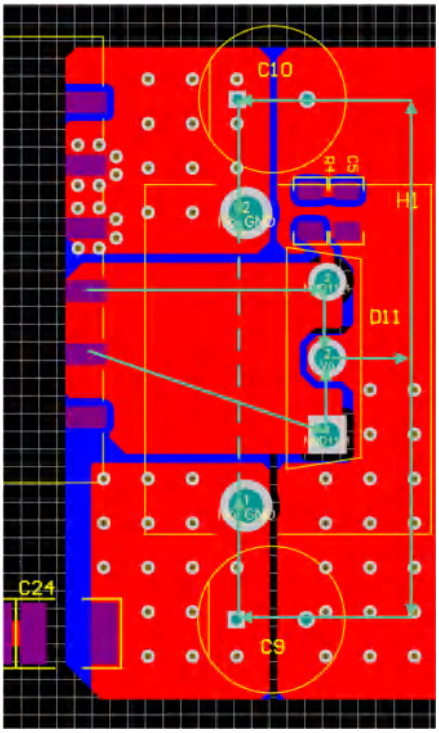


图 9-25. Secondary-Side Power Loop Routing

4) The AUX feedback loop should be minimized. This loop includes components C13, D13, and the transformer AUX winding (T1 pins 6, 5).

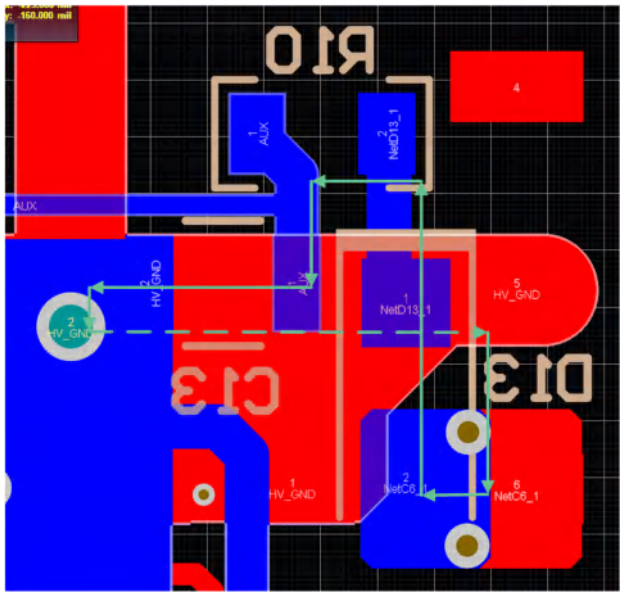


图 9-26. AUX Feedback Loop Routing

5) The loop of the high-voltage clamp must be minimized. This loop includes D1, D3, R2//R28, and D7. All these components should be on the same layer.

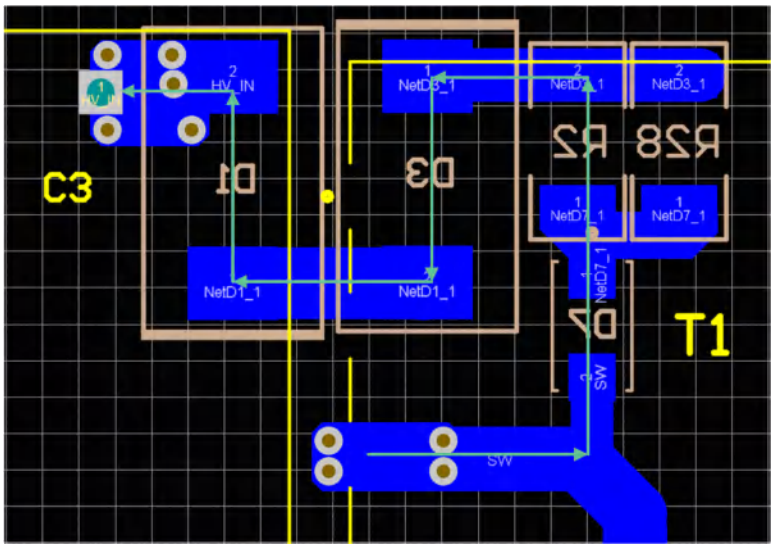


图 9-27. High-Voltage Clamp Loop Routing

6) The Y-type capacitor from the isolation ground to the power ground (C14, C24) should route back to the single point ground without disturbing the signal ground around the controller.

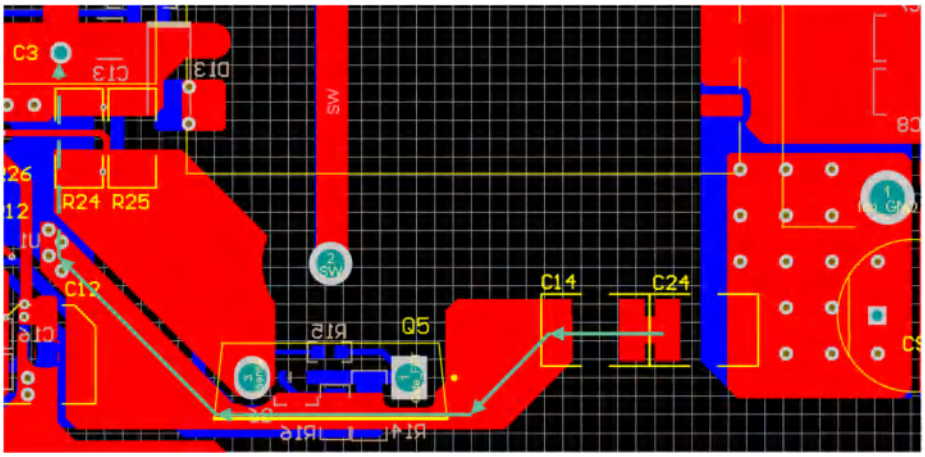


图 9-28. Y-Capacitor Ground Routing

7) The trace from the OUT pin (U1 pin 6) to the gate of the switching MOSFET (Q5-1) must be as short as possible and relatively wide. Do not use vias in this path.

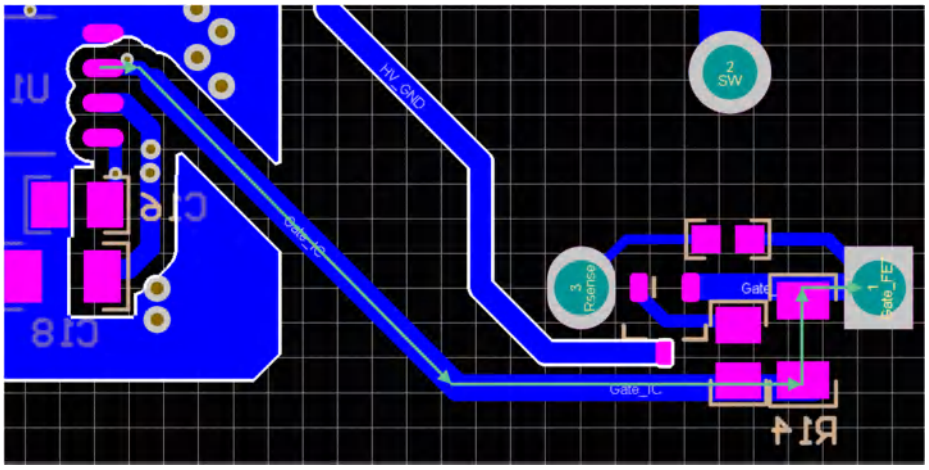


图 9-29. Gate Drive (OUT) Trace Routing

8) The collector of the PNP gate pull-down transistor (Q6 pin 3) should route directly back to the single point ground without disturbing the signal ground around the controller.

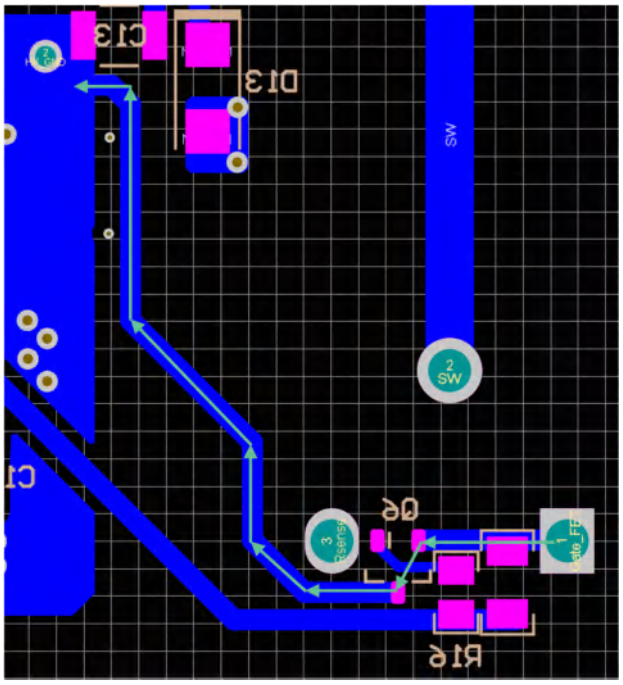


图 9-30. Gate Pull-Down PNP Transistor Collector Routing

9) The connection from the current sense resistors (R24/R25) to the low-pass filter (R21, C22) and on to the CS pin must be direct and it must avoid noisy signals. For example, do not route this trace near the MOSFET gate drive or SW node.

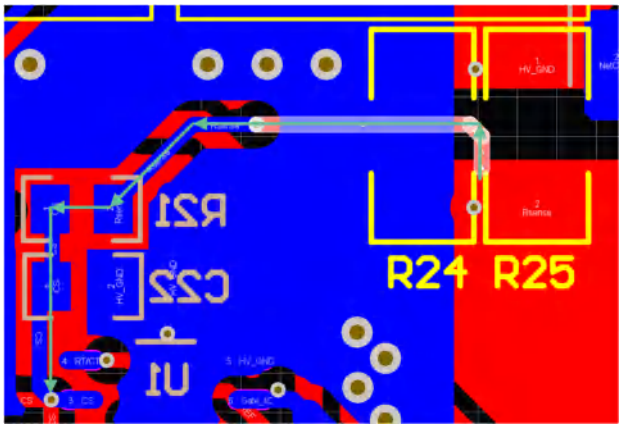


图 9-31. Current Sense Trace Routing

10) The loop formed by the R-C snubber (R4, C5) around the output rectifier diode (D11) should be minimized. Do not use vias in this path.

11) The VDD pin must have a ceramic capacitor (C18) located as close as possible.

12) The VREF pin must have a ceramic capacitor (C16) located as close as possible.

13) The compensation components (R18, C19, C20) must be located near the COMP pin.

14) The feedback divider components (R17, R19, R20) must be located near the FB pin.

15) The frequency setting components (R12, C15) must be located near the RT/CT pin.

9.4 Power Supply Recommendations

The absolute maximum supply voltage is 30 V, including any transients that may be present. If this voltage is exceeded, device damage is likely. Thus, the supply pin must be decoupled as close to the GND pin as possible. Also, because no clamp is included in the device, the supply pin must be protected from external sources which could exceed the 30-V level.

To prevent false triggering due to leading edge noises, an RC current sense filter may be required on CS. Keep the time constant of the RC filter well below the minimum on-time pulse width.

To prevent noise problems with high-speed switching transients, bypass VREF to ground with a ceramic capacitor close to the device package. A minimum of 0.1-µF ceramic capacitor is required. Additional VREF bypassing is required for external loads on the reference. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.2 Documentation Support

10.2.1 Related Documentation

(UCC28C5x-Q1 Technical Documents)

10.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links (*to be updated*)

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC28C50-Q1	Click here	Click here	Click here	Click here	Click here
UCC28C51-Q1	Click here	Click here	Click here	Click here	Click here
UCC28C52-Q1	Click here	Click here	Click here	Click here	Click here
UCC28C53-Q1	Click here	Click here	Click here	Click here	Click here
UCC28C54-Q1	Click here	Click here	Click here	Click here	Click here
UCC28C55-Q1	Click here	Click here	Click here	Click here	Click here

10.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28C50QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C50Q
UCC28C50QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C50Q
UCC28C51QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C51Q
UCC28C51QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C51Q
UCC28C52QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C52Q
UCC28C52QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C52Q
UCC28C53QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C53Q
UCC28C53QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C53Q
UCC28C54QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C54Q
UCC28C54QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C54Q
UCC28C55QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C55Q
UCC28C55QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C55Q
UCC28C56HQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	8C56HQ
UCC28C56HQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	8C56HQ
UCC28C56LQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	8C56LQ
UCC28C56LQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	8C56LQ
UCC28C57HQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	8C57HQ
UCC28C57HQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	8C57HQ
UCC28C57LQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	8C57LQ
UCC28C57LQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	8C57LQ
UCC28C58QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C58Q
UCC28C58QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C58Q
UCC28C59QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C59Q
UCC28C59QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	28C59Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

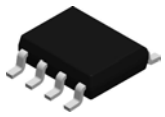
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UCC28C50-Q1, UCC28C51-Q1, UCC28C52-Q1, UCC28C53-Q1, UCC28C54-Q1, UCC28C55-Q1, UCC28C56H-Q1, UCC28C56L-Q1, UCC28C57H-Q1, UCC28C57L-Q1, UCC28C58-Q1, UCC28C59-Q1 :

- Catalog : UCC28C50, UCC28C51, UCC28C52, UCC28C53, UCC28C54, UCC28C55, UCC28C56H, UCC28C56L, UCC28C57H, UCC28C57L, UCC28C58, UCC28C59

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

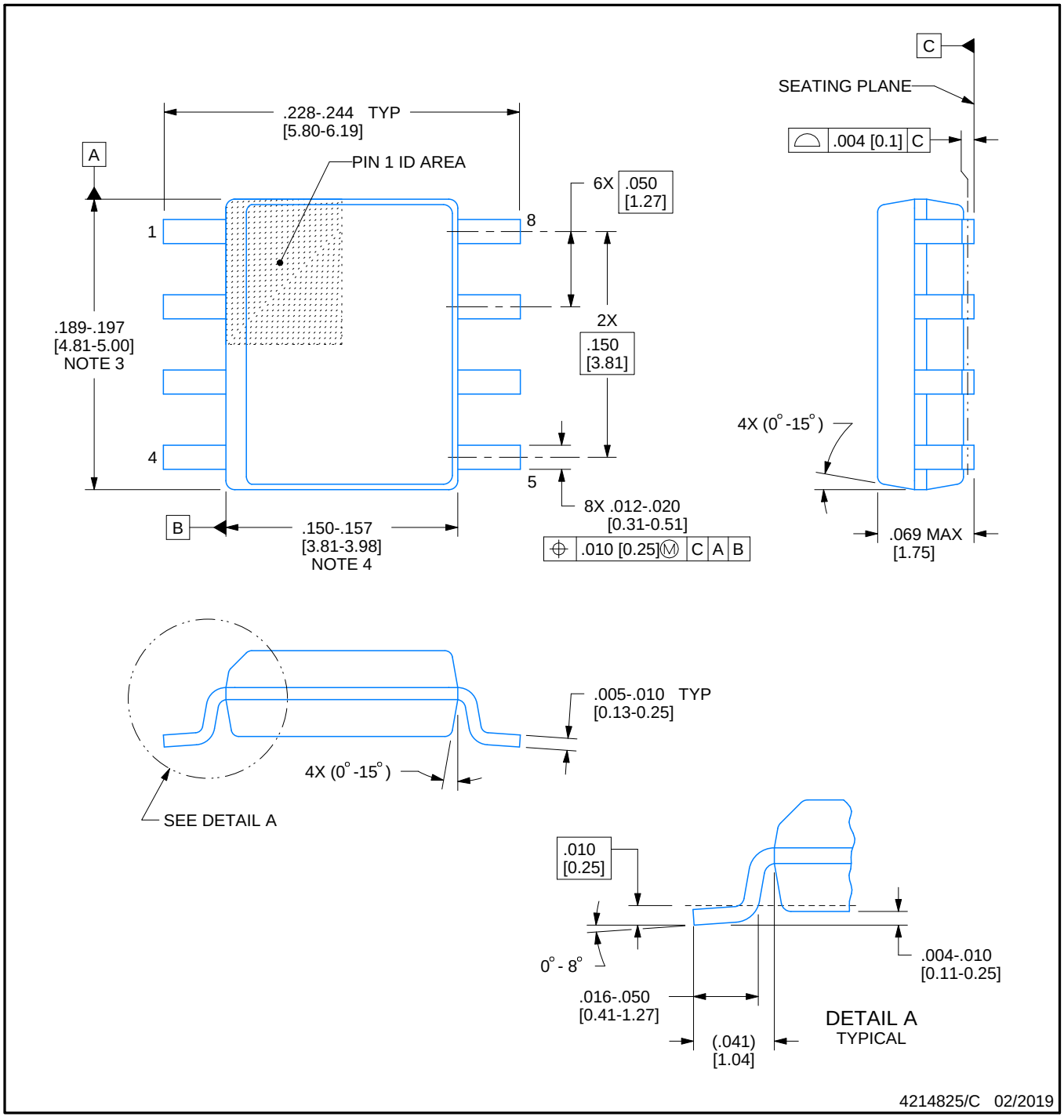


PACKAGE OUTLINE

D0008A

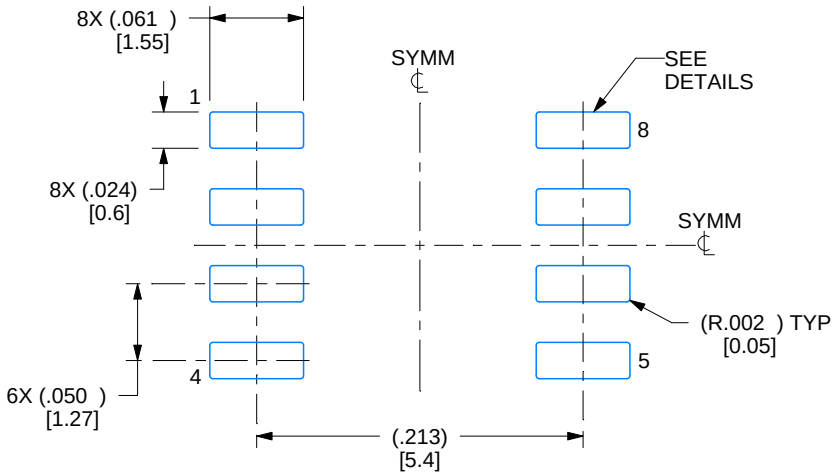
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

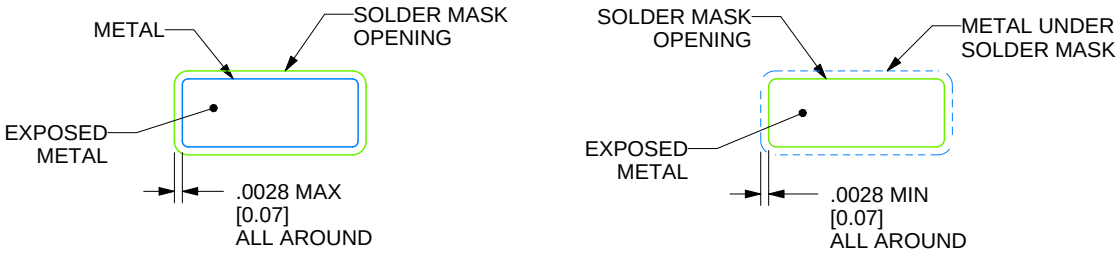


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

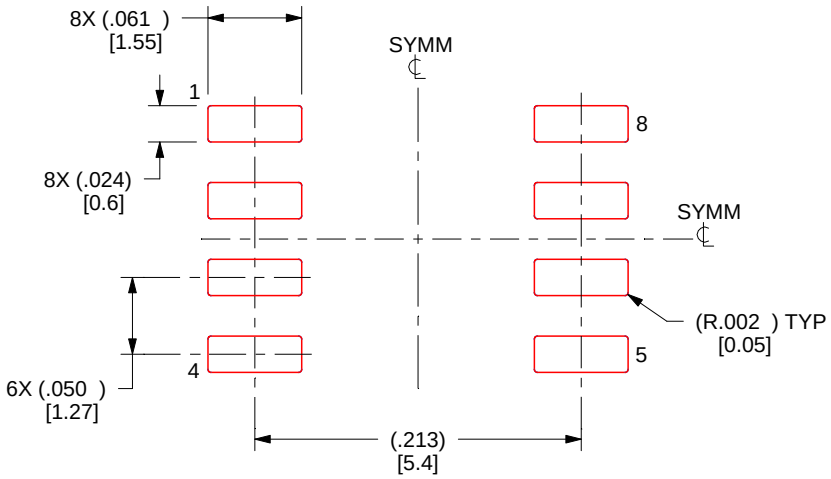
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月