UCC28880 700V 最低静态电流离线开关

1 特性

- 集成式功率金属氧化物半导体场效应晶体管 (MOSFET)（开关），漏源电压额定值为 700V
- 集成高压电流源，用于生成内部低压电源
- 软启动
- 自偏置开关（直接在经整流的市电电压下启动和运行）
- 支持降压、降压/升压和反激拓扑结构
- 器件静态电流 <100μA
- 性能优异，可防止电感器电流击穿
- 保护
  - 电流限制保护
  - 过载和输出短路保护
  - 过热保护

2 应用

- AC-DC 电源（在温度和输入电压范围内的输出电流高达 100mA）
- 计量、家庭自动化、基础设施开关模式电源 (SMPS)
- 晶闸管 (TRIAC) 驱动器的低侧降压拓扑
- 家用电器、大型家用电器和发光二极管 (LED) 驱动器

3 说明

UCC28880 在一个单片器件中集成了控制器和 700V 功率 MOSFET。 该器件还集成了高压电流源，能够在经整流的市电电压下直接启动和运行。

而且其静态电流较低，能够提供出色的效率。 凭借 UCC28880，使用最少的外部元件即可构建降压、降压/升压以及反激拓扑等最为常用的转换器拓扑。

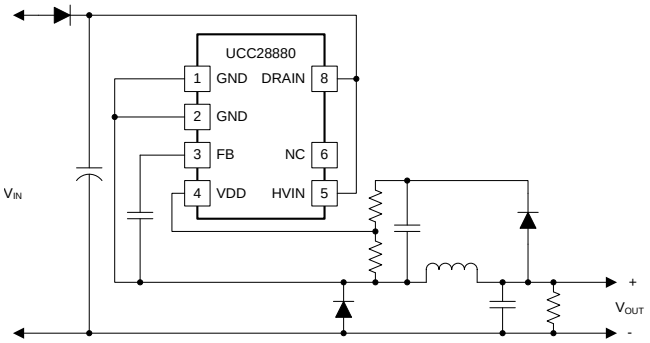
UCC28880 集成了软启动功能，用于控制功率级启动，能够最大程度减小对功率级元件的压力。

器件信息(1)

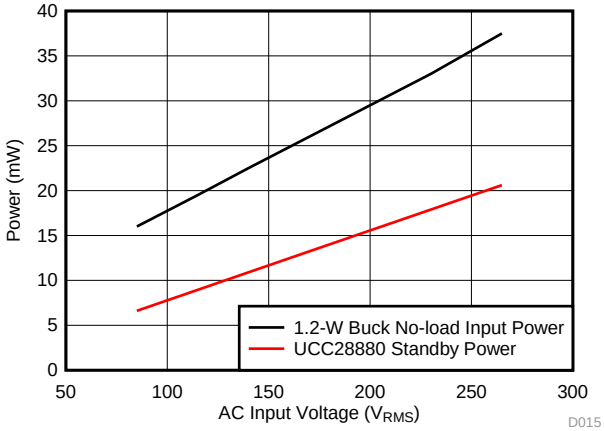
部件号	封装	封装尺寸（标称值）
UCC28880	小外形尺寸集成电路 (SOIC) (7)	5.00mm x 6.20mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



功率与输入电压间的关系



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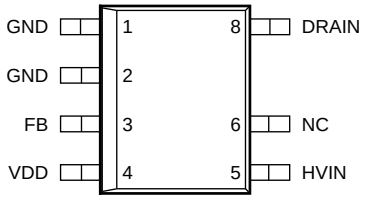
4 修订历史记录

日期	修订版本	注释
2014 年 7 月	*	最初发布。

5 Pin Configuration and Functions

Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	G	Ground
GND	2	G	Ground
FB	3	I	Feedback terminal
VDD	4	O	Supply pin, supply is provided by internal LDO
HVIN	5	P	Supply pin
NC	6	N/C	Not internally connected
DRAIN	8	P	Drain pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
HVIN		–0.3	700 (3)	V
DRAIN		Internally clamped	700 (3)	V
I_{DRAIN}	Positive drain current single pulse, pulse max duration 25 µs		320	mA
I_{DRAIN}	Negative drain current	–320		mA
FB		–0.3	6	V
VDD		–0.3	6	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. These ratings apply over the operating ambient temperature ranges unless otherwise noted.
(3) T_A = 25°C

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature 1.6 mm (1/16 inch) from case 10 seconds			260	
$V_{(ESD)}$	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Human Body Model (HBM) per ANSI/ESDA/JEDEC JS-001, HVIN pin (1)	–1500	1500	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}	Voltage On VDD pin		5		V
V_{FB}	Voltage on FB pin	–0.2		5	V
T_A	Operating ambient temperature	–40		105	°C
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC28880 SOIC (D) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	85	
ψ_{JT}	Junction-to-top characterization parameter	6.4	
ψ_{JB}	Junction-to-board characterization parameter	76	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{HVIN} = 30 V, $T_A = T_J$ = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HVIN(min)}$	Minimum Voltage to startup				30	V
I_{NL}	Internal supply current, no load	FB = 1.25 V (> V_{FB_TH})		58	100	µA
I_{FL}	Internal supply current, full load	FB = 0.75 V (> V_{FB_TH})		72	120	µA
I_{CH0}	Charging VDD Cap current	V_{VDD} = 0 V,	–3.8	–1.6	–0.4	mA
I_{CH1}	Charging VDD Cap current	V_{VDD} = 4.4V, V_{FB} = 1.25 V	–3.40	–1.30	–0.25	mA
V_{VDD}	Internally regulated low Voltage supply (supplied from HVIN pin)		4.5	5.0	5.5	V
V_{FB_TH}	FB pin reference threshold		0.94	1.02	1.10	V
$V_{VDD(on)}$	VDD turn-on threshold	VDD low-to-high	3.55	3.92	4.28	V
$\Delta V_{VDD(uvlo)}$	VDDON - VDD turn-off threshold	VDD high-to-low	0.28	0.33	0.38	V
D_{MAX}	Maximum Duty Cycle	FB = 0.75 V	45%		55%	
I_{LIMIT}	Current Limit	Static, T_A = –40°C			300	mA
		Static, T_A = 25°C	170	210	260	mA
		Static, T_A = 125°C	140			mA
$T_{J(stop)}$	Thermal Shutdown Temperature	Internal junction temperature		150		°C
$T_{J(hyst)}$	Thermal Shutdown Hysteresis	Internal junction temperature		50		°C
BV	Power Mosfet Breakdown Voltage	T_J = 25°C	700			°C
$R_{DS(on)}$	Power MOSFET On-Resistance (includes internal sense-resistor)	I_D = 30 mA, T_J = 25°C		32	40	Ω
		I_D = 30 mA, T_J = 125°C		55	68	Ω
DRAIN_$I_{LEAKAGE}$	Power MOSFET off state leakage current	V_{DRAIN} = 700V, T_J = 25°C			5	µA
		V_{DRAIN} = 400 V, T_J = 125°C			20	µA
HVIN_I_{OFF}	HVIN off state current	V_{HVIN} = 700 V, T_J = 25°C, V_{VDD} = 5.8 V	4.0	7.5	12.0	µA
		V_{HVIN} = 400 V, T_J = 125°C, V_{VDD} = 5.8 V			20	µA

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SW(max)}$	Maximum switching frequency		52	62	75	kHz
t_{ON_MAX}	Maximum switch on time (current limiter not triggered),	FB = 0.75 V	5.7	7.6	9.5	µs
t_{OFF_MIN}	Minimum switch off time follows every t_{ON} time,	FB = 0.75 V	5.7	7.6	9.5	µs
t_{MIN}	Minimum on time		0.17	0.22	0.30	µs
$t_{OFF(ovl)}$	Max off time (OL condition), $t_{OFF(ovl)} = t_{SW} - t_{ON(max)}$		130	200	270	µs

6.7 Typical Characteristics

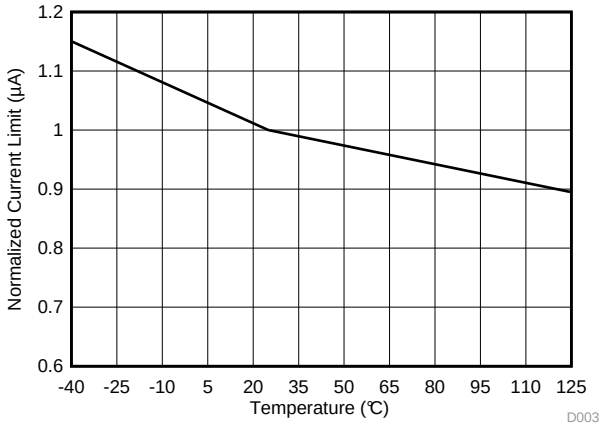


Figure 1. I_{LIMIT} vs Temperature

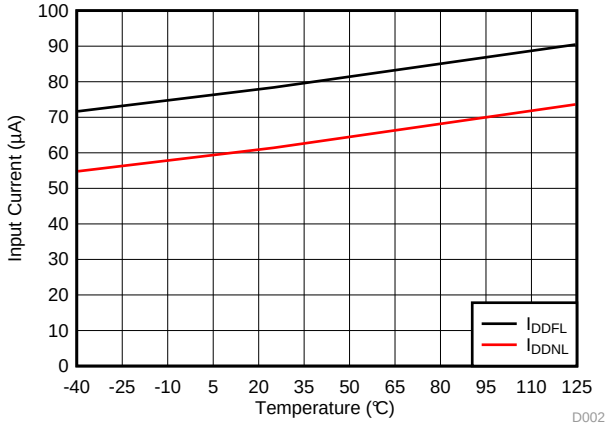


Figure 2. I_{LIMIT} vs Drain Current Slope

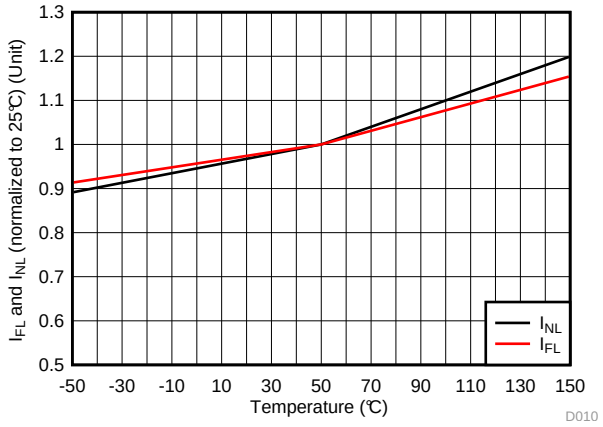


Figure 3. I_{NL} and I_{FL} vs Temperature

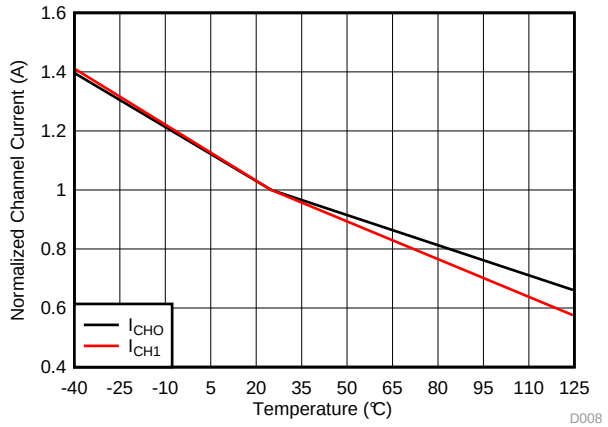


Figure 4. I_{CH0} and I_{CH1} vs Temperature

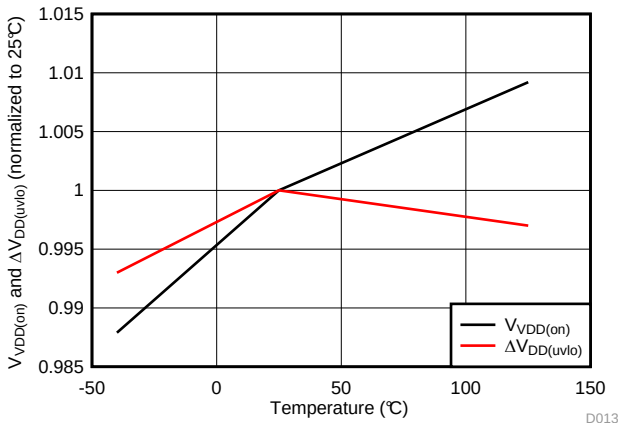


Figure 5. $V_{VDD(on)}$ and ΔV_{UVLO} vs Temperature

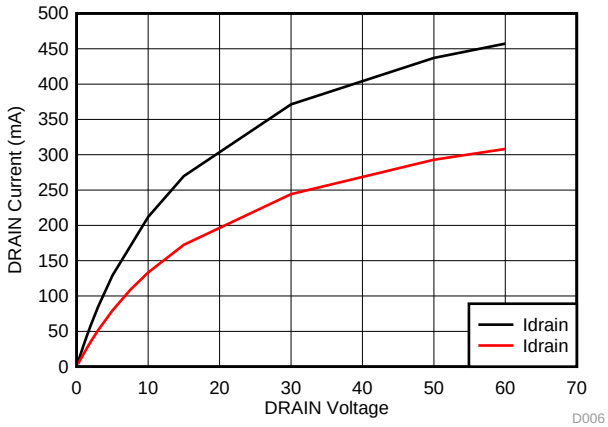


Figure 6. I_{DS} vs V_{DS} at 25°C and 125°C

Typical Characteristics (continued)

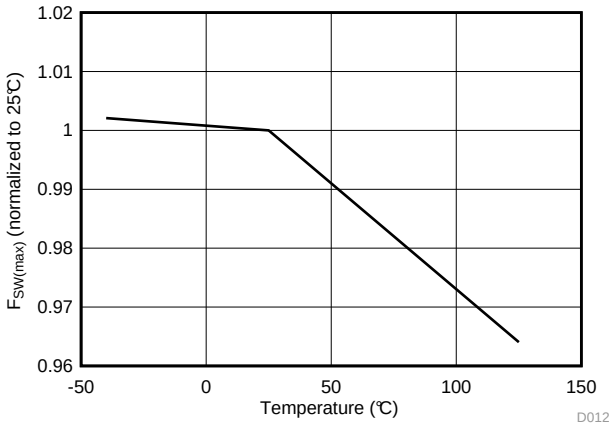


Figure 7. Maximum Switching Frequency vs Temperature

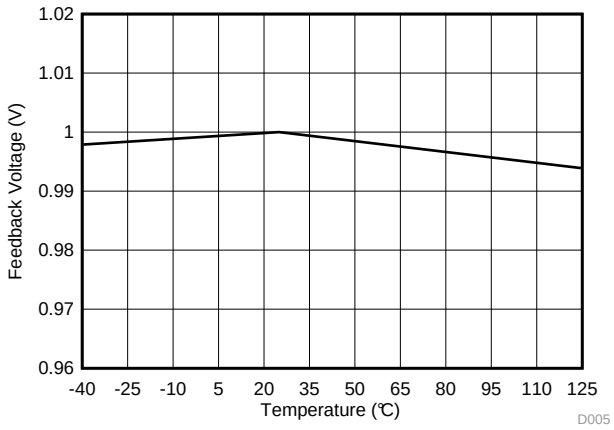


Figure 8. V_{FB_TH} vs Temperature

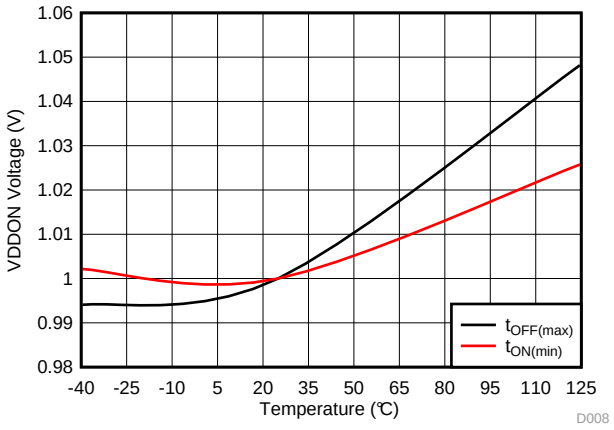


Figure 9. $t_{ON(max)}$ and $t_{OFF(min)}$ vs Temperature

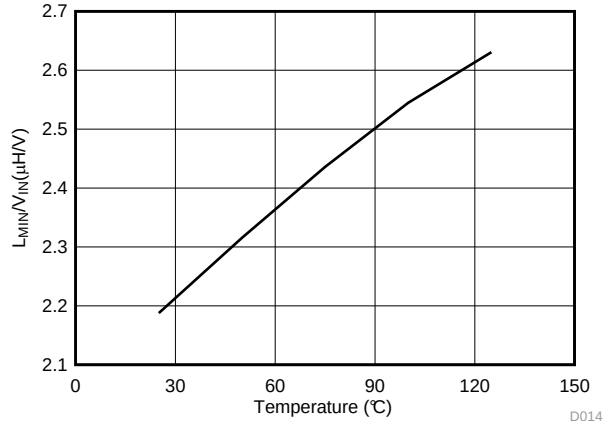


Figure 10. $(L_{MIN}/V_{IN})_{MIN}$ vs Temperature

7 Detailed Description

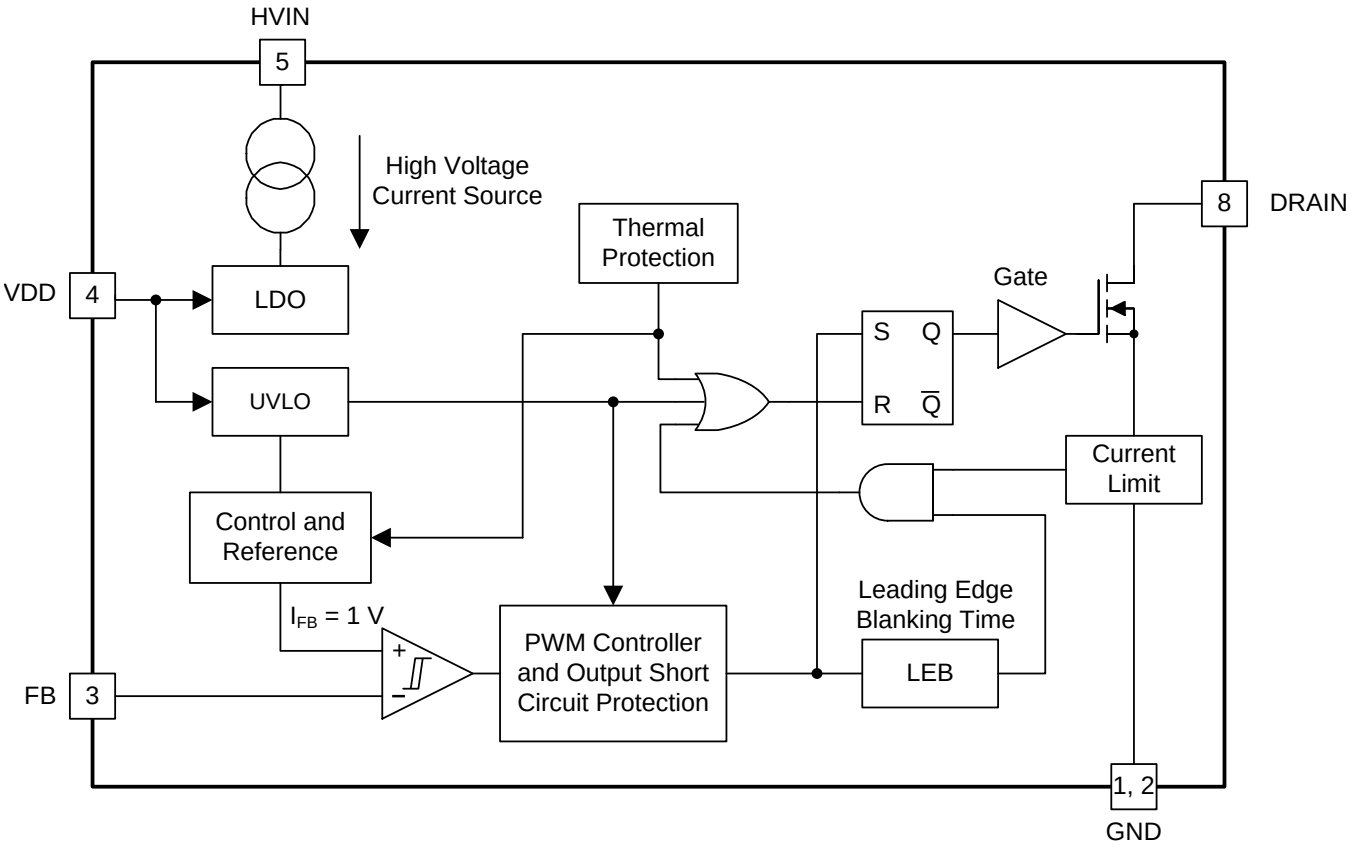
7.1 Overview

The UCC28880 integrates a controller and a 700-V power MOSFET into one monolithic device. The device also integrates a high-voltage current source, enabling start up and operation directly from the rectified mains voltage.

The low-quiescent current of the device enables excellent efficiency. The device is suitable for non-isolated AC-to-DC low-side buck and buck-boost configurations with level-shifted direct feedback, but also more traditional high-side buck, buck boost and low-power flyback converters with low standby power can be built using a minimum number of external components.

The device generates its own internal low-voltage supply (5 V referenced to the device's ground, GND) from the integrated high-voltage current source. The PWM signal generation is based on a maximum constant ON-time, minimum OFF-time concept, with the triggering of the ON-pulse depending on the feedback voltage level. Each ON-pulse is followed by a minimum OFF-time to ensure that the power MOSFET is not continuously driven in an ON-state. The PWM signal is AND-gated with the signal from a current limit circuit. No internal clock is required, as the switching of the power MOSFET is load dependent. A special protection mechanism is included to avoid runaway of the inductor current when the converter operates with the output shorted or in other abnormal conditions that can lead to an uncontrolled increase of the inductor current. This special protection feature keeps the MOSFET current at a safe operating level. The device is also protected from other fault conditions with thermal shutdown, under-voltage lockout and soft-start features.

7.2 Functional Block Diagram



7.3 Feature Description

The device integrates a 700-V rated power MOSFET switch, a PWM controller, a high-voltage current source to supply a low-voltage power supply regulator, a bias and reference block, and the following protection features, current limiter, Over Temperature Protection (OTP), Under Voltage Lockout (UVLO) and overload protection for situations like short circuit at the output.

In low-side buck and buck-boost topologies, the external level-shifted direct feedback circuit can be implemented by two resistors and a high-voltage PNP transistor.

The positive high-voltage input of the converter node (VIN+) functions as a system reference ground for the output voltage in low-side topologies. In the low-side buck topology the output voltage is negative with respect to the positive high-voltage input (VIN+), and in low-side buck-boost topology the output voltage is positive with respect to the positive high-voltage input (VIN+).

In high-side buck configuration, as well as in non-isolated flyback configuration, the output voltage is positive with respect to the negative high-voltage input (VIN-), which is the system reference ground.

The device has a low-standby power consumption (no-load condition), only 18 mW (typical) when connected to a 230-V_{AC} mains and 9 mW when connected to an 115-V_{AC} mains.

The standby power does not include the power dissipated in the external feedback path, the power dissipated in the external pre-load, the inductor in the freewheeling diode and the converter input stage (rectifiers and filter).

7.4 Device Functional Modes

7.4.1 Startup Operation

The device includes a high-voltage current source connected between the HVIN pin and the internal supply for the regulator. When the voltage on the HVIN pin rises, the current source is activated and starts to supply current to the internal 5-V regulator. The 5-V regulator charges the external capacitor connected between VDD pin and GND pin. When the VDD voltage exceeds the VDD turn on threshold ($V_{VDD(on)}$) device starts operations. The minimum voltage across HVIN and GND pins to ensure enough current to charge the capacitance on VDD pin is $V_{HVIN(min)}$. At the First switching cycle the minimum MOSFET off time is set to be > 100 µs and cycle-by-cycle is progressively reduced up to $t_{OFF(min)}$ providing soft start.

7.4.2 Feedback and Voltage Control Loop

The feedback circuit consists of a voltage comparator with the positive input connected to an internal reference voltage (referenced to GND) and the negative input connected to FB pin. When the feedback voltage at the FB pin is below the reference voltage V_{FB_TH} logic high is generated at the comparator output. This logic high triggers the PWM controller, which generates the PWM signal turning on the MOSFET. When the feedback voltage at the FB pin is above the reference voltage, it indicates that the output voltage of the converter is above the targeted output voltage set by the external feedback circuitry and MOSFET cannot be turned on.

Device Functional Modes (continued)

7.4.3 PWM Controller

The PWM controller's input comes from the feedback comparator. When the feedback comparator output goes high, the PWM controller is triggered. This starts the ON-time generation. The ON-time pulse is defined as $t_{ON(max)}$ and at the end of every ON-time pulse an OFF-time (logic low) pulse starts. The OFF-time pulse is long as $t_{OFF(min)}$ during converter normal operation, it can be longer up to $t_{OFF(ovl)}$ at start up or if risk of inductor current runaway is detected. The output of the PWM controller is the PWM signal (See Figure 11). After the OFF-time pulse has ended, the PWM controller can again receive the feedback comparator's output. If the feedback comparator's output is still high, then a new ON-time pulse followed by an OFF-time pulse is generated for the PWM signal. If the feedback comparator's output is low at the point the OFF-time has ended, then the PWM controller continues to output a logic low signal at the output (the PWM signal). The PWM signal stays low until the feedback comparator output goes high, at which point the PWM controller is again triggered, and the ON-time + OFF-time pulse is generated.

The PWM controller does not need a clock signal, and the PWM signal is load dependent. The PWM signal's maximum frequency is set to $f_{SW(max)} = (1/(t_{ON(max)} + t_{OFF(min)}))$ which occurs when the voltage on the FB pin is continuously below V_{FB_TH}.

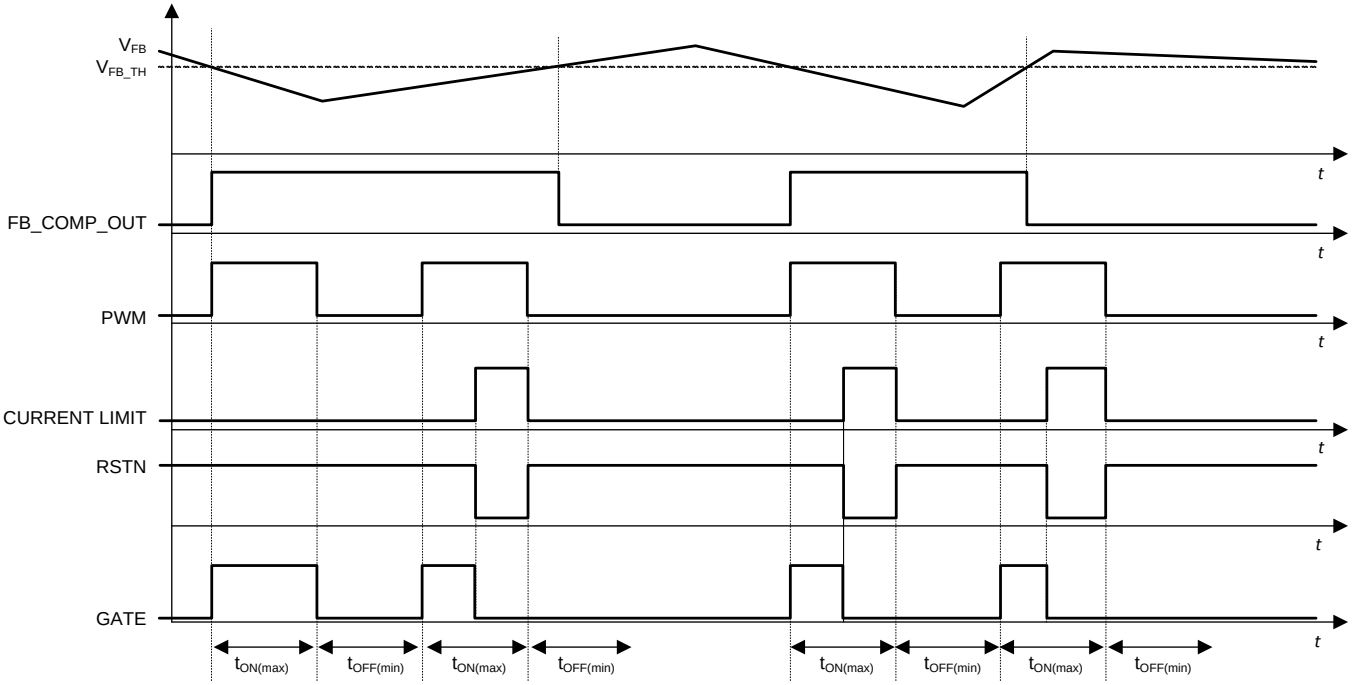


Figure 11. UCC28880 Timing Diagram

Device Functional Modes (continued)

7.4.4 Current Limit

The current limit circuit senses the current through the power MOSFET. The sensing circuit is located between the source of the power MOSFET and the GND pin. When the current in the power MOSFET exceeds the threshold I_{LIMIT}, the internal current limit signal goes high, which sets the internal RSTN signal low. This disables the power MOSFET by driving its gate low. The current limit signal is set back low after the falling edge of the PWM signal. After the rising edge of the GATE signal, there is a blanking time. During this blanking time, the current limit signal cannot go high.

7.4.5 Inductor Current Runaway Protection

To protect the device from overload conditions, including a short circuit at the output, the PWM controller incorporates a protection feature which prevents the inductor current from runaway. When the output is shorted the inductor demagnetization is very slow, low di/dt, and when the next switching cycle starts energy stored in the inductance is still high. After the MOSFET switches on, the current starts to rise from pre-existing DC value and reaches the current-limit value in a short duration of time. Because of the intrinsic minimum on-time of the device the MOSFET on-time cannot be lower than t_{MIN}, in an overload or output short circuit the energy inductance is not discharged sufficiently during MOSFET off-time, it is possible to lose control of the current leading to a runaway of the inductor current. To avoid this, if the ON time is less than t_{ON_TO} (t_{ON_TO} is a device internal time out), the controller increases the MOSFET OFF time (t_{OFF}). If the MOSFET ON-time is longer than t_{ON_OL} then t_{OFF} is decreased. The controller increases t_{OFF}, cycle-by-cycle, through discrete steps until the ON-time continues to stay below t_{ON_TO}. The t_{OFF} is increased up to $t_{OFF(ovl)}$ after that, if teh ON-time is still below t_{ON_OL} the off time is kept equal to $t_{OFF(ovl)}$. The controller decreases t_{OFF} cycle-by-cycle until the ON-time continues to stay above t_{ON_TO} up to $t_{OFF(min)}$. This mechanism prevents control loss of the inductor current and prevents over stress of the MOSFET (see typical waveforms in Figure 12 and Figure 13). At start up, the t_{OFF} is set to $t_{OFF(ovl)}$ and reduced cycle-by-cycle (if the ON time is longer than t_{ON_TO}) up to $t_{OFF(min)}$ providing a soft start for the power stage.

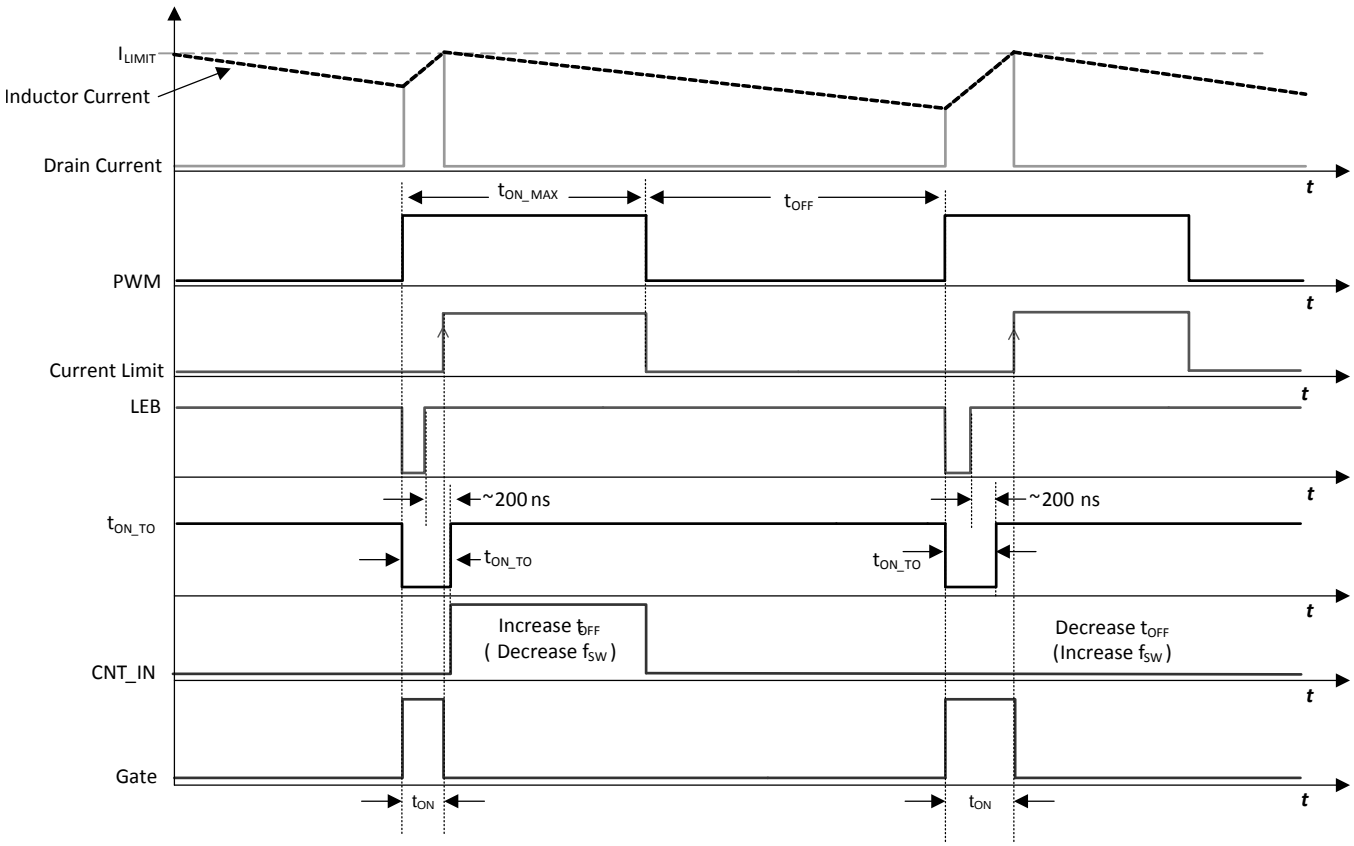


Figure 12. Current Runaway Protection Logic Timing Diagram

Device Functional Modes (continued)

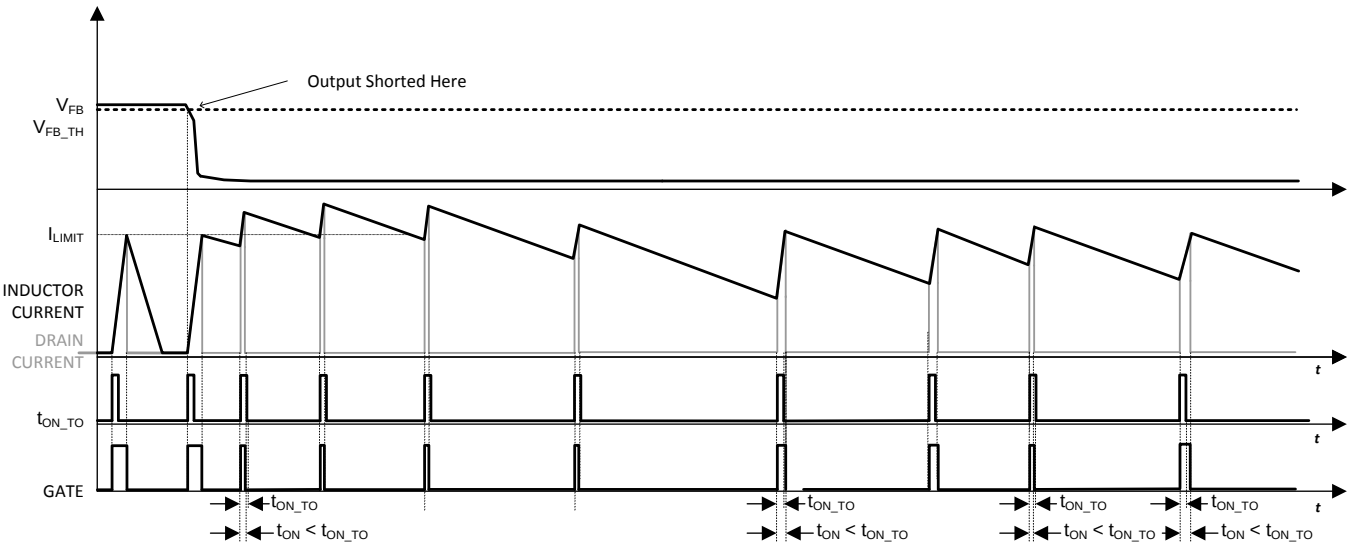


Figure 13. Current Runaway Protection, Inductor and MOSFET Current

A minimal value needs to be imposed on the inductance value to avoid nuisance tripping of the protection feature that prevents the loss of control of the inductor current. Inadvertent operation of the protection feature limits the output-power capability of the converter. This condition depends on the converter's maximum input operating voltage and temperature. Use Equation 1 to calculate your minimum inductance value.

$$L > \left[\left(\frac{L_{MIN}}{V_{IN}}\right)_{MIN}\right] T_{R(max)} \times V_{IN(max)} \quad (1)$$

The value of Equation 1 can be found by characterization graph of Figure 10.

If the inductance value is too low, such that the MOSFET on-time is always less than t_{ON_TO} timeout and the device progressively increases the MOSFET off-time up to $t_{OFF(ovl)}$, the output power is reduced and the converter fails to supply the load.

7.4.6 Over-Temperature Protection

If the junction temperature rises above $T_{J(stop)}$, the over-temperature protection is triggered. This disables the power MOSFET switching. To re-enable the switching of the MOSFET the junction temperature has to fall by $T_{J(hyst)}$ below the $T_{J(stop)}$ where the device moves out of over temperature.

8 Application and Implementation

8.1 Application Information

The UCC28880 can be used in various application topologies with direct or isolated feedback. The device can be used in low-side buck, where the output voltage is negative, or as a low-side buck-boost configuration, where the output voltage is positive. In both configurations the common reference node is the positive input node (VIN+). The device can also be configured as a LED driver in either of the above mentioned configurations. If the application requires the AC-to-DC power supply output to be referenced to the negative input node (VIN-), the UCC28880 can also be configured as a traditional high-side buck as shown in Figure 17. In this configuration, the voltage feedback is sampling the output voltage VOUT, making the DC regulation less accurate and load dependent than in low-side buck configuration, where the feedback is always tracking the VOUT. However, high-conversion efficiency can still be obtained.

8.2 Typical Application

8.2.1 12-V, 100-mA Low-Side Buck Converter

Figure 14 shows a typical application example of a non-isolated power supply, where the UCC28880 is connected in a low-side buck configuration having an output voltage that is negative with respect to the positive input voltage (VIN+). The output voltage is set to 12 V in this example, but can easily be changed by changing the value of R_{FB1}. This application can be used for a wide variety of household appliances and automation, or any other applications where mains isolation is not required.

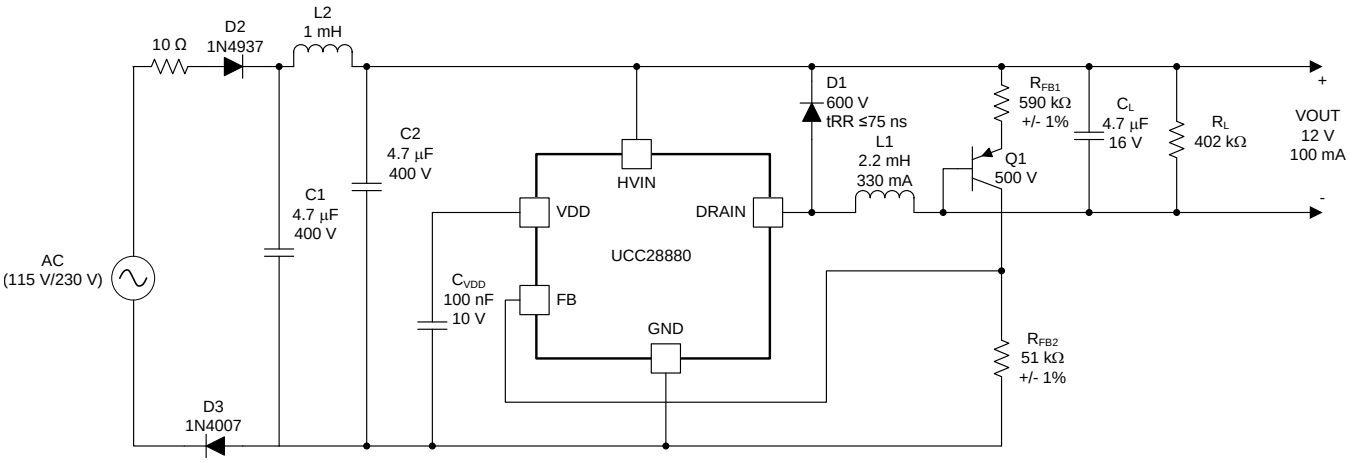


Figure 14. Universal Input, 12-V, 100-mA Output Low-Side Buck

8.2.1.1 Design Requirements

Table 1. Table 1 Design specification

DESCRIPTION		MIN	MAX	UNIT
Design Input				
V_{IN}	AC input voltage	85	265	V_{RMS}
f_{LINE}	Line frequency	47	63	Hz
I_{OUT}	Output current	0	100	mA
Design Requirements				
P_{NL}	No-load input power		50	mW
V_{OUT}	Output voltage	12	13	V
ΔV_{OUT}	Output voltage ripple		350	mV
η	Converter efficiency	68%		

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Input Stage (R_F, D2, D3, C1, C2, L2)

- Resistor R_F is a flame-proof fusible resistor. R_F limits the inrush current, and also provide protection in case any component failure causes a short circuit. Value for its resistance is generally selected between 4.7 Ω to 15 Ω.
- A half-wave rectifier is chosen and implemented by diode D2 (1N4937). It is a general purpose 1-A, 600-V rated diode. It has a fast reverse recovery time (200 ns) for improved differential-mode-conducted EMI noise performance. Diode D3 (1N4007) is a general purpose 1-A, 1-kV rated diode with standard reverse recovery time (>500 ns), and is added for improved common-mode-conducted EMI noise performance. D3 can be removed and replaced by a short if not needed.
- EMI filtering is implemented by using a single differential-stage filter (C1-L2-C2).

Capacitors C1 and C2 in the EMI filter also acts as storage capacitors for the high-voltage input DC voltage (VIN).The required input capacitor size can be calculated according formula (1).

$$C_{BULKmin} = \frac{\frac{2 \times P_{IN}}{f_{LINE(min)}} \times \left\{ \frac{1}{RCT} - \frac{1}{2 \times \pi} \times \arccos\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right\}}{2 \times V_{IN(min)}^2 - V_{BULK(min)}^2}$$

where

- $C_{BULK(min)}$ is minimum value for the total input capacitor value (C1 + C2 in the schematic of Figure 14).
- RCT = 1 in case a single wave rectifier and RCT = 2 in case of full-wave rectifier (for the schematic reported in Figure 20 RCT = 1 because of a single rectifier).
- P_{IN} is the converter input power.
- $V_{IN(min)}$ is the minimum RMS value of the AC input voltage.
- $V_{BULK(min)}$ is the minimum allowed voltage value across bulk capacitor during converter operation.
- $f_{LINE(min)}$ is the minimum line frequency when the line voltage is $V_{IN(min)}$.

The converter input power can be easily calculated as follow:

- The converter maximum output power is: $P_{OUT} = I_{OUT}$ x V_{OUT} = 0.1 A x 12.5 V = 1.25 W
- Assuming the efficiency η = 68.% the input power is $P_{IN} = P_{OUT}/\eta$ = 1.765 W

Using the following values for the other parameters

- $V_{BULK(min)}$ = 80 V
- $V_{IN(min)}$ = 85 V_{RMS} (from design specification table)
- $f_{LINE(min)}$ = 57 Hz (2)

$C_{BULK(min)}$ = 6.96 µF. Considering that electrolytic capacitors, generally used as bulk capacitor, have 20% of tolerance in value, the minimum nominal value required for C_{BULK} is:

$$C_{BULKn(min)} > \frac{C_{BULK(min)}}{(1 - TOL_{CBULK})} 8.7\,\mu F \quad (3)$$

Select C1 and C2 to be 4.7µF each (C_{BULK} = 4.7 µF + 4.7 µF = 9.4 µF > $C_{BULKn(min)}$).

By using a full-wave rectifier allows a smaller capacitor for C1 and C2, almost 50% smaller.

8.2.1.2.2 Regulator Capacitor (C_{VDD})

Capacitor C_{VDD} acts as the decoupling capacitor and storage capacitor for the internal regulator. A 100-nF, 10-V rated ceramic capacitor is enough for proper operation of the device's internal LDO.

8.2.1.2.3 Freewheeling Diode (D1)

The freewheeling diode has to be rated for high-voltage with as short as possible reverse-recovery time (t_{rr}).

The maximum reverse voltage that the diode should experience in the application, during normal operation, is given by Equation 4.

$$V_{D1(max)} = \sqrt{2} \times V_{IN(max)} = \sqrt{2} \times 265\,V = 375\,V \tag{4}$$

A margin of 20% is generally considered.

The chosen freewheeling diode for the application example is a 600-V, 1-A rated diode with a $t_{rr} \leq 75$ ns. It is possible to use a diode with higher t_{rr} but this leads to higher switching losses and lower efficiency.

8.2.1.2.4 Inductor (L1)

Initial calculations:

Ripple current at full load:

$$\Delta I_L = MIN\left(I_{LIMIT}{}^2 \times \left(I_{LIMIT} - I_{OUT}\right)\right) \tag{5}$$

Average MOSFET conduction minimum duty cycle at full load and maximum input voltage is:

$$D_{MIN} = \frac{V_{OUT} + V_d}{V_{IN(max)} - V_d} \tag{6}$$

If the converter operates in continuous conduction mode:

$$D_{MIN} = 2 \times \frac{I_{OUT}}{I_{LIMIT}} \frac{V_{OUT} + V_d}{V_{IN(max)} = V_d} \tag{7}$$

Maximum allowed switching frequency at VIN_MAX and full load:

$$F_{SW\_VIN(max)} = MIN\left(\frac{D_{MIN}}{t_{ON\_TO}} f_{SW(max)}\right) \tag{8}$$

I_{LIMIT} = 150 mA, the worst case but assuming ΔI_L = 100mA.

The converter works in continuous conduction mode ($\Delta I_L < I_{LIMIT}$) so the

$$D_{MIN} = \frac{V_{OUT} + V_d}{V_{IN(max)} - V_d} = 3.61\% \tag{9}$$

The maximum allowed switching frequency is:

$$F_{SW\_VIN(max)} = MIN\left(\frac{D_{MIN}}{t_{ON\_TO}} f_{SW(max)}\right) = f_{SW(max)} = 66\,kHz \tag{10}$$

The duty cycle does not force the MOSFET on time to go below t_{ON_TO}. If $D_{MIN}/T_{ON\_TO} < f_{SW(max)}$, the switching frequency is reduced by current runaway protection and the maximum average switching frequency is lower than $f_{SW(max)}$.

The minimum inductance value satisfies both the following conditions:

$$L1 > \frac{V_{OUT} + V_d}{\Delta I_L \times f_{SW\_VIN(max)}} = 2\,mH \tag{11}$$

$$L1 > \left[\left(\frac{L_{MIN}}{V_{IN}}\right) MIN\right] T_{J(max)} \times V_{IN(max)}\, L1 > \frac{V_{IN(max)}}{I_{LIMIT}} \times t_{ON\_TO} = \left(2.65 \times \frac{\mu H}{V} \times 375\,V\right) \cong 1\,mH \tag{12}$$

In the application example, 2.2 mH is selected as the minimum standard value that satisfy Equation 11 and Equation 12.

8.2.1.2.5 Output Capacitor (CL)

The value of the output capacitor impacts the output ripple. Depending on the combination of capacitor value and equivalent series resistor (R_{ESR}). A larger capacitor value also has an impact on the start-up time. For a typical application, the capacitor value can start from 47 µF, to hundreds of µF. A guide for sizing the capacitor value can be calculated by the following equations:

$$C_L > 4 \times \frac{I_{LIMIT} - I_{OUT}}{f_{SW(max)} \times \Delta V_{OUT}} = 4 \times \frac{270\,mA - 100\,mA}{350\,mV \times 66\,kHz} = 30\,\mu F \quad (13)$$

$$R_{ESR} < \frac{\Delta V_{OUT}}{I_{LIMIT}} = 1\,\Omega \quad (14)$$

Take into account that both C_L and R_{ESR} contribute to output voltage ripple. A first pass capacitance value can be selected and the contribution of C_L and R_{ESR} to the output voltage ripple can be evaluated. If the total ripple is too high the capacitance value has to increase or R_{ESR} value must be reduced. In the application example C_L was selected (47 µF) and it has an R_{ESR} of 0.3 Ω. So the R_{ESR} contributes for 1/3 of the total ripple. The formula that calculates C_L is based on the assumption that the converter operates in burst of four switching cycles. The number of bursts per cycle could be different, the formula for C_L is a first approximation.

8.2.1.2.6 Load Resistor (R_L)

The resistor should be chosen so that the output current in any standby/no-load condition is higher than the leakage current through the integrated power MOSFET. If the standby load current is ensured to always be larger than the specified $I_{LEAKAGE}$, the R_L is not needed. If OVP protection is required for safety reasons, then a zener could be placed across the output (not fitted in the application example). In the application example R_L = 402 kΩ. This ensures a minimum load current of at least ~30 µA when V_{OUT} = 12 V.

8.2.1.2.7 Feedback Path (Q1, R_{FB1}, R_{FB2})

The feedback path of Q1, R_{FB1} and R_{FB2} implements a level-shifted direct feedback. R_{FB2} sets the current through the feedback path, and R_{FB1} sets the output voltage. Q1 acts as the level shifter and needs to be rated for high voltage. The output voltage is determined as follows:

$$V_{OUT} = V_{FB\_TH} \times \frac{R_{FB1}}{R_{FB2}} + V_{BE}$$

where

- V_{OUT} is the output voltage.
- V_{FB_TH} is the FB pin voltage threshold = V_{FB_TH}.
- V_{BE} is the base-Emitter saturation voltage of the external PNP transistor.
- R_{FB1} is the external resistor setting the output voltage (depending on the current set by R_{FB2}, and the V_{be}).
- R_{FB2} is the external resistor setting the current through the external feedback path. (15)

For the application example a target of ~20-µA of current is selected through the external feedback path (I_{FB}).

$$R_{FB2} = \frac{V_{FB\_TH}}{I_{FB}} = \frac{1.0\,V}{\approx 20\,\mu A} = 50\,k\Omega \quad (16)$$

Choose a standard resistor size for R_{FB2} = 51 kΩ. For the high-voltage PNP transistor choose a 500-V rated transistor with a V_{BE} ≈ 0.5 V for the feedback current. To achieve the 12-V output voltage R_{FB1} needs to be:

$$R_{FB1} = \frac{V_{OUT} - V_{BE}}{V_{FB\_TH}} \times R_{FB1} = \frac{12\,V - 0.5\,V}{1\,V} \times 51\,k\Omega = 586\,k\Omega \quad (17)$$

Choose a standard resistor size for R_{FB1} = 591 kΩ.

To change the output voltage, change the value for R_{FB1}. For example, to target a 5-V output voltage, R_{FB1} should be changed to a 230-kΩ resistor.

Accuracy of the output-voltage level depends proportionally on the variation of V_{FB_TH}, and on the absolute accuracy of V_{BE} according to Equation 16 and Equation 17.

The current through the feedback path is connected over the high voltage input (VIN), and this feedback current is always on. Higher current provides less noise-sensitive feedback, the feedback current should be minimized in order to minimize the total power consumption.

8.2.1.3 Application Curves

Figure 15 shows the efficiency diagram of the converter, a design previous discussed. Figure 16 shows the output voltage vs output current diagram. The two diagrams were obtained by measuring efficiency (Figure 15), output current and output voltage (Figure 16) moving resistive load value from infinite (load disconnected) up to zero (output shorted). The different curves of the diagram correspond to different AC input voltage.

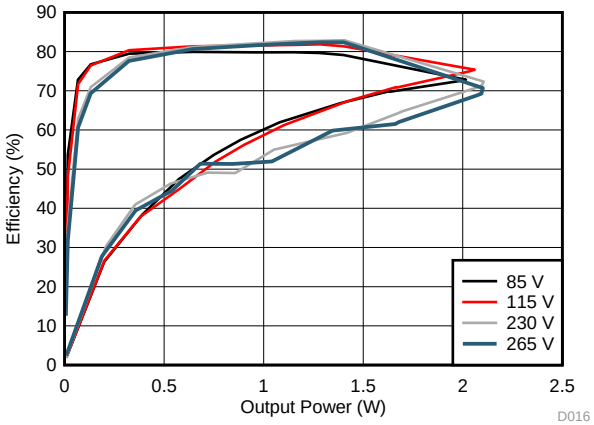


Figure 15. Efficiency vs Output Power Diagrams

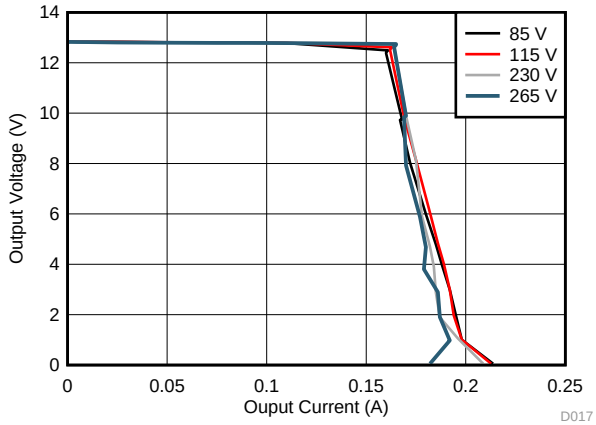


Figure 16. Output Voltage vs Output Current Diagram

Table 2 shows converter efficiency. Table 3 shows the converter input power in no-load conditions and output shorted conditions. The no-load condition shows the converter stand-by performance.

Table 2. Converter Efficiency

VIN_AC (VRMS)	LOAD (mA)	EFFICIENCY (%)	AVERAGE EFFICIENCY (%)
115	25	80.3	81.3
	50	81.4	
	75	81.6	
	100	81.9	
230	25	78.5	81.2
	50	81.1	
	75	82.1	
	100	82.7	

Table 3. No-Load and Output Shorted Converter Input Power

V_{IN} (V_{RMS})	NO LOAD P_{IN} (mW)	OUTPUT SHORTED P_{IN} (mW)	OUTPUT SHORTED I_{OUT} (mA)
85	16	453	214
115	19.5	435	213
140	22.5	417	211
170	26	443	213
230	33	430	209
265	37.5	344	182

8.2.2 12-V, 100-mA, High-Side Buck Converter

Figure 17 shows a typical application example of a non-isolated power supply, where the UCC28880 is connected in a high-side buck configuration having an output voltage that is positive with respect to the negative high-voltage input (VIN-).

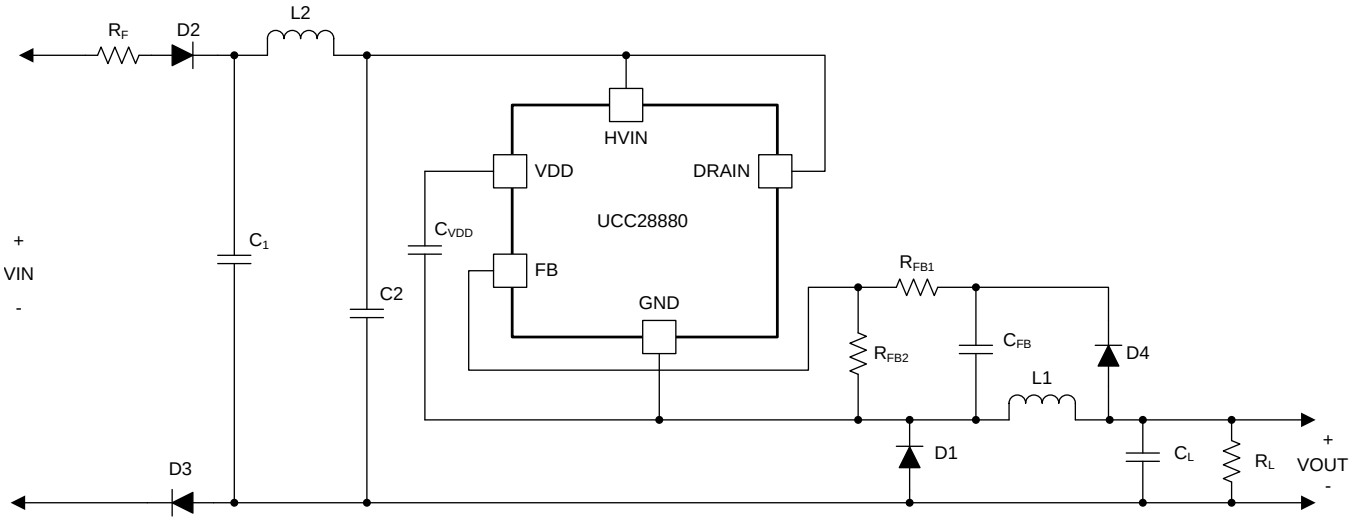


Figure 17. High-Side Buck Converter Schematic

8.2.2.1 Design Requirements

Table 4. 2 Design specification

DESCRIPTION		MIN	MAX	UNIT
Design Input				
V_{IN}	AC input Voltage	85	265	V_{RMS}
f_{LINE}	Line frequency	47	63	Hz
I_{OUT}	Output current	0	100	mA
Design requirements				
P_{NL}	No-load input power		50	mW
V_{OUT}	Output voltage	12	14	V
ΔV_{OUT}	Output voltage ripple		250	mV
η	Converter efficiency	68%		

8.2.2.2 Detailed Design Procedure

The low-side buck converter and high-side buck converter design procedures are very similar.

8.2.2.2.1 Feedback path (C_{FB}, R_{FB1} and R_{FB2}) and Load Resistor (R_L)

In low-side buck converter the output voltage is always sensed by the FB pin and UCC28880 internal controller can turn on the MOSFET on VOUT. In high-side buck converter applications the information on the output voltage value is stored on C_{FB} capacitor. This information is not updated in real time. The information on C_{FB} capacitor is updated just after MOSFET turn-off event. When the MOSFET is turned off, the inductor current forces the freewheeling diode (D1 in Figure 17) to turn on and the GND pin of UCC28880 goes negative at $-V_{d1}$ (where V_{d1} is the forward drop voltage of diode D1) with respect to the negative terminal of bulk capacitor (C1 in Figure 17). When D1 is on, through diode D4, the C_{FB} capacitor is charged at $V_{OUT} – V_{d4} + V_{d1}$. Set the output voltage regulation level using Equation 18.

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT(T)} - V_{d4} + V_{d1} - V_{FB\_TH}}{V_{FB\_TH}} \cong \frac{V_{OUT(T)} - V_{FB\_TH}}{V_{FB\_TH}}$$

where

- V_{FB_TH} is the FB pin reference voltage.
- V_{OUT_T} is the target output voltage.
- R_{FB1}, R_{FB2} is the resistance of the resistor divider connected with FB pin (see Figure 17)
- The capacitor C_{FB} after D1 is discharged with a time constant that is τfb = C_{FB} x (R_{FB1} + R_{FB2}).
- Select the time constant τ_{FB}, given in Equation 19 (18)

$$\tau_{FB} = C_{FB} \times \left(R_{FB1} + R_{FB2}\right) \cong \frac{1}{10} \times C_L \times R_L \quad (19)$$

The time constant selection leads to a slight output-voltage increase in no-load or light-load conditions. In order to reduce the output-voltage increase, increase τ_{FB}. The drawback of increasing τ_{FB} is t in high-load conditions V_{OUT} could drop.

8.2.2.3 Application Curves

Figure 18 shows the output voltage vs output current. Different plots correspond to different converter AC input voltages. Figure 19 shows efficiency changes vs output power. Different plots correspond to different converter AC input voltages.

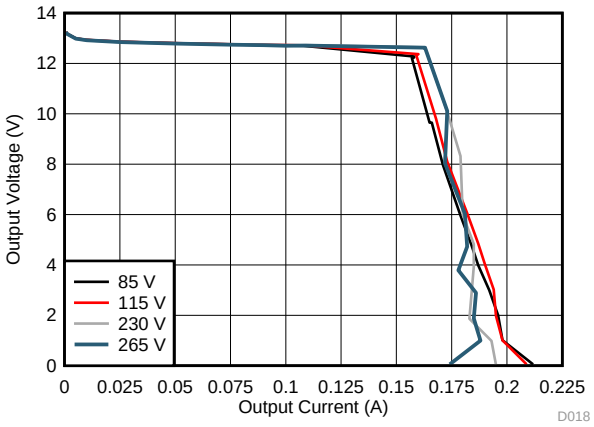


Figure 18. Output IV Characteristic

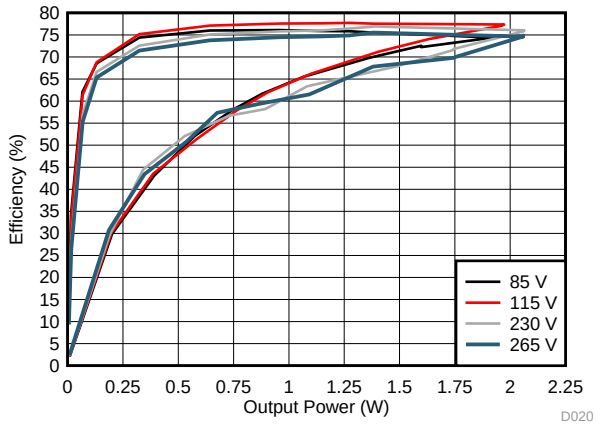


Figure 19. Efficiency vs P_{OUT}

Table 5. Converter Efficiency

V_{IN_AC} (V_{RMS})	LOAD (mA)	EFFICIENCY (%)	AVERAGE EFFICIENCY (%)
115	25	75.2	76.8
	50	77.1	
	75	77.6	
	100	77.7	
230	25	72.6	74.8
	50	75.1	
	75	75.7	
	100	76.3	

Table 6. No-Load and Output Shorted Converter Input Power

V_{IN} (V_{RMS})	NO LOAD P_{IN} (mW)	OUTPUT SHORTED P_{IN} (mW)	OUTPUT SHORTED I_{OUT} (mA)
85	31	415	212
115	34	399	209
140	36	414	211
170	38	401	208
230	44	394	195
265	47	333	174

8.2.3 Additional UCC28880 Application Topologies

8.2.3.1 Low-Side Buck and LED Driver – Direct Feedback (level-shifted)

Features include:

- Output Referenced to Input
- Negative Output (V_{OUT}) with Respect to VIN+
- Step Down: $V_{OUT} < V_{IN}$
- Direct Level-Shifted Feedback

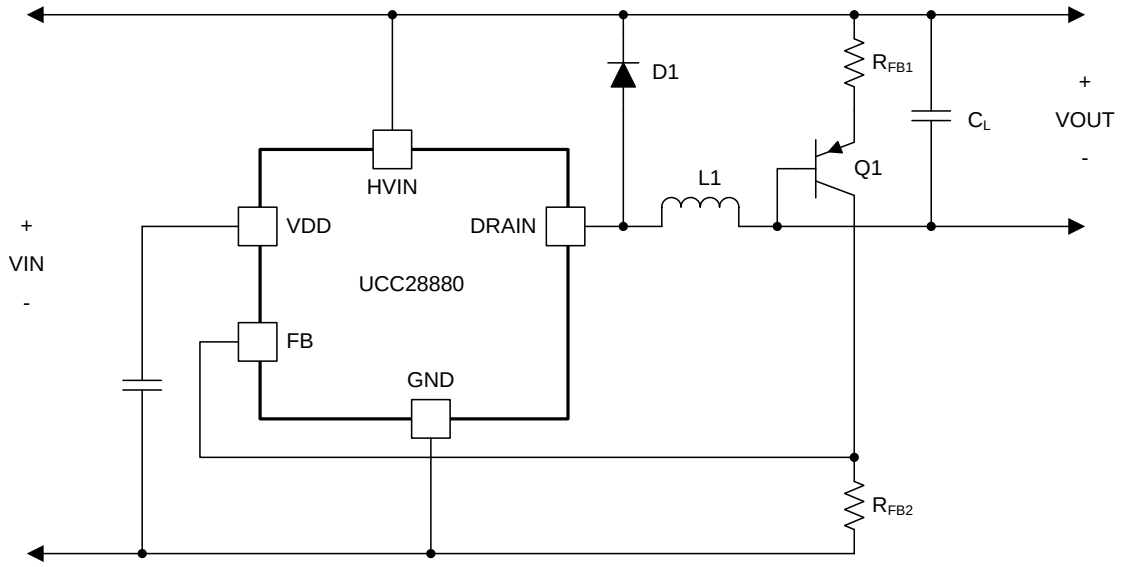


Figure 20. Low-Side Buck – Direct feedback (level-shifted)

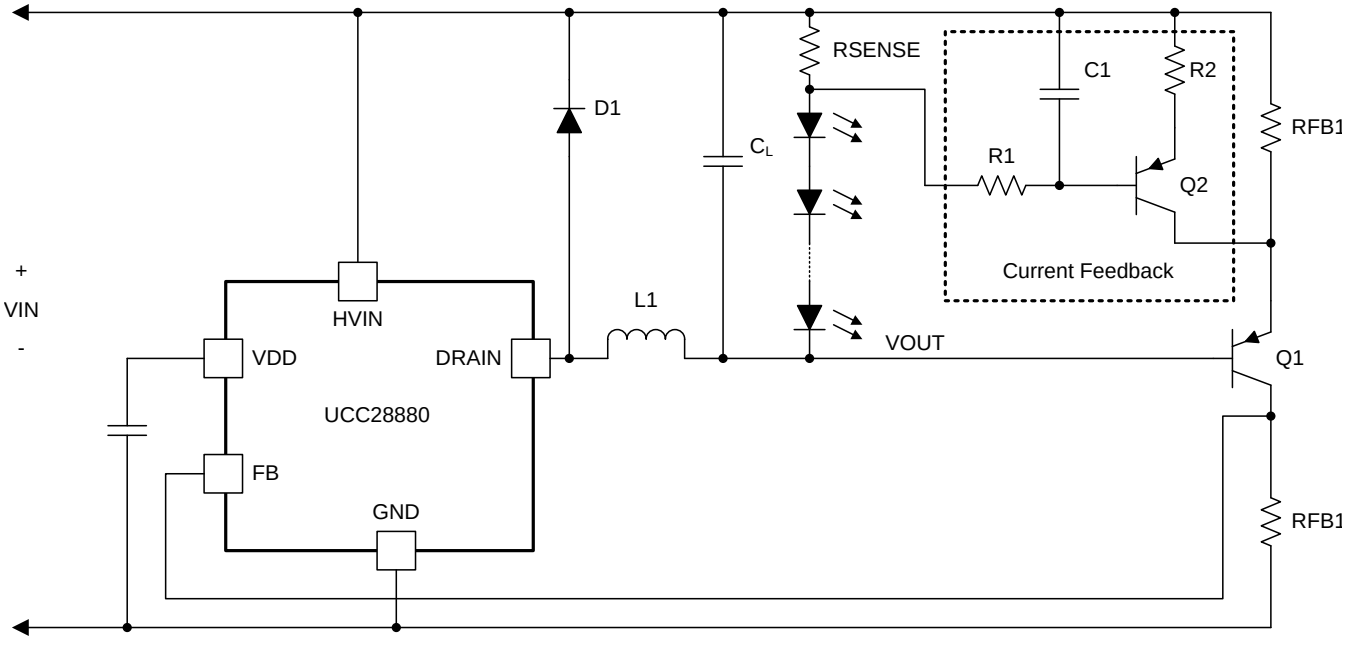


Figure 21. Low-Side Buck LED Driver – Direct feedback (level-shifted)

8.2.3.2 12-V, 100-mA High-Side Buck Converter

Features include:

- Output Referenced to Input
- Positive Output (V) with Respect to VIN-
- Step Down (V_{OUT} < V_{IN})

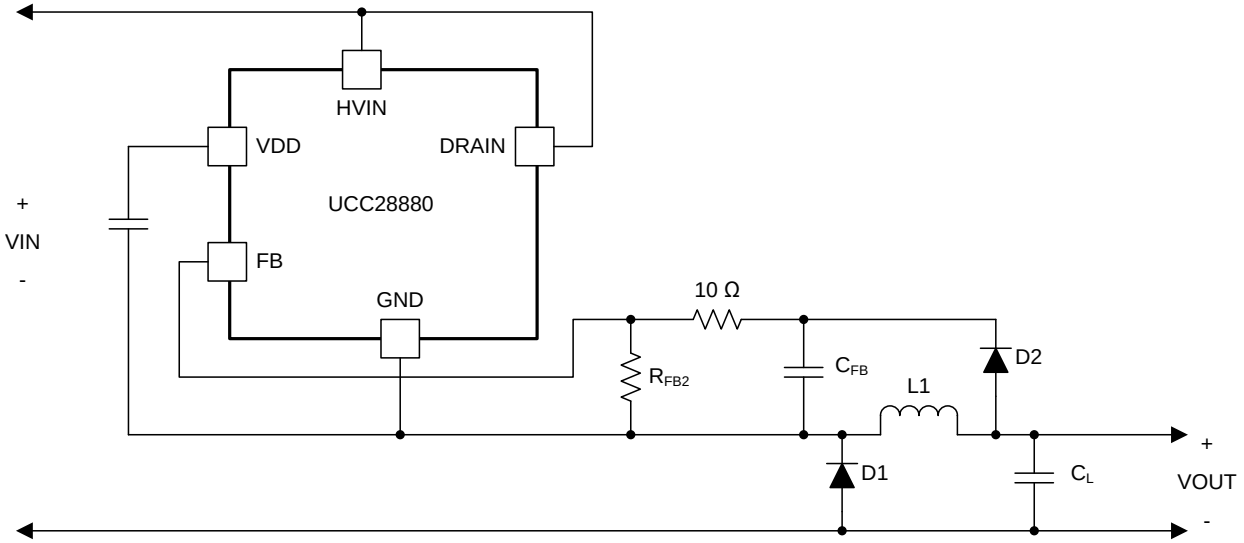


Figure 22. High-Side Buck Converter Schematic

8.2.3.3 Non-Isolated, Low-Side Buck-Boost Converter

Features Include:

- Output referenced to input
- Positive output (V_{OUT}) with respect to VIN+
- Step Up, Step Down: V_{OUT} </> V_{IN}
- Direct Level-Shifted Feedback

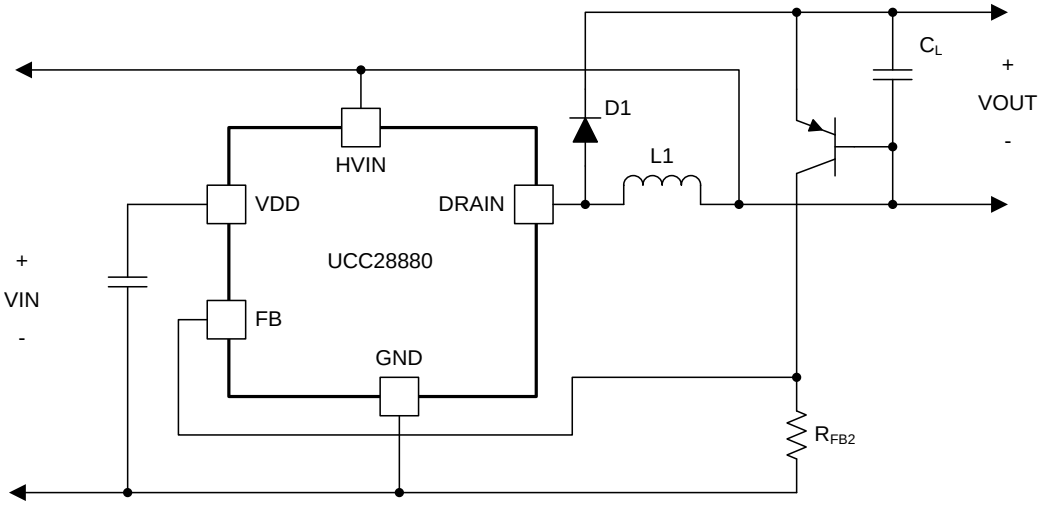


Figure 23. Low-Side Buck-Boost Converter

8.2.3.4 9.5 Non-Isolated, High-Side Buck-Boost Converter

Features include:

- Output Referenced to Input
- Positive Output (V_{OUT}) with Respect to VIN-
- Step Up, Step Down: V_{OUT} </> V_{IN}

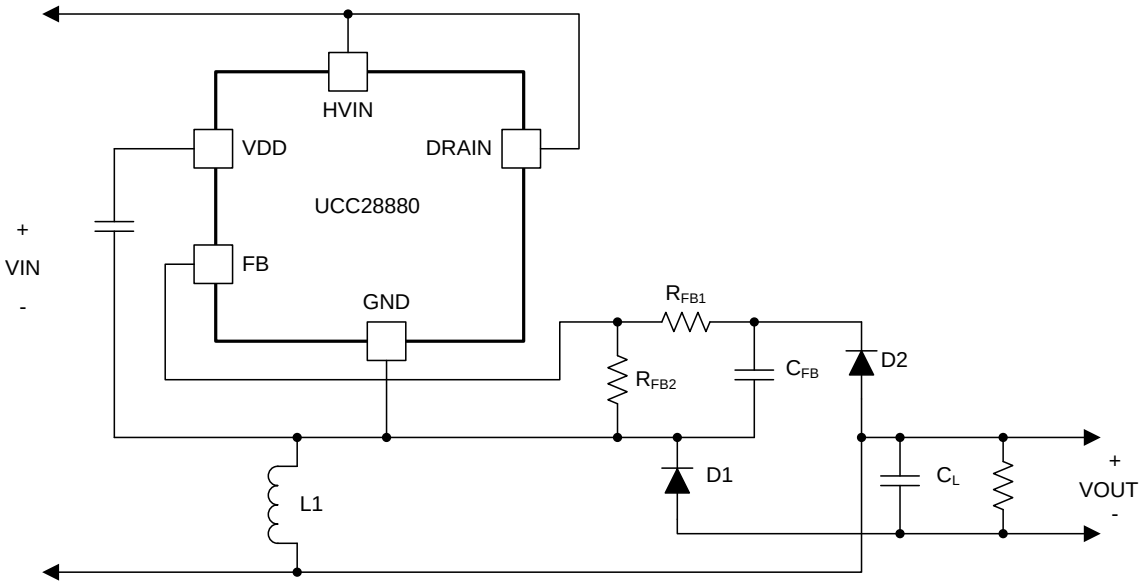


Figure 24. High-Side Buck-Boost Converter

8.2.3.5 9.6 Non-Isolated Flyback Converter

Features include:

- Output Referenced to Input
- Positive Output (V_{OUT}) with Respect VIN-
- Direct Feedback

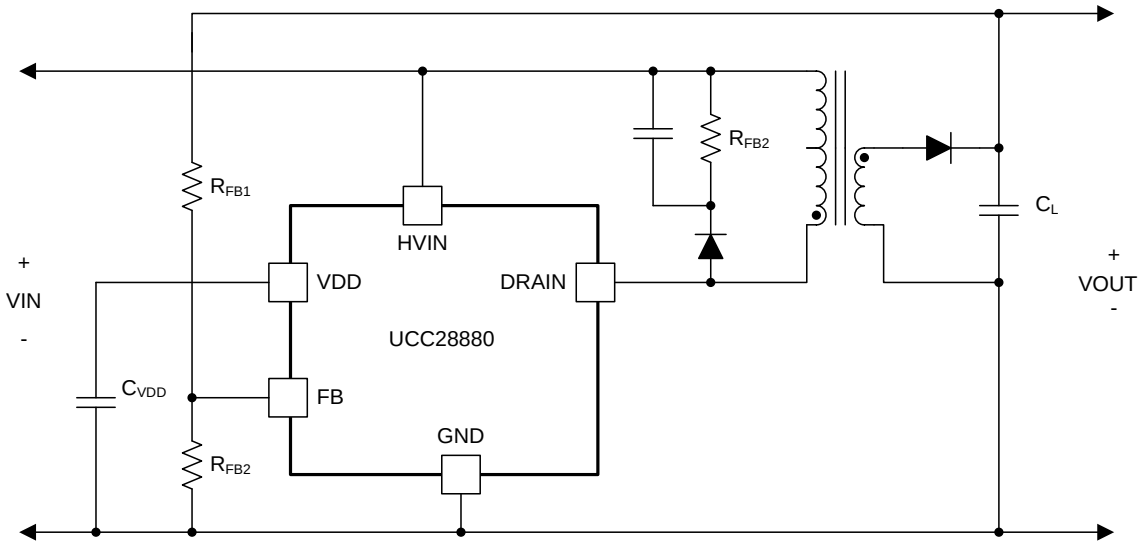


Figure 25. Non-Isolated Flyback Configuration

8.2.3.6 Isolated Flyback Converter

Features include:

- Output Isolated from
- Input Direct Feedback

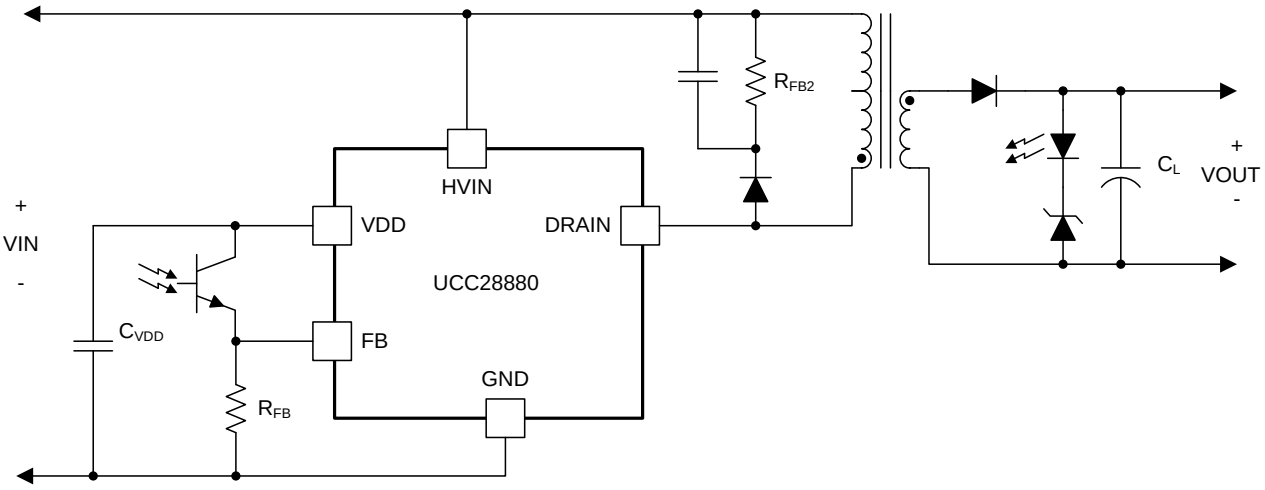


Figure 26. Isolated Flyback Converter

9 Power Supply Recommendations

The VDD capacitor recommended value is 100 nF to ensure high phase margin of the internal 5V- regulator and it should be placed close to VDD pin and GND pins to minimize the series resistance and inductance.

The VDD pin provides a regulated 5V output but it is not intended as a supply for external load. Do not supply VDD pin with external voltage source (for example the auxiliary winding of flyback converter).

Always keep GND pin 1 and GND pin 2 connected together with the shortest possible connection.

10 Layout

10.1 Layout Guidelines

- In both buck and buck-boost low-side configurations, the copper area of the switching node DRAIN should be minimized to reduce EMI.
- Similarly, the copper area of the FB pin should be minimized to reduce coupling to feedback path. Loop C_L, Q1, R_{FB1} should be minimized to reduce coupling to feedback path.
- In buck and buck-boost high side the GND, VDD and FB pins are all part of the switching node so the copper area connected with these pins should be minimized
- Minimum distance between 700-V coated traces is 1.41 mm (60 mils).

10.2 Layout Example

Figure 27 shows and example PCB layout for UCC28880 in low-side buck configuration.

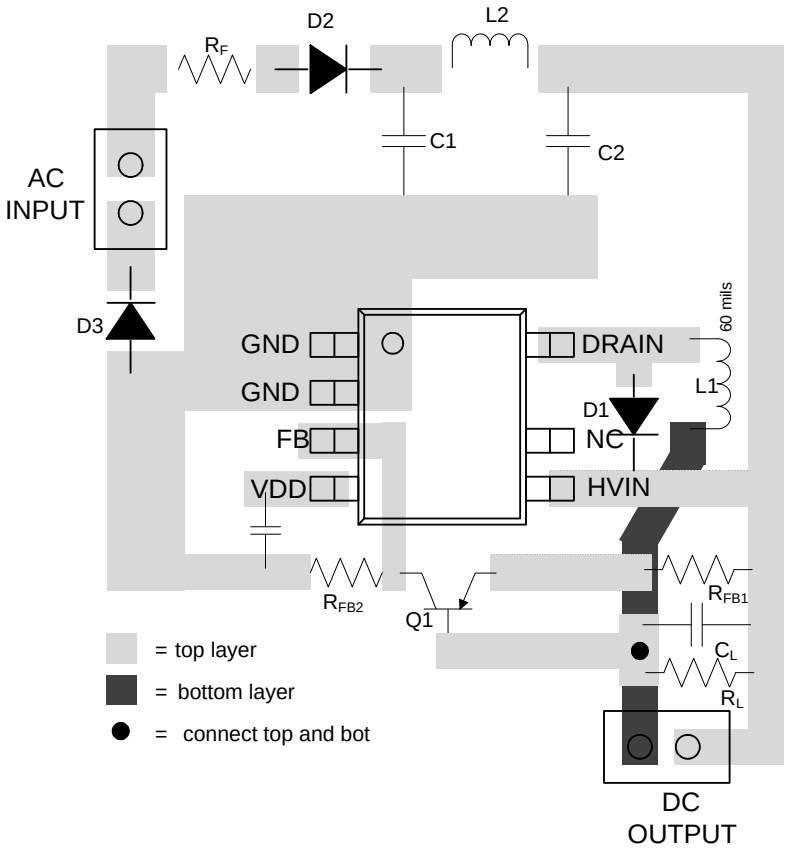


Figure 27. UCC28880 Layout Example

11 器件和文档支持

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28880D	NRND	Production	SOIC (D) | 7	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28880
UCC28880D.B	NRND	Production	SOIC (D) | 7	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28880
UCC28880DR	NRND	Production	SOIC (D) | 7	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28880
UCC28880DR.B	NRND	Production	SOIC (D) | 7	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28880

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

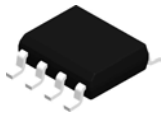
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

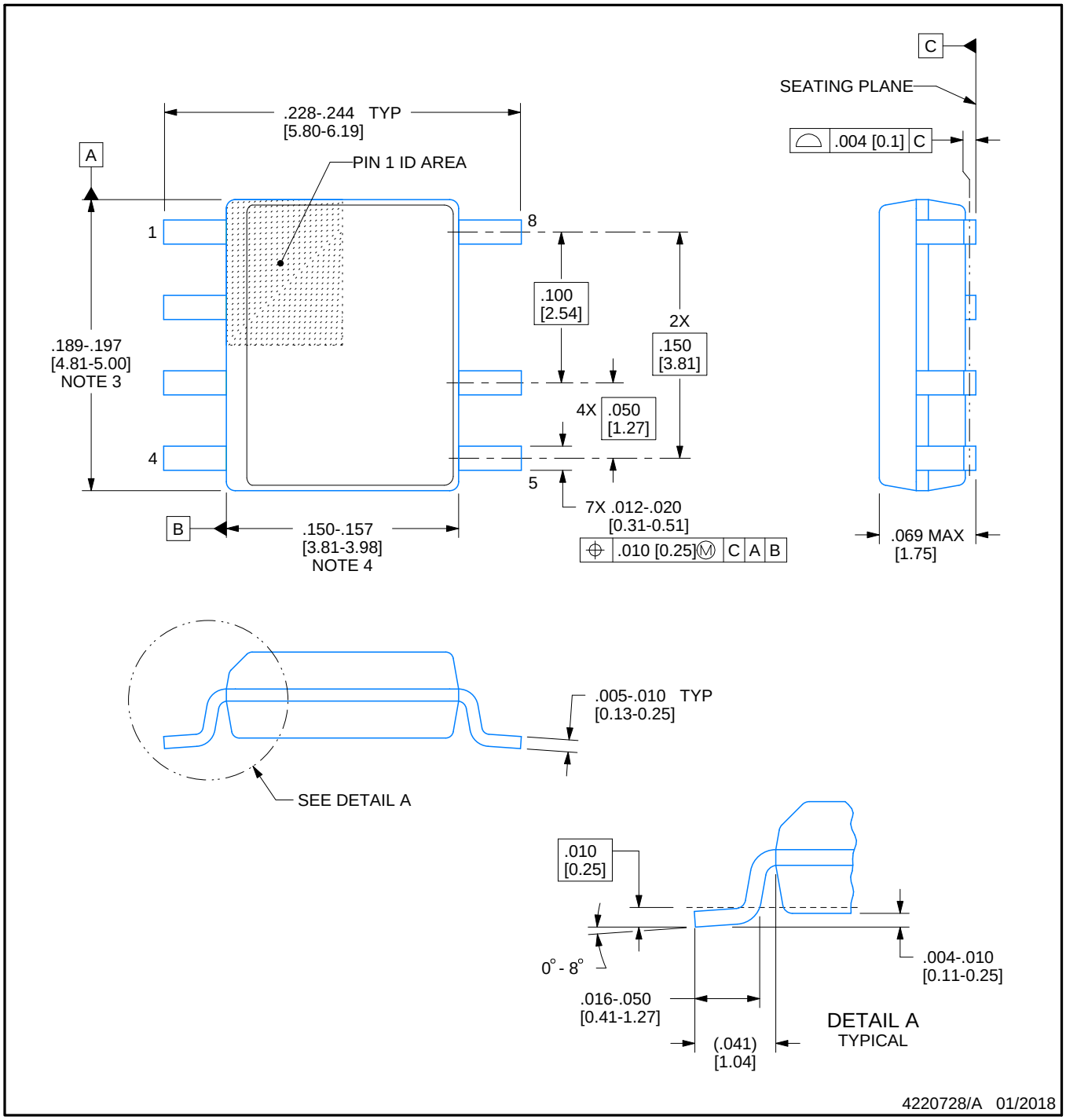


PACKAGE OUTLINE

D0007A

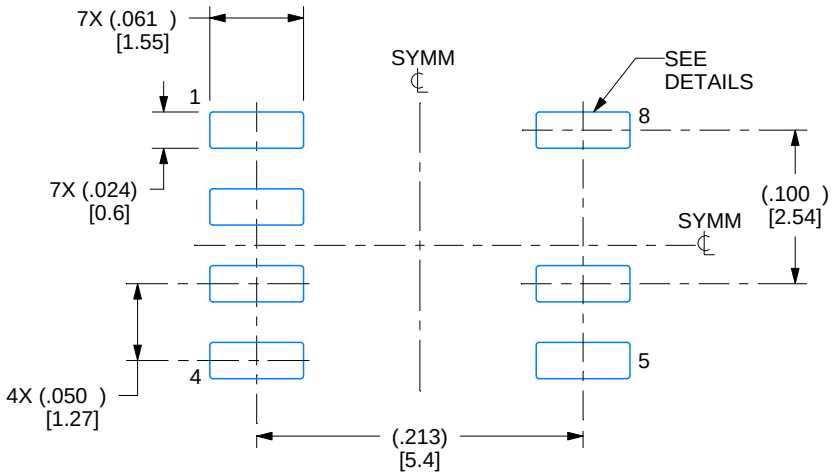
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

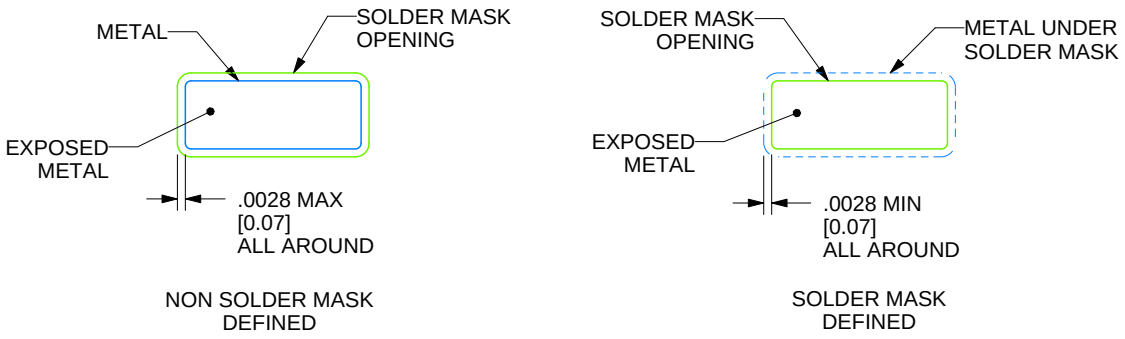


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4220728/A 01/2018

NOTES: (continued)

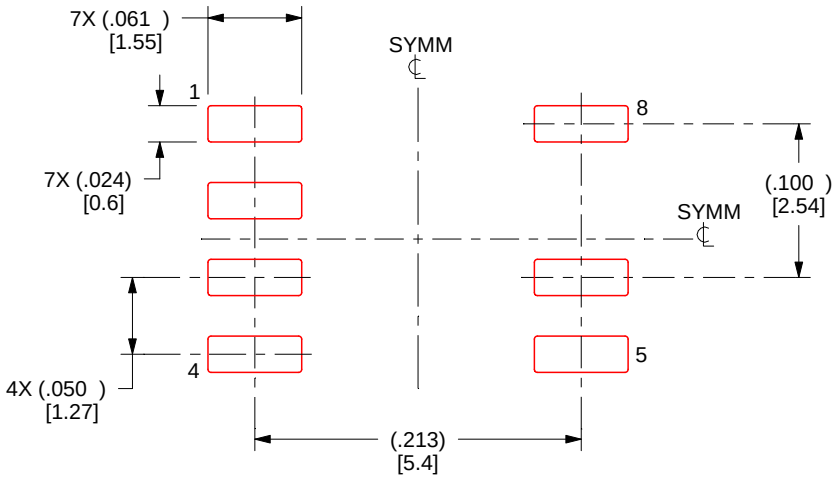
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0007A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4220728/A 01/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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