UCC28722 具有一次侧稳压和 BJT 驱动功能的恒压、恒流控制器

1 特性

- 低于 50mW 的无负载功耗
- 一次侧稳压 (PSR) 免除了对光耦合器的需要
- 动态双极性结型晶体管 (BJT) 驱动
- 线路和负载具有 ±5% 电压调节和电流调节能力
- 80kHz 最大开关频率可实现高功率密度充电器设计
- 针对最高总体效率的准谐振谷值开关运行
- 宽 VDD 范围允许使用小型偏置电容器
- 输出过压、低线路和过流保护功能
- 可编程电缆补偿
- 小外形尺寸晶体管 (SOT) 23-6 封装

2 应用

- 用于消费类电子产品的 USB 兼容适配器和充电器
  - 智能电话
  - 平板电脑
  - 摄像机
- 适用于电视和台式机的备用电源
- 白色家电

3 说明

UCC28722 反激电源控制器无需使用光耦合器即可提供单独输出的恒定电压 (CV) 和恒定电流 (CC) 输出稳压。此器件处理来自一次侧电源开关和辅助反激式绕组的信息，以对输出电压和电流进行精确控制。

可动态控制工作状态并定制调制配置文件，支持在所有负载条件下高效运行，并且不会影响输出瞬态响应。

UCC28722 所采用的控制算法使得工作效率符合甚至超过现行标准。输出驱动接口与双极型晶体管功率开关相连实现了低成本转换器设计。带有谷值开关的断续导通模式 (DCM) 减少了开关损耗，调制开关频率和一次侧峰值电流振幅（FM 和 AM）可在整个负载和线路范围内保持高转换效率。

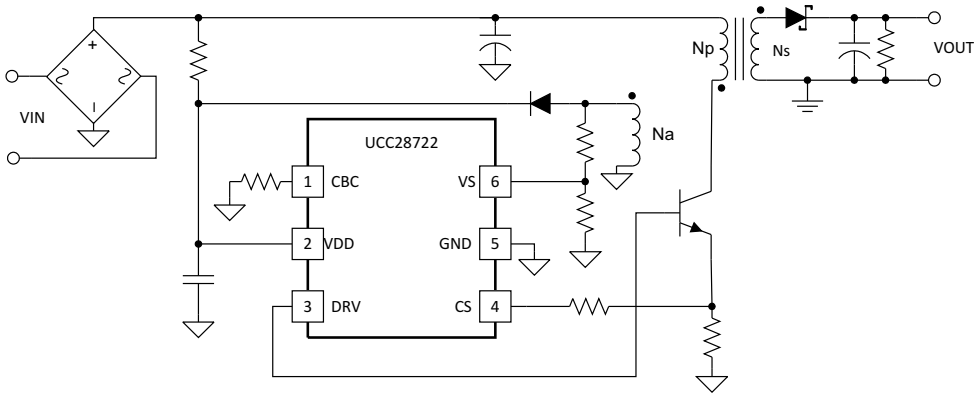
此控制器的最大开关频率为 80kHz，并且一直保持对变压器内峰值一次侧电流的控制。输出过压和过流以及输入欠压保护 特性 有助于抑制一次侧和二次侧应力分量。此外，UCC28722 可通过设定外部电阻来补偿电缆中的压降。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC28722	DBV (6)	2.90mm x 1.60mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化的应用示意图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (January 2014) to Revision B **Page**

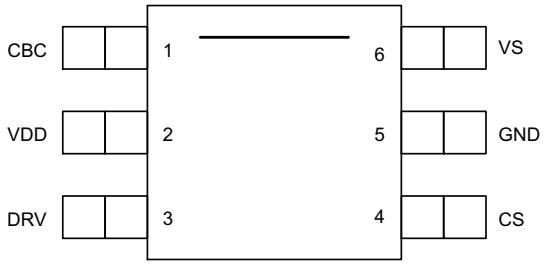
- 已添加*ESD 额定值表，特性 说明*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Original (December 2013) to Revision A **Page**

- 已更改 简化应用示意图。 ... 1
- Changed Supply current, fault values from 95 µA and 170 µA to 2.00 mA and 2.65 mA. ... 5
- Changed Bias Supply Current vs VDD Voltage image. ... 6
- Changed Operating Current vs Junction Temperature image. ... 6
- Changed Functional Block Diagram. ... 8
- Changed Simplified Flyback Convertor image. ... 11
- Changed C_{DD} equation. ... 20

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CBC	1	I	Cable compensation is a programming pin for compensation of cable voltage drop. Cable compensation is programmed with a resistor to GND.
CS	4	I	Current sense input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage is used to monitor and control the peak primary current. A series resistor can be added to this pin to compensate the peak switch current levels as the AC-mains input varies.
DRV	3	O	Drive is an output used to drive the base of an external high voltage NPN transistor.
GND	5	—	The ground pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal return paths.
VDD	2	I	VDD is the bias supply input pin to the controller. A carefully-placed bypass capacitor to GND is required on this pin.
VS	6	I	Voltage sense is an input used to provide voltage and timing feedback to the controller. This pin is connected to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider is used to program the AC-mains run and stop thresholds and line compensation at the CS pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{VDD}	Bias supply voltage, VDD			38	V
I_{DRV}	Continuous base current sink			50	mA
I_{DRV}	Continuous base current source			Self-limiting	mA
I_{VS}	Peak current, VS			–1.2	mA
V_{DRV}	Base drive voltage at DRV		–0.5	Self-limiting	V
	Voltage	VS	–0.75	7	V
		CS, CBC	–0.5	5	V
T_J	Operating junction temperature		–55	150	°C
	Lead temperature 0.6 mm from case for 10 seconds			260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Bias supply operating voltage	9		35	V
C_{VDD}	VDD bypass capacitor	1.0		10	µF
R_{CBC}	Cable-compensation resistance	10			kΩ
I_{VS}	VS pin current	−1			mA
T_J	Operating junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		UCC28722 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, R_{CBC} = open, T_A = -40°C to 125°C, $T_A = T_J$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state		2.00	2.65	mA
I_{WAIT}	Supply current, wait	I_{DRV} = 0, wait state		95	170	µA
I_{START}	Supply current, start	I_{DRV} = 0, V_{VDD} = 18 V, start state, I_{HV} = 0		1.0	1.5	µA
I_{FAULT}	Supply current, fault	I_{DRV} = 0, fault state		2.00	2.65	mA
UNDERVOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turnon threshold	V_{VDD} low to high	19	21	23	V
$V_{VDD(off)}$	VDD turnoff threshold	V_{VDD} high to low	7.2	7.7	8.3	V
VS INPUT						
V_{VSR}	Regulating level	Measured at no-load condition, T_J = 25°C(1)	3.99	4.05	4.11	V
V_{VSNC}	Negative clamp level	I_{VS} = –300 µA, volts below ground	190	250	325	mV
I_{VSB}	Input bias current	V_{VS} = 4 V	–0.25	0	0.25	µA
CS INPUT						
$V_{CST(max)}$	Max CS threshold voltage	V_{VS} = 3.7 V	730	780	820	mV
$V_{CST(min)}$	Min CS threshold voltage	V_{VS} = 4.35 V	170	190	220	mV
K_{AM}	AM control ratio	$V_{CST(max)}$ / $V_{CST(min)}$	3.6	4.0	4.4	V/V
V_{CCR}	Constant current regulating level	CC regulation constant	314	330	347	mV
K_{LC}	Line compensation current ratio	I_{VSLS} = –300 µA, I_{VSLS} / current out of CS pin	24.0	25.0	28.6	A/A
T_{CSLEB}	Leading-edge blanking time	DRV output duration, V_{CS} = 1 V	230	290	355	ns
DRIVER						
$I_{DRS(max)}$	Maximum DRV source current	V_{DRV} = 2 V, V_{VDD} = 9 V, V_{VS} = 3.85 V	31	37	42	mA
$I_{DRS(min)}$	Minimum DRV source current	V_{DRV} = 2 V, V_{VDD} = 9 V, V_{VS} = 4.30 V	15	19	23	mA
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 10 mA		1	2.4	Ω
V_{DRCL}	DRV clamp voltage	V_{VDD} = 35 V		5.9	7	V
R_{DRVSS}	DRV pulldown in start state			20	25	kΩ
TIMING						
$f_{SW(max)}$	Maximum switching frequency	V_{VS} = 3.7 V	72	80	89	kHz
$f_{SW(min)}$	Minimum switching frequency	V_{VS} = 4.35 V	570	650	750	Hz
t_{ZTO}	Zero-crossing timeout delay		2.4	3.1	3.7	µs
PROTECTION						
V_{OVP}	Overvoltage threshold	At VS input, T_J = 25°C(1)	4.49	4.60	4.75	V
V_{OCP}	Overcurrent threshold	At CS input	1.4	1.5	1.6	V
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin increasing	188	225	277	µA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin decreasing	70	80	100	µA
K_{VSL}	VS line sense ratio	$I_{VSL(run)}$ / $I_{VSL(stop)}$	2.45	2.80	3.05	A/A
$T_{J(stop)}$	Thermal shutdown temperature	Internal junction temperature		165		°C
CABLE COMPENSATION						
$V_{CBC(max)}$	Cable compensation maximum voltage	Voltage at CBC at full load	2.9	3.1	3.5	V
$V_{CVS(min)}$	Minimum compensation at VS	V_{CBC} = open, change in VS regulating level at full load	–55	–15	25	mV
$V_{CVS(max)}$	Maximum compensation at VS	V_{CBC} = 0 V, change in VS regulating level at full load	270	320	385	mV

(1) The regulating level and over voltage at VS decreases with temperature by 0.8 mV/°C. This compensation is included to reduce the power supply output voltage variance over temperature.

6.6 Typical Characteristics

VDD = 25 V, unless otherwise noted.

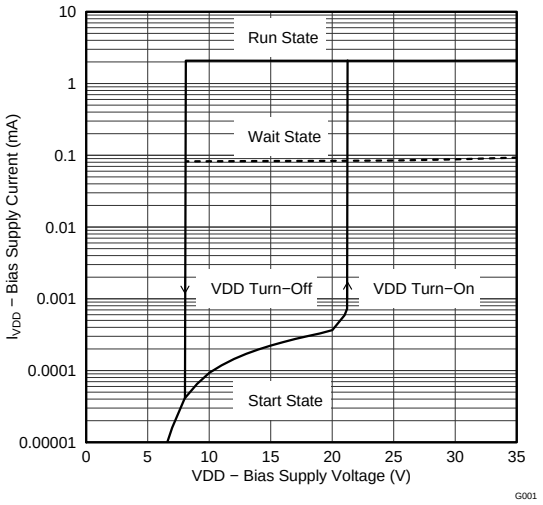


Figure 1. Bias Supply Current vs VDD Voltage

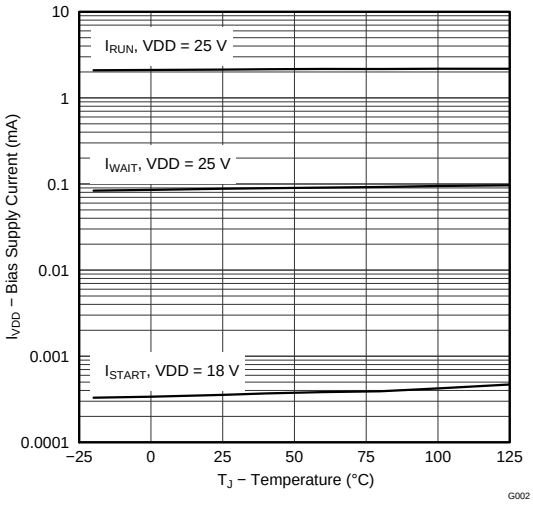


Figure 2. Operating Current vs Junction Temperature

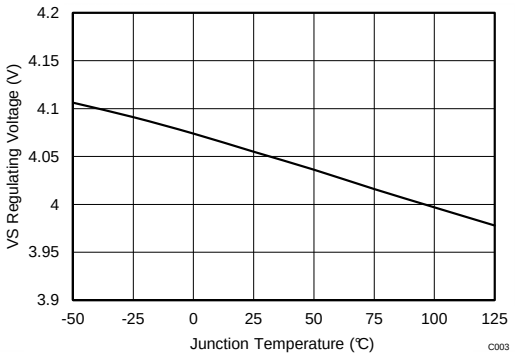


Figure 3. VS Pin Regulation Voltage vs Junction Temperature

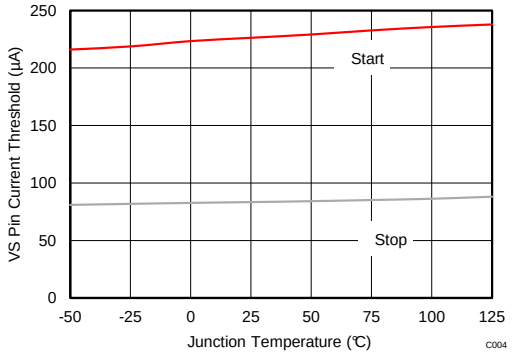


Figure 4. VS Pin Start and Stop Thresholds vs Junction Temperature

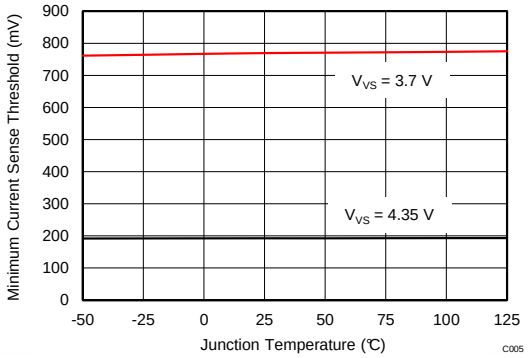


Figure 5. Current Sense Threshold vs Temperature

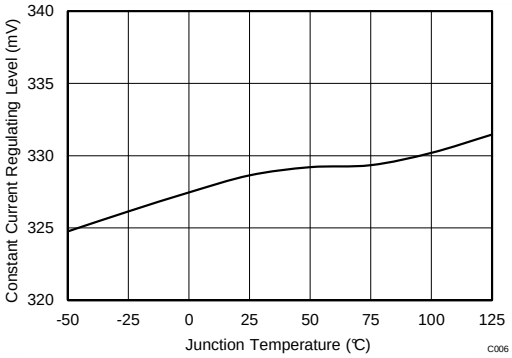


Figure 6. Constant Current Regulation Level vs Junction Temperature

Typical Characteristics (continued)

VDD = 25 V, unless otherwise noted.

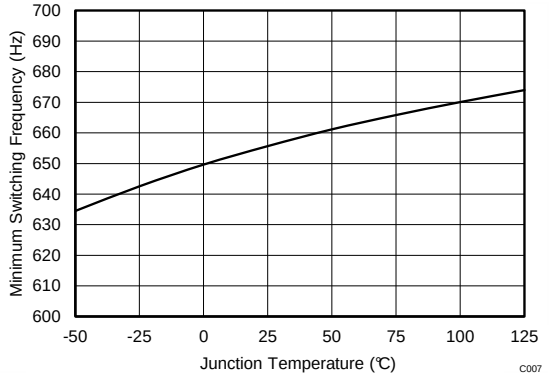


Figure 7. Minimum Switching Frequency vs Junction Temperature

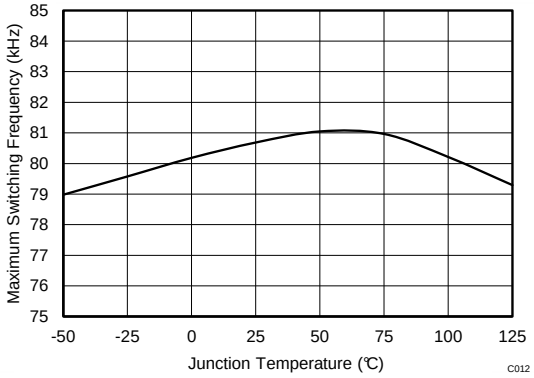


Figure 8. Maximum Switching Frequency vs Junction Temperature

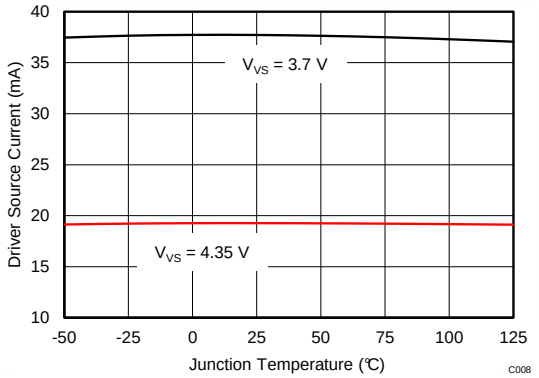


Figure 9. Driver Output Source Current vs Junction Temperature

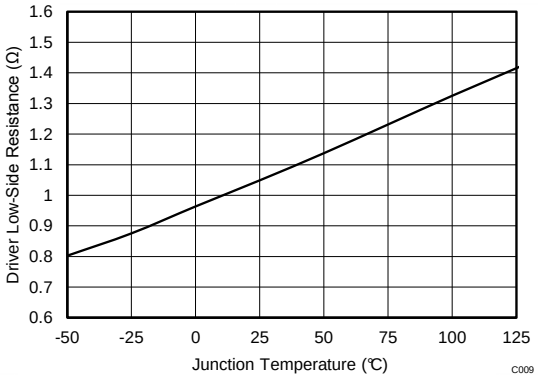


Figure 10. Driver Pull Down Resistance vs Junction Temperature

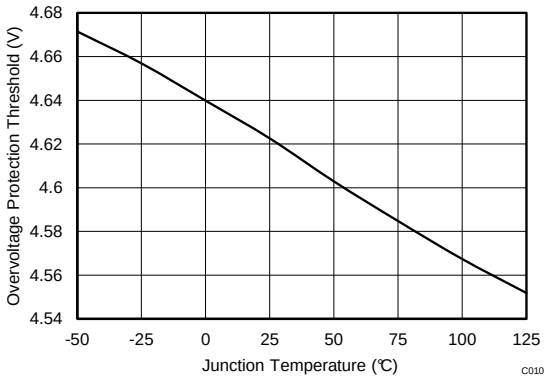


Figure 11. Over Voltage Protection Threshold vs Junction Temperature

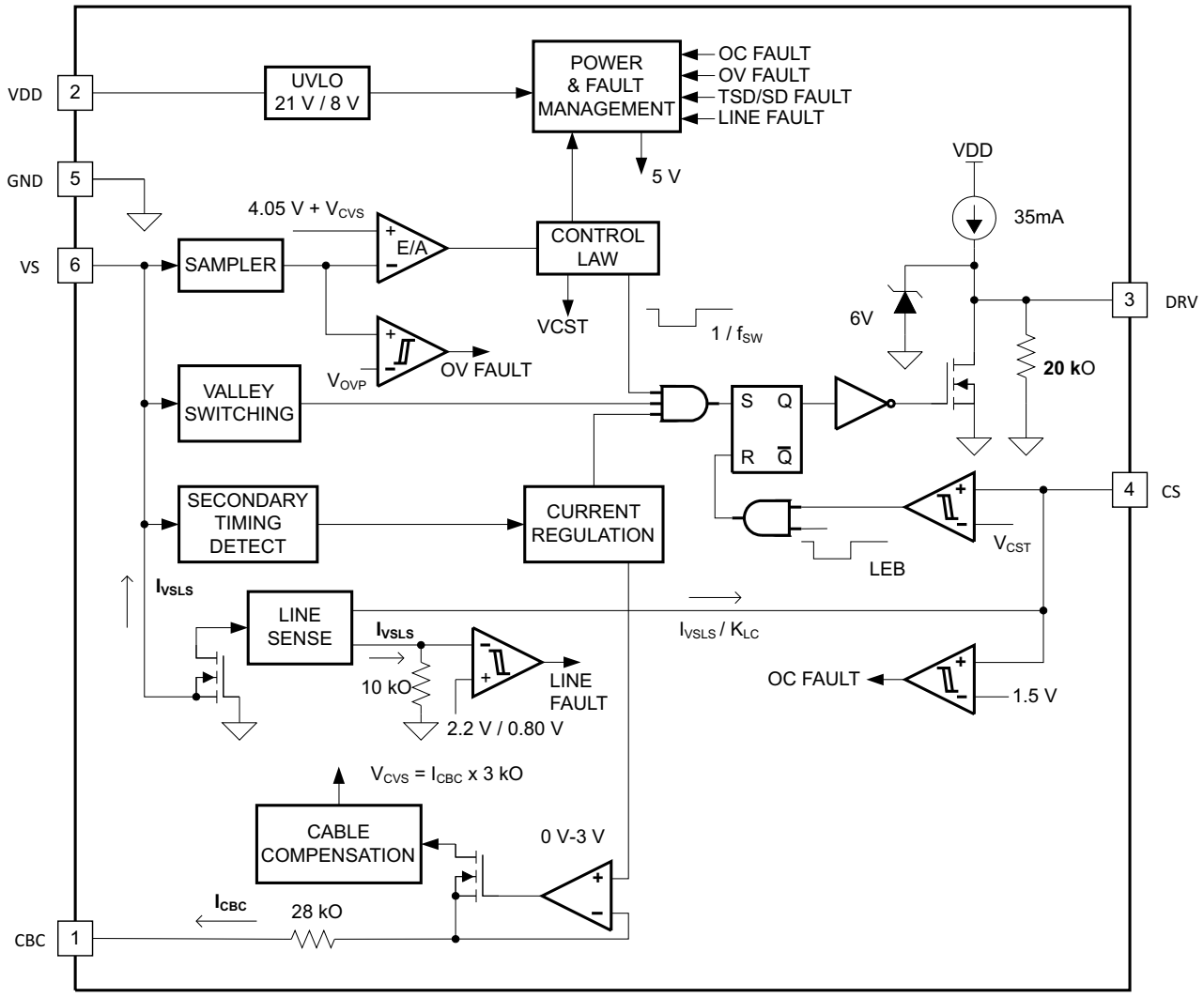
7 Detailed Description

7.1 Overview

The UCC28722 is a flyback power supply controller that provides accurate voltage and constant current regulation with primary-side feedback, eliminating the need for opto-coupler feedback circuits. The controller operates in discontinuous conduction mode with valley-switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversion efficiency across the load range. The control law provides a wide-dynamic operating range of output power, which allows the power designer to achieve less than 75-mW of stand-by power.

During low-power operating ranges, the device has power-management features to reduce the device operating current at operating frequencies below 28 kHz. Accurate voltage and constant current regulation, fast dynamic response, and fault protection are achieved with primary-side control. A complete charger solution can be realized with a straightforward design process, low cost and low component count.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Bias Voltage Supply (VDD)

The VDD pin is connected to a bypass capacitor to ground. The VDD turnon UVLO threshold is 21 V and turnoff UVLO threshold is 7.7 V, with an available operating range up to 35 V on VDD. The USB charging specification requires the output current to operate in constant-current mode from 5 V to a minimum of 2 V, which is easily achieved with a nominal VDD of approximately 22 V. The additional VDD headroom (up to 35 V) allows for VDD to rise due to the leakage energy delivered to the VDD capacitor in high-load conditions.

NOTE

It is possible for the start-up resistor to supply more current to the VDD node than the IC will consume at higher bulk input voltages. A Zener diode clamp is required on the VDD pin to keep the VDD pin voltage within limits if this is the case.

7.3.2 Ground (GND)

There is one ground reference external to the device for the base drive current and analog signal reference. TI recommends placing the VDD bypass capacitor close to GND and VDD with short traces to minimize noise on the VS and CS signal pins.

7.3.3 Voltage-Sense (VS)

The VS pin is connected to a resistor divider from the auxiliary winding to ground. The output-voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. Timing information for achieving valley-switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VS pin. Avoid placing a filter capacitor on this input because it would interfere with accurate sensing of this waveform.

The VS pin also senses the bulk capacitor voltage to provide for AC-input run and stop thresholds, and to compensate the current-sense threshold across the AC-input range. During the transistor on-time, the VS pin is clamped to approximately 250 mV below GND and the current out of the VS pin is sensed. For the AC-input run and stop function, the run threshold on VS is 225 µA and the stop threshold is 80 µA. The values for the auxiliary voltage divider upper-resistor (R_{S1}) and lower-resistor (R_{S2}) can be determined by Equation 1 and Equation 2.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (1)$$

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio.
- $V_{IN(run)}$ is the AC RMS voltage to enable turnon of the controller (run).
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the switch on-time (see *Electrical Characteristics*).

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \quad (2)$$

where

- V_{OCV} is the converter regulated output voltage.
- V_F is the output rectifier forward drop at near-zero current.
- N_{AS} is the transformer auxiliary to secondary turns ratio.
- R_{S1} is the VS divider high-side resistance.
- V_{VSR} is the CV regulating level at the VS input (see *Electrical Characteristics*).

Feature Description (continued)

7.3.4 Base Drive (DRV)

The DRV pin is connected to the NPN transistor base pin. The driver provides a base drive signal limited to 7 V. The turn-on characteristic of the driver is a 19-mA to 37-mA current source that is scaled with the current sense threshold dictated by the operating point in the control scheme. When the minimum current sense threshold is being used, the base drive current is also at its minimum value. As the current sense threshold is increased to the maximum, the base drive current scales linearly to its maximum of 35-mA typical. The turn-off current is determined by the low-side driver $R_{DS(on)}$.

7.3.5 Current Sense (CS)

The current-sense pin is connected through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The current-sense threshold is 0.78 V for $I_{PP(max)}$ and 0.19 V for $I_{PP(min)}$. The series resistor R_{LC} provides the function of feedforward line compensation to eliminate change in I_{PP} due to change in di/dt and the propagation delay of the internal comparator and NPN transistor turn-off time. There is an internal leading-edge blanking time of approximately 300 ns to eliminate sensitivity to the turnon current spike. It should not be necessary to place a bypass capacitor on the CS pin. The value of R_{CS} is determined by the target output current in constant current (CC) regulation. The values of R_{CS} and R_{LC} can be determined by Equation 3 and Equation 4. The term η_{XFMR} is intended to account for the energy stored in the transformer but not delivered to the secondary, which includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

7.3.5.1 Example

With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias power-to-output power ratio of 1.5%, the η_{XFMR} value is approximately: 1 – 0.05 – 0.035 – 0.015 = 0.9.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (3)$$

where

- V_{CCR} is a current regulation constant (see *Electrical Characteristics*).
- N_{PS} is the transformer primary-to-secondary turns ratio (a ratio of 13 to 15 is recommended for 5-V output).
- I_{OCC} is the target output current in constant-current regulation.
- η_{XFMR} is the transformer efficiency.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (4)$$

where

- R_{S1} is the VS pin high-side resistor value.
- R_{CS} is the current-sense resistor value.
- t_D is the current-sense delay including NPN transistor turn-off delay, add approximately 50 ns to transistor delay.
- N_{PA} is the transformer primary-to-auxiliary turns ratio.
- L_P is the transformer primary inductance.
- K_{LC} is a current-scaling constant (see *Electrical Characteristics*).

Feature Description (continued)

7.3.6 Cable Compensation (CBC)

The cable compensation pin is connected to a resistor to ground to program the amount of output voltage compensation to offset cable resistance. The cable compensation block provides a 0-V to 3-V voltage level on the CBC pin corresponding to $I_{OCC(max)}$ output current. Connecting a resistance from CBC to GND programs a current that is summed into the VS feedback divider, increasing the regulation voltage as I_{OUT} increases. There is an internal series resistance of 28 kΩ to the CBC pin that sets a maximum cable compensation of a 5-V output to 400 mV when CBC is shorted to ground. The CBC resistance value can be determined by Equation 5.

$$R_{CBC} = \frac{V_{CBC(max)} \times 3\ k\Omega \times (V_{OCV} + V_F)}{V_{VSR} \times V_{OCBC}} - 28\ k\Omega \quad (5)$$

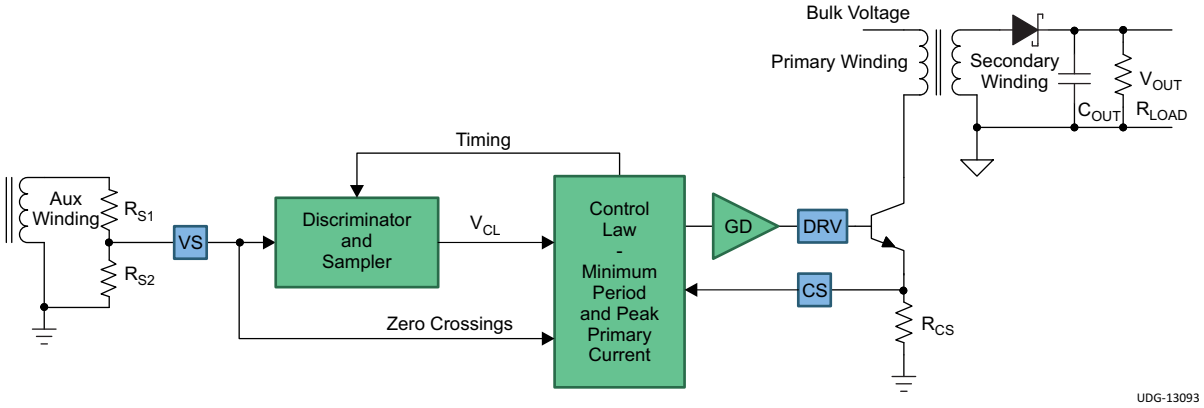
where

- V_{OCV} is the regulated output voltage.
- V_F is the diode forward voltage in V.
- V_{OCBC} is the target cable compensation voltage at the output terminals.
- $V_{CBC(max)}$ is the maximum voltage at the cable compensation pin at the maximum converter output current (see *Electrical Characteristics*).
- V_{VSR} is the CV regulating level at the VS input (see *Electrical Characteristics*).

7.4 Device Functional Modes

7.4.1 Primary-Side Voltage Regulation

Figure 12 illustrates a simplified flyback convertor with the main voltage regulation blocks of the device shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary-side control.



The main voltage regulation blocks are shown.

Figure 12. Simplified Flyback Convertor

In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. As shown in Figure 13, it is clear there is a down slope representing a decreasing total rectifier (V_F) and resistance voltage drop ($I_S R_S$) as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, ensure that the discrimantor:

- Reliably recognizes the leakage inductance reset, ringing, and ingores
- Continuously samples the auxiliary voltage during the down slope after the ringing is diminished
- Captures the error signal at the time the secondary winding reaches zero current

The internal reference on VS is 4.05 V. Temperature compensation on the VS reference voltage of –0.8-mV/°C offsets the change in the output rectifier forward voltage with temperature. The resistor divider is selected as outlined in the VS pin description.

Device Functional Modes (continued)

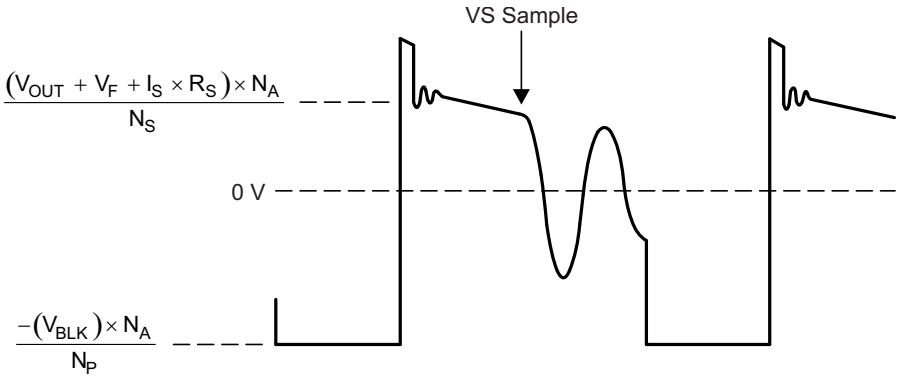


Figure 13. Auxiliary Winding Voltage

The UCC28722 includes a VS signal sampler that uses discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are some conditions that must be met on the auxiliary winding signal to ensure reliable operation. These conditions are the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to Figure 14 for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin. The first detail to examine is the duration of the leakage inductance reset pedestal, t_{LK_RESET} in Figure 14. Because this can mimic the waveform of the secondary current decay followed by a sharp downslope, it is important to keep the leakage reset time less than 600 ns for I_{PRI} minimum, and less than 2.2 µs for I_{PRI} maximum. The second detail is the amplitude of ringing on the V_{AUX} waveform following t_{LK_RESET}. The peak-to-peak voltage at the VS pin should be less than approximately 100 mV_{p-p} at least 200 ns before the end of the demagnetization time, t_{DM}. If there is a concern with excessive ringing, it usually occurs during light or no-load conditions, when t_{DM} is at the minimum. The tolerable ripple on VS scales up when measured at the auxiliary winding by R_{S1} and R_{S2}, and is equal to 100 mV × (R_{S1} + R_{S2}) / R_{S2} when measured directly at the auxiliary winding.

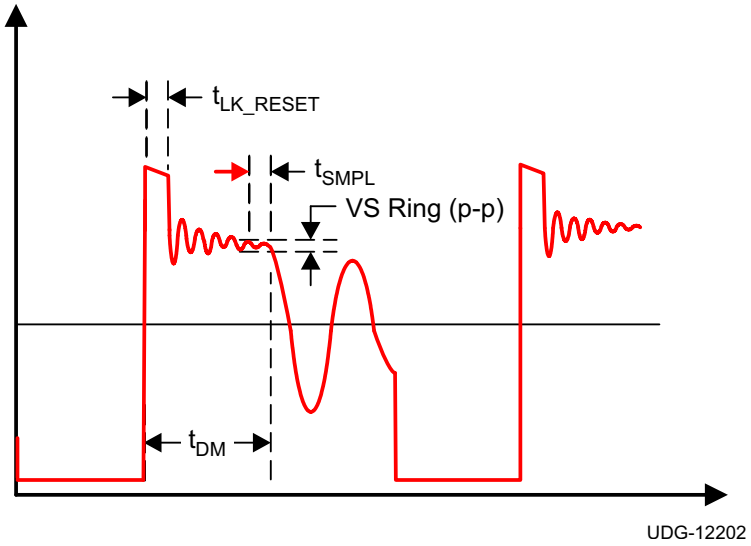


Figure 14. Auxiliary Waveform Details

During voltage regulation, the controller operates in frequency modulation mode and amplitude modulation mode as illustrated in Figure 15. The internal operating frequency limits of the device are 80 kHz, $f_{SW(max)}$ and 650 Hz, $f_{SW(min)}$. The transformer primary inductance and primary peak current chosen sets the maximum operating frequency of the converter. The output preload resistor and efficiency at low power determines the converter minimum operating frequency. There is no stability compensation required for the UCC28722.

Device Functional Modes (continued)

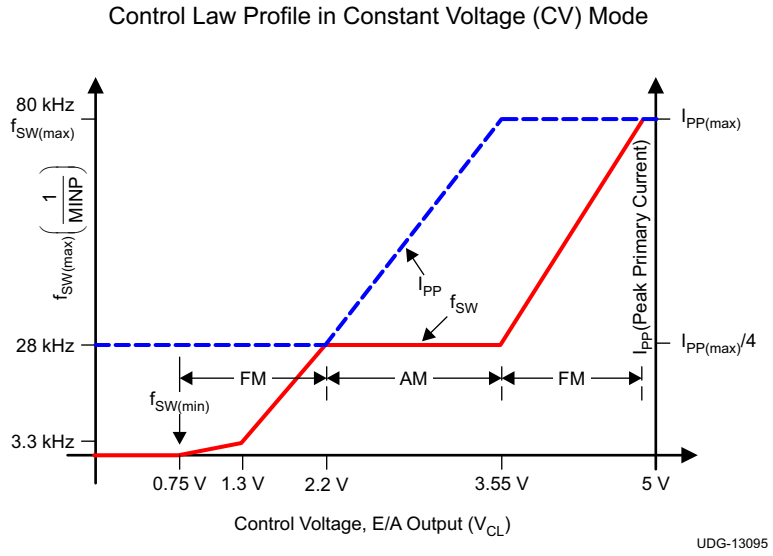


Figure 15. Frequency and Amplitude Modulation Modes During Voltage Regulation

7.4.2 Primary-Side Current Regulation

Timing information at the VS pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary-peak current is at $I_{PP(max)}$. Referring to Figure 16, the primary-peak current, turns ratio, secondary demagnetization time (t_{DM}), and switching period (t_{SW}) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by Equation 6. When the average output current reaches the regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turnoff threshold.

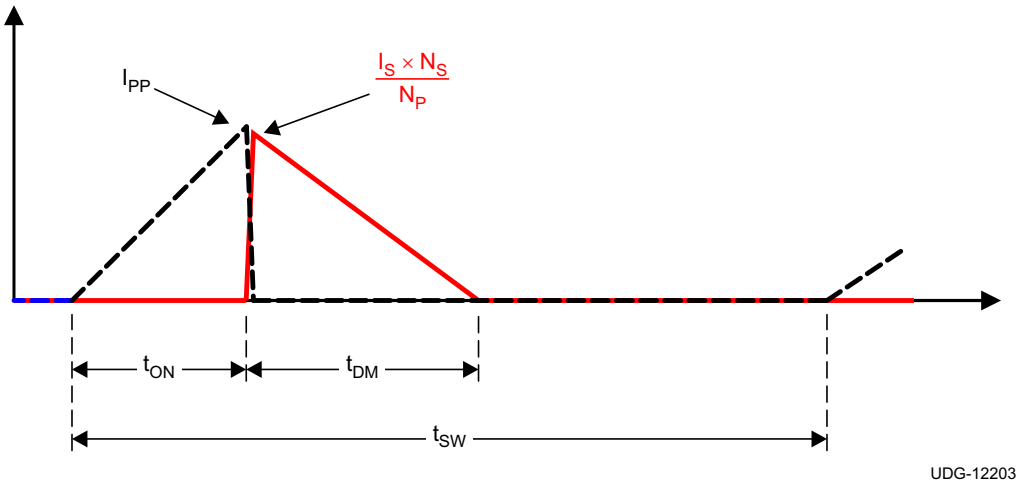


Figure 16. Transformer Currents

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{t_{SW}} \quad (6)$$

Device Functional Modes (continued)

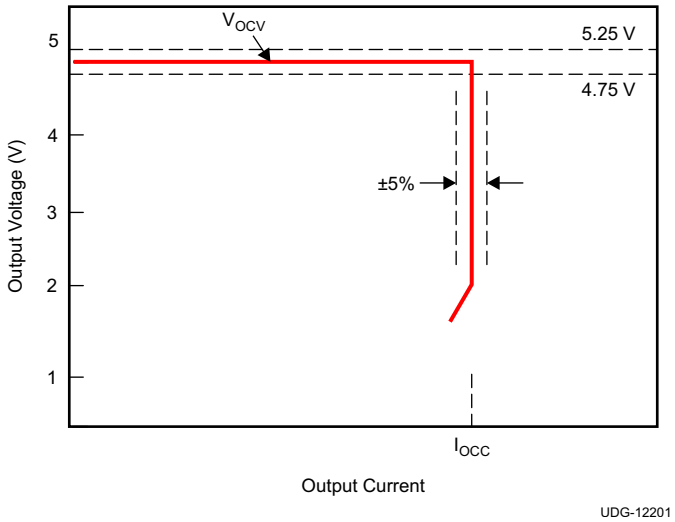


Figure 17. Typical Target Output V-I Characteristic

7.4.3 Valley Switching

The UCC28722 utilizes valley switching to reduce switching losses in the transistor, to reduce induced-EMI, and to minimize the turnon current spike at the sense resistor. The controller operates in valley-switching in all load conditions unless the collector voltage (V_C) ringing has subsided.

Referring to Figure 18, the UCC28722 operates in a valley-skipping mode in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_C.

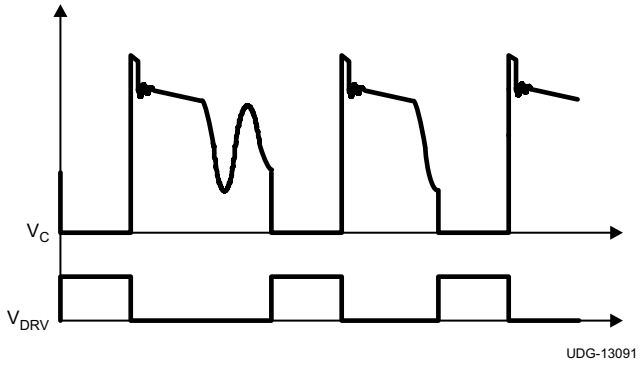


Figure 18. Valley-Skipping Mode

7.4.4 Start-Up Operation

An external resistor connected from the bulk capacitor voltage (V_{BLK}) to the VDD pin charges the VDD capacitor. The amount of startup current that is available to charge the VDD capacitor is dependent on the value of this external startup resistor. Larger values supply less current and increase startup time but at the expense of increasing standby power and decreasing efficiency at high input voltage and light loading. When VDD reaches the 21-V UVLO turnon threshold, the controller is enabled, the converter starts switching. The initial three cycles are limited to $I_{PP(min)}$. After the initial three cycles at minimum $I_{PP(min)}$, the controller responds to the condition dictated by the control law. The converter will remain in discontinuous mode during charging of the output capacitors, maintaining a constant output current until the output voltage is in regulation.

Device Functional Modes (continued)

NOTE

It is possible for the startup resistor to supply more current to the VDD node than the IC will consume at higher bulk input voltages. A Zener diode clamp will be required on the VDD pin to keep the VDD pin voltage within limits if this is the case.

7.4.5 Fault Protection

The UCC28722 provides comprehensive fault protection. Protection functions include the following:

- Output over-voltage fault
- Input under-voltage fault
- Internal over-temperature fault
- Primary over-current fault
- CS pin fault
- VS pin fault

A UVLO reset and restart sequence applies for all fault protection events.

The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 115% of the nominal V_{OUT}, the device stops switching and the internal current consumption is I_{FAULT} which discharges the VDD capacitor to the UVLO turnoff threshold. After that, the device returns to the start state and a start-up sequence ensues.

The UCC28722 always operates with cycle-by-cycle primary peak current control. The normal operating range of the CS pin is 0.78 V to 0.195 V. There is additional protection if the CS pin reaches 1.5 V. This results in a UVLO reset and restart sequence.

The line input run and stop thresholds are determined by current information at the VS pin during the transistor on-time. While the VS pin is clamped close to GND during the transistor on-time, the current through R_{S1} is monitored to determine a sample of the bulk capacitor voltage. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage. The run current threshold is 225 µA and the stop current threshold is 80 µA.

The internal over-temperature protection threshold is 165°C. If the junction temperature reaches this threshold the device initiates a UVLO reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC28722 flyback power supply controller provides constant voltage (CV) and constant current (CC) output regulation to help meet USB-compliant adaptors and charger requirements. This device uses the information obtained from auxiliary winding sensing (VS) to control the output voltage and does not require optocoupler or TL431 feedback circuitry. Not requiring optocoupler feedback reduces the component count and makes the design more cost effective and efficient.

8.2 Typical Application

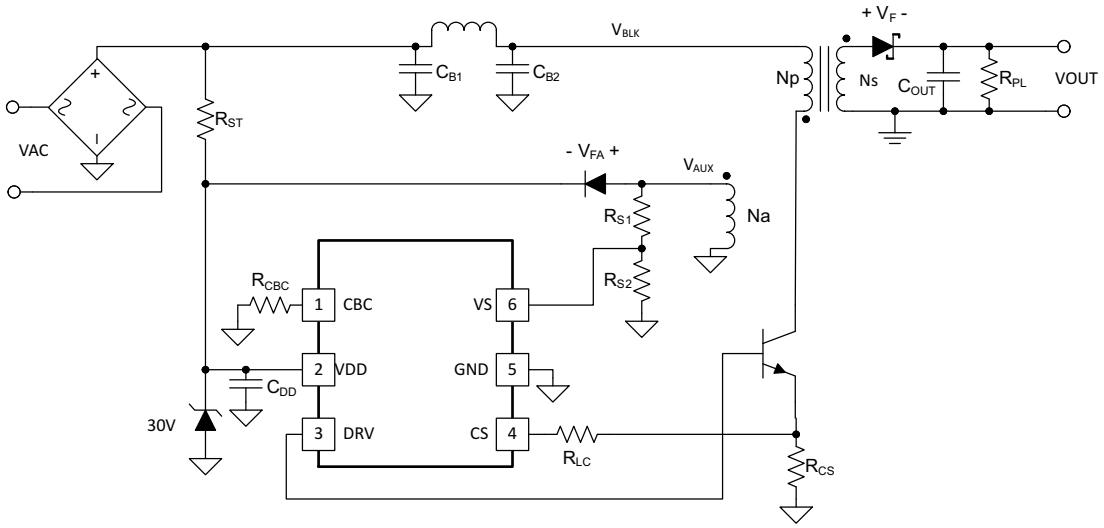


Figure 19. Design Procedure Application Example

Typical Application (continued)

8.2.1 Design Requirements

The design parameters are listed in Table 1.

Table 1. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	RMS Input Voltage		100 ($V_{IN(MIN)}$)	115/230	240	V
f_{LINE}	Line Frequency		47	50/60	64	Hz
$V_{IN(RUN)}$	Brownout Voltage	I_{OUT} = Nom		70		V
OUTPUT CHARACTERISTICS						
V_{OCV}	Output Voltage	V_{IN} = Nom, I_{OUT} = NOM	4.75	5	5.25	V
V_{RIPPLE}	Output Voltage Ripple	V_{IN} = Nom, I_O = Max			0.15	V
I_{OUT}	Output Current	V_{IN} = Min to Max		1	1.05	A
	Output OVP	I_{OUT} = Min to Max		5.75		V
	Transient Response					
	Load Step (I_{TRAN} = 0.6 A)	(0.1 to 0.6 A) or (0.6 to 0.1 A) $V_{O\Delta}$= 0.9 V for Calculations	4.1	5	6	V
SYSTEMS CHARACTERISTICS						
f_{MAX}	Switching Frequency			70		kHz
η	Full Load Efficiency (115/230 V RMS input)	I_{OUT} = 1 A	75%			

8.2.2 Detailed Design Procedure

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC28722 controller. Refer to Figure 19 for component names and network locations. The design procedure equations use terms that are defined in *Stand-by Power Estimate* through *Startup Resistance and Startup Time*.

8.2.2.1 Stand-by Power Estimate

Assuming no-load stand-by power is a critical design parameter, determine estimated no-load power based on target converter maximum switching frequency and output power rating.

The followingEquation 7 estimates the stand-by power of the converter.

$$P_{SB\_CONV} = \frac{P_{OUT} \times f_{MIN}}{\eta_{SB} \times K_{AM}^2 \times f_{MAX}} \quad (7)$$

For a typical USB charger application, the bias power during no-load is approximately 2.5 mW. This is based on 25-V VDD and 100-µA bias current. The output preload resistor can be estimated by V_{OCV} and the difference in the converter stand-by power and the bias power. Equation 8 shows output preload resistance accounts for bias power estimated at 2.5 mW.

$$R_{PL} = \frac{V_{OCV}^2}{P_{SB\_CONV} - 2.5\,mW} \quad (8)$$

Typical startup resistance values for R_{STR} range from 1 MΩ to 5MΩ to achieve 2 s startup time. The capacitor bulk voltage for the loss estimation is the highest voltage for the stand-by power measurement, typically 325 V_{DC}, see Equation 9.

$$P_{RSTR} = \frac{V_{BLK}^2}{R_{STR}} \quad (9)$$

For the total stand-by power estimation add an estimated 2.5 mW for snubber loss to the converter stand-by power loss, see Equation 10 and Equation 11.

$$P_{SB} = P_{SB\_CONV} + 2.5\,mW \quad (10)$$

$$P_{SB} = P_{SB\_CONV} + P_{RSTR} + 2.5\,mW \quad (11)$$

8.2.2.2 Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input capacitance, C_{B1} and C_{B2} total, in order to determine the maximum Np to Ns turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency are used to determine the input capacitance requirement.

Maximum input power is determined based on V_{OCV}, I_{OCC}, and the full-load efficiency target, see Equation 12.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \quad (12)$$

Equation 13 provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{2P_{IN} \times \left(0.25 + \frac{1}{2\Pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right)}{\left(2V_{IN(min)}^{2} - V_{BULK(min)}^{2}\right) \times f_{LINE}} \quad (13)$$

8.2.2.3 Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM quasi-resonant time.

Initially determine the maximum available total duty cycle of the on time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{CE} voltage is 1/2 of the DCM resonant period, or 1 µs assuming 500-kHz resonant frequency. D_{MAX} can be determined using Equation 14.

$$D_{MAX} = 1 - \left(\frac{t_R}{2} \times f_{MAX}\right) - D_{MAGCC} \quad (14)$$

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined with the equation below. D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant-current, CC, operation. It is set internally by the UCC28722 at 0.425. The total voltage on the secondary winding needs to be determined; which is the sum of V_{OCV}, the secondary rectifier V_F, and the cable compensation voltage (V_{OCBC}). For the 5-V USB charger applications, a turns ratio range of 13 to 15 is typically used, see Equation 15.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times \left(V_{OCV} + V_F + V_{OCBC}\right)} \quad (15)$$

Once an optimum turns ratio is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28722 constant-current regulation is achieved by maintaining a maximum D_{MAG} duty cycle of 0.425 at the maximum primary current setting. The transformer turns ratio and constant-current regulating voltage determine the current sense resistor for a target constant current.

Since not all of the energy stored in the transformer is transferred to the secondary, a transformer efficiency term is included in Equation 16. This efficiency number includes the core and winding losses, leakage inductance ratio, and bias power ratio to rated output power. For a 5-V, 1-A charger example, bias power of 1.5% is a good estimate. An overall transformer efficiency of 0.9 is a good estimate to include 3.5% leakage inductance, 5% core and winding loss, and 1.5% bias power.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (16)$$

The primary transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency and output and transformer power losses are included in Equation 17 and Equation 18. Initially determine transformer primary current.

Primary current is simply the maximum current sense threshold divided by the current sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \tag{17}$$

$$L_P = \frac{2\left(V_{OCV} + V_F + V_{OCBC}\right) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^{\ 2} \times f_{MAX}} \tag{18}$$

The secondary winding to auxiliary winding transformer turns ratio (N_{AS}) is determined by the lowest target operating output voltage in constant-current regulation and the VDD UVLO of the UCC28722. There is additional energy supplied to VDD from the transformer leakage inductance energy which allows a lower turns ratio to be used in many designs Equation 19

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} \tag{19}$$

8.2.2.4 Transformer Parameter Verification

The transformer turns ratio selected affects the transistor V_C and secondary rectifier reverse voltage so these should be reviewed. The UCC28722 does require a minimum on time of the transistor (t_{ON}) and minimum D_{MAG} time (t_{DMAG}) of the secondary rectifier in the high line, minimum load condition. The selection of f_{MAX}, L_P and R_{CS} affects the minimum t_{ON} and t_{DMAG}.

The secondary rectifier and transistor voltage stress can be determined by Equation 20.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \tag{20}$$

For the transistor V_C voltage stress, Equation 21, an estimated leakage inductance voltage spike (V_{LK}) needs to be included.

$$V_{CPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F + V_{OCBC}\right) \times N_{PS} + V_{LK} \tag{21}$$

Equation 22 and Equation 23 are used to determine if the minimum t_{ON} target of 300 ns and minimum t_{DMAG} target of 1.2 µs is achieved.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)} \times V_{CST(min)}}{V_{CST(max)}} \tag{22}$$

$$t_{DMAG(min)} = \frac{t_{ON} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \tag{23}$$

8.2.2.5 Output Capacitance

The output capacitance value is typically determined by the transient response requirement from no-load. For example, in some USB charger applications there is a requirement to maintain a minimum V_O of 4.1 V with a load-step transient of 0 mA to 500 mA . Equation 24 assumes that the switching frequency can be at the UCC28722 minimum of $f_{SW(min)}$.

$$C_{OUT} = \frac{I_{TRAN}\left(\frac{1}{f_{SW(min)}} + 150\ \mu s\right)}{V_{O\Delta}} \tag{24}$$

Another consideration of the output capacitor is the ripple voltage requirement which is reviewed based on secondary peak current and ESR. A margin of 20% is added to the capacitor ESR requirement in Equation 25.

$$R_{ESR} = \frac{V_{RIPPLE} \times 0.8}{I_{PP(max)} \times N_{PS}} \quad (25)$$

8.2.2.6 VDD Capacitance, C_{DD}

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation. At this time, the auxiliary winding can sustain the voltage to the UCC28722. The total output current available to the load and to charge the output capacitors is the constant-current regulation target, I_{OCC}. Equation 26 assumes all the output current of the flyback is available to charge the output capacitance from 0 V to V_{OCC}. If the converter is going to be loaded during the time the output is ramping from 0 V to V_{OCC}, that load current must be subtracted for the available output current limit value, I_{OCC}. There is 1 V of margin added to VDD in the calculation.

$$C_{DD} = \frac{\left(I_{RUN} + I_{DRS(max)} \times \left(1 - D_{magcc}\right)\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{\left(V_{DD(on)} - V_{DD(off)}\right) - 1\ V} \quad (26)$$

NOTE

The typical ceramic capacitor of sufficient ratings for use here varies considerably in effective capacitance as the voltage across the capacitor changes. As the capacitor voltage increases beyond 25% of its rated voltage, the effective capacitance can become significantly less than the nominal capacitance at zero bias. This equation calculated the effective capacitance needed over the 8V to 21V range, not the nominal zero bias capacitance required. Evaluation of the particular capacitor chosen for this function is strongly recommended to ensure adequate capacitance over the 8V to 21V range.

8.2.2.7 VS Resistor Divider, Line Compensation, and Cable Compensation

The VS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on transformer auxiliary to primary turns ratio and desired input voltage operating threshold in Equation 27.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (27)$$

The low-side VS pin resistor is selected based on desired V_O regulation voltage in Equation 28.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times \left(V_{OCV} + V_F\right) - V_{VSR}} \quad (28)$$

The UCC28722 can maintain tight constant-current regulation over input line by utilizing the line compensation feature. The line compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and expected base drive and transistor turnoff delay in Equation 29. Assume a 50-ns internal delay in the UCC28722.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (29)$$

The UCC28722 has adjustable cable drop compensation. The resistance for the desired compensation level at the output terminals can be determined using Equation 30.

$$R_{CBC} = \frac{V_{CBC(max)} \times 3\ k\Omega \times \left(V_{OCV} + V_F\right)}{V_{VSR} \times V_{OCBC}} - 28\ k\Omega \quad (30)$$

8.2.2.8 Startup Resistance and Startup Time

When the VDD capacitor is known, there is a tradeoff to be made between startup time and overall standby input power to the converter. Faster startup time requires a smaller startup resistance, which results in higher standby input power in Equation 31.

$$R_{STR} = \frac{\sqrt{2} \times V_{IN(min)}}{I_{START} + \frac{V_{DD(on)} \times C_{DD}}{T_{STR}}} \quad (31)$$

8.2.3 Application Curves

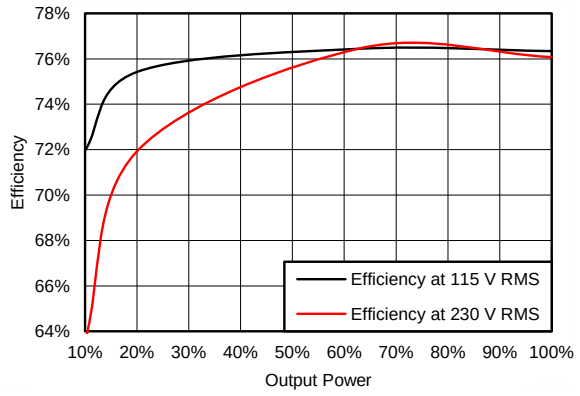


Figure 20. Efficiency

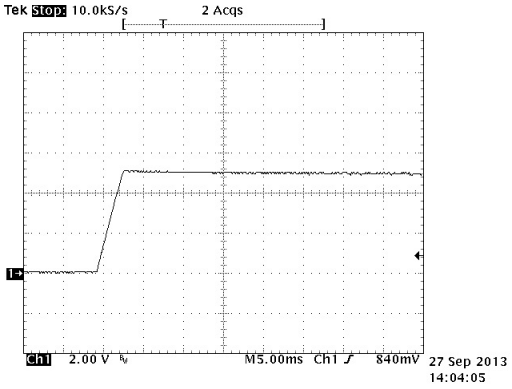


Figure 21. Output at Start-up 115-V RMS, No Load

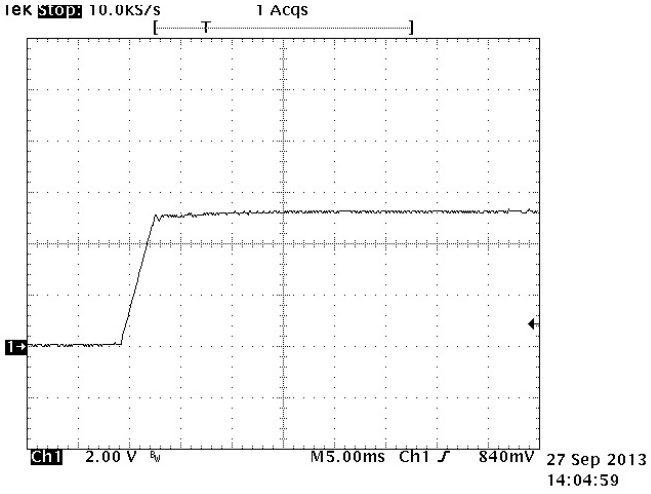


Figure 22. Output at Start-up 115-V RMS, 5-Ω Load

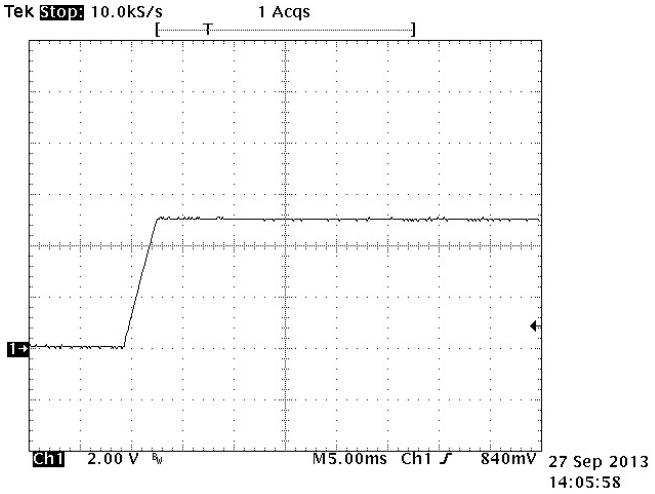


Figure 23. Output at Start-up 230-V RMS, No Load

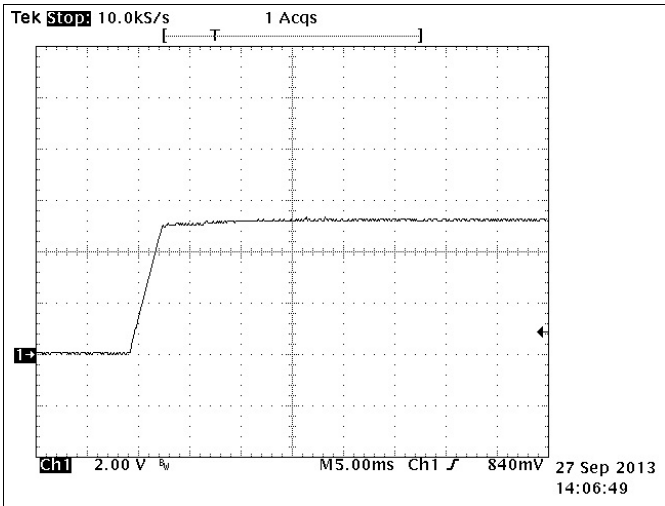
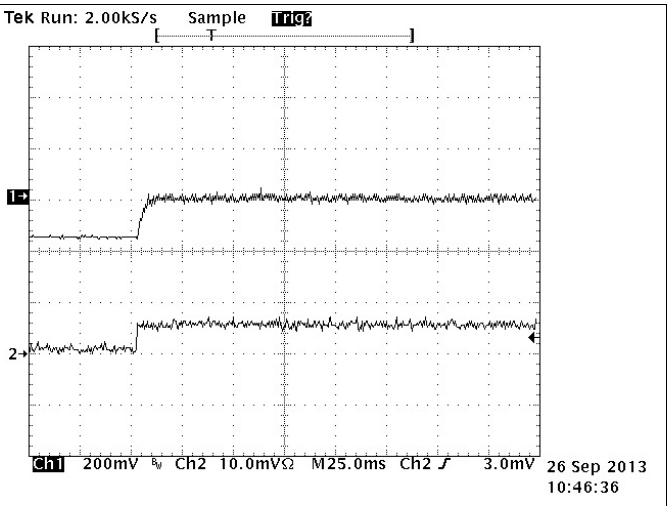
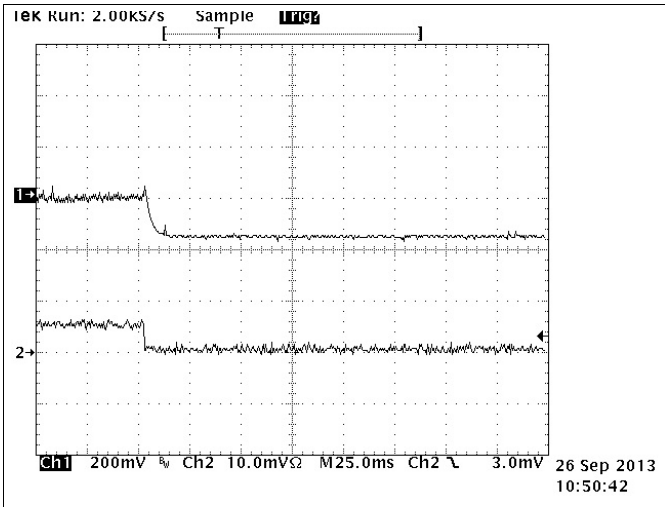


Figure 24. Output at Start-up 230-V RMS, 5-Ω Load



CH1 = V_{OCV} with 5-V offset, CH2 = I_{OUT}

Figure 25. Load Transients (0.1- to 0.6-A Load Step)



CH1 = V_{OCV} with 5-V offset, CH2 = I_{OUT}

Figure 26. Load Transient (0.6- to 0.1-A Load Step)

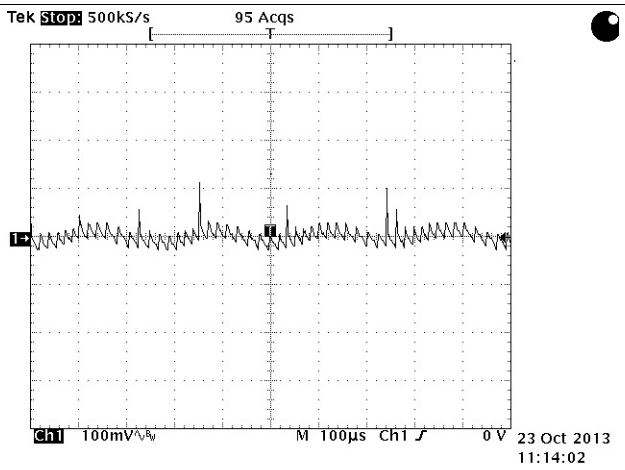


Figure 27. Output Ripple CH1 = V_{OCV} at Supply Output

9 Power Supply Recommendations

The UCC28722 is intended for AC/DC adapters and chargers with input voltage range of 85 $VAC_{(rms)}$ to 265 $VAC_{(rms)}$ using Flyback topology. This device can be used in other applications and converter topologies with different input voltages. Ensure that all voltages and currents are within the *Recommended Operating Conditions* and *Absolute Maximum Ratings* of the device. To maintain output current regulation over the entire input voltage range, design the converter to operate close to f_{MAX} when in full-load conditions. To improve thermal performance, increase the copper area connected to GND pins.

10 Layout

10.1 Layout Guidelines

- High frequency bypass Capacitor C7 should be placed arcoss Pin 2 and 5 as close as you can get it to the pins.
- Resistor R15 and C7 form a low pass filter and the connection of R15 and C7 should be as close to the VDD pin as possible.
- C9 should be put as close to CS pin and R10 as possible. This forms a low pass filter with R10.
- The connection for C9 and R10 should be as close to the CS pin as possible.
- C9 may not be required in all designs. However, it is wise to put a place holder for it in your design.
- The VS pin controls the output voltage through the transformer turns ratio and the voltage divider of R7 and R9. The trace with between the R7, R9 and VS pin should be as short as possible to reduce and eliminate possible EMI coupling.
- The IC ground and power ground should meet at the return of the bulk capacitors (C4 and C5). Ensure that high frequency and high current from the power stage does not go through the signal ground
  - The high frequency and high current path that you need to be cautious of on the primary is C4, C5 +, T1(P1,P2), Q1e, Q1c, R13 to the return of C4 and C5.
- Keep all high current loops as short as possible.
- Keep all high current and high frequency traces away from or perpendicular to other traces in the design.
- Traces on the voltage clamp formed by D1, R1, D4 and C4 as short as possible.
- C4 return needs to be as close to the bulk capacitor supply as possible. This reduces the magnitude of dv/dt caused by large di/dt.
- Avoid mounting semiconductors under magnetics.

10.2 Layout Example

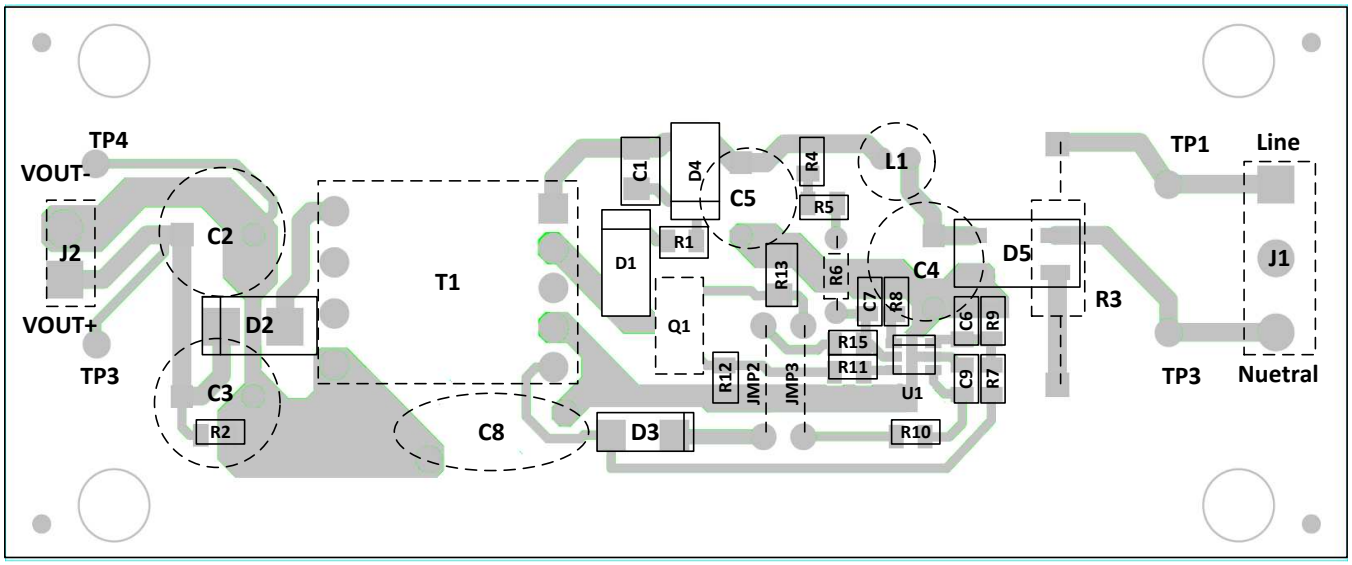


Figure 28. PCB Layout Example

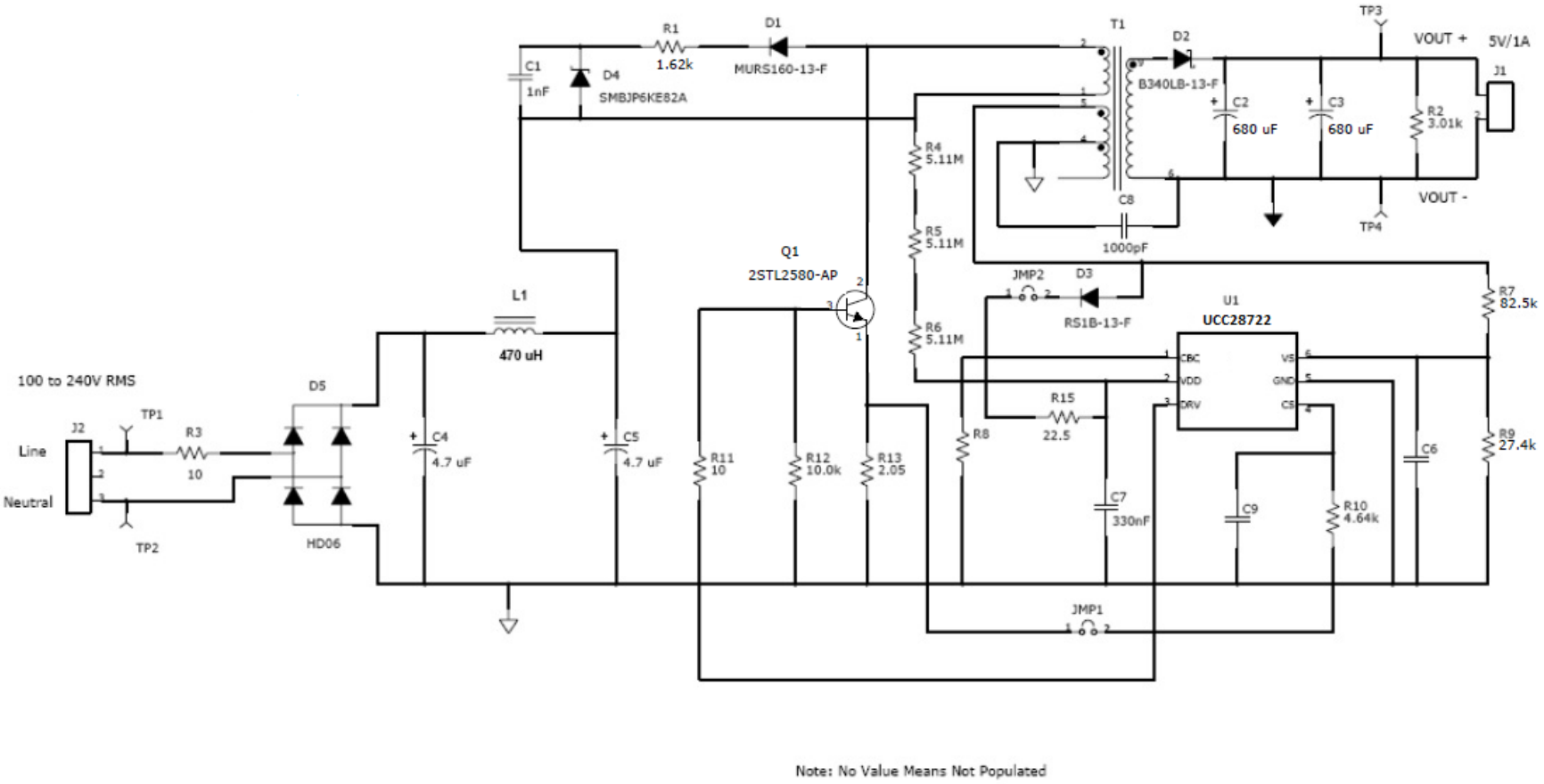


Figure 29. 5-W USB Adapter Schematic

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

11.1.1.1 术语定义

11.1.1.1.1 法拉电容术语

- **C_{BULK}**：CB1 和 CB2 的总输入电容。
- **C_{DD}**：VDD 引脚上所需的最小电容。
- **C_{OUT}**：所需的最小输出电容。

11.1.1.1.2 占空比术语

- **D_{MAGCC}**：CC 中的二次侧二极管导通占空比，0.425。
- **D_{MAX}**：晶体管导通时间占空比。

11.1.1.1.3 频率术语（以赫兹为单位）

- **f_{LINE}**：最小线路频率。
- **f_{MAX}**：转换器的目标满载最大开关频率。
- **f_{MIN}**：转换器的最小开关频率，为器件的 $f_{SW(min)}$ 限值增加 15% 裕度。
- **$f_{SW(min)}$**：最小开关频率（请参见*电气特性*）。

11.1.1.1.4 电流术语（以安培为单位）

- **I_{OCC}**：转换器目标恒流输出。
- **$I_{PP(max)}$**：变压器一次侧最大电流。
- **I_{START}**：启动偏置电源电流（请参见*电气特性*）。
- **I_{TRAN}**：所需的正负载阶跃电流。
- **$I_{VSL(run)}$**：VS 引脚运行电流（请参见*电气特性*）。
- **I_{DRS}**：驱动器拉电流（请参见电气特性）。

11.1.1.1.5 电流和电压调节术语

- **K_{AM}**：一次侧峰峰值电流比（请参见*电气特性*）。
- **K_{LC}**：电流调节常量（请参见*电气特性*）。

11.1.1.1.6 变压器术语

- **L_P**：变压器一次侧电感。
- **N_{AS}**：变压器辅助侧与二次侧的匝数比。
- **N_{PA}**：变压器一次侧与辅助侧的匝数比。
- **N_{PS}**：变压器一次侧与二次侧的匝数比。

11.1.1.1.7 功率术语（以瓦特为单位）

- **P_{IN}**：转换器的最大输入功率。
- **P_{OUT}**：转换器的满载输出功率。
- **P_{RSTR}**：VDD 启动电阻的功耗。
- **P_{SB}**：总待机功耗。
- **P_{SB_CONV}**：P_{SB}与启动电阻和缓冲器损耗的差值。

11.1.1.1.8 电阻术语（以 Ω 为单位）

- **R_{CS}**：一次侧电流编程电阻。
- **R_{ESR}**：输出电容器的总 ESR。
- **R_{PL}**：转换器输出端的预载电阻。
- **R_{S1}**：高侧 VS 引脚电阻。

器件支持 (接下页)

- R_{S2}：低侧 VS 引脚电阻。
- R_{STR}：启动电阻。

11.1.1.1.9 时序术语（以秒为单位）

- T_D：包括晶体管关断延迟在内的电流感测延迟；添加 50ns 至晶体管延迟。
- $T_{DMAG(min)}$：二次侧整流器的最短导通时间。
- $T_{N(min)}$：晶体管的最短导通时间。
- t_R：断续导通模式 (DCM) 期间的谐振频率。
- t_{ST}：启动时间

11.1.1.1.10 电压术语（以伏特为单位）

- V_{BLK}：用于待机功耗测量的大容量电容最高电压。
- $V_{BULK（最小值）}$：满功率条件下 C_{B1} 和 C_{B2} 的最低电压。
- V_{OCBC}：输出引脚的目标电缆补偿电压。
- $V_{CBC(max)}$：最大转换器输出电流条件下 CBC 引脚的最大电压（请参见*电气特性*）。
- V_{CCR}：恒流调节电压（请参见*电气特性*）。
- $V_{CST(max)}$：CS 引脚的最大电流感测阈值（请参见*电气特性*）。
- $V_{CST(min)}$：CS 引脚的最小电流感测阈值（请参见*电气特性*）。
- $V_{DD(off)}$：UVLO 关断电压（请参见*电气特性*）。
- $V_{DD(on)}$：UVLO 导通电压（请参见*电气特性*）。
- $V_{O\Delta}$：负载阶跃瞬态期间允许的输出压降。
- V_{CPK}：高压线条件下的晶体管集电极到发射极电压峰值
- V_F：电流接近零时的二次侧整流器正向压降。
- V_{FA}：辅助整流器正向压降。
- V_{LK}：估计的漏感能量复位电压。
- V_{OCV}：经稳压的转换器输出电压。
- V_{OCC}：恒流稳压条件下的最低目标转换器输出电压。
- V_{REV}：二次侧整流器的峰值反向电压。
- V_{RIPPLE}：满载条件下的输出峰峰值纹波电压。
- V_{VSR}：VS 输入端的 CV 调节电平（请参见*电气特性*）。

11.1.1.1.11 交流电压术语（以 V_{RMS} 为单位）

- $V_{IN(max)}$：转换器的最大输入电压。
- $V_{IN(min)}$：转换器的最小输入电压。
- $V_{IN(min)}$：转换器的输入启动（运行）电压。

11.1.1.1.12 效率术语

- η_{SB}：无载条件下估算的转换器效率，其中不包括启动电阻或偏置损耗。对于一个 5V USB 充电器应用，60% 到 65% 是一个很好的初步估算值。
- η：转换器总体效率。
- η_{XFMR}：变压器一次侧与二次侧之间的功率传输效率。

11.2 文档支持

11.2.1 相关文档

请参见如下文档：*《UCC28722/UCC28720 5W USB BJT 反激设计示例》*，SLUA700

11.3 社区资源

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11.4 商标

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11.5 静电放电警告

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28722DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U722
UCC28722DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U722
UCC28722DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U722
UCC28722DBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U722

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

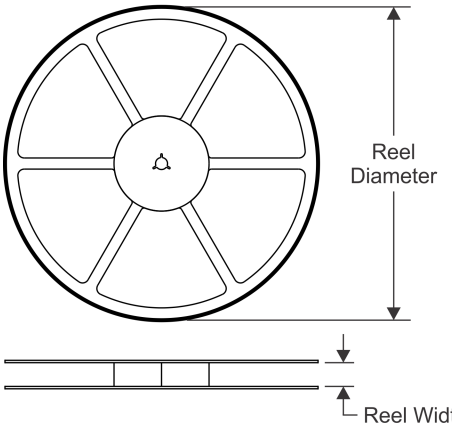
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

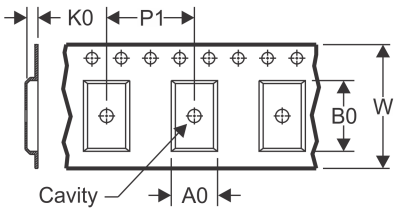
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

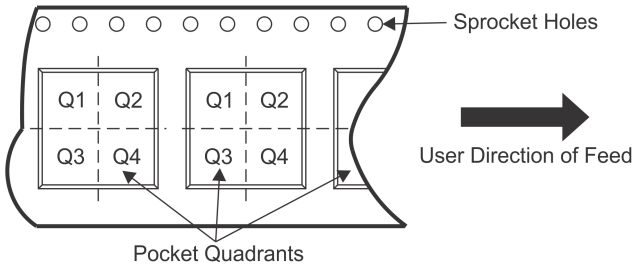


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

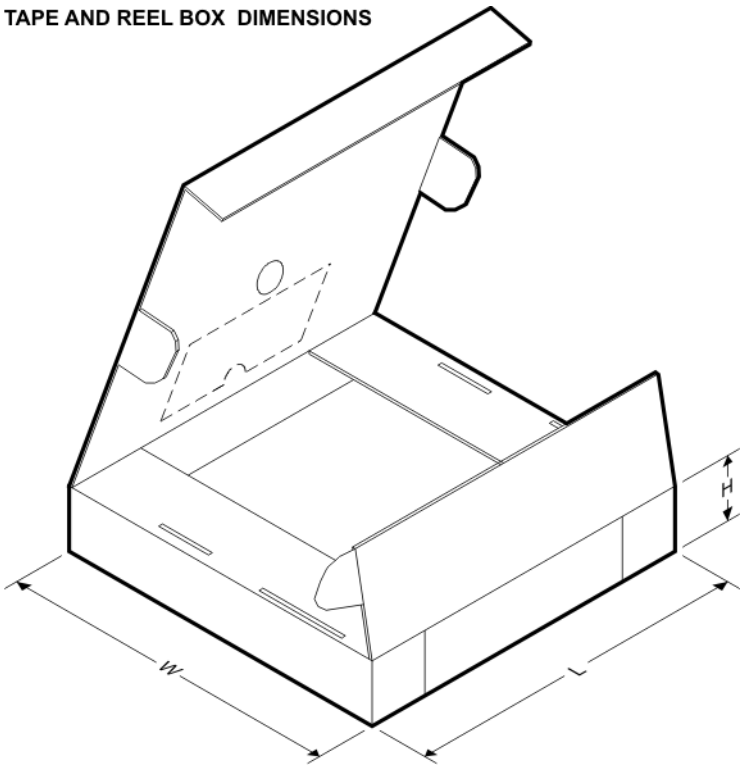
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28722DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28722DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

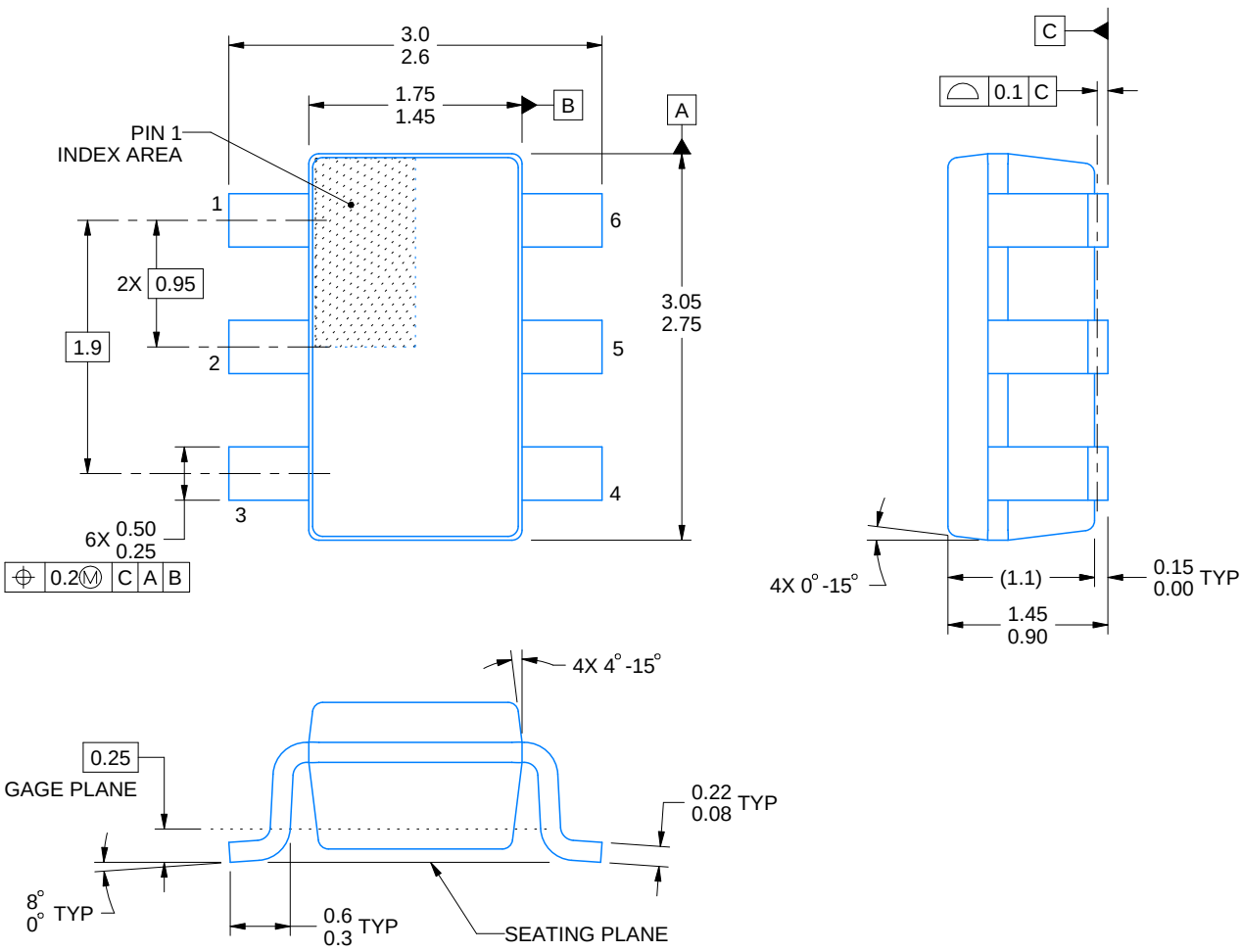
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28722DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC28722DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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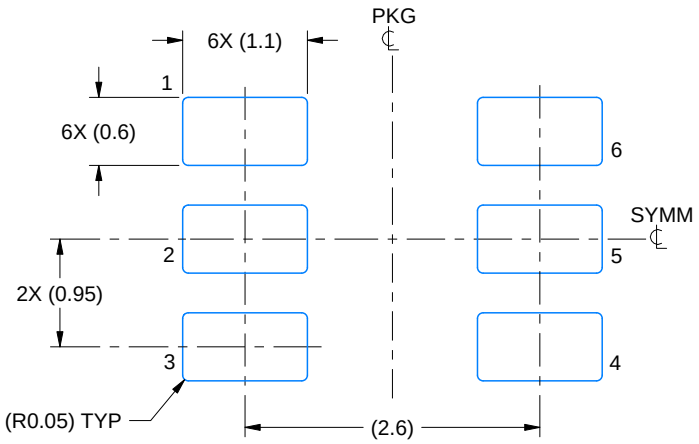
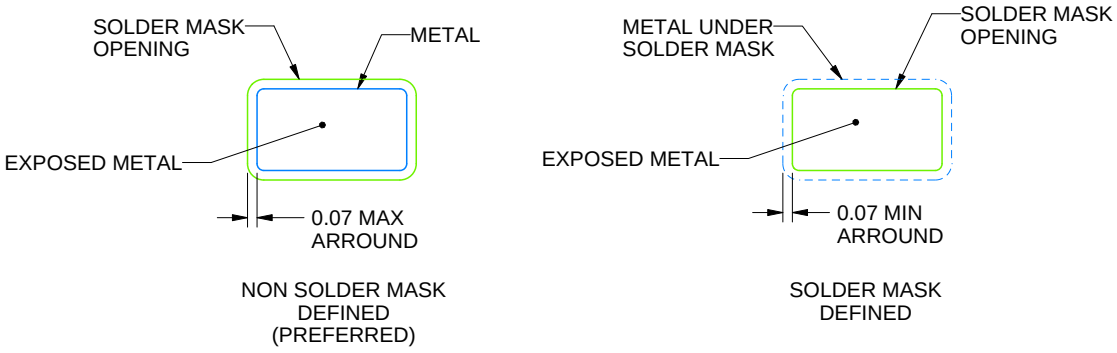
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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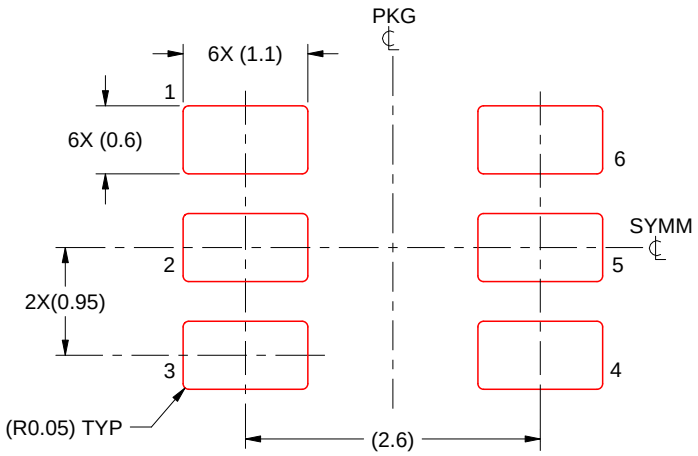
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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