

UCC27201A-Q1 具有 8V UVLO 功能的汽车级 120V、3A/3A 半桥驱动器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：器件温度等级 1
- 40°C 至 +150°C 的结温范围
- HS 引脚上的负电压处理能力：-18V
- 可驱动两个采用高侧/低侧配置的 N 沟道 MOSFET
- 最大引导电压：120V
- 最大 VDD 电压：20V
- 片上 0.65V V_F 、0.65 Ω R_D 自举二极管
- 22ns 传播延迟时间
- 3A 灌电流，3A 拉电流输出
- 1000pF 负载时上升时间为 8ns，下降时间为 7ns
- 1ns 延迟匹配
- 用于高侧和低侧驱动器的欠压锁定功能
- 采用 8 引脚 PowerPAD™ SOIC-8 (DDA) 封装

2 应用

- 汽车直流/直流转换器和 OBC
- 两轮车/三轮车牵引驱动器和电池包
- 电动助力转向 (EPS)
- 无线充电
- 智能玻璃模块

3 说明

UCC27201A-Q1 高频 N 沟道 MOSFET 驱动器由 120V 自举二极管和高侧/低侧驱动器组成，其中高侧/低侧驱动器配有独立输入，可更大限度提高控制灵活性。这可在半桥式、全桥式、两开关正激式和有源箝位正激式转换器中提供 N 沟道 MOSFET 控制。低侧和高侧栅极驱动器是独立控制的，并在彼此的接通和关断之间实现了 1ns 的延迟匹配。UCC27201A-Q1 的 HS 引脚最高能够承受 -18V 电压，这使得其在电源噪声环境下的性能得到了改善。

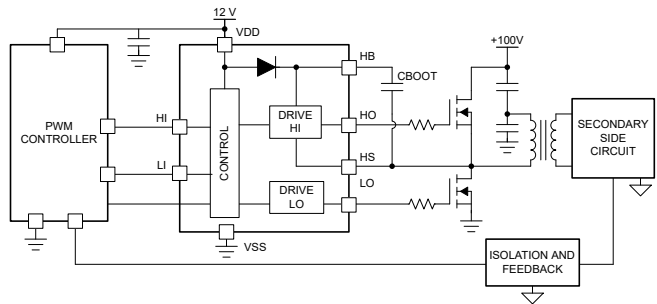
由于在芯片上集成了一个自举二极管，因此无需采用外部分立式二极管。高侧和低侧驱动器均配有欠压锁定功能，如果驱动电压低于规定的阈值，则强制将输出置为低电平。

UCC27201A-Q1 具有 TTL 兼容阈值，并且采用带有散热焊盘的 8 引脚 SOIC 封装。

器件信息

器件型号	封装 ⁽¹⁾	本体尺寸 (标称值)
UCC27201A-Q1	DDA (PowerPAD™ SOIC, 8)	4.9mm × 3.9mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用示意图



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4 Pin Configuration and Functions

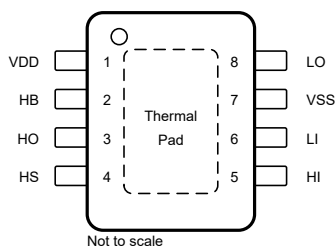


图 4-1. DDA PowerPAD™ 8-Pin SOIC-8 (Top View)

表 4-1. Pin Functions

PIN		I/O ⁽²⁾	DESCRIPTION
NO.	NAME		
1	VDD	P	Positive supply to the lower gate driver. De-couple this pin to VSS (GND). Typical decoupling capacitor range is 0.22 μ F to 1.0 μ F.
2	HB	P	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 μ F to 0.1 μ F, the value is dependant on the gate charge of the high-side MOSFET however.
3	HO	O	High-side output. Connect to the gate of the high-side power MOSFET.
4	HS	P	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
5	HI	I	High-side input.
6	LI	I	Low-side input.
7	VSS	G	Negative supply terminal for the device which is generally grounded.
8	LO	O	Low-side output. Connect to the gate of the low-side power MOSFET.
Pad ⁽¹⁾	PowerPAD™	G	Electrically referenced to V _{SS} (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

(1) The thermal pad is not directly connected to any leads of the package; however, it is electrically and thermally connected to the substrate which is the ground of the device.

(2) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range and all voltages are with respect to V_{SS} (unless otherwise noted).⁽¹⁾

			MIN	MAX	UNIT
V_{DD}	Supply voltage		- 0.3	20	V
V_{HI}, V_{LI}	Input voltages on HI and LI		- 0.3	20	V
V_{LO}	Output voltage on LO	DC	- 0.3	$V_{DD} + 0.3$	V
		Repetitive pulse < 100 ns ⁽²⁾	- 2	$V_{DD} + 0.3$	
V_{HO}	Output voltage on HO	DC	$V_{HS} - 0.3$	$V_{HB} + 0.3$	V
		Repetitive pulse < 100 ns ⁽²⁾	$V_{HS} - 2$	$V_{HB} + 0.3$, ($V_{HB} - V_{HS} < 20$)	
V_{HS}	Voltage on HS	DC	- 1	120	V
		Repetitive pulse < 100 ns ⁽²⁾	- 18	120	
V_{HB}	Voltage on HB		- 0.3	120	V
	Voltage on HB-HS		- 0.3	20	V
T_J	Operating junction temperature		- 40	150	°C
T_{stg}	Storage temperature		- 65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

- (2) Values are verified by characterization and are not production tested.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over operating free-air temperature range and all voltages are with respect to V_{SS} (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	8	12	17	V
V_{HS}	Voltage on HS	- 1		105	V
	Voltage on HS (repetitive pulse < 100 ns) ⁽¹⁾	- 15		110	
V_{HB}	Voltage on HB	$V_{HS} + 8.0, V_{DD} - 1$		$V_{HS} + 17, 115$	
SR_{HS}	Voltage slew rate on HS			50	V/ns
T_J	Operating junction temperature	- 40		150	°C

- (1) Values are verified by characterization and are not production tested.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UCC27201A-Q1	UNIT
		DDA (PowerPad™ SOIC)	
		8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20	°C/W

5.4 Thermal Information (续)

THERMAL METRIC ⁽¹⁾		UCC27201A-Q1	UNIT
		DDA (PowerPad™ SOIC)	
		8 Pins	
ψ_{JT}	Junction-to-top characterization parameter	6.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

5.5 Electrical Characteristics

$V_{DD} = V_{HB} = 12\text{ V}$, $V_{HS} = V_{SS} = 0\text{ V}$, No load on LO or HO, $T_A = T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS					
I_{DD}	VDD quiescent current $V_{LI} = V_{HI} = 0\text{ V}$		0.11	0.8	mA
I_{DDO}	VDD operating current $f = 500\text{ kHz}$, $C_{LOAD} = 0$		1	3	mA
I_{HB}	Boot voltage quiescent current $V_{LI} = V_{HI} = 0\text{ V}$		0.065	0.8	mA
I_{HBO}	Boot voltage operating current $f = 500\text{ kHz}$, $C_{LOAD} = 0$		0.9	3	mA
I_{HBS}	HB to VSS quiescent current $V_{HS} = V_{HB} = 105\text{ V}$		0.0005	1	μA
I_{HBSO}	HB to VSS operating current $f = 500\text{ kHz}$, $C_{LOAD} = 0$		0.03		mA
INPUT					
V_{HIT}	Input voltage high threshold	1.9	2.3	2.7	V
V_{LIT}	Input voltage low threshold	1.3	1.6	1.9	V
V_{IHYS}	Input voltage hysteresis		0.7		V
R_{IN}	Input pulldown resistance $V_{IN} = 3\text{ V}$		68		kΩ
UNDervoltage PROTECTION (UVLO)					
V_{DDR}	VDD rising threshold	6.2	7.1	7.8	V
V_{DDHYS}	VDD threshold hysteresis		0.5		V
V_{HBR}	VHB rising threshold	5.8	6.7	7.2	V
V_{HBHYS}	VHB threshold hysteresis		0.4		V
BOOTSTRAP DIODE					
V_F	Low-current forward voltage $I_{VDD-HB} = 100\text{ μA}$		0.65	0.85	V
V_{FI}	High-current forward voltage $I_{VDD-HB} = 100\text{ mA}$		0.85	1.1	V
R_D	Dynamic resistance, $\Delta V_F / \Delta I$ $I_{VDD-HB} = 120\text{ mA}$ and 100 mA		0.65	1	Ω
LO GATE DRIVER					
V_{LOL}	Low level output voltage $I_{LO} = 100\text{ mA}$		0.1	0.4	V
V_{LOH}	High level output voltage $I_{LO} = -100\text{ mA}$, $V_{LOH} = V_{DD} - V_{LO}$		0.13	0.42	V
	Peak pullup current ⁽¹⁾ $V_{LO} = 0\text{ V}$		3		A
	Peak pulldown current ⁽¹⁾ $V_{LO} = 12\text{ V}$		3		A
HO GATE DRIVER					
V_{HOL}	Low level output voltage $I_{HO} = 100\text{ mA}$		0.1	0.4	V
V_{HOH}	High level output voltage $I_{HO} = -100\text{ mA}$, $V_{HOH} = V_{HB} - V_{HO}$		0.13	0.42	V
	Peak pullup current ⁽¹⁾ $V_{HO} = 0\text{ V}$		3		A
	Peak pulldown current ⁽¹⁾ $V_{HO} = 12\text{ V}$		3		A

(1) Parameter not tested in production.

5.6 Switching Characteristics

$V_{DD} = V_{HB} = 12\text{ V}$, $V_{HS} = V_{SS} = 0\text{ V}$, No load on LO or HO, $T_A = T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROPAGATION DELAYS						
t_{DLFF}	VLI falling to VLO falling	$C_{LOAD} = 0\text{ pF}$, from V_{LIT} of LI to 90% of LO falling		22	50	ns
t_{DHFF}	VHI falling to VHO falling	$C_{LOAD} = 0\text{ pF}$, from V_{HIT} of HI to 90% of HO falling		22	50	ns
t_{DLRR}	VLI rising to VLO rising	$C_{LOAD} = 0\text{ pF}$, from V_{LIT} of LI to 10% of LO rising		22	50	ns
t_{DHRR}	VHI rising to VHO rising	$C_{LOAD} = 0\text{ pF}$, from V_{HIT} of HI to 10% of HO rising		22	50	ns
DELAY MATCHING						
t_{MON}	LI ON, HI OFF			1	7	ns
t_{MOFF}	LI OFF, HI ON			1	7	ns
OUTPUT RISE AND FALL TIME						
t_{R_LO}	LO rise time	$C_{LOAD} = 1000\text{ pF}$, from 10% to 90%		8		ns
t_{R_HO}	HO rise time	$C_{LOAD} = 1000\text{ pF}$, from 10% to 90%		8		ns
t_{F_LO}	LO fall time	$C_{LOAD} = 1000\text{ pF}$, from 10% to 90%		7		ns
t_{F_HO}	HO fall time	$C_{LOAD} = 1000\text{ pF}$, from 10% to 90%		7		ns
$t_{R_LO_p1}$	LO rise time (3 V to 9 V)	$C_{LOAD} = 0.1\text{ }\mu\text{F}$, (3V to 9V)		0.26	0.6	$\mu\text{ s}$
$t_{R_HO_p1}$	HO rise time (3 V to 9 V)	$C_{LOAD} = 0.1\text{ }\mu\text{F}$, (3V to 9V)		0.26	0.6	$\mu\text{ s}$
$t_{F_LO_p1}$	LO fall time (9 V to 3 V)	$C_{LOAD} = 0.1\text{ }\mu\text{F}$, (9V to 3V)		0.22	0.6	$\mu\text{ s}$
$t_{F_HO_p1}$	HO fall time (9 V to 3 V)	$C_{LOAD} = 0.1\text{ }\mu\text{F}$, (9V to 3V)		0.22	0.6	$\mu\text{ s}$
MISCELLANEOUS						
t_{IN_PW}	Minimum input pulse width that changes the output LO			50		ns
t_{IN_PW}	Minimum input pulse width that changes the output HO			50		ns
t_{OFF_BSD}	Bootstrap diode turnoff time ^{(1) (2)}	$I_F = 20\text{ mA}$, $I_{REV} = 0.5\text{ A}$ ⁽³⁾		20		ns

(1) Parameter not tested in production.

(2) Typical values for $T_A = 25^\circ\text{C}$.

(3) I_F : Forward current applied to bootstrap diode, I_{REV} : Reverse current applied to bootstrap diode.

5.7 Timing Diagrams

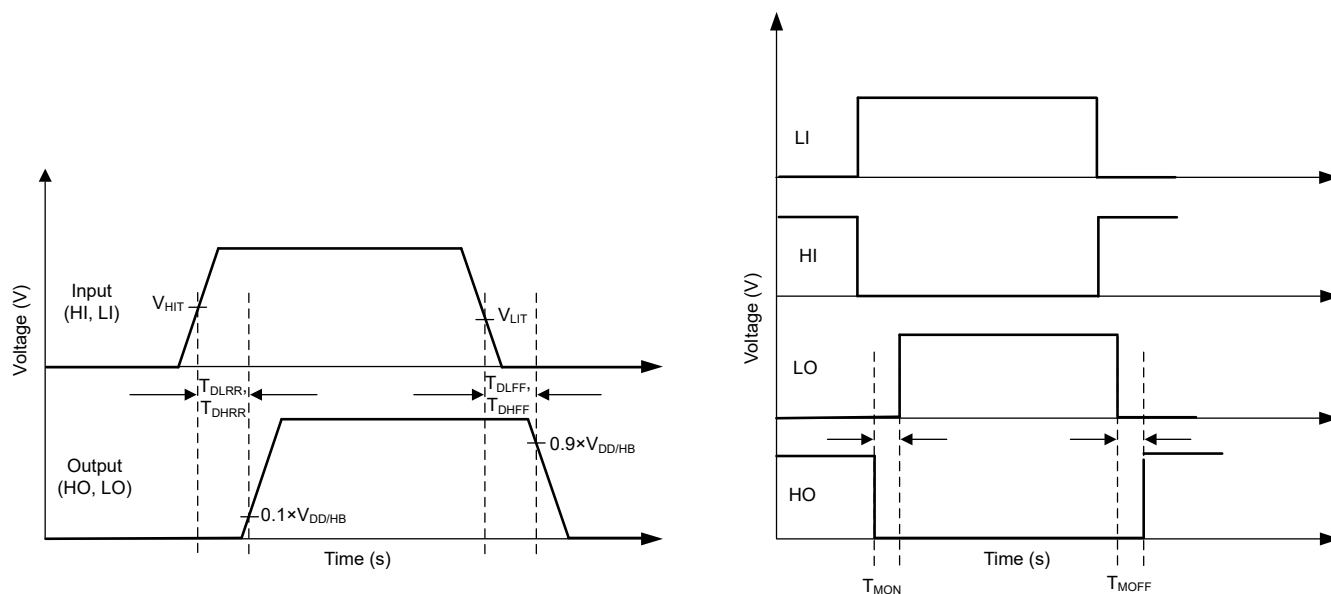


图 5-1. Timing Diagrams

5.8 Typical Characteristics

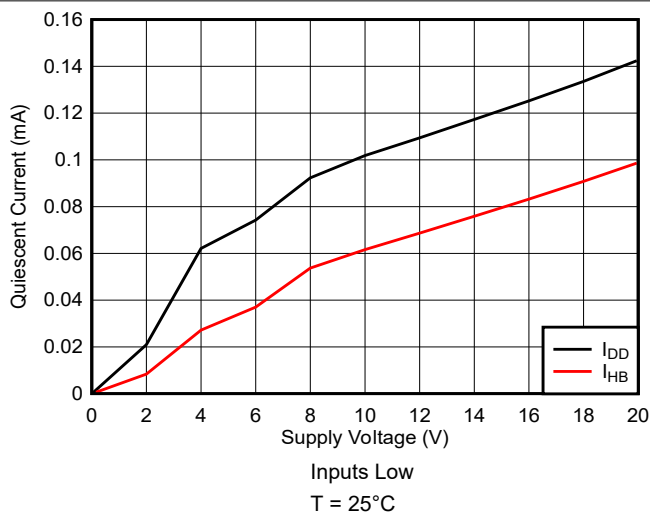


图 5-2. Quiescent Current vs Supply Voltage

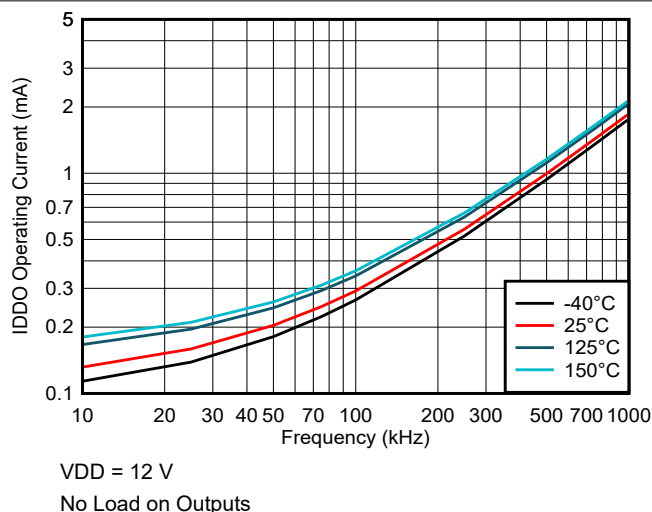


图 5-3. IDD Operating Current vs Frequency

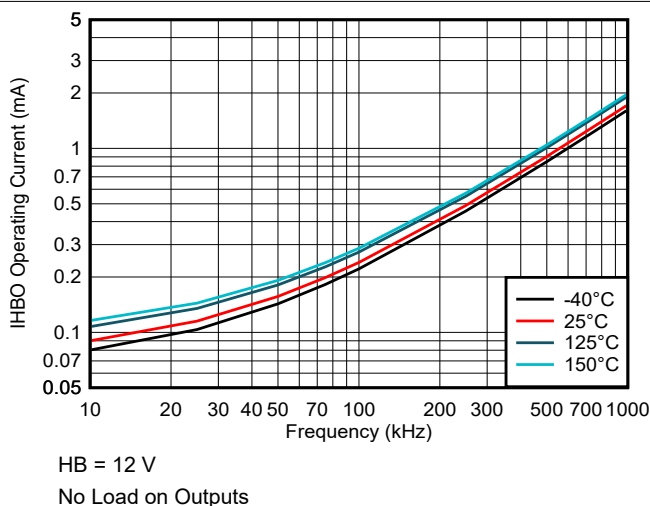


图 5-4. Boot Voltage Operating Current vs Frequency

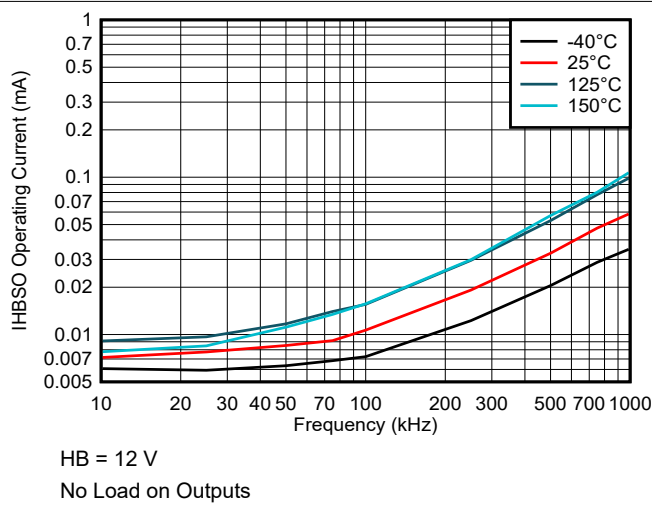


图 5-5. HB to VSS Operating Current vs Frequency

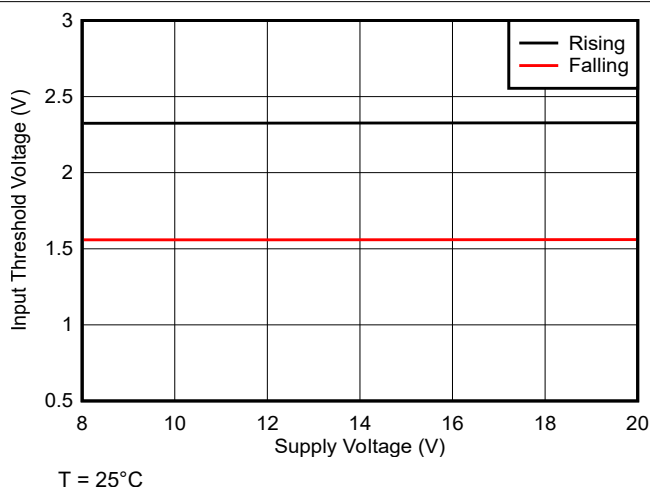


图 5-6. Input Threshold vs Supply Voltage

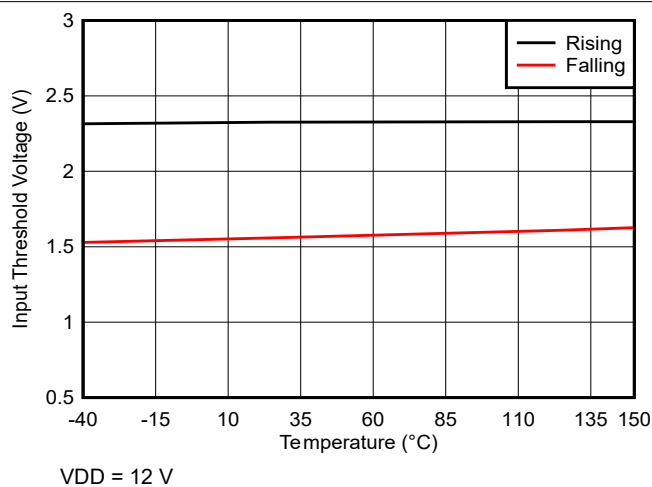


图 5-7. Input Threshold vs Temperature

5.8 Typical Characteristics (continued)

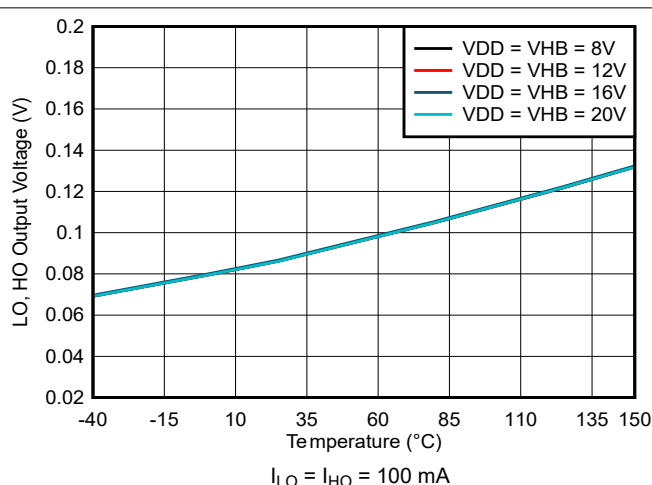


图 5-8. LO and HO Low Level Output Voltage vs Temperature

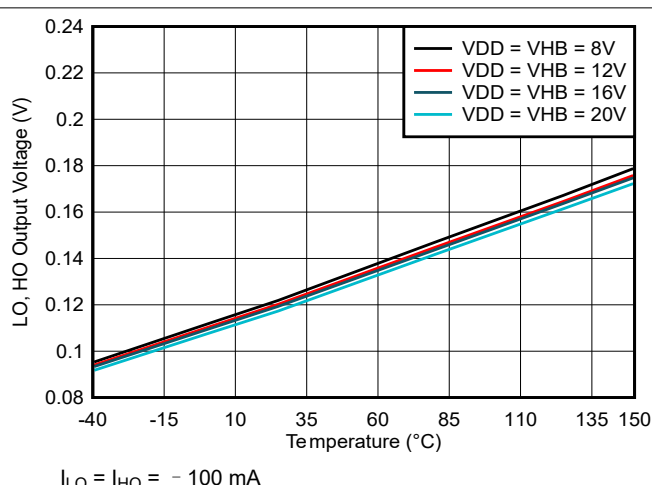


图 5-9. LO and HO High Level Output Voltage vs Temperature

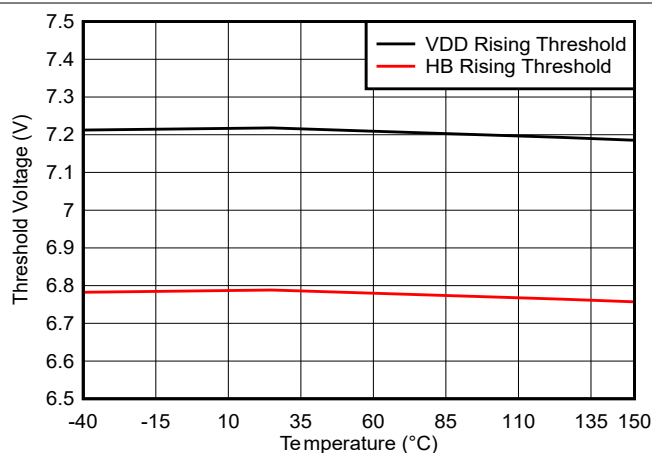


图 5-10. Undervoltage Lockout Threshold vs Temperature

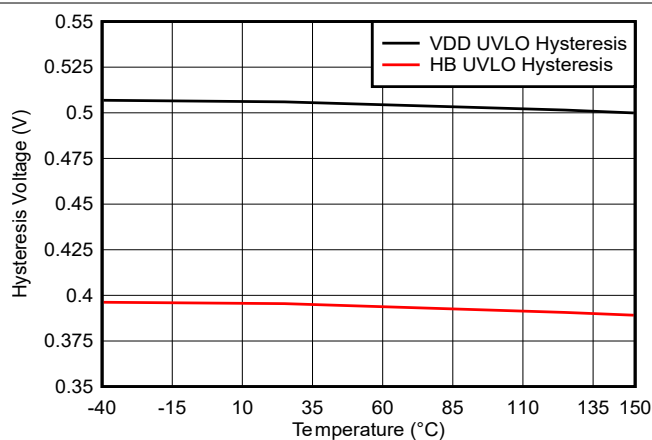


图 5-11. Undervoltage Lockout Threshold Hysteresis vs Temperature

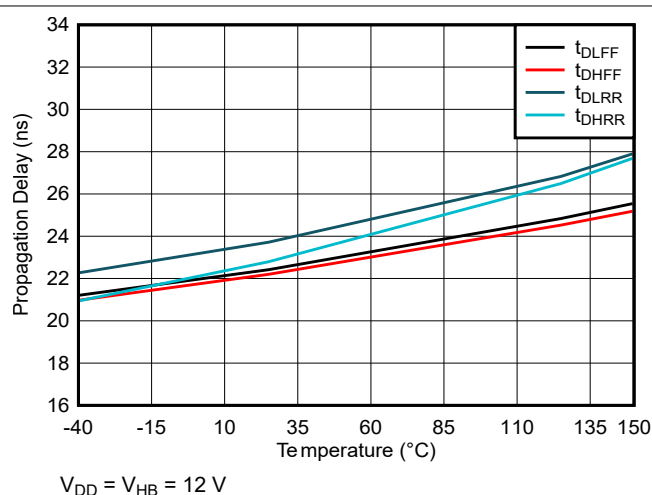


图 5-12. Propagation Delays vs Temperature

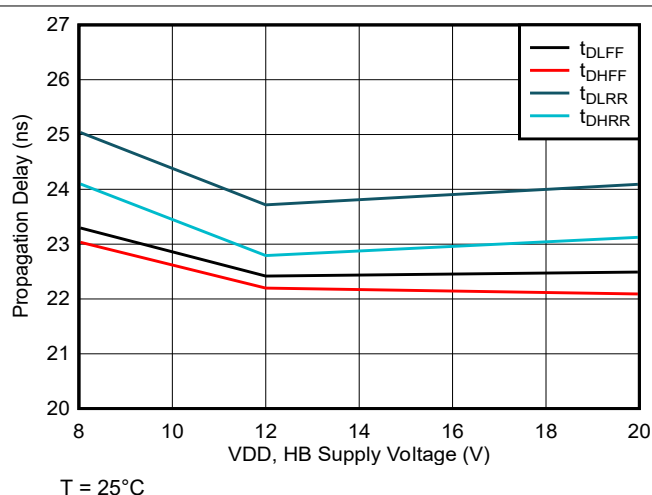


图 5-13. Propagation Delay vs Supply Voltage

5.8 Typical Characteristics (continued)

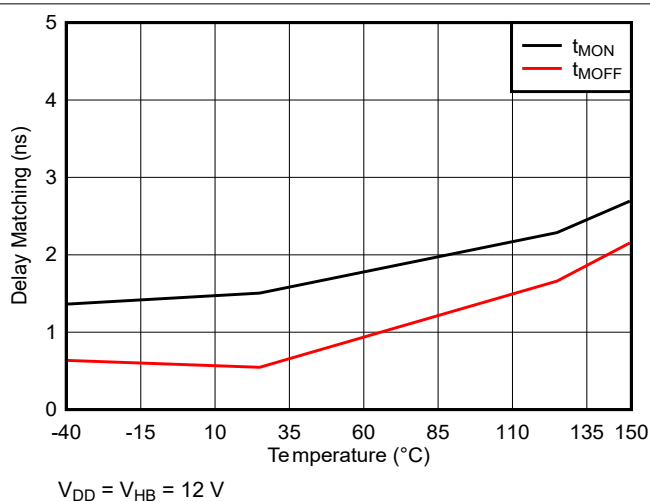


图 5-14. Delay Matching vs Temperature

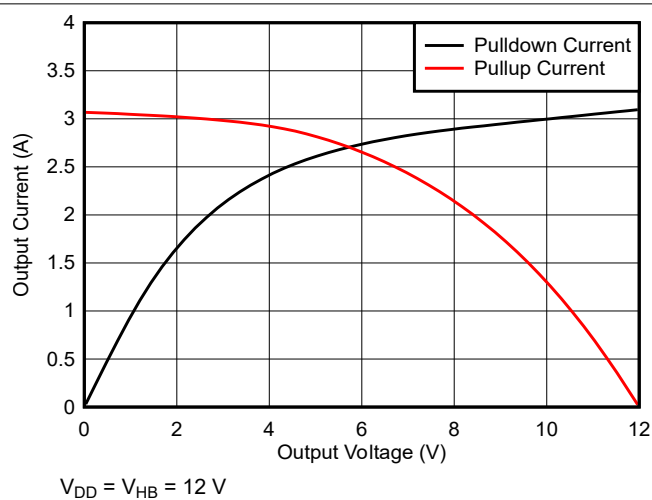


图 5-15. Output Current vs Output Voltage

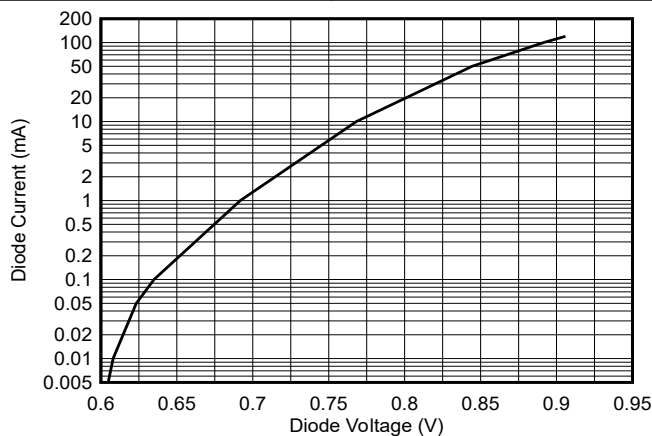


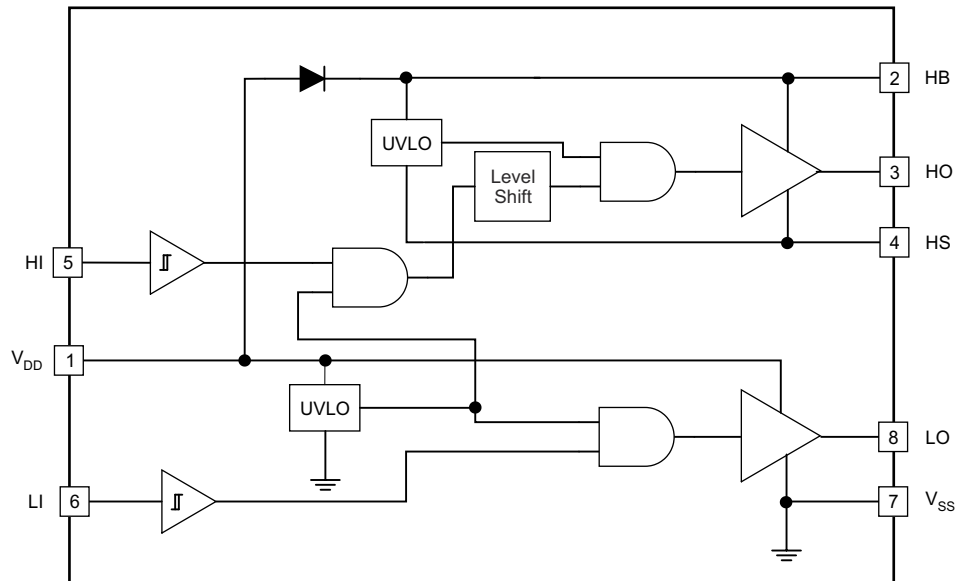
图 5-16. Diode Current vs Diode Voltage

6 Detailed Description

6.1 Overview

The UCC27201A-Q1 is a high-side/low-side driver. The high-side and low-side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27201A-Q1. The HI and LI inputs are TTL-compatible. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to VSS which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Input Stages

The input stages provide the interface to the PWM output signals. The input stages of the UCC27201A-Q1 incorporate an open drain configuration to provide the lower input thresholds. The input impedance is 68k Ω nominal and input capacitance is approximately 4pF. The 68k Ω is a pull-down resistance to VSS (ground). The logic level compatible input provides a rising threshold of 2.3V typical and a falling threshold of 1.6V typical.

6.3.2 UVLO (Under Voltage Lockout)

The bias supplies for the high-side and low-side drivers have UVLO protection. VDD as well as VHB to VHS differential voltages are monitored. The VDD UVLO disables both drivers when VDD is below the specified threshold. The rising VDD threshold is 7.1V with 0.5V hysteresis. The VHB UVLO disables only the high-side driver when the VHB to VHS differential voltage is below the specified threshold. The VHB UVLO rising threshold is 6.7V with 0.4V hysteresis.

6.3.3 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

6.3.4 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27201A-Q1 driver. The diode anode is connected to VDD and cathode connected to VHB. With the VHB capacitor connected to HB and the HS pins, the VHB capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

6.3.5 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from VDD to VSS and the high-side is referenced from VHB to VHS.

6.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See [节 6.3.2](#) for more information on UVLO operation mode. In normal mode, the output stage is dependent on the states of the HI and LI pins.

表 6-1. Device Logic Table

HI PIN	LI PIN	HO ⁽¹⁾	LO ⁽²⁾
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to HS.

(2) LO is measured with respect to VSS.

7 Application and Implementation

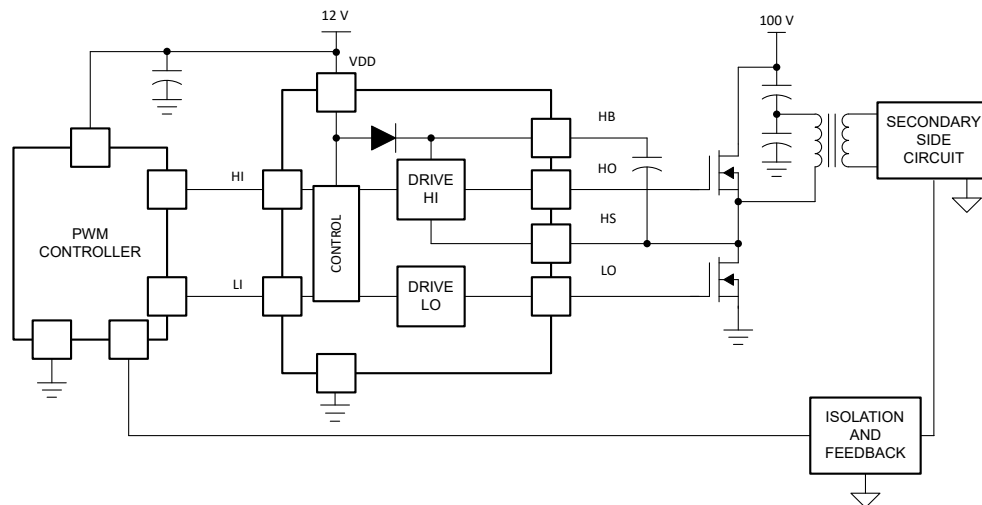
备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3V signal to the gate-drive voltage (such as 12V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

7.2 Typical Application



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图 7-1. UCC27201A-Q1 Typical Application Diagram

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1.

表 7-1. Design Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, VDD	12V
Voltage on HS, VHS	0V to 100V
Voltage on HB, VHB	12V to 112V
Output current rating, IO	- 3A to 3A

表 7-1. Design Specifications (续)

DESIGN PARAMETER	EXAMPLE VALUE
Operating frequency	200kHz

7.2.2 Detailed Design Procedure

7.2.2.1 Input Threshold Type

The UCC27201A-Q1 device features TTL compatible input threshold logic with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the [Electrical Characteristics](#) table for the actual input threshold voltage levels and hysteresis specifications for the UCC27201A-Q1 device.

7.2.2.2 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the [Absolute Maximum Ratings](#) table. Different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from 8V to 17V, the UCC27201A-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs, IGBTs, and wide-bandgap power semiconductors.

7.2.2.3 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible in order to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds with the targeted power MOSFET. The system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV_{DS}/dt of 20V/ns or higher with a DC bus voltage of 400V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 20ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in the SPP20N60C3 data sheet is 33nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(TH)}$.

To achieve the targeted dV_{DS}/dt , the gate driver must be capable of providing the Q_{GD} charge in 20ns or less. In other words a peak current of 1.65A ($= 33nC / 20ns$) or higher must be provided by the gate driver. The UCC27201A-Q1 gate driver is capable of providing 3A peak sourcing current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The overdrive capability provides an extra margin against part-to-part variations in the Q_{GD} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. In order to illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle ($\frac{1}{2} \times I_{PEAK} \times \text{time}$) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

7.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27201A-Q1 device features 22ns (typical) propagation delays, which ensures very little pulse distortion and allows operation at very high-frequencies. See the [Electrical Characteristics](#) table for the propagation and switching characteristics of the UCC27201A-Q1 device.

7.2.2.5 Power Dissipation

Power dissipation of the gate driver has two portions as shown in [方程式 1](#).

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

Use [方程式 2](#) to calculate the DC portion of the power dissipation (PDC).

$$PDC = I_Q \times V_{DD} \quad (2)$$

where

- I_Q is the quiescent current for the driver.

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The UCC27201A-Q1 features very low quiescent currents (refer to the [Electrical Characteristics](#) table) and contain internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the PDC on the total power dissipation within the gate driver can be safely assumed to be negligible. The power dissipated in the gate-driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G , which is very close to input bias supply voltage V_{DD})
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by [方程式 3](#).

$$EG = \frac{1}{2} C_{LOAD} \times V_{DD}^2 \quad (3)$$

- where
- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged and when it is discharged. This leads to a total power loss given by [方程式 4](#).

$$PG = C_{LOAD} \times V_{DD}^2 \times f_{SW} \quad (4)$$

where

- f_{SW} is the switching frequency

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g , determine the power that must be dissipated when switching a capacitor which is calculated using the equation $Q_g = C_{LOAD} \times V_{DD}$ to provide [方程式 5](#) for power.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_G \times V_{DD} \times f_{SW} \quad (5)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on and off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

7.2.3 Application Curves

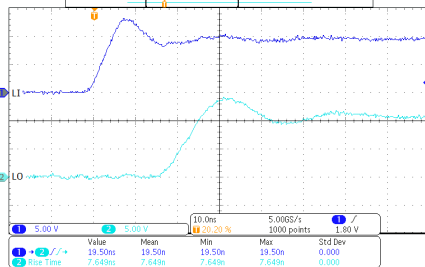


图 7-2. LO Rise Time and LI to LO Turn-on Propagation Delay

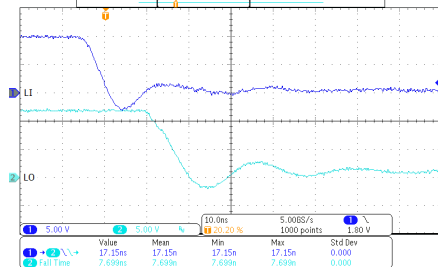


图 7-3. LO Fall Time and LI to LO Turn-off Propagation Delay

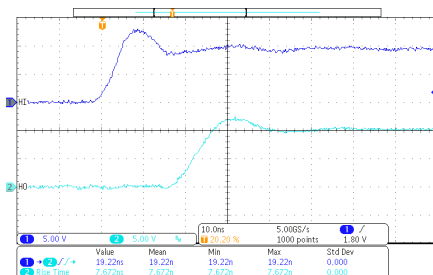


图 7-4. HO Rise Time and HI to HO Turn-on Propagation Delay

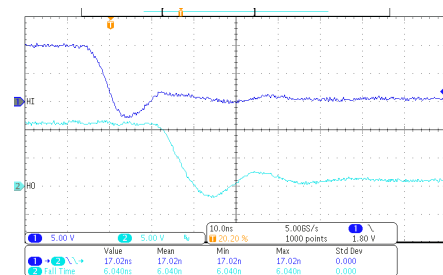


图 7-5. HO Fall Time and HI to HO Turn-off Propagation Delay

8 Power Supply Recommendations

The bias supply voltage range for which the device is rated to operate is from 8V to 17V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the V(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 3V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 17V. The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD(hys). Therefore, ensuring that, while operating at or near the 8V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the V(OFF) threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the VDD pin voltage has exceeded above the V(ON) threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the LO pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the LO pin a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that a local bypass capacitor is provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends using a capacitor in the range 0.22 μ F to 4.7 μ F between VDD and GND. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore a 0.022 μ F to 0.1 μ F local decoupling capacitor is recommended between the HB and HS pins.

9 Layout

9.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules should be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and V_{HB} (bootstrap) capacitors as close as possible to the driver.
- Pay close attention to the GND trace. Use the thermal pad of the DDA package as GND by connecting it to the VSS pin (GND). *Note: The GND trace from the driver goes directly to the source of the MOSFET but should not be in the high current path of the MOSFET(S) drain or source current.*
- Use similar rules for the HS node as for GND for the high side driver.
- Use wide traces for LO and HO closely following the associated GND or HS traces. 60 mil to 100 mil width is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node needs to be routed from one layer to another. For GND the number of vias needs to be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid L_I and H_I (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.
- Keep in mind that a poor layout can cause a significant drop in efficiency versus a good PCB layout and can even lead to decreased reliability of the whole system.

9.2 Layout Example

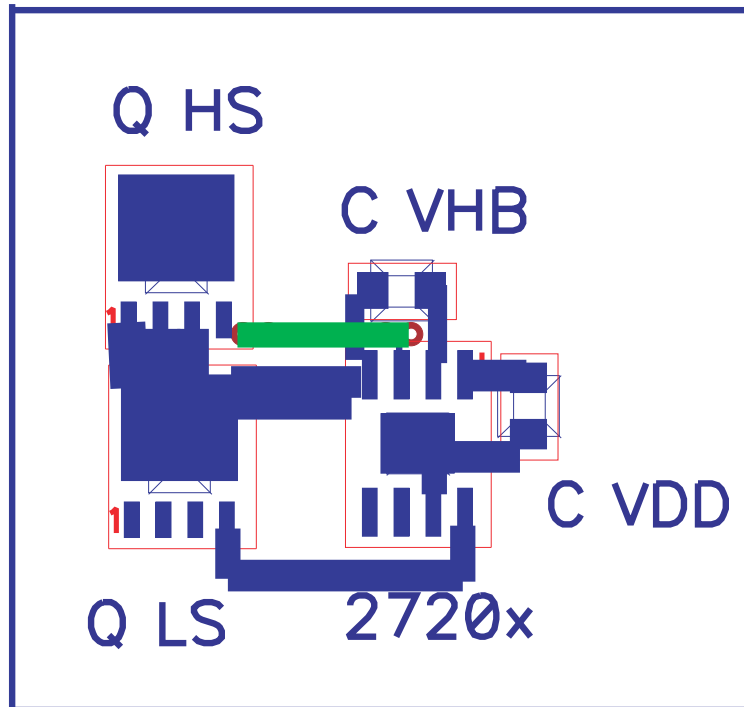


图 9-1. Example Component Placement

10 Device and Documentation Support

10.1 第三方产品免责声明

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10.2 Documentation Support

10.2.1 Related Documentation

For additional information, see the following:

1. PowerPAD™ Thermally Enhanced Package ([SLMA002](#))
2. PowerPAD™ Made Easy ([SLMA004](#))

10.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

10.5 Trademarks

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TI E2E™ is a trademark of Texas Instruments.

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10.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (March 2016) to Revision C (July 2024)	Page
• 更改了文档标题以反映器件的主要特性。对若干规格进行了小幅更新以反映器件特性。	1
• 更新了“特性”部分：1) 删除了 HBM 和 CDM ESD 分类等级，以遵循最新的 TI 数据表标准。2) 将结温范围从“-40°C 至 140°C”更改为“-40°C 至 150°C”。3) 删除了 DMK 封装，因为该器件已停产。4) 将典型传播延迟从 20ns 更改为 22ns。5) 删除了“工作频率大于 1MHz”，因为开关频率不是指定的参数。6) 将典型自举二极管电阻从 0.6 Ω 更改为 0.65 Ω	1
• 更新了“应用”部分，添加了 5 大典型应用列表。	1
• 更新了“说明”部分：1) 删除了与 UCC27200 和 UCC27201 产品的比较。2) 澄清了 -18V HS 容差是绝对最大值规格。3) 删除了对 DMK 封装的引用。	1
• Updated Pin Configuration and Functions Functions section - deleted 10-pin VSON DMK package information and updated PowerPAD description.....	3
• Updated Absolute Maximum Ratings section to remove "Power dissipation at TA = 25°C" and "Lead temperature (soldering, 10s)". Power dissipation can be calculated with thermal metrics in "Thermal Information" table.....	4
• Updated Recommended Operating Conditions: Operating Junction Temperature maximum changed from 140°C to 150°C.....	4
• Updated Thermal Information section to reflect device characteristics.	4
• Updated Supply Currents specifications in the Electrical Characteristics table: 1) I _{DD} typical changed (From: 0.4mA. To: 0.11mA). 2) I _{DDO} typical changed (From: 3.8mA. To: 1mA). 3) I _{DDO} maximum changed (From: 5.5mA. To: 3mA. 4) I _{HB} typical changed (From: 0.4mA. To: 0.065mA). 5) I _{HBO} typical changed (From: 2.5mA. To: 0.9mA). 6) I _{HBO} maximum changed (From: 4mA. To: 3mA). 7) I _{HBS} test condition changed to match V _{HS} maximum recommended operating conditions (From: 110V. To: 105V). 8) I _{HBSO} typical changed (From: 0.1mA. To: 0.03mA).....	4
• Updated Input specifications in the Electrical Characteristics table: 1) V _{HIT} specifications changed (From: 1.7V typical, 2.5V maximum. To: 1.9V minimum, 2.3V typical, 2.7V maximum). 2) V _{LIT} specifications changed (From: 0.8V minimum, 1.6V typical. To: 1.3V minimum, 1.6V typical, 1.9V maximum). 3) V _{IHYS} typical changed (From: 100mV. To: 700mV). 4) R _{IN} specifications changed from (100k Ω minimum, 200k Ω typical, 350k Ω maximum. To: 68k Ω typical).	4
• Updated Bootstrap diode specifications in the Electrical Characteristics table: 1) R _D test conditions changed (From: 100mA and 80mA. To: 120mA and 100mA). 2) R _D typical changed (From: 0.6 Ω . To: 0.65 Ω). Updated LO/HO Gate Driver specifications in the Electrical Characteristics table: 1) V _{LOL} typical changed (From 0.18V. To 0.1V). 2) V _{LOH} typical changed (From: 0.25V. To: 0.13V).	4
• Removed specifications with test conditions "-40°C to 125°C T _J ", since all parameters are specified from -40°C to 150°C T _J (unless otherwise noted).	4
• Changed Propagation Delays typical specification (From: 20ns. To: 22ns).....	4
• Updated Output Rise and Fall Time specifications: 1) t _R typical changed (From: 0.35us. To: 0.26us). 2) t _F typical changed (From: 0.3us. To: 0.22us).	4
• Updated timing diagrams.....	7
• Updated all plots in Typical Characteristics section to reflect the device's typical specification.	8
• Updated Input Stages section to match the input typical specification in the electrical characteristics table - changed 200kΩ pull-down resistance, 1.7V input rising threshold to 8kΩ pull-down resistance, 2.3V input rising threshold.	11
• Updated Typical Application section to display a different application diagram, updated Design Requirements section, and updated Detailed Design procedure section since information in previous revision of data sheet had an outdated circuit with obsolete part numbers.	13
• Changed application curves to display propagation delay and rise/fall time plots.	17

- Changed Power Supply Recommendations section to correctly describe that LO is sourced from VDD and HO is sourced from HB. 18

Changes from Revision A (October 2015) to Revision B (March 2016) Page

- Added 10-Pin VSON DMK Package information.....3
-

Changes from Revision * (May 2015) to Revision A (October 2015) Page

- Changed $I_{LO} = I_{HO} = -100$ mA condition to $I_{LO} = I_{HO} = 100$ mA 8
 - Changed $I_{LO} = I_{HO} = 100$ mA condition to $I_{LO} = I_{HO} = -100$ mA 8
-

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27201AQDDARQ1	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	201AQ1
UCC27201AQDDARQ1.A	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	201AQ1
UCC27201AQDDARQ1.B	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	201AQ1
UCC27201AQDMKRQ1	Active	Production	VSON (DMK) 10	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	UCC 27201AQ
UCC27201AQDMKRQ1.A	Active	Production	VSON (DMK) 10	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	UCC 27201AQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27201A-Q1 :

- Catalog : [UCC27201A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27201AQDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UCC27201AQDMKRQ1	VSON	DMK	10	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27201AQDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
UCC27201AQDMKRQ1	VSON	DMK	10	2500	346.0	346.0	33.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA0008B

PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4214849/A 08/2016

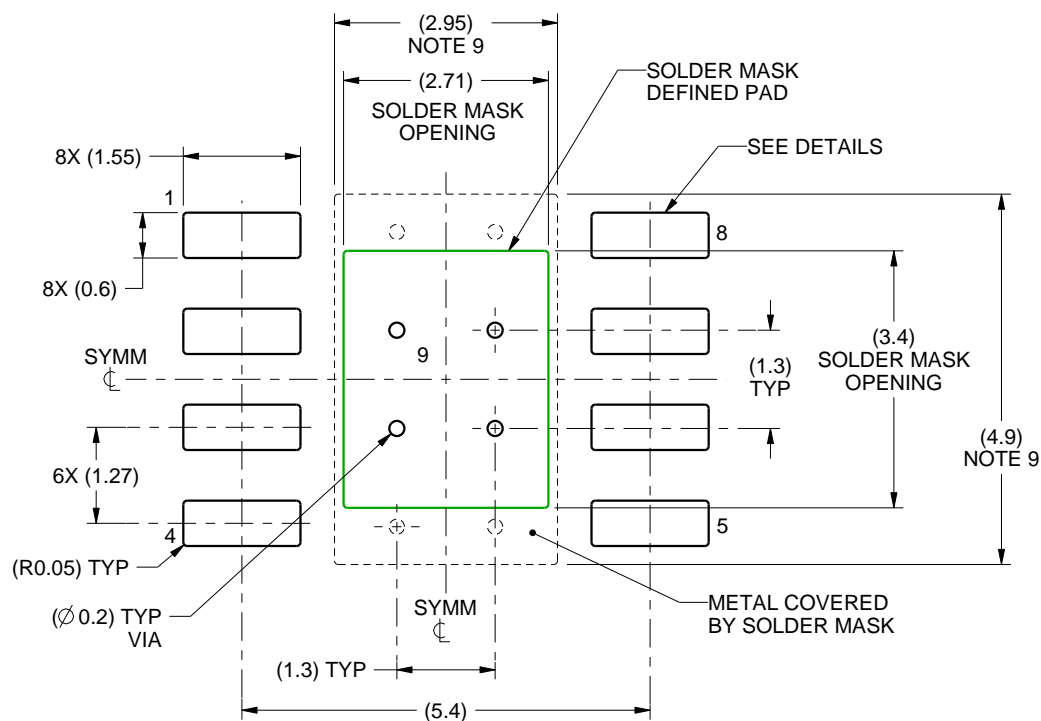
NOTES:

PowerPAD is a trademark of Texas Instruments.

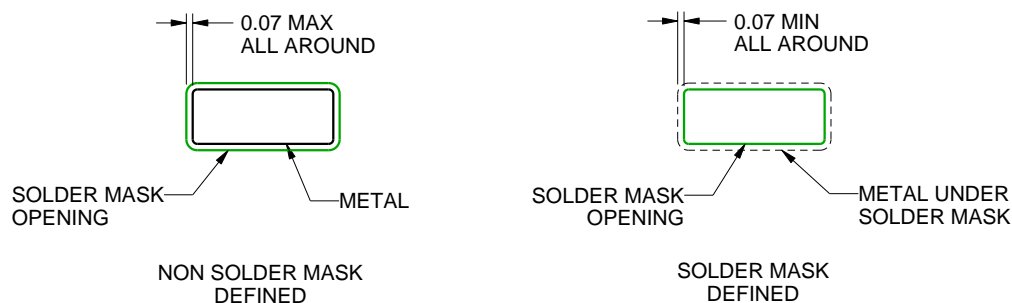
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

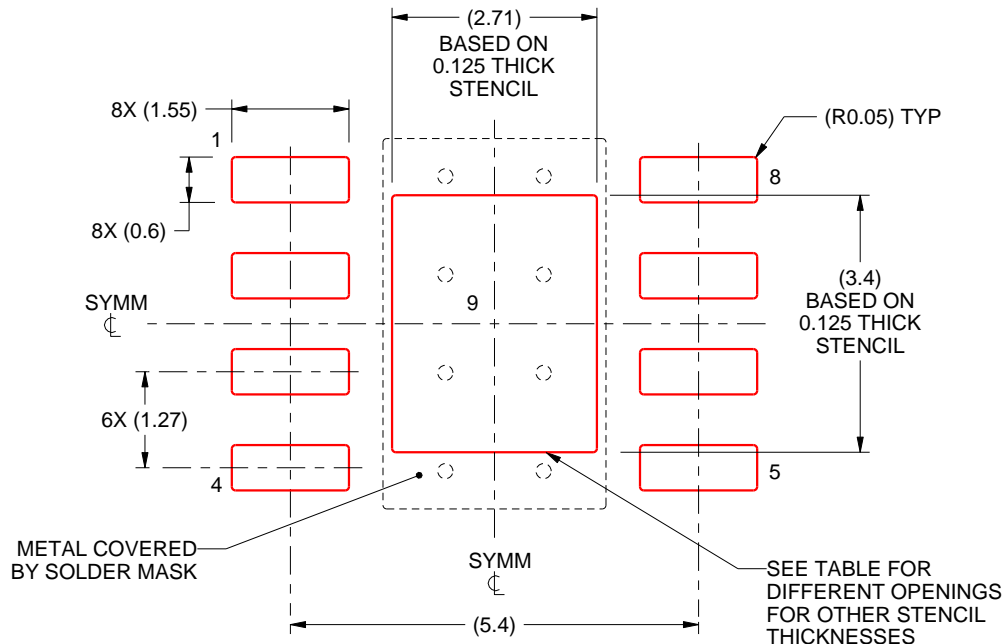
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

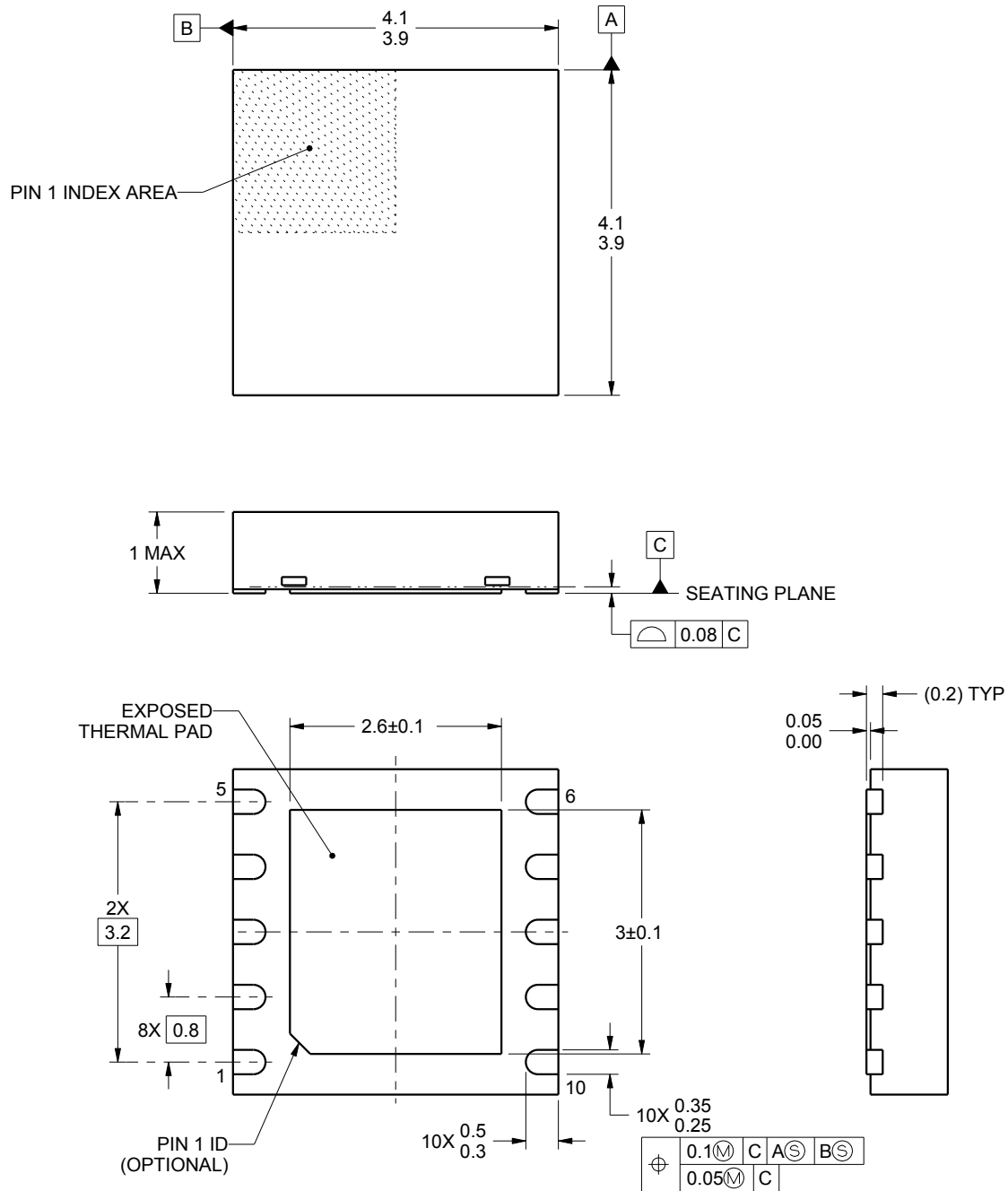
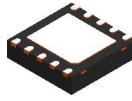
DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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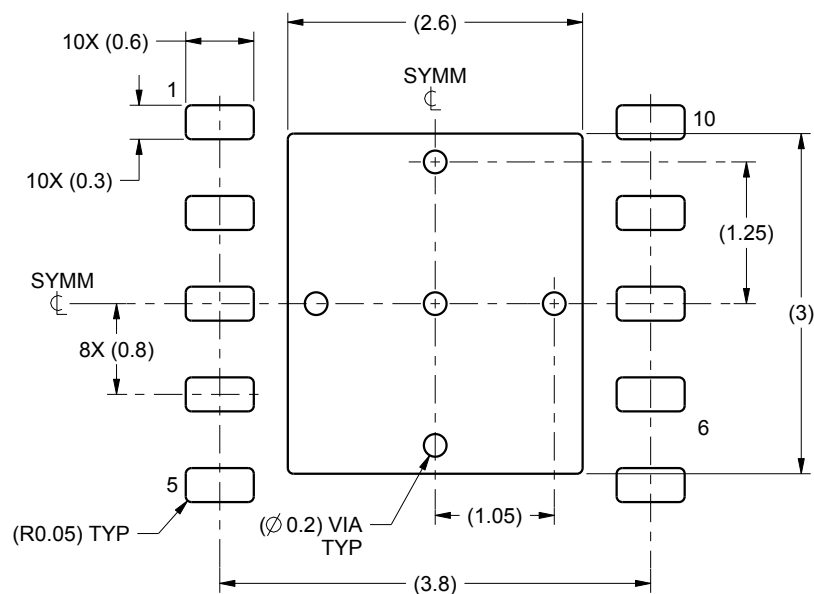
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

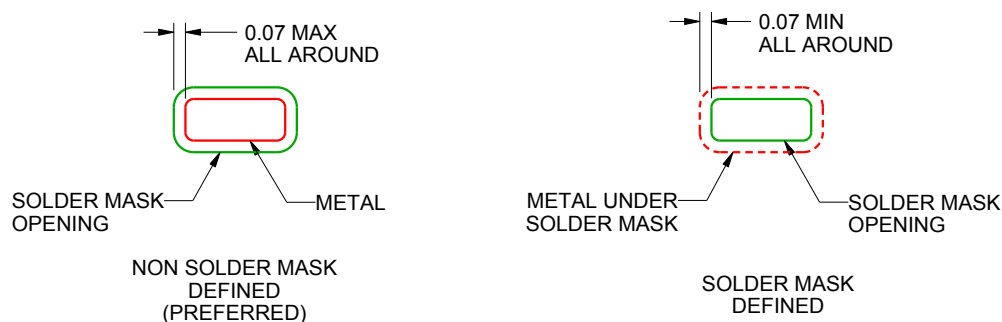
DMK0010A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

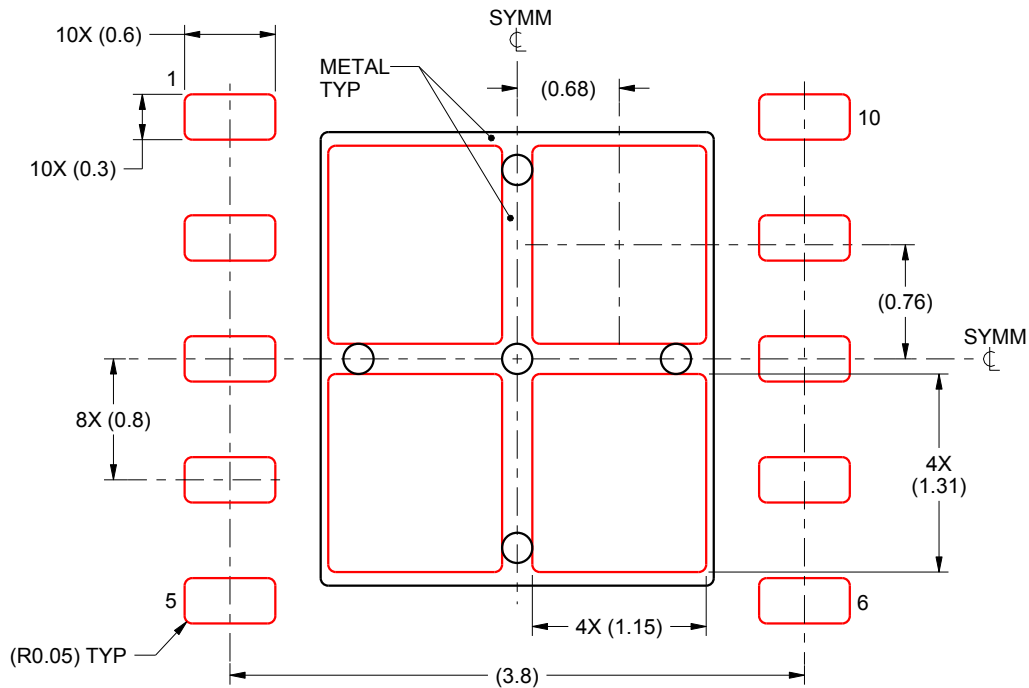
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DMK0010A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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