UCC24650 用于快速瞬态 PSR 的 200V 唤醒监视器

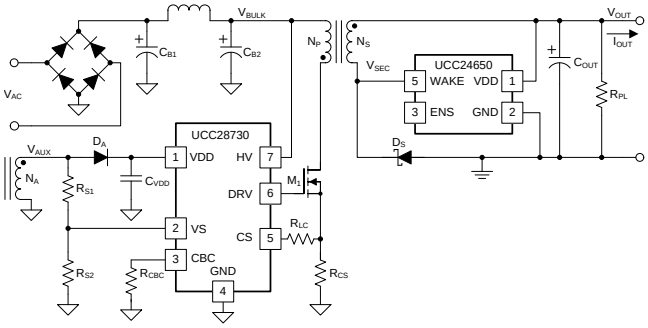
1 特性

- 具有出色的负载瞬态性能和零待机功耗
- 实现最小输出电容，以降低 ΔV_{OUT}
- 无需外部元件
- <50μA 的器件电流补偿（典型值）
- 5V 至 28V 输出监视能力
- 3% 电压浮动检测（专利申请中）
- 200V 唤醒开关
- 可使能和禁用 SR 控制器、继电器控制或其他辅助电路
- 5 引脚小外形尺寸晶体管 (SOT)-23 封装

2 应用

- < 5mW *零功耗*待机应用
- 面向消费类电子产品的适配器和充电器
  - 智能手机、平板电脑、机顶盒
- TV 和监视器电源
- 家用电器开关电源 (SMPS)
  - 冰箱、洗衣机、空调
- 面向照明和家用自动化的工业电源

简化应用电路原理图



3 说明

UCC24650 是一款易于使用的二次侧电压监视器，可定期测量其自身的 VDD 电压。 当相对上一读数存在 3% 浮动时，会向接收一次侧稳压 (PSR) 控制器发送*唤醒*警报信号。 该器件功耗较低，有助于在许多应用中实现小于 5mW 的*零功耗*待机损耗。

接地基准整流器上连接了一个内部 200V 金属氧化物半导体场效应晶体管 (MOSFET) 开关，可向反激变压器二次侧绕组提供限流脉冲，从而将信号耦合至一次侧控制器。 在检测到控制器驱动的开关活动之前，将以 33kHz 的频率重复发送该信号。

相对浮动检测功能可将电压调节至 5V 与 28V 之间的任一电压。*唤醒*警报功能可实现超低待机频率，从而以最大限度降低开关损耗，并减小响应重载阶跃所需的输出电容。 此监视器与能够检测*唤醒*信号的控制器搭配使用，例如 UCC28730 PSR 反激控制器。

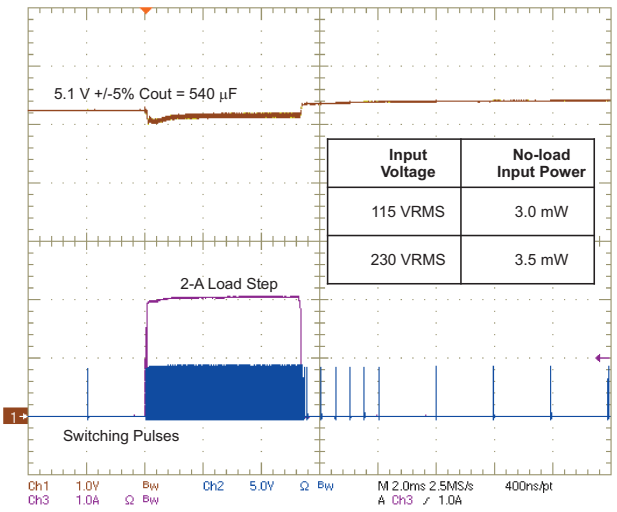
UCC24650 还提供了使能和禁用信号，可用于在无载条件下控制二次侧电路，从而降低待机功耗。 此类电路可以是同步整流控制器或继电器驱动器等。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC24650	SOT-23 (5)	2.92mm × 1.30mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

快速全负载阶跃响应



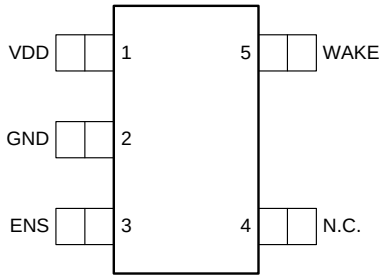
目录

4 修订历史记录

日期	修订版本	注释
2015 年 2 月	*	最初发布。

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



A. (N.C. = No connection internally)

Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
VDD	1	P	VDD is the bias supply input pin to the controller. This pin is continuously monitored to detect when the VDD voltage droops by approximately –3% of the previously sampled level. The VDD level is sampled and stored at the end of each power cycle generated by the PSR. The device is disabled when the VDD voltage is below the UVLO threshold.
GND	2	G	The ground pin is both the reference pin for the controller and the low-side return for the WAKE output. Take special care to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal return paths.
ENS	3	O	Enable secondary circuit is an open-drain MOSFET output that enables a compatible synchronous rectifier (SR) controller or other secondary-side circuitry. ENS is open during normal operation and becomes low-impedance to GND when each switching period remains greater than t_{DISS} (177 µs typical) for 63 consecutive cycles. ENS becomes high-impedance again when the switching period operates at less than t_{ENS} (57 µs typical) for 32 cumulative cycles. If the ENS function is not used, this terminal should be connected to GND.
N/C	4	—	The no-connection pin has no internal electrical connection.
WAKE	5	I/O	WAKE is a multi-function pin which connects to the transformer secondary winding, directly across the ground-referenced diode or rectifier. As an input, it monitors voltage pulses due to primary-side controller activity and triggers sampling of the VDD voltage at the end of each power cycle. When the WAKE voltage falls below 55 mV for >500 ns, the device becomes armed to deliver a power cycle detect (PCD) pulse internally. When the WAKE voltage subsequently rises above 55 mV, a PCD pulse is delivered to reset the oscillator, clock the PCD counter, and trigger a new sample of the VDD voltage. If the VDD voltage droops to 97% of the last sampled value, WAKE is driven as an output. As an output, it injects current into the transformer winding for 1 µs at a 33-kHz rate until a power cycle is detected. The maximum magnitude that this current may achieve is limited internally.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VCC	–0.5	30	V
	WAKE	(2)	230	
	ENS	–0.5	7	
Source current	WAKE		10	mA
	ENS		1	
Sink current	WAKE		Self-limiting	mA
	ENS		0.5	
T_J	Operating junction temperature	–55	150	°C
T_{lead}	Lead temperature 0.6 mm from case for 10 s		260	
T_{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The WAKE pin is normally brought below GND by a system-level rectifier. A negative voltage level is not of concern provided that the absolute maximum source current limit is observed.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except pin 5	±2000	V
			Pin 5	±1500	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}	Bias-supply operating voltage	4.5		28	V
V_{WAKE}	WAKE pin voltage			200	V
V_{ENS}	ENS pin voltage(1)	0		6	V
t_{PCD}	Power cycle detect interval			40	ms
T_J	Operating junction temperature range	–40		125	°C

(1) The UCC24650 enters a manufacturing test mode when ENS is driven below 0 V and normal operation is impaired during this condition. If the ENS function is not used, connect ENS to GND to avoid triggering the test mode by noise on an open pin.

6.4 Thermal Information

THERMAL METRIC(1)		UCC24650 DBV 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	200.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	125.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	35.8	
ψ_{JT}	Junction-to-top characterization parameter	18.4	
ψ_{JB}	Junction-to-board characterization parameter	35.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{VDD} = 5 V, V_{WAKE} = 5 V, –40°C ≤ T_A ≤ 125°C, T_J = T_A, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY INPUT						
I_{VDD28}	Supply current	V_{VDD} = 28 V, V_{WAKE} = 28 V	43	63	83	µA
I_{VDD5}	Supply current	V_{VDD} = 5 V, V_{WAKE} = 5 V	30	41	52	µA
$V_{UVLO(on)}$	UVLO turn-on voltage at VDD	V_{VDD} rising threshold	3.6	4.0	4.4	V
$V_{UVLO(hyst)}$	UVLO hysteresis	$V_{UVLO(on)}$ – V_{VDD} falling threshold	170	250	330	mV
WAKE INPUT						
V_{PCD}	PCD voltage threshold	V_{WAKE} high to low	10	55	100	mV
I_{WAKE}	Input bias current, out of pin	V_{WAKE} = 0 V		0	0.1	µA
$I_{WAKE(lkg)cool}$ (1)	Input leakage current, into pin, cool	V_{WAKE} = 200 V, -40°C ≤ T_J ≤ 85°C		0	0.2	µA
$I_{WAKE(lkg)hot}$ (1)	Input leakage current, into pin, hot	V_{WAKE} = 200 V, 85°C ≤ T_J ≤ 125°C		0	3	µA
WAKE-UP FUNCTION						
$\Delta V_{VDD5(cool)}$ (1) (2)	Droop threshold, over cool temperature range	Drop in V_{VDD} following a power-cycle detect by 40 ms, V_{VDD} falling from 5 V, dv/dt = –250 V/s, –40°C ≤ T_J ≤ 85°C	–2.30%	–2.77%	–3.20%	
$\Delta V_{VDD5(hot)}$ (1) (2)	Wake-up droop threshold, over hot temperature range	Drop in V_{VDD} following a power-cycle detect by 40 ms, V_{VDD} falling from 5 V, dv/dt = –250 V/s, 85°C ≤ T_J ≤ 125°C	–1.50%	–2.74%	–4.0%	
ΔV_{VDD28} (1) (2)	Wake-up droop threshold, over full temperature range	Drop in V_{VDD} following a power-cycle detect by 40 ms, V_{VDD} falling from 28 V, dv/dt = –250 V/s	–2.3%	–2.7%	–3.2%	
$I_{WAKE(on)25}$	Wake-up drive current, room temperature	V_{WAKE} = 4 V, T_J = 25°C	20	27		mA
$I_{WAKELMT}$	Wake-up current limit	V_{VDD} = 28 V, V_{WAKE} = 28 V	35	48	60	mA
ENABLE SECONDARY CIRCUIT FUNCTION						
$I_{ENS(lkg)}$	ENS switch leakage current	V_{ENS} = 5 V, off-state		0	0.1	µA
$R_{ENS(RDS(on))}$	ENS switch on-resistance	I_{ENS} = 100 µA, on-state	1.3	2.7	5.0	kΩ

(1) Device parameter characterized during development. Not production tested, except at 25°C.
(2) For droop threshold at higher dv/dt, see *Typical Characteristics*.

6.6 Timing Requirements

over operating free-air temperature range, V_{VDD} = 5 V, V_{WAKE} = 5 V, –40°C ≤ T_A ≤ 125°C, T_J = T_A, (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_{PCD(min)}$	PCD minimum time for $V_{WAKE} < V_{PCD}$	350	500	650	ns
$t_{SW(max)}$	PCD maximum period for ΔV_{VDD}			40	ms

6.7 Switching Characteristics

over operating free-air temperature range, V_{VDD} = 5 V, V_{WAKE} = 5 V, –40°C ≤ T_A ≤ 125°C, T_J = T_A, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP FUNCTION						
t_{WAKE}	Wake-up pulse width	ΔV_{VDD} ≥ –5% after PCD	0.7	1	1.3	µs
$t_{WAKE(rep)}$	Wake-up repeat period	ΔV_{VDD} ≥ –5% after PCD	21	30	39	µs
ENABLE SECONDARY CIRCUIT FUNCTION						
t_{ENS} (1)	Qualifying t_{SW} to enable secondary circuit	WAKE input toggling	40	57	74	µs
N_{ENS}	Cumulative cycles to enable secondary circuit	$t_{SW} < t_{ENS}$	32			cycles
t_{DISS} (1)	Qualifying t_{SW} to disable secondary circuit	WAKE input toggling	124	177	230	µs
N_{DISS}	Consecutive cycles to disable secondary circuit	$t_{SW} > t_{DISS}$	63			cycles

(1) By design, the ratio of t_{ENS} to t_{DISS} remains within ±10% of typical, over all conditions. Not production tested.

6.8 Typical Characteristics

V_{VDD} = 5 V, V_{WAKE} = 5 V, T_A = 25°C, T_J = T_A, (unless otherwise noted)

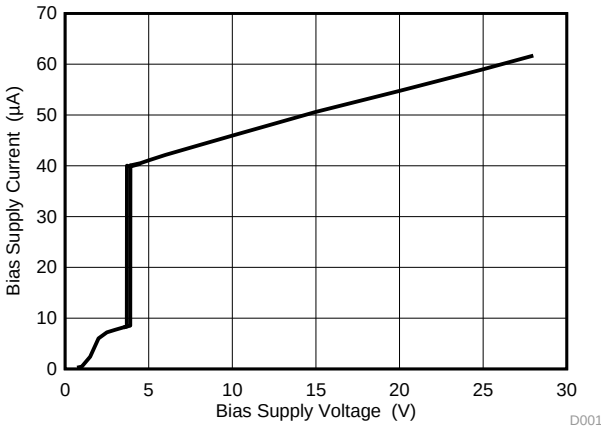


Figure 1. Bias Supply Current vs Bias Supply Voltage

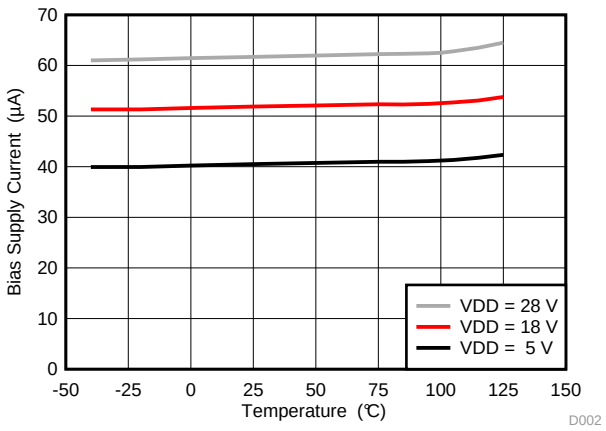


Figure 2. Bias Supply Current vs Temperature

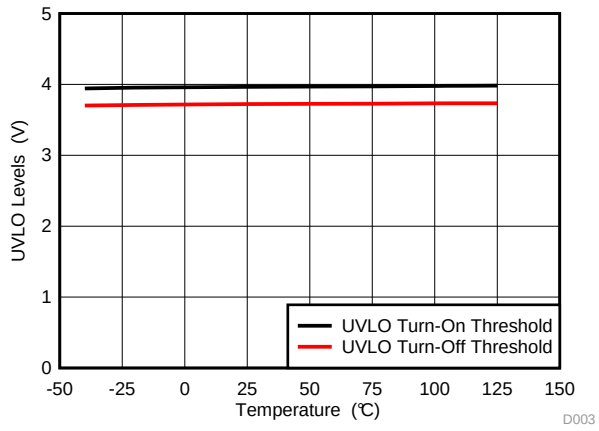
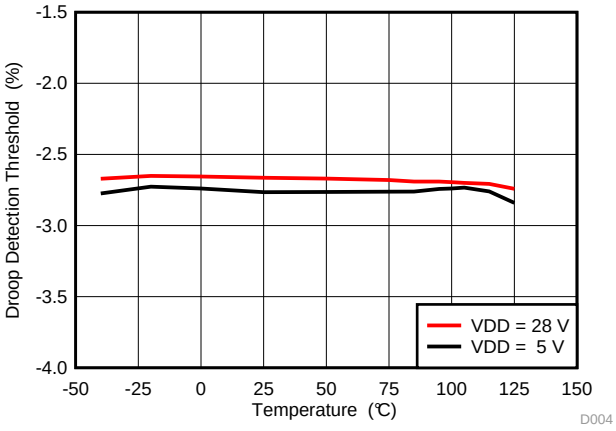


Figure 3. UVLO Thresholds vs Temperature



dv/dt = 250 V/s

Figure 4. Droop Detection Threshold vs Temperature

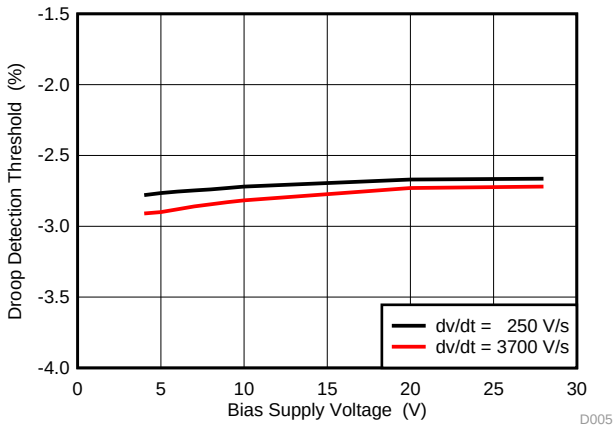


Figure 5. Droop Detection Threshold vs Bias Voltage

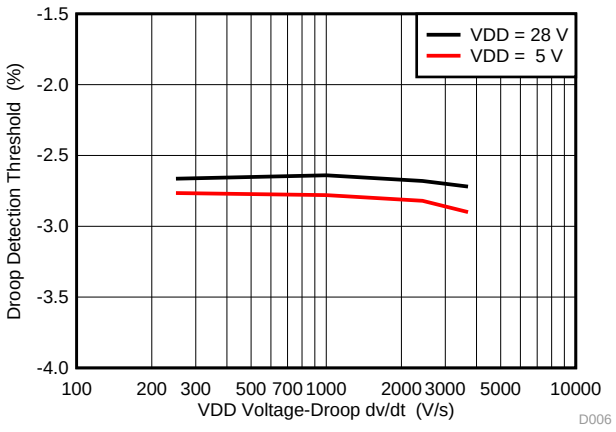
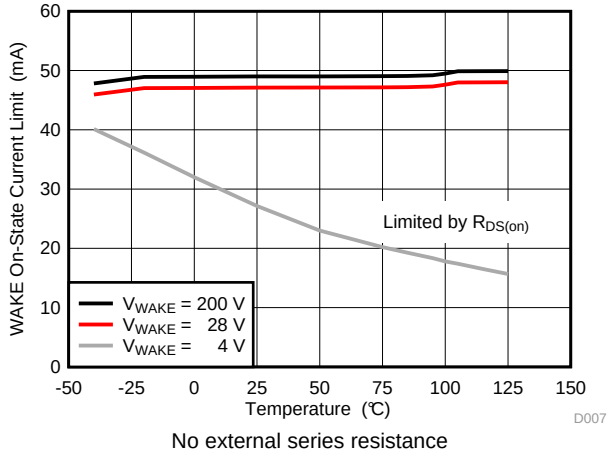


Figure 6. Droop Detection Threshold vs Droop dv/dt

Typical Characteristics (continued)

V_{VDD} = 5 V, V_{WAKE} = 5 V, T_A = 25°C, T_J = T_A, (unless otherwise noted)



No external series resistance

Figure 7. WAKE Current Limit vs Temperature

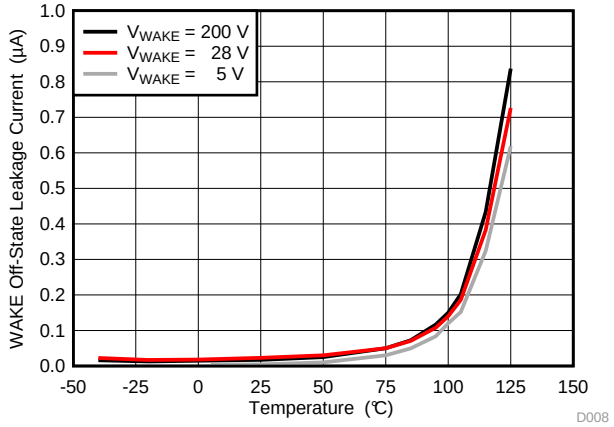


Figure 8. WAKE Leakage Current vs Temperature

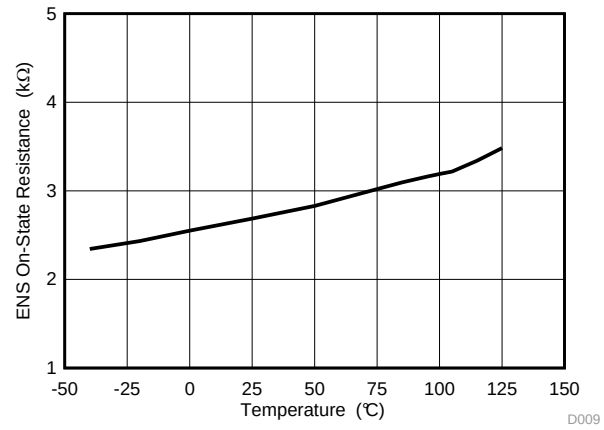


Figure 9. ENS On-Resistance vs Temperature

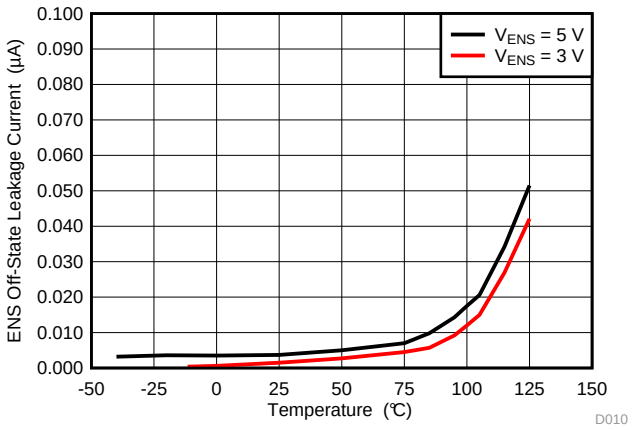


Figure 10. ENS Leakage Current vs Temperature

7 Detailed Description

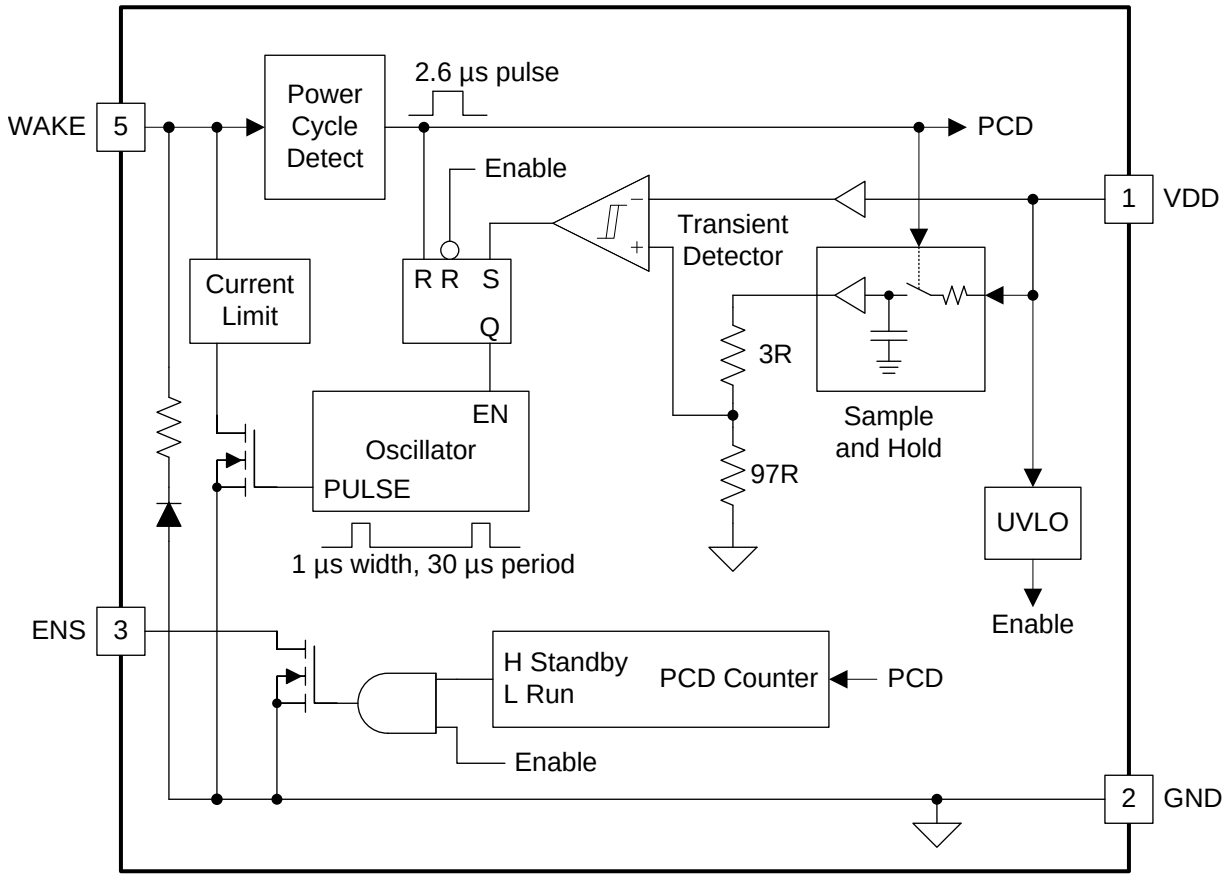
7.1 Overview

The UCC24650 is a voltage monitor designed to alert a companion primary-side controller device when the monitor detects a relative droop of approximately 3% on its VDD input. Commonly known as a *wake-up* device, the UCC24650 is normally used in isolated-flyback power supply applications using primary-side regulation (PSR). Because the PSR controller may operate at very-low frequencies during light-load or no-load conditions, it cannot detect a sudden load step that may occur between power cycles and the output voltage may fall out of regulation. The UCC24650 can detect the voltage droop and *wake-up* a compatible PSR controller to increase its switching frequency before the output falls too low. This action significantly reduces the amount of output capacitance needed to achieve an acceptable transient response.

At the end of each power cycle delivered by the PSR controller, the UCC24650 droop monitor refreshes an internally stored voltage scaled to 97% of the VDD voltage. If the monitor detects a droop of VDD to the level of the stored voltage, the WAKE signal is connected to GND by an internal low-impedance switch. The WAKE signal transmits a current pulse across the isolation transformer to a compatible PSR controller, such as the UCC28730, capable of detecting the *wake-up* signal on the primary side of the transformer.

The UCC24650 is also capable of disabling a compatible SR controller, such as the UCC24610, during light-load conditions to minimize standby power. The ENS output signal is driven *low* after a fixed sustained count of low-frequency power pulses, and can re-enable the SR controller after a cumulative count of 32 higher-frequency power pulses. The ENS output may also be used to drive other secondary circuitry compatible with the ENS operating parameters.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 UVLO Block

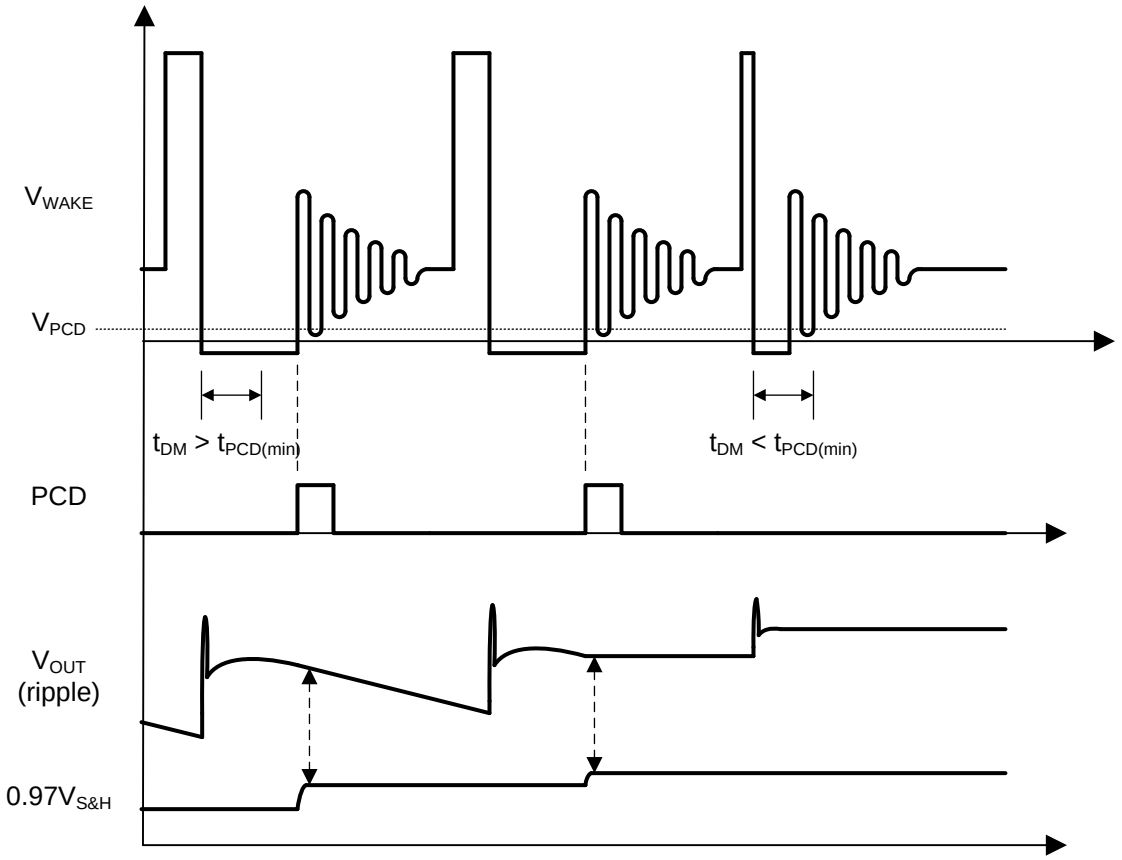
The UCC24650 device can operate over a bias supply voltage range from approximately 4 to 28 V. All functions are disabled and bias supply current is quiescent until the UVLO turn-on threshold is exceeded. When enabled, all functions remain operational until the VDD voltage falls below the UVLO turn-off threshold.

To ensure that *wake-up* pulses can be successfully driven, make sure the output voltage droop at VDD during a load-step does not fall below the maximum UVLO turn-off threshold before at least one *wake-up* pulse can be issued. This imposes a practical limit on the lowest nominal no-load voltage allowable at VDD before the maximum load step is applied.

7.3.2 PCD

After the UCC24650 has been turned on and enabled, the WAKE pin is used to detect the power-cycle waveforms at the flyback transformer secondary winding. This winding voltage can be at wide-ranging levels, but the PCD block arms the sample-and-hold (S&H) block to acquire a reference voltage reading at VDD when certain criteria are met. The PCD block triggers the S&H block at the end of the demagnetization time, t_{DM}, provided that the voltage at WAKE has remained below the V_{PCD} threshold for longer than $t_{PCD(min)}$, to ensure that the sampled voltage is free of transient deviations and noise. Consequently, this imposes a minimum demagnetization-time constraint on the flyback design to provide adequate signal for the PCD function.

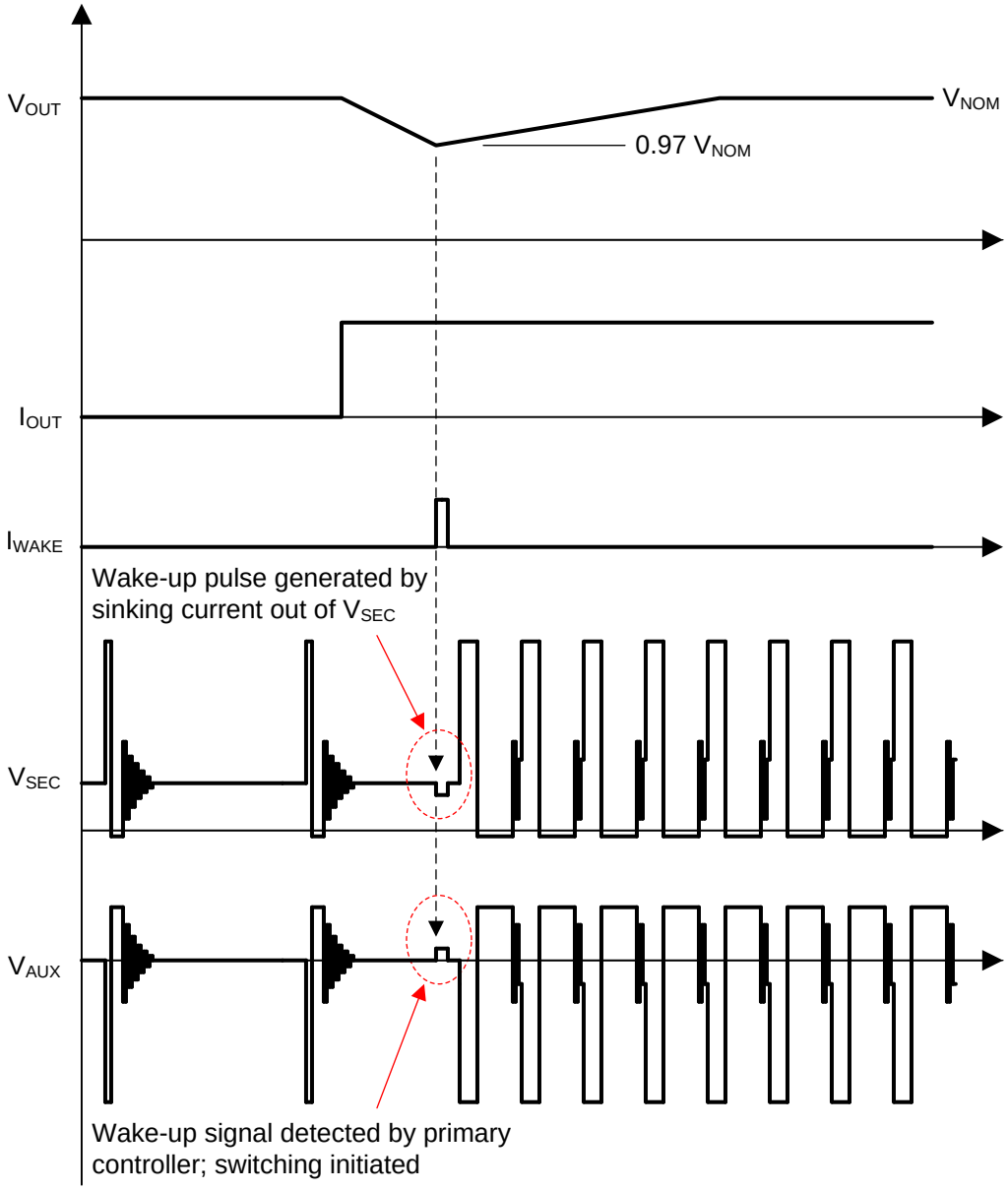
Figure 11 illustrates the behavior of the device for power-cycles that do meet the criteria and for those that do not. The *wake-up* reference voltage, which is stored internally as approximately 97% of the sampled VDD voltage, is updated at every PCD pulse to change proportionally with the changes in output voltage. Disturbances at the WAKE input which do not meet the PCD criteria do not affect the stored reference voltage.



A. Not to scale

Figure 11. Timing Diagram of Internal PCD Signal

Feature Description (continued)



A. Not to scale

Figure 12. Simplified Timing Diagram of System Behavior

7.3.3 Sample, Hold, and Transient Detector

The sample-and-hold function (S&H) monitors the VDD voltage, samples that voltage during a PCD pulse, and holds the buffered sample constant during the interval between power cycles. The held sample is scaled to about 97% of the external voltage to serve as a –3% droop-detection threshold reference voltage. The external VDD voltage is continually compared to the internal droop reference by the transient detection comparator, and a *wake-up* signal is triggered if VDD falls below the droop-reference voltage.

The S&H droop-reference voltage is refreshed at the end of each power cycle detected by the PCD function, to track minor changes in output voltage. The droop-reference voltage is held accurately for PCD intervals less than $t_{SW(max)}$, but may drift either higher or lower during longer intervals.

Feature Description (continued)

7.3.4 Wake Pulse Generator and WAKE Switch

The WAKE pin not only functions as a PCD input as described in *PCD*, but also serves as an output driver to accomplish the *wake-up* function. An integrated N-channel MOSFET switch is connected between WAKE and GND and is driven by the WAKE-pulse oscillator when the conditions for *wake-up* are met (see *Functional Block Diagram*). Each *wake-up* pulse is of short duration to limit internal dissipation and is repeated periodically until a PSR-driven power cycle is detected or until VDD has fallen to the UVLO turn-off threshold.

Figure 13 shows two possible typical system responses. The solid lines indicate the successful *wake-up* of a compatible PSR controller from the *sleeping* or *Wait* state between low-frequency power cycles. After a load step causes the output voltage (at VDD) to cross the previously stored reference voltage, the WAKE output drives a current pulse to the PSR controller which responds with multiple power cycles to restore regulation. At each power cycle, the reference voltage is refreshed and further WAKE pulses are suppressed. In the case where the PSR controller does not respond to the first *wake-up* pulse, the dotted lines indicate that the *wake-up* pulses are repeated, the reference voltage is not refreshed, and the output voltage continues to fall.

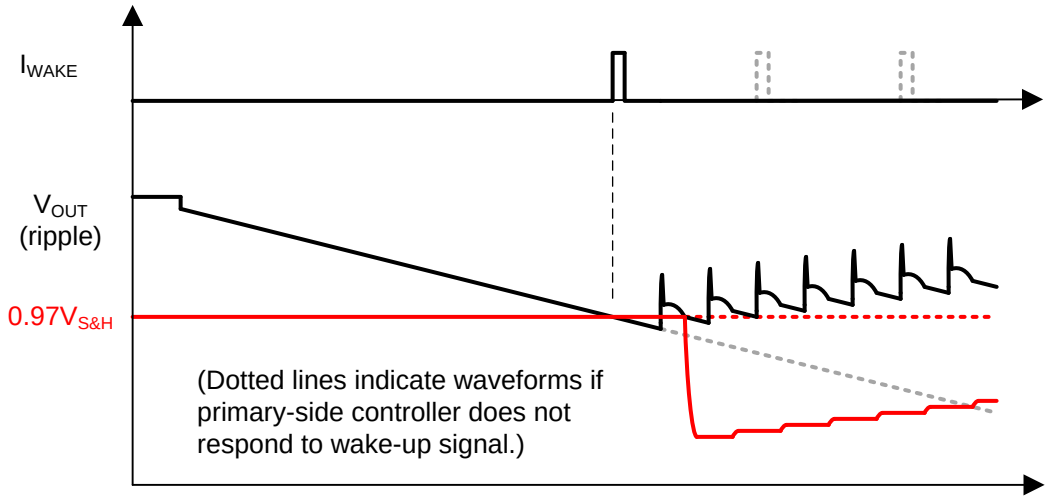


Figure 13. System Response to Wake-Up Signal After Load-Transient Event

In the event that a power cycle occurs during the droop before V_{OUT} has reached the WAKE threshold, the S&H reference is updated to the V_{OUT} voltage at that moment. This may extend the droop by another 3% before the WAKE threshold is reached and the condition for a *wake-up* signal is met, effectively delaying the *wake-up* as illustrated by Figure 14 and Figure 15.

Feature Description (continued)

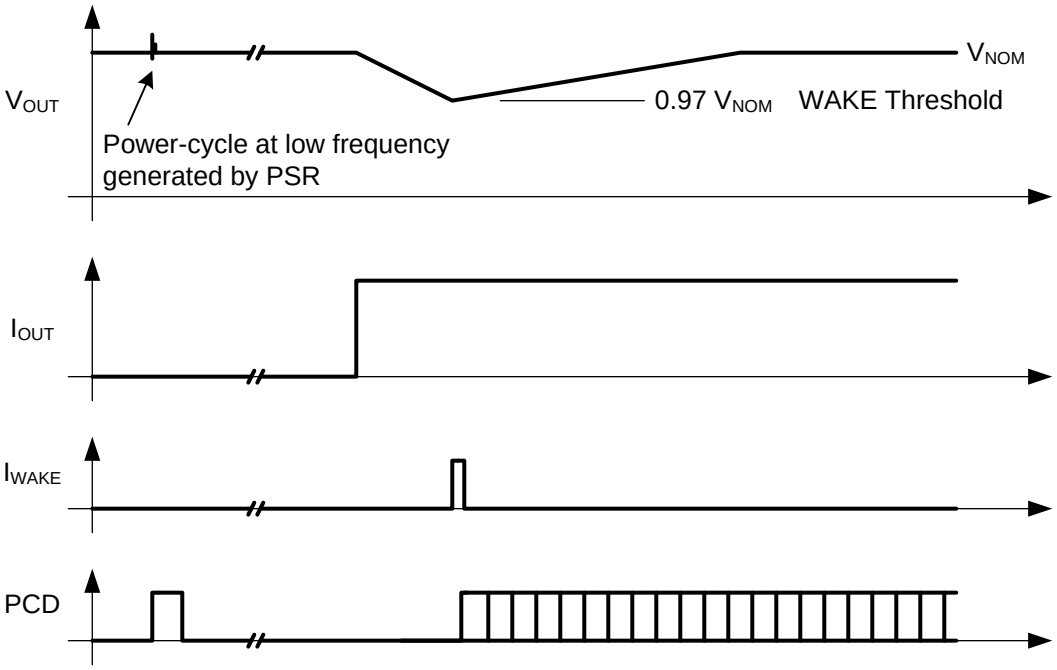


Figure 14. Simplified Typical System Response to Wake-Up Signal After Load-Transient Event

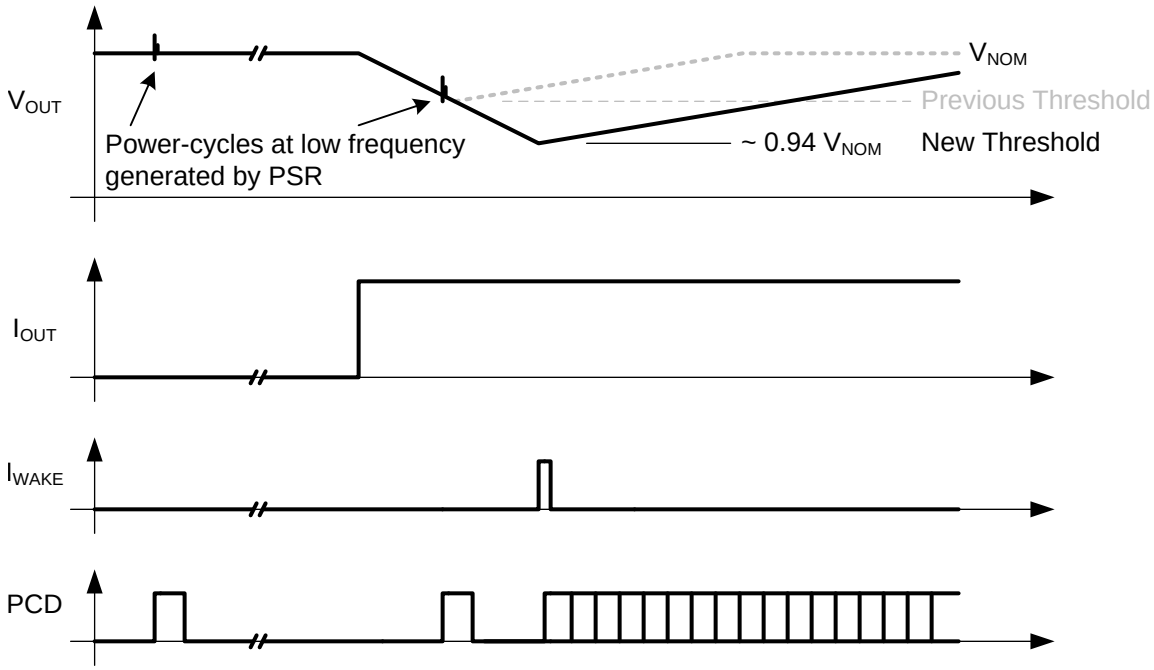


Figure 15. Simplified Delayed System Response to Wake-Up Signal After Load-Transient Event

The typical on-state resistance of the WAKE switch is approximately 150 Ω at 25°C and varies with junction temperature. Consequently, the wake-pulse current capability in low-voltage applications also varies with temperature (see Figure 7 in the *Typical Characteristics*). A built-in current limit prevents excess pulse current and power dissipation in higher-voltage applications.

Feature Description (continued)

In a typical isolated-flyback PSR topology, the wake-pulse current establishes a signal voltage across the system impedance, which consists mainly of the parallel combination of the primary magnetizing inductance, L_M, and the switched-node capacitance, C_{SWN}, scaled by the transformer turns-ratio.

In applications with higher output voltages, some rectifier diodes may exhibit high forward voltage drop characteristics, along with possible additional voltage due to package inductance and stray inductance. This negative forward voltage is impressed on the WAKE input with respect to GND, as shown in Figure 16.

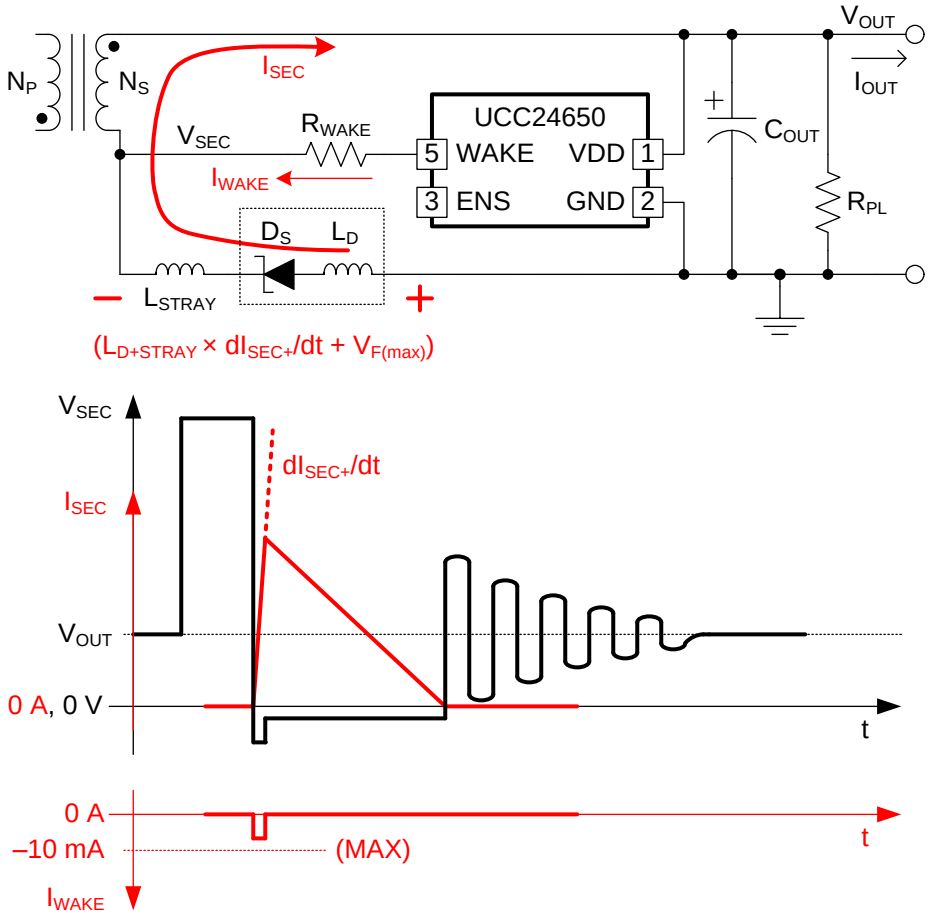


Figure 16. High dI_{SEC}/dt may Generate Significant I_{WAKE}.

To avoid exceeding the maximum source-current rating for WAKE (see *Absolute Maximum Ratings*), a series resistance may be required to limit the WAKE current. Its value is calculated by Equation 1. However, this resistance presents additional impedance to the WAKE signal current that can be developed. Do not oversize R_{WAKE} to avoid depressing the *Wake-Up* signal level at the PSR detection input. A trade-off between the level of reverse-current limiting and the WAKE signal drive level may be necessary.

$$R_{WAKE} \geq \frac{\left(V_{F(max)} + L_{SUM} dI_{SEC+} / dt\right) - 0.7\ V}{10\ mA} \quad (1)$$

where

- $V_{F(max)}$ is the highest forward voltage drop expected.
- L_{SUM} is the combined stray and package inductance.

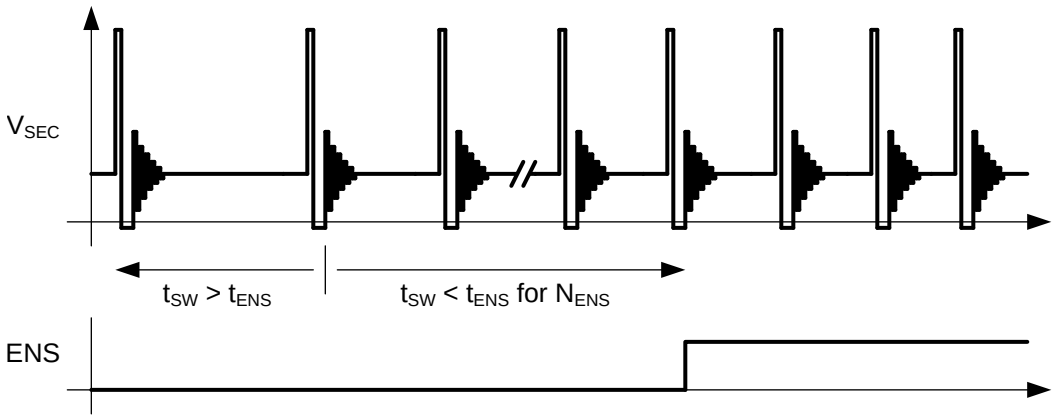
Feature Description (continued)

7.3.5 PCD Counter and ENS Switch

Some PSR applications may use an SR in place of the output diode rectifier to improve efficiency. For applications using the UCC24610 SR controller, the UCC24650 device provides the ENS output which can be used to enable the SR controller when the switching frequency is high, and disable it when the switching frequency is very low, to reduce standby power dissipation. Although the ENS function is specifically optimized for use with the UCC24610 device, it may also be used for other purposes provided the ENS pin is operated within its specified limits.

The ENS output consists of an open-drain, N-channel MOSFET switch with on-resistance of approximately 2.7 kΩ at 25°C. A PCD counter (see *Functional Block Diagram*) monitors the time intervals between pulses and determines whether to turn on or off the ENS switch. At power-up, the ENS switch is off (high-impedance open-drain state) by default, and remains that way as long as the power-cycle period, t_{SW}, is less than the disable qualifying interval, t_{DISS}, to keep the SR controller enabled. After $t_{SW} > t_{DISS}$ for a count of at least 63 consecutive power cycles, the ENS switch is turned on (low-impedance to GND) to disable the SR controller. This disable-count is reset to zero if any switching cycle period occurs where $t_{SW} < t_{DISS}$. This consecutive count requirement ensures that the switching frequency is consistently low enough to justify disabling the SR controller to minimize its bias power.

There is considerable hysteresis in the qualifying interval timing, so the ENS switch remains on (SR or other secondary circuit is disabled) until t_{SW} becomes less than the enable qualifying interval, t_{ENS}. In other words, the switching frequency is increasing. When $t_{SW} < t_{ENS}$ for 32 cumulative power cycles, the ENS switch is turned off and the SR controller is enabled. When ENS is in the *Low* state, the cumulative count allows any number of switching cycles with $t_{SW} > t_{ENS}$ without resetting the count. Figure 17 and Figure 18 show these ENS state transitions based on the switching period timing and interval count.

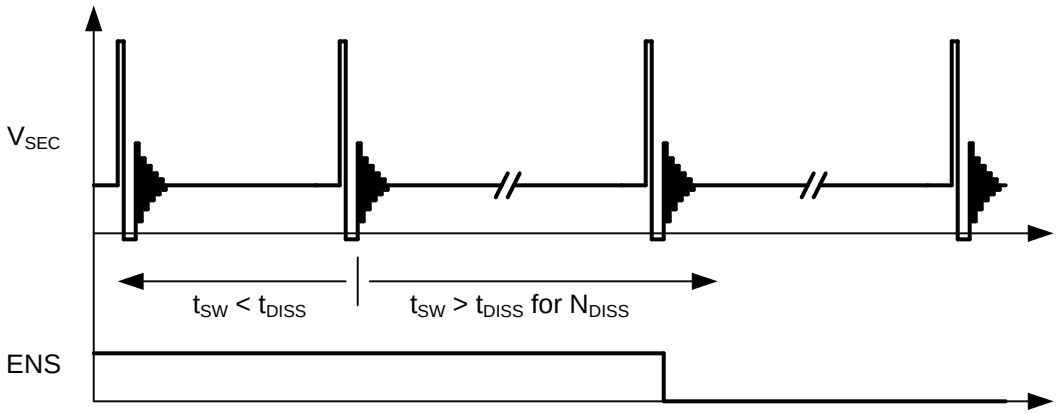


A. Not to scale

Figure 17. Simplified Timing Diagram of ENS Behavior for Gradual Increase of Load

Only 32 shorter t_{SW} intervals are necessary to re-enable the SR controller to avoid excess rectifier dissipation as the system load increases. However, these shorter intervals (higher frequency) are not required to be consecutive, so that ENS is allowed to toggle *High* eventually, even if the switching frequency is not yet consistently higher. This method ensures that the SR or other circuitry is not prevented from re-enabling if the frequency is not consistent due to variable loads.

Feature Description (continued)



A. Not to scale

Figure 18. Simplified Timing Diagram of ENS Behavior for Gradual Decrease of Load

At least 63 consecutive counts of $t_{SW} > t_{DISS}$ are necessary to disable the SR controller, to ensure that random deviations in t_{SW} do not unnecessarily disrupt normal SR operation. In this manner, the ENS function is heavily skewed in favor of keeping the SR controller enabled, unless it is consistently operated at a very-low frequency, particularly during no-load operation. ENS is not affected in the case of a *wake-up* event, and the count is not changed. After a *wake-up*, the switching frequency generally increases quite rapidly, so the ENS switch is turned off to re-enable the SR controller as soon as the count of $t_{SW} < t_{ENS}$ reaches 32. Depending on the previous cumulative switching period history, the time to re-enable the SR controller may be anywhere between 32 switching cycles and immediate.

7.4 Device Functional Modes

The UCC24650 operates as a voltage monitor in either of two modes: ENS output is *High* (driver is off), or ENS output is *Low* (driver is on). In either mode, when the monitor detects a 3% droop in the VDD voltage, it triggers a *Wake-Up* signal on the WAKE pin.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC24650 *Wake-Up* monitor is intended to be used with the UCC28730 PSR controller in off-line isolated DCM flyback converters. The UCC24650 signals the UCC28730 that the output voltage has drooped. This allows the PSR controller to react to a load increase even while operating at extremely-low switching frequencies. This pair of devices also operates at very-low bias currents to facilitate the achievement of <5 mW of input power consumption during the no-load operating condition.

8.2 Typical Application

A typical application for the UCC24650 uses the compatible UCC28730 PSR controller to regulate an isolated low-voltage DC output from a high-voltage AC source. As shown in Figure 19 and Figure 20, the output rectification can use a ground-referenced diode, or a ground-referenced synchronous rectifier, respectively.

NOTE

These figures are simplified to illustrate the basic application of the UCC24650 and do not show all of the components and networks needed for an actual converter design.

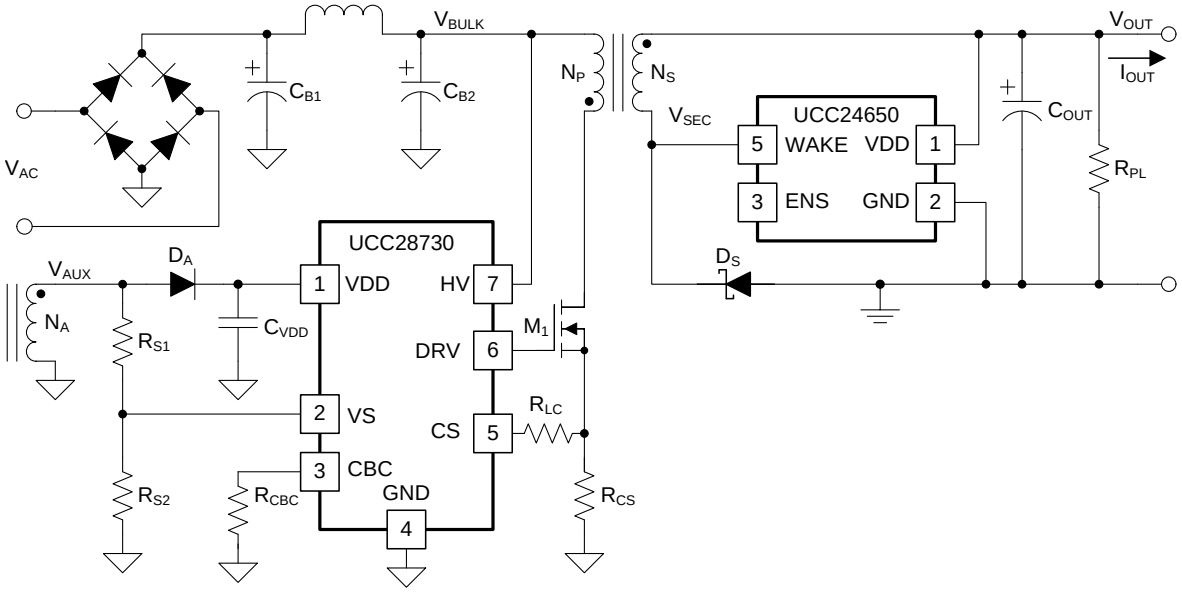


Figure 19. Simplified Application With Ground-Referenced Diode

Typical Application (continued)

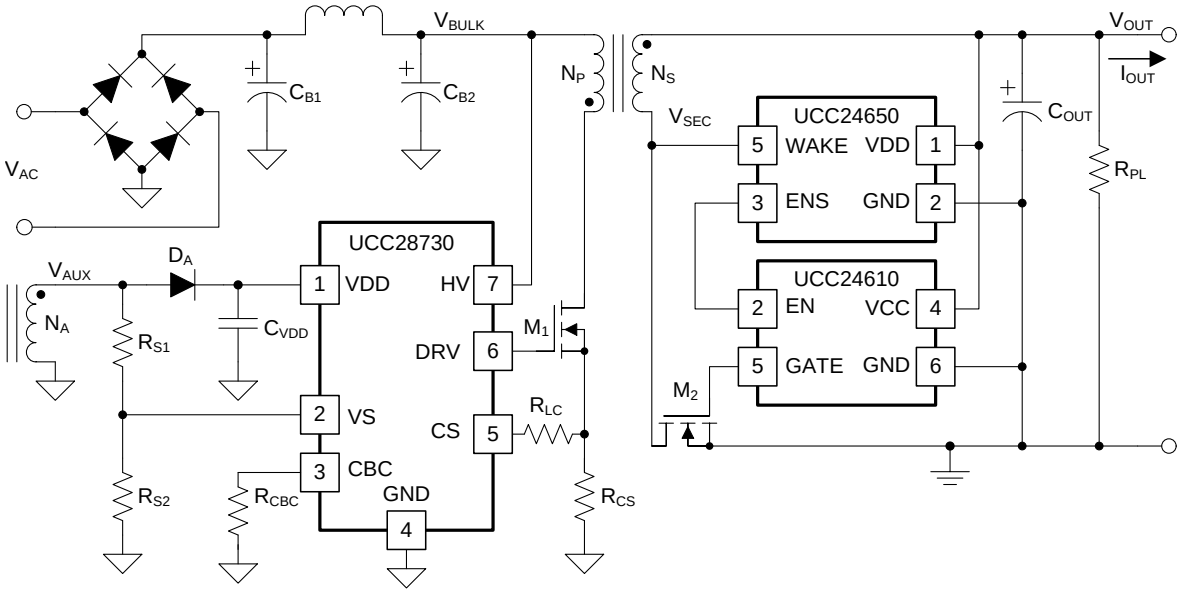


Figure 20. Simplified Application With Ground-Referenced Synchronous Rectifier

8.2.1 Design Requirements

Among the usual converter design requirements, the UCC24650 is especially suited to aid in achieving fast load-transient response and extremely-low input standby power. In many cases, the designer can achieve <5 mW of standby power, often referred to as *Zero-Power*.

8.2.2 Detailed Design Procedure

There is little design work required to use this device. Most calculations involve verification that the external conditions remain within the device's various parameter operating limits.

Major design items to cover are:

- Ensure sufficient margin between lowest droop expected and the device UVLO threshold. The UVLO threshold is approximately 3.75 V and the compatible PSR controller usually requires some short time to respond to the WAKE signal and arrest the load-step droop. The minimum regulation voltage compatible with the use of this device must account for the anticipated droop plus any additional droop due to threshold reset and PSR response limitations.
- Ensure the maximum switching period $t_{SW(max)}$ is not exceeded, or the droop threshold may drift lower or higher and become inaccurate.
- Ensure the system-level V_{OUT} overshoot remains below the device VDD absolute maximum rating.
- Ensure the system-level V_{SEC} spike overshoot remains below the device WAKE absolute maximum rating.
- Ensure the system switched-node impedance allows sufficient signal amplitude so that the PSR controller is able to detect it. If necessary, a PNP emitter-follower buffer may be inserted between the WAKE pin and the secondary winding to boost the *wake-up* signal current level.
- Determine WAKE series resistance to limit current out of terminal, if necessary.

Typical Application (continued)

8.2.3 Application Curves

The following figures indicate the transient response of a 5-V, 10-W flyback converter which receives a pulsed step-load of 2 A while operating in the no-load standby condition. Figure 24 indicates the no-load standby input power consumption achieved by this converter over the full AC input range. *Zero-Power* operation is achieved while retaining fast transient response to a full load step.

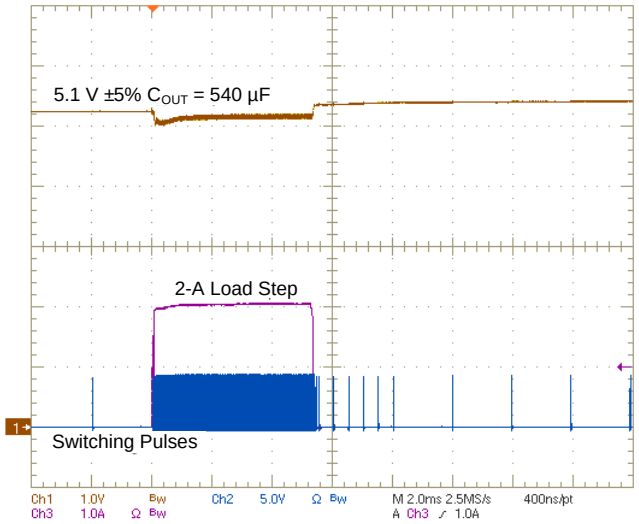


Figure 21. 2-A Load Step During Standby Operation

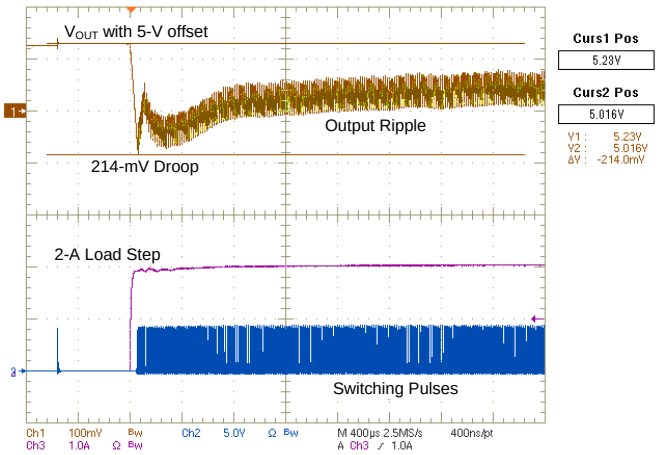


Figure 22. Transient Response Detail for 2-A Load Step

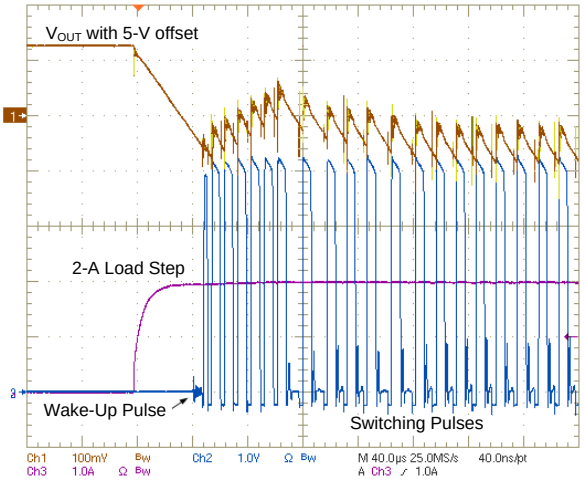


Figure 23. Wake-Up Pulse Triggering Response from UCC28730 Primary-Side Controller

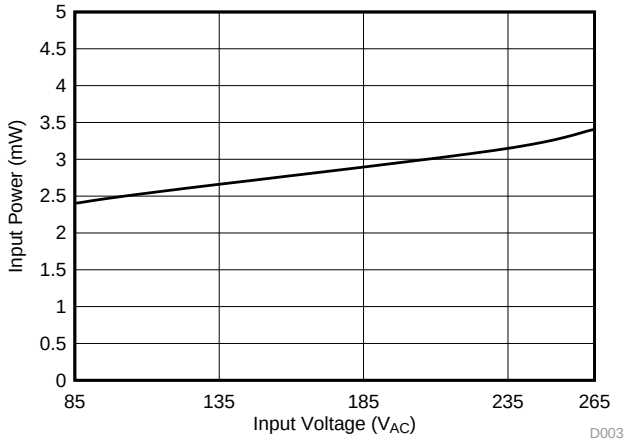


Figure 24. No-Load Input Power Consumption for a 5-V, 10-W Converter

9 Power Supply Recommendations

The VDD pin of the UCC24650 is intended to connect directly to the output voltage of a PSR-flyback converter in the range of 5 to 28 V. Because the device monitors VDD to detect a 3% droop to trigger the *wake-up* function, the converter output voltage should be sufficiently filtered to avoid false trigger from excessive steady-state ripple voltage, relative to the output voltage. The UCC24650 captures its reference voltage at the end of each flyback demagnetization time to avoid the influence of ringing and switching noise. Converter output capacitance should be sufficient to maintain ΔV_{OUT} between switching cycles to less than the droop detection threshold.

Avoid an excessive rate of rise on VDD to ensure correct device operation. Ensure that the dv/dt <0.1 V/µs on VDD, or the device may not function until power is removed and restored at a slower rate.

10 Layout

10.1 Layout Guidelines

There are no critical layout requirements. TI recommends to use the usual industry good-practice layout guidelines and principles.

To increase the reliability and feasibility of the project, TI recommends adhering to the following guidelines for PCB layout:

- Connect the WAKE and GND signals close to the output rectifier pads to minimize the effect of high di/dt and stray inductance on the WAKE pin voltage at the beginning of the flyback demagnetization time. It is not so important to minimize the WAKE and GND sense track lengths, rather to minimize the inductance between the two sense points at the rectifier.
- If ENS is not used, connect it to the GND pin to prevent the ENS input voltage from going below GND due to possible system noise.

10.2 Layout Example

The partial layout example of Figure 25 demonstrates an effective component and track arrangement for low-noise operation on a single-layer PCB. Actual board layout must conform to the constraints on a specific design, so many variations are possible.

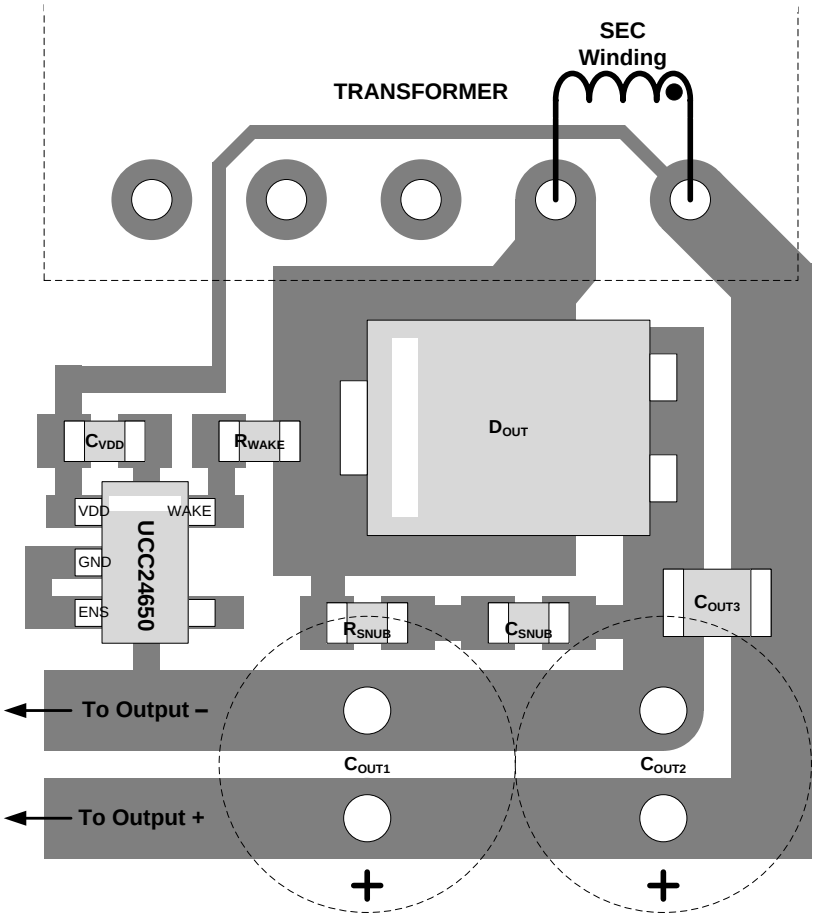


Figure 25. UCC24650 Partial Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

- *《UCC28730 具有 CVCC 和唤醒监视功能的零功耗待机 PSR 反激控制器》*，SLUSBL5
- 《UCC28730EVM-552 EVM 用户指南，*使用 UCC28730EVM-552*》，SLUUB75

11.2 商标

All trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC24650DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U650
UCC24650DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U650
UCC24650DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U650
UCC24650DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U650

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

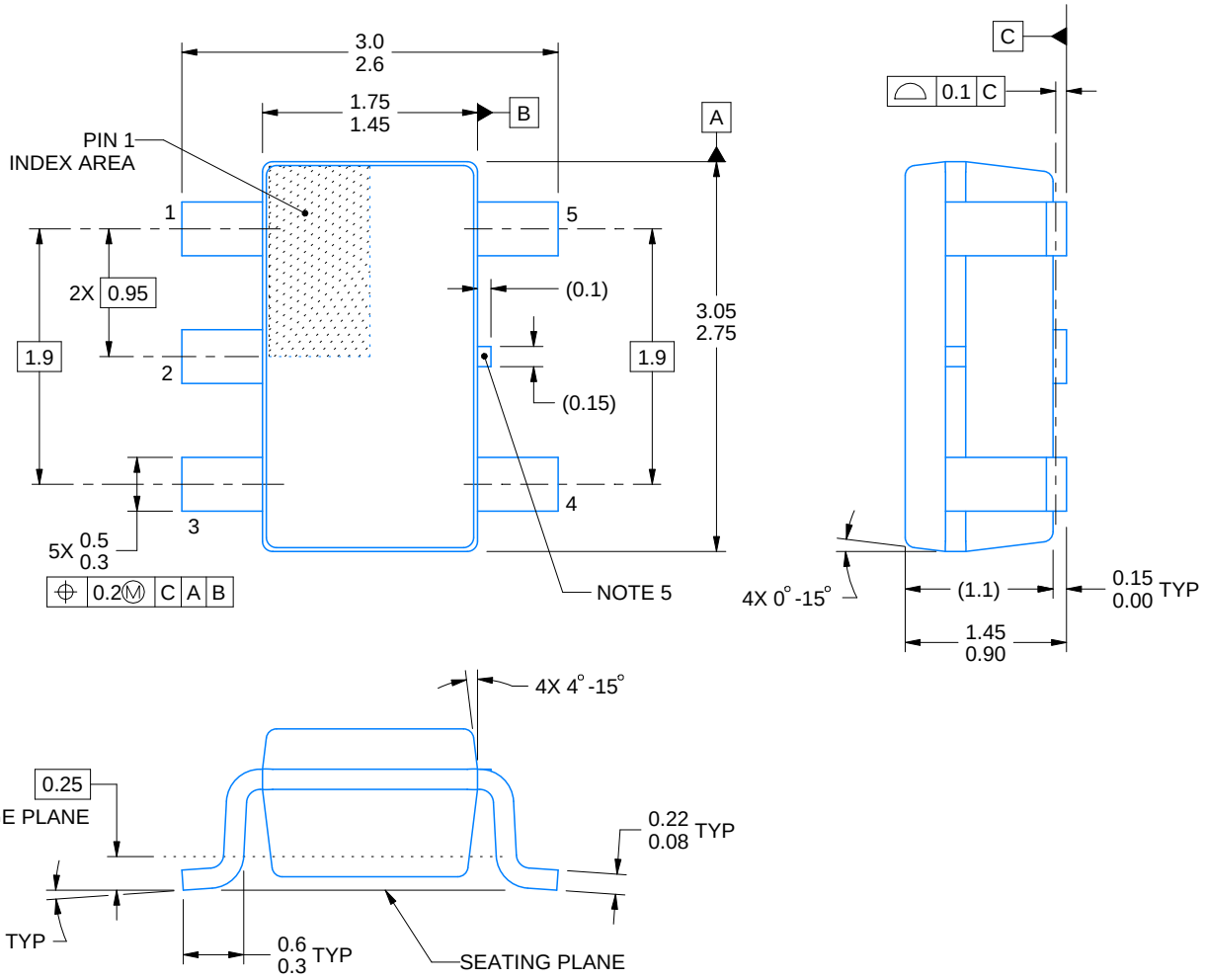
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

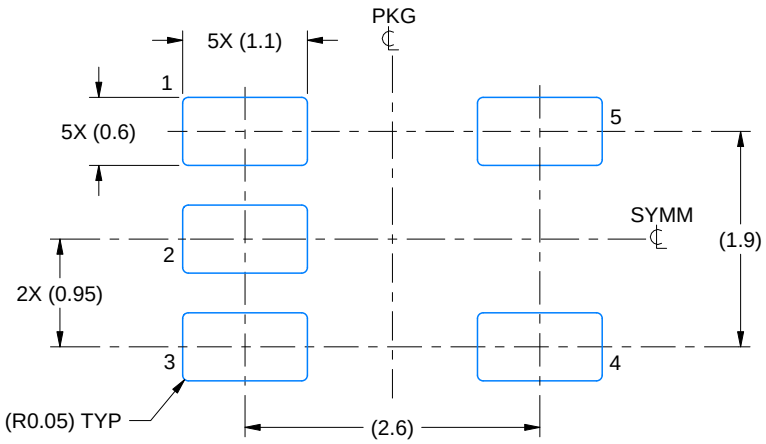
SMALL OUTLINE TRANSISTOR



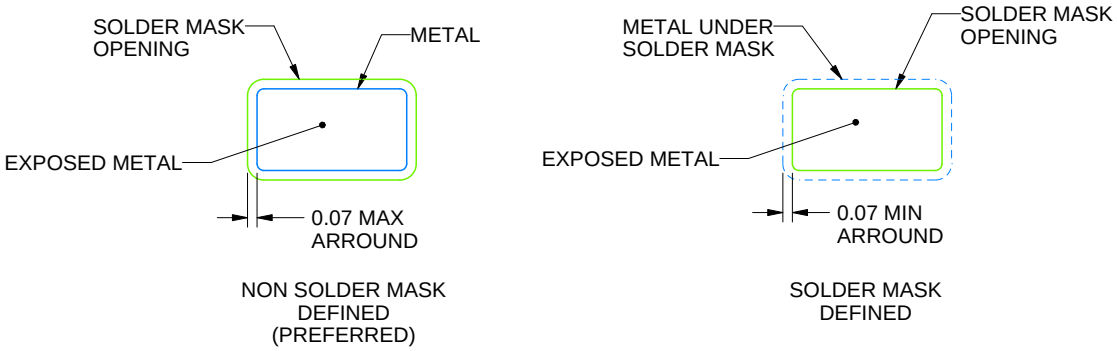
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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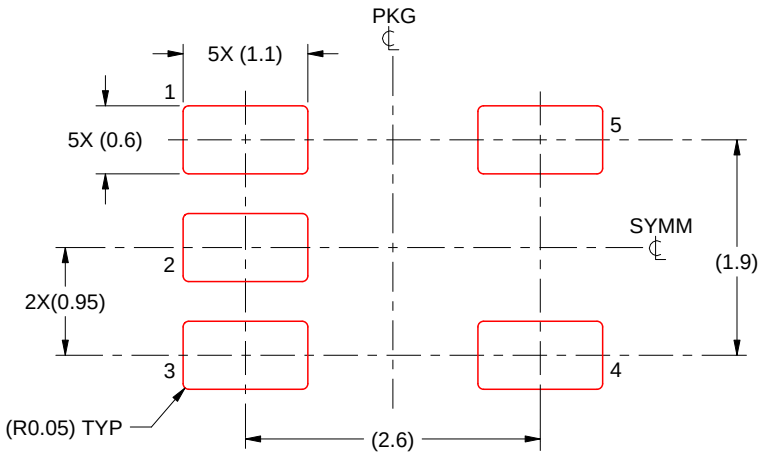
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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