

UCC21717-Q1 适用于 SiC/IGBT 并具有主动保护、隔离式模拟检测和高 CMTI 的汽车类 10A 拉电流/灌电流增强型隔离式单通道栅极驱动器

1 特性

- 5.7kV_{RMS} 单通道隔离式栅极驱动器
- 符合面向汽车应用的 AEC-Q100 标准
 - 器件温度等级 1：-40°C 至 +125°C 环境温度工作温度范围
- **功能安全质量管理型**
 - 可提供用于功能安全系统设计的文档
- 高达 2121V_{pk} 的 SiC MOSFET 和 IGBT
- 33V 最大输出驱动电压 (VDD-VEE)
- ±10A 驱动强度和分离输出
- 150V/ns 最小 CMTI
- 具有 270ns 快速响应时间的过流保护
- 4A 内部有源米勒钳位
- 在故障条件下提供 400mA 软关断
- 具有 PWM 输出的隔离式模拟传感器
 - 采用 NTC、PTC 或热敏二极管的温度感应
 - 高电压直流链路或相电压
- 过流警报 FLT 和通过 RST/EN 重置
- 使用 RST/EN 禁用器件会触发软关断
- 抑制输入引脚上小于 40ns 的噪声瞬态和脉冲
- RDY 上的 12V VDD UVLO (具有电源正常指示功能)
- 具有高达 5V 过冲/欠冲瞬态电压抗扰度的输入/输出
- 130ns (最大) 传播延迟和 30ns (最大) 脉冲/器件间偏移
- SOIC-16 DW 封装, 爬电距离和间隙 > 8mm
- 工作结温范围: -40°C 至 150°C

2 应用

- 适用于 EV 的牵引逆变器
- 车载充电器和充电桩
- 用于 HEV/EV 的直流/直流转换器

3 说明

UCC21717-Q1 是一款电隔离单通道栅极驱动器, 设计用于驱动高达 1700V 的 SiC MOSFET 和 IGBT。它具有先进的集成保护特性、出色的动态性能和稳健性。UCC21717-Q1 具有高达 ±10A 的峰值拉电流和灌电流。

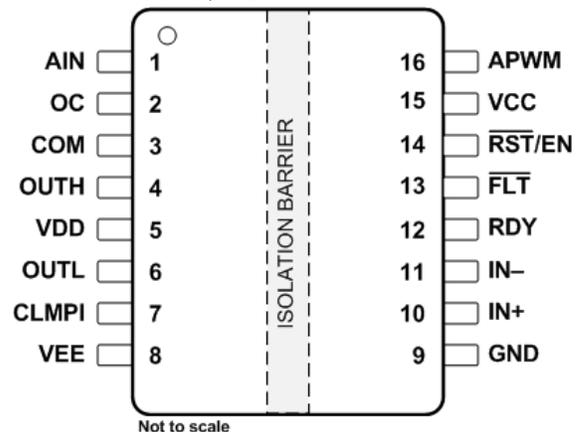
输入侧通过 SiO₂ 电容隔离技术与输出侧相隔离, 支持高达 1.5kV_{RMS} 的工作电压、12.8kV_{PK} 的浪涌抗扰度, 隔离栅寿命超过 40 年, 并提供较低的器件间偏斜, 共模噪声抗扰度 (CMTI) 大于 150V/ns。

UCC21717-Q1 包括先进的保护特性, 如快速过流和短路检测、分流电流检测支持、故障报告、有源米勒钳位、输入和输出侧电源 UVLO (用于优化 SiC 和 IGBT 开关行为) 和稳健性。可以利用隔离式模拟至 PWM 传感器更轻松地进行温度或电压感测, 从而进一步提高驱动器的多功能性并简化系统设计工作量、尺寸和成本。

器件信息

| 器件型号 | 封装 ⁽¹⁾ | 本体封装尺寸 (标称值) |
|-------------|-------------------|----------------|
| UCC21717-Q1 | DW (SOIC, 16) | 10.3mm × 7.5mm |

(1) 有关所有可用封装, 请参阅节 13。



器件引脚配置



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4 Pin Configuration and Functions

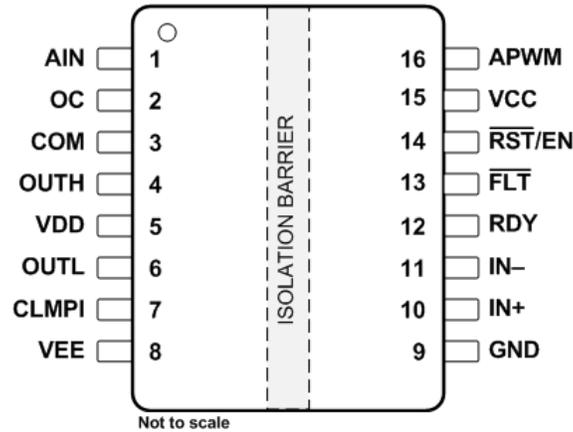


图 4-1. UCC21717-Q1 DW Package SOIC 16 Pins Top View

表 4-1. Pin Functions

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|--------|-----|--------------------|---|
| NAME | NO. | | |
| AIN | 1 | I | Isolated analog sensing input, parallel a small capacitor to COM for better noise immunity. Tie to COM if unused. |
| OC | 2 | I | Over current detection pin, support lower threshold for SenseFET, DESAT, and shunt resistor sensing. Tie to COM is unused. |
| COM | 3 | P | Common ground reference, connecting to emitter pin for IGBT or source pin for SiC-MOSFET |
| OUTH | 4 | O | Gate driver output pull up |
| VDD | 5 | P | Positive supply rail for gate drive voltage, Bypassing a >10- μ F capacitor to COM to support specified gate driver source peak current capability. Place decoupling capacitor close to the pin. |
| OUTL | 6 | O | Gate driver output pull down |
| CLMPI | 7 | O | Internal Active miller clamp, connecting this pin directly to the gate of the power transistor. Leave floating or tie to VEE if unused. |
| VEE | 8 | P | Negative supply rail for gate drive voltage. Bypassing a >10- μ F capacitor to COM to support specified gate driver sink peak current capability. Place decoupling capacitor close to the pin. |
| GND | 9 | P | Input power supply and logic ground reference |
| IN+ | 10 | I | Non-inverting gate driver control input. Tie to VCC if unused. |
| IN - | 11 | I | Inverting gate driver control input. Tie to GND if unused. |
| RDY | 12 | O | Power good for VCC-GND and VDD-COM. RDY is open drain configuration and can be paralleled with other RDY signals |
| FLT | 13 | O | Active low fault alarm output upon over current or short circuit. FLT is in open drain configuration and can be paralleled with other faults |
| RST/EN | 14 | I | The RST/EN serves two purposes: 1) Enable soft shutdown of the output side. The output is turned off by a soft turn off (STO) if EN is set to low; 2) Resets the OC condition signaled on FLT pin if terminal RST/EN is set to low for more than 1000ns. A reset of signal FLT is asserted at the rising edge of terminal RST/EN. For automatic RESET function, this pin only serves as an EN pin. Enable / shutdown of the output side. The FET is turned off by a soft turn-off, if terminal EN is set to low. |
| VCC | 15 | P | Input power supply from 3V to 5.5V, bypassing a >1- μ F capacitor to GND. Place decoupling capacitor close to the pin. |
| APWM | 16 | O | Isolated Analog Sensing PWM output. Leave floating if unused. |

(1) P = Power, G = Ground, I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-------------------------------------|--|-----------|---------|------|
| VCC | VCC - GND | - 0.3 | 6 | V |
| VDD | VDD - COM | - 0.3 | 36 | V |
| VEE | VEE - COM | - 17.5 | 0.3 | V |
| V _{MAX} | VDD - VEE | - 0.3 | 36 | V |
| IN+, IN-, RST/EN | DC | GND - 0.3 | VCC | V |
| | Transient, less than 100 ns ⁽²⁾ | GND - 5.0 | VCC+5.0 | V |
| AIN | Reference to COM | - 0.3 | 5 | V |
| OC | Reference to COM | - 0.3 | 6 | V |
| OUTH, OUTL, CLMPI | DC | VEE - 0.3 | VDD | V |
| | Transient, less than 100 ns ⁽²⁾ | VEE - 5.0 | VDD+5.0 | V |
| RDY, FLT, APWM | | GND - 0.3 | VCC | V |
| I _{FLT} , I _{RDY} | FLT and RDY pin input current | | 20 | mA |
| I _{APWM} | APWM pin output current | | 20 | mA |
| T _J | Junction Temperature | - 40 | 150 | °C |
| T _{stg} | Storage Temperature | - 65 | 150 | °C |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
- (2) Values are verified by characterization on bench.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±4000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1500 | |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|----------------------|--|---------|---------|------|
| VCC | VCC-GND | 3 | 5.5 | V |
| VDD | VDD-COM | 13 | 33 | V |
| VEE | VEE-COM | -16 | 0 | V |
| V _{MAX} | VDD-VEE | | 33 | V |
| IN+, IN-, RST/EN | Reference to GND, High level input voltage | 0.7xVCC | VCC | V |
| | Reference to GND, Low level input voltage | 0 | 0.3xVCC | V |
| AIN | Reference to COM | 0.6 | 4.5 | V |
| t _{RST/EN} | Minimum pulse width that reset the fault | 1000 | | ns |
| t _{RST/STO} | Minimum pulse width that triggers STO | 5 | | µs |
| T _A | Ambient temperature | - 40 | 125 | °C |
| T _J | Junction temperature | - 40 | 150 | °C |

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | UCC21717-Q1 | UNIT |
|-------------------------------|--|-------------|------|
| | | DW (SOIC) | |
| | | 16 | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 68.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 27.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 32.9 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 14.1 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 32.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|--|-----|-----|-----|------|
| P_D | Maximum power dissipation (both sides) | VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/- = 5V, 150kHz, 50% Duty Cycle for 10nF load, T _a = 25°C | | | 985 | mW |
| P_{D1} | Maximum power dissipation (side-1) | | | | 20 | mW |
| P_{D2} | Maximum power dissipation (side-2) | | | | 965 | mW |

5.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|--|--|--|-------|------------------|
| GENERAL | | | | |
| CLR | External clearance ⁽¹⁾ | Shortest terminal-to-terminal distance through air | > 8 | mm |
| CPG | External creepage ⁽¹⁾ | Shortest terminal-to-terminal distance across the package surface | > 8 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | > 17 | μm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | > 600 | V |
| | Material Group | According to IEC 60664 - 1 | I | |
| | Overvoltage Category per IEC 60664 - 1 | Rated mains voltage ≤ 300 V _{RMS} | I-IV | |
| | | Rated mains voltage ≤ 600 V _{RMS} | I-IV | |
| | | Rated mains voltage ≤ 1000 V _{RMS} | I-III | |
| DIN EN IEC 60747-17 (VDE 0884-17)⁽²⁾ | | | | |
| V_{IORM} | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 2121 | V _{PK} |
| V_{IOWM} | Maximum isolation working voltage | AC voltage (sine wave); time-dependent dielectric breakdown (TDDb) test | 1500 | V _{RMS} |
| | | DC voltage | 2121 | V _{DC} |
| V_{IMP} | Maximum impulse voltage | Tested in air, 1.2/50- μ s waveform per IEC 62368-1 | 8000 | V _{PK} |
| V_{IOTM} | Maximum transient isolation voltage | V _{TEST} = V _{IOTM} , t = 60 s (qualification test) | 8000 | V _{PK} |
| | | V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production test) | 8000 | V _{PK} |
| V_{IOSM} | Maximum surge isolation voltage ⁽³⁾ | Test method per IEC 62368-1, 1.2/50 μ s waveform | 12800 | V _{PK} |

5.6 Insulation Specifications (续)

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|------------------|---|---|--------------------|------------------|
| q _{pd} | Apparent charge ⁽⁴⁾ | Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} = 2545 V _{PK} , t _m = 10 s | ≤ 5 | pC |
| | | Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} = 3394 V _{PK} , t _m = 10 s | ≤ 5 | |
| | | Method b1: At routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} = 3977 V _{PK} , t _m = 1 s | ≤ 5 | |
| C _{IO} | Barrier capacitance, input to output ⁽⁵⁾ | V _{IO} = 0.5 × sin(2π ft), f = 1 MHz | ~ 1 | pF |
| R _{IO} | Insulation resistance, input to output ⁽⁵⁾ | V _{IO} = 500 V, T _A = 25°C | ≥ 10 ¹² | Ω |
| | | V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C | ≥ 10 ¹¹ | |
| | | V _{IO} = 500 V at T _S = 150°C | ≥ 10 ⁹ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| UL 1577 | | | | |
| V _{ISO} | Withstand isolation voltage | V _{TEST} = V _{ISO} = 5700 V _{RMS} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} = 6840 V _{RMS} , t = 1 s (100% production) | 5700 | V _{RMS} |

- Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
- This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- Apparent charge is electrical discharge caused by a partial discharge (pd).
- All pins on each side of the barrier tied together creating a two-pin device.

5.7 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---|---|-----|-----|------|------|
| I _S | Safety input, output, or supply current | R _{θJA} = 68.3°C/W, V _{DD} = 15 V, V _{EE} = -5V, T _J = 150°C, T _A = 25°C | | | 61 | mA |
| | | R _{θJA} = 68.3°C/W, V _{DD} = 20 V, V _{EE} = -5V, T _J = 150°C, T _A = 25°C | | | 49 | |
| P _S | Safety input, output, or total power | R _{θJA} = 68.3°C/W, V _{DD} = 20 V, V _{EE} = -5V, T _J = 150°C, T _A = 25°C | | | 1220 | mW |
| T _S | Maximum safety temperature | | | | 150 | °C |

- The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, R_{qJA}, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: T_J = T_A + R_{qJA} · P, where P is the power dissipated in the device. T_{J(max)} = T_S = T_A + R_{qJA} · P_S, where T_{J(max)} is the maximum allowed junction temperature. P_S = I_S · V_I, where V_I is the maximum supply voltage.

5.8 Electrical Characteristics

VCC = 3.3 V or 5.0 V, 1- μ F capacitor from VCC to GND, VDD - COM = 20 V, 18 V or 15 V, COM - VEE = 5 V, 8 V or 15 V, C_L = 100pF, -40°C < T_J < 150°C (unless otherwise noted) ^{(1) (2)}.

| Parameter | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|------|------|------|------------|
| VCC UVLO THRESHOLD AND DELAY | | | | | | |
| V _{VCC_ON} | VCC - GND | | 2.55 | 2.7 | 2.85 | V |
| V _{VCC_OFF} | | | 2.35 | 2.5 | 2.65 | V |
| V _{VCC_HYS} | | | | 0.2 | | V |
| t _{VCCFIL} | VCC UVLO deglitch time | | 10 | | | μ s |
| t _{VCC+ to OUT} | VCC UVLO on delay to output high | IN+ = VCC, IN - = GND | 28 | 37.8 | 50 | μ s |
| t _{VCC- to OUT} | VCC UVLO off delay to output low | | 5 | 10 | 15 | μ s |
| t _{VCC+ to RDY} | VCC UVLO on delay to RDY high | RST/EN = VCC | 30 | 37.8 | 50 | μ s |
| t _{VCC- to RDY} | VCC UVLO off delay to RDY low | | 5 | 10 | 15 | μ s |
| VDD UVLO THRESHOLD AND DELAY | | | | | | |
| V _{VDD_ON} | VDD - COM | | 10.5 | 12 | 12.8 | V |
| V _{VDD_OFF} | | | 9.9 | 10.7 | 11.8 | V |
| V _{VDD_HYS} | | | | 0.8 | | V |
| t _{VDDFIL} | VDD UVLO deglitch time | | 5 | | | μ s |
| t _{VDD+ to OUT} | VDD UVLO on delay to output high | IN+ = VCC, IN - = GND | 2 | 5 | 8 | μ s |
| t _{VDD- to OUT} | VDD UVLO off delay to output low | | 5 | 10 | | μ s |
| t _{VDD+ to RDY} | VDD UVLO on delay to RDY high | RST/EN = VCC | | 10 | 15 | μ s |
| t _{VDD- to RDY} | VDD UVLO off delay to RDY low | | | 10 | 15 | μ s |
| VCC, VDD QUIESCENT CURRENT | | | | | | |
| I _{VCCQ} | VCC quiescent current | OUT(H) = High, f _S = 0Hz, AIN=2V | 2.5 | 3 | 4 | mA |
| | | OUT(L) = Low, f _S = 0Hz, AIN=2V | 1.45 | 2 | 2.75 | mA |
| I _{VDDQ} | VDD quiescent current | OUT(H) = High, f _S = 0Hz, AIN=2V | 3.6 | 4 | 5.9 | mA |
| | | OUT(L) = Low, f _S = 0Hz, AIN=2V | 3.1 | 3.7 | 5.3 | mA |
| LOGIC INPUTS - IN+, IN- and RST/EN | | | | | | |
| V _{INH} | Input high threshold | VCC=3.3V | | 1.85 | 2.31 | V |
| V _{INL} | Input low threshold | | 0.99 | 1.52 | | V |
| V _{INHYS} | Input threshold hysteresis | | | 0.33 | | V |
| I _{IH} | Input high level input leakage current | V _{IN} = VCC | | 90 | | μ A |
| I _{IL} | Input low level input leakage current | V _{IN} = GND | | -90 | | μ A |
| R _{IND} | Input pins pull down resistance | | | 55 | | k Ω |
| R _{INU} | Input pins pull up resistance | | | 55 | | k Ω |
| T _{INFIL} | IN+, IN - and RST/EN deglitch (ON and OFF) filter time | f _S = 50kHz | 28 | 40 | 60 | ns |
| T _{RSTFIL} | Deglitch filter time to reset FLT | | 500 | 650 | 800 | ns |
| GATE DRIVER STAGE | | | | | | |
| I _{OUTH} | Peak source current | C _L = 0.18 μ F, f _S = 1kHz | | 10 | | A |
| I _{OUTL} | Peak sink current | | | 10 | | A |
| R _{OUTH} ⁽³⁾ | Output pull-up resistance | I _{OUTH} = -0.1A | | 2.5 | | Ω |
| R _{OUTL} | Output pull-down resistance | I _{OUTL} = 0.1A | | 0.3 | | Ω |
| V _{OUTH} | High level output voltage | I _{OUTH} = -0.2A, VDD = 18V | | 17.5 | | V |
| V _{OUTL} | Low level output voltage | I _{OUTL} = 0.2A | | 60 | | mV |
| ACTIVE PULLDOWN | | | | | | |

5.8 Electrical Characteristics (续)

VCC = 3.3 V or 5.0 V, 1- μ F capacitor from VCC to GND, VDD - COM = 20 V, 18 V or 15 V, COM - VEE = 5 V, 8 V or 15 V, C_L = 100pF, -40°C < T_J < 150°C (unless otherwise noted) ^{(1) (2)}.

| Parameter | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|------|-----------|------|----------|
| V _{OUTPD} | Output active pull down on OUTL | I _{OUTL(typ)} = 0.1×I _{OUTL(typ)} , VDD=OPEN, VEE=COM | 1.5 | 2.0 | 2.5 | V |
| INTERNAL ACTIVE MILLER CLAMP | | | | | | |
| V _{CLMPH} | Miller clamp threshold voltage | Reference to VEE | 1.5 | 2.0 | 2.5 | V |
| V _{CLMPI} | Output low clamp voltage | I _{CLMPI} = 1A | | VEE + 0.5 | | V |
| I _{CLMPI} | Output low clamp current | V _{CLMPI} = 0V, VEE = - 2.5V | | 4.0 | | A |
| R _{CLMPI} | Miller clamp pull down resistance | I _{CLMPI} = 0.2A | | 0.6 | | Ω |
| t _{DCLMPI} | Miller clamp ON delay time | C _L = 1.8nF | | 15 | 50 | ns |
| SHORT CIRCUIT CLAMPING | | | | | | |
| V _{CLP-OUT(H)} | V _{OUTH} - VDD | OUT = High, I _{OUT(H)} = 500mA, t _{CLP} =10 μ s | | 0.9 | | V |
| V _{CLP-OUT(L)} | V _{OUTL} - VDD | OUT = High, I _{OUT(L)} = 500mA, t _{CLP} =10 μ s | | 1.8 | | V |
| V _{CLP-CLMPI} | V _{CLMPI} -VDD | OUT = High, I _{CLMPI} = 20mA, t _{CLP} =10 μ s | | 1.0 | | V |
| OC PROTECTION | | | | | | |
| I _{DCHG} | OC pull down current | V _{OC} = 1V | | 40 | | mA |
| V _{OCTH} | Detection threshold | | 0.63 | 0.7 | 0.77 | V |
| V _{OCL} | Voltage when OUTL = Low | Reference to COM, I _{OC} = 5mA | | 0.13 | | V |
| t _{OCFIL} | OC fault deglitch filter | | 95 | 120 | 180 | ns |
| t _{OCOFF} | OC propagation delay to OUTL 90% | | 150 | 270 | 400 | ns |
| t _{OCFLT} | OC to FLT low delay | | 300 | 530 | 750 | ns |
| INTERNAL SOFT TURN OFF | | | | | | |
| I _{STO} | Soft turn-off current on fault condition | V _{DD} -V _{EE} = 20 V, V _{OUTL} -COM = 8 V | 250 | 400 | 570 | mA |
| INTERNAL SOFT TURN OFF (TRIGGERED BY RST/EN) | | | | | | |
| t _{RSTPD} | RST/EN going low propagation delay to OUTL 90% | | | 400 | | ns |
| ISOLATED TEMPERATURE SENSE AND MONITOR (AIN - APWM) | | | | | | |
| V _{AIN} | Analog sensing voltage range | | 0.6 | | 4.5 | V |
| I _{AIN} | Internal current source | V _{AIN} =2.5V, -40°C < T _J < 150°C | 196 | 203 | 209 | μ A |
| f _{APWM} | APWM output frequency | V _{AIN} =2.5V | 380 | 400 | 420 | kHz |
| BW _{AIN} | AIN-APWM Bandwidth | | | 10 | | kHz |
| D _{APWM} | APWM Duty Cycle | V _{AIN} =0.6V | 86.5 | 88 | 89.5 | % |
| | | V _{AIN} =2.5V | 48.5 | 50 | 51.5 | % |
| | | V _{AIN} =4.5V | 7.5 | 10 | 11.5 | % |
| FLT AND RDY REPORTING | | | | | | |
| t _{RDYHLD} | VDD UVLO RDY low minimum holding time | | 0.55 | | 1 | ms |
| t _{FLTMUTE} | Output mute time on fault | Reset fault through RST/EN | 0.55 | | 1 | ms |
| R _{ODON} | Open drain output on resistance | I _{ODON} = 5mA | | 30 | | Ω |
| V _{ODL} | Open drain low output voltage | | | | 0.3 | V |
| COMMON MODE TRANSIENT IMMUNITY | | | | | | |
| CMTI | Common-mode transient immunity | | 150 | | | V/ns |

(1) Currents are positive into and negative out of the specified terminal.

- (2) All voltages are referenced to COM unless otherwise notified.
- (3) For internal PMOS only. Refer to Driver Stage for effective pull-up resistance.

5.9 Switching Characteristics

VCC = 5.0 V, 1-μF capacitor from VCC to GND, VDD - COM = 20V, 18V or 15V, COM - VEE = 3 V, 5 V or 8 V, C_L = 100pF, -40°C < T_J < 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|-------------------------------------|-----|-----|-----|------|
| t _{PDLH} | Propagation delay time low-to-high | | 60 | 90 | 130 | ns |
| t _{PDHL} | Propagation delay time low-to-high | | 60 | 90 | 130 | ns |
| PWD | Pulse width distortion (t _{PDHL} -t _{PDLH}) | | | | 30 | ns |
| t _{sk-pp} | Part to part skew | Rising or falling propagation delay | | | 30 | ns |
| t _r | Driver output rise time | C _L = 10nF | | 33 | | ns |
| t _f | Driver output fall time | C _L = 10nF | | 27 | | ns |
| f _{MAX} | Maximum switching frequency | | | | 1 | MHz |

5.10 Insulation Characteristics Curves

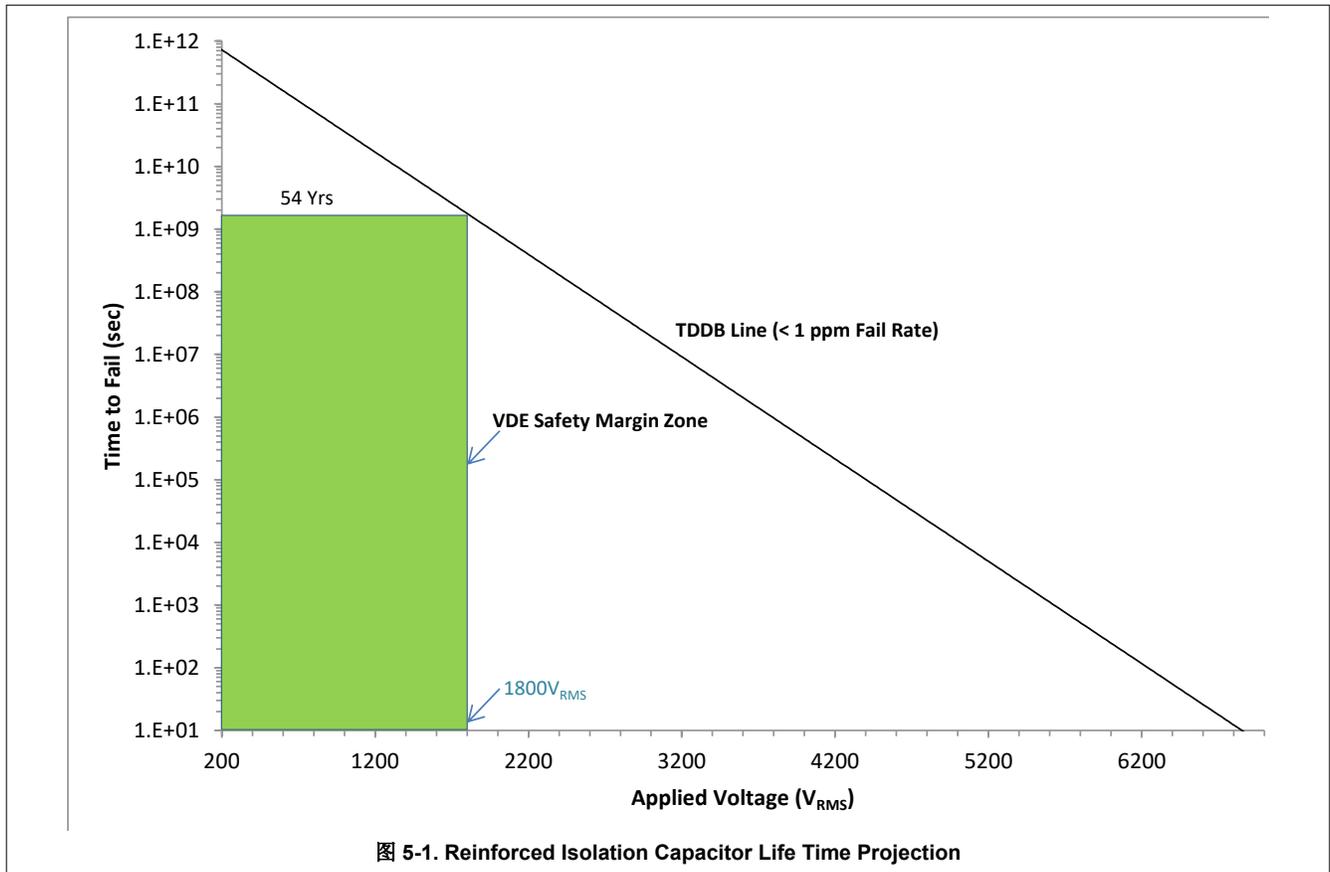
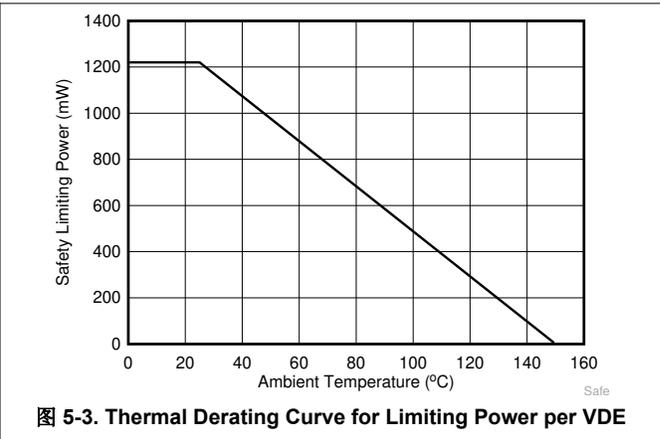
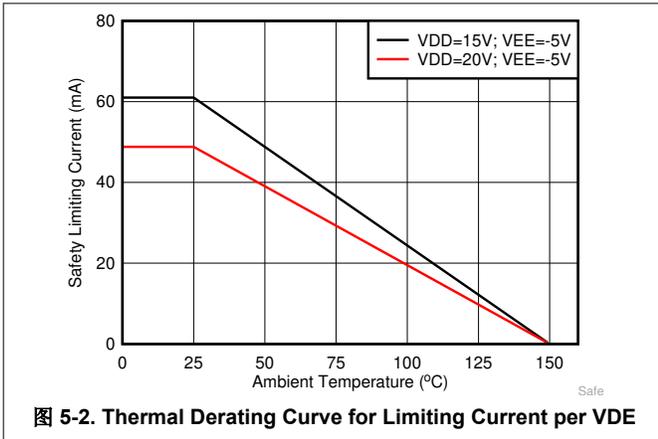


图 5-1. Reinforced Isolation Capacitor Life Time Projection

5.10 Insulation Characteristics Curves (continued)



5.11 Typical Characteristics

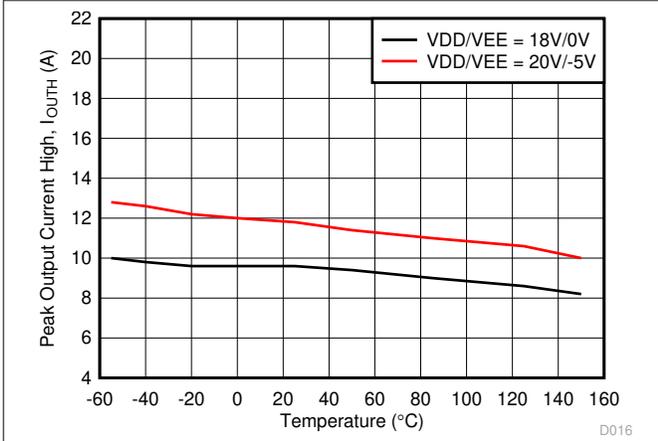


图 5-4. Output High Drive Current vs. Temperature

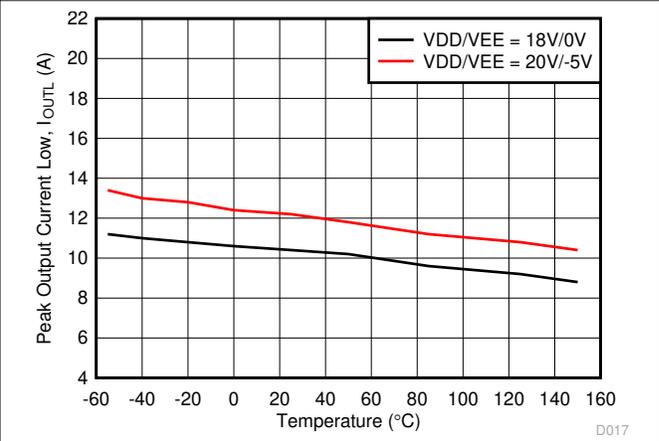


图 5-5. Output Low Driver Current vs. Temperature

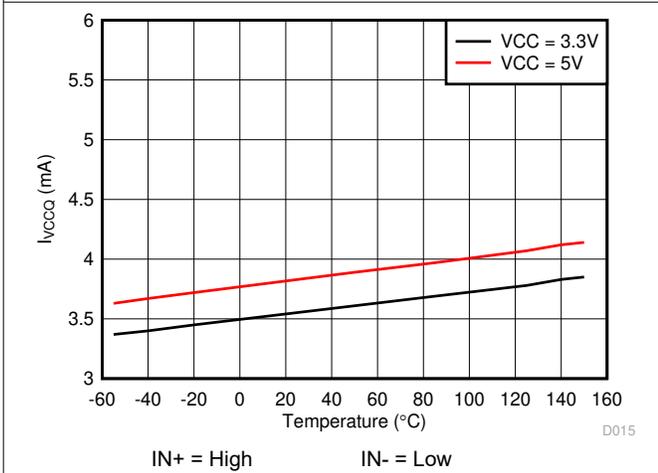


图 5-6. I_{VCCQ} Supply Current vs. Temperature

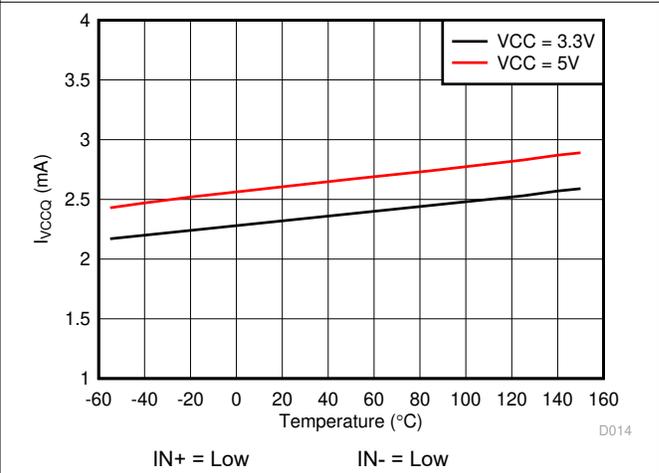


图 5-7. I_{VCCQ} Supply Current vs. Temperature

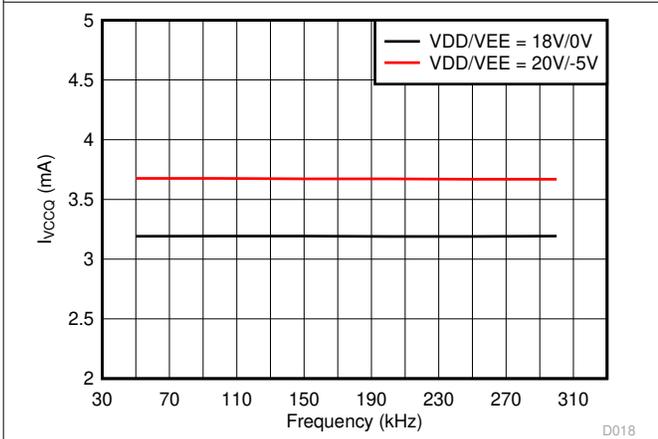


图 5-8. I_{VCCQ} Supply Current vs. Input Frequency

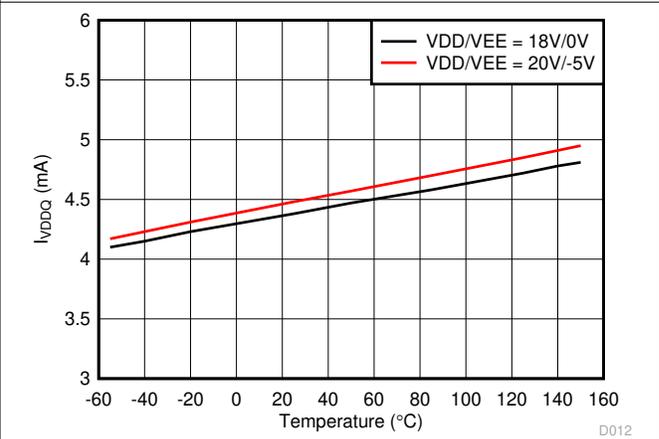
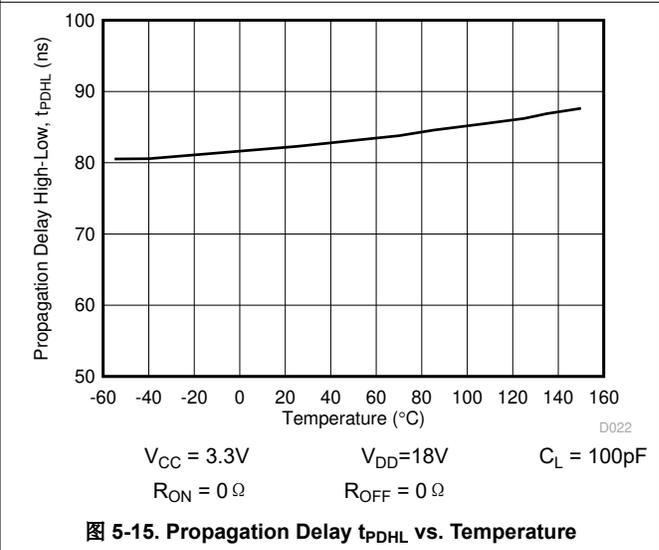
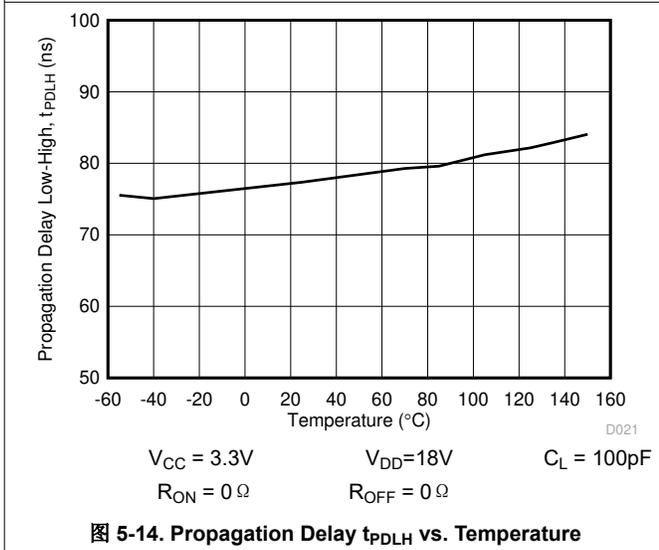
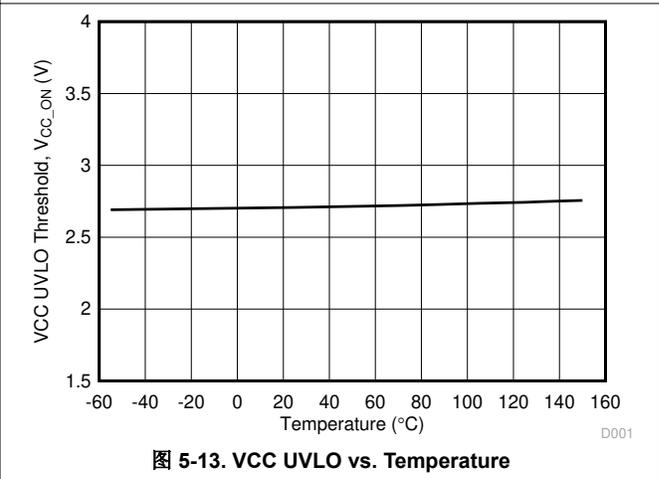
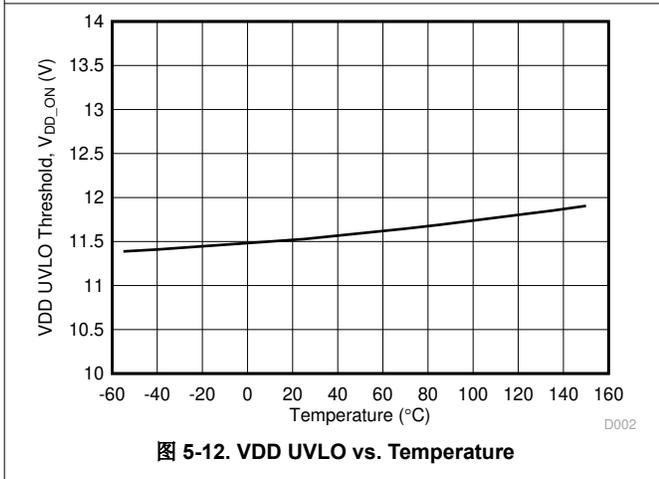
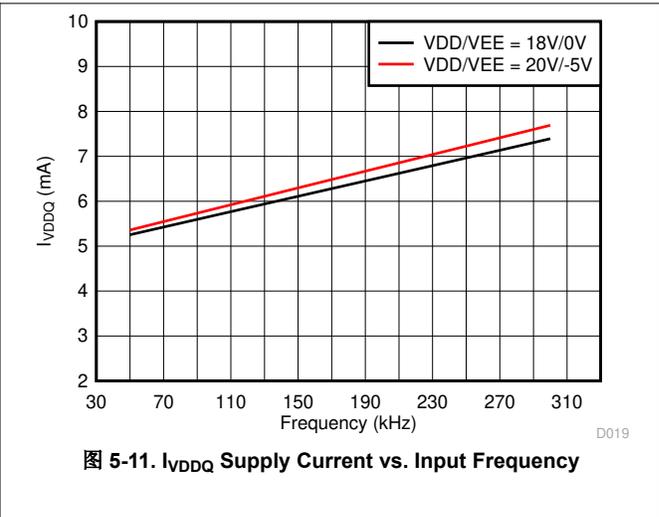
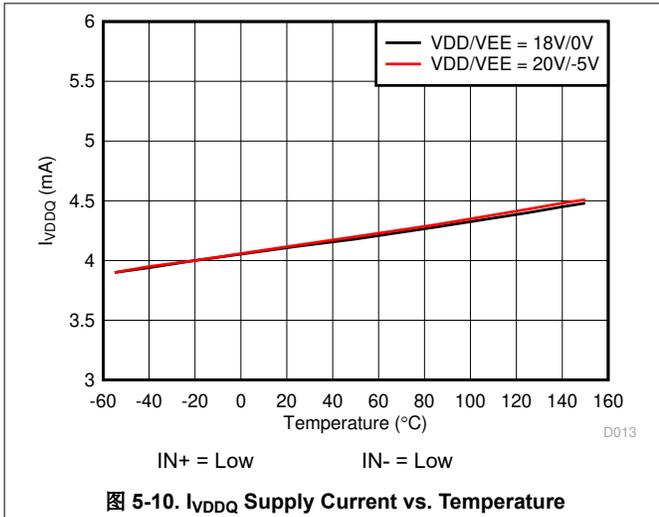
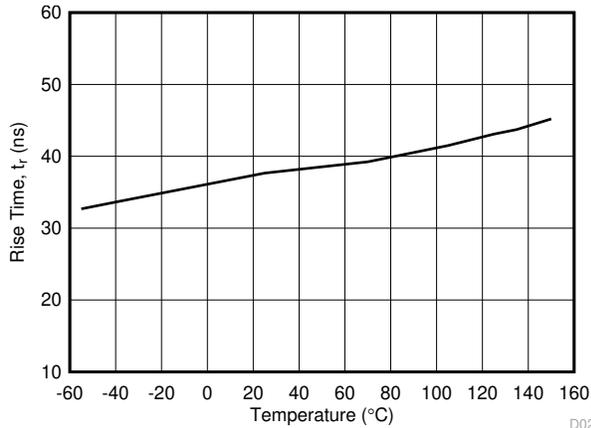


图 5-9. I_{VDDQ} Supply Current vs. Temperature

5.11 Typical Characteristics (continued)

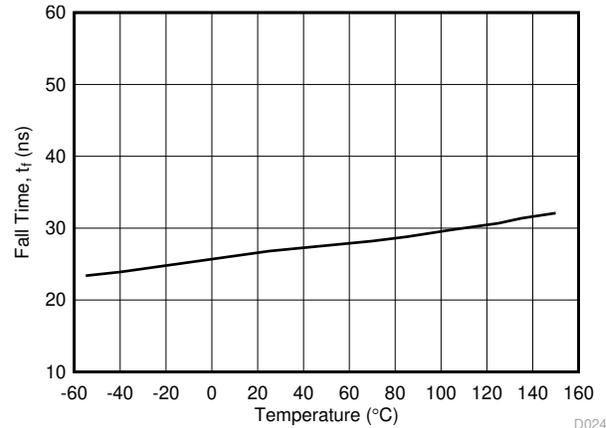


5.11 Typical Characteristics (continued)



$V_{CC} = 3.3V$ $V_{DD} = 18V$ $C_L = 10nF$
 $R_{ON} = 0\Omega$ $R_{OFF} = 0\Omega$

图 5-16. t_r Rise Time vs. Temperature



$V_{CC} = 3.3V$ $V_{DD} = 18V$ $C_L = 10nF$
 $R_{ON} = 0\Omega$ $R_{OFF} = 0\Omega$

图 5-17. t_f Fall Time vs. Temperature

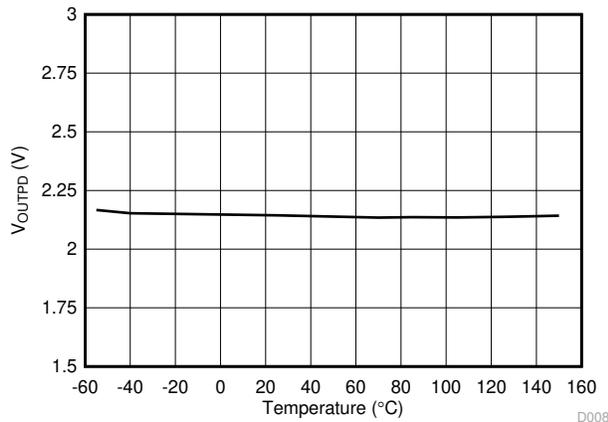


图 5-18. V_{OUTPD} Output Active Pulldown Voltage vs. Temperature

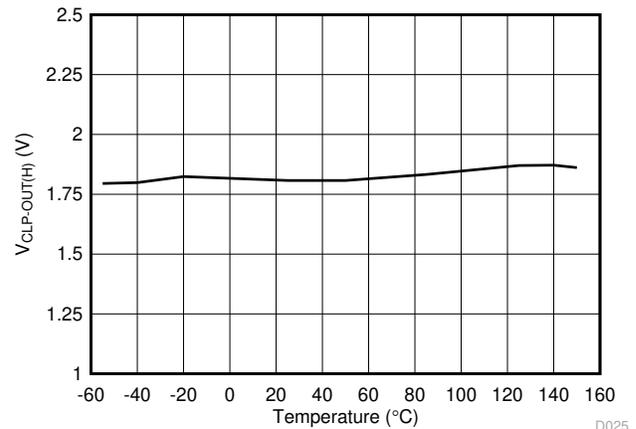


图 5-19. $V_{CLP-OUT(H)}$ Short Circuit Clamping Voltage vs. Temperature

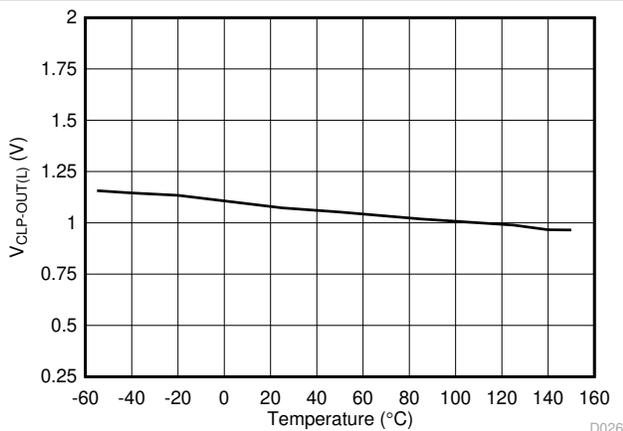


图 5-20. $V_{CLP-OUT(L)}$ Short Circuit Clamping Voltage vs. Temperature

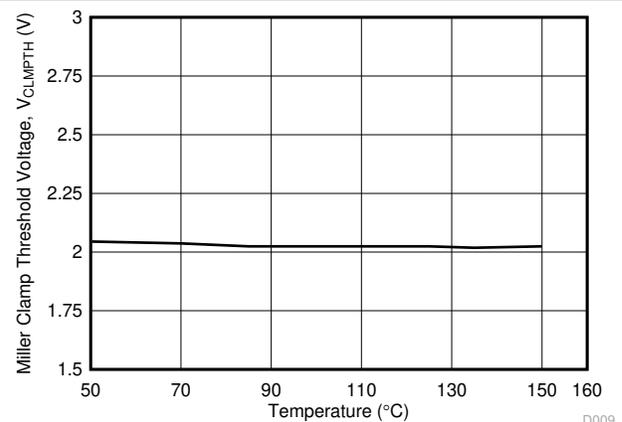


图 5-21. V_{CLMPH} Miller Clamp Threshold Voltage vs. Temperature

5.11 Typical Characteristics (continued)

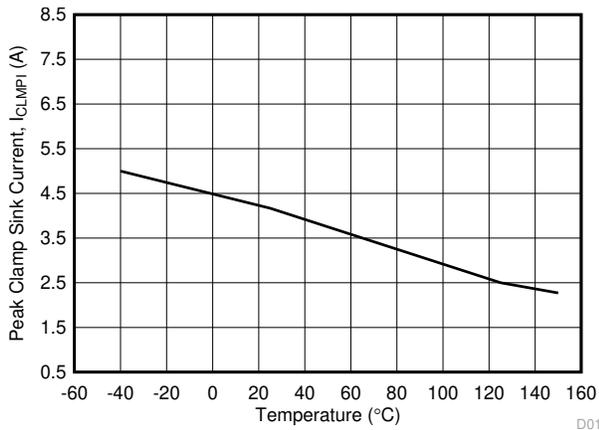


图 5-22. I_{CLMPl} Miller Clamp Sink Current vs. Temperature

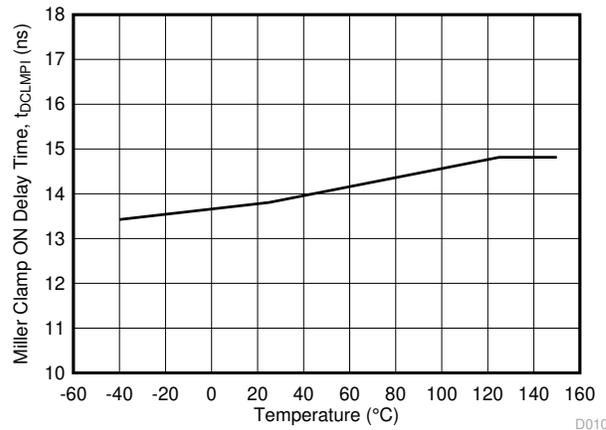


图 5-23. t_{DCLMPl} Miller Clamp ON Delay Time vs. Temperature

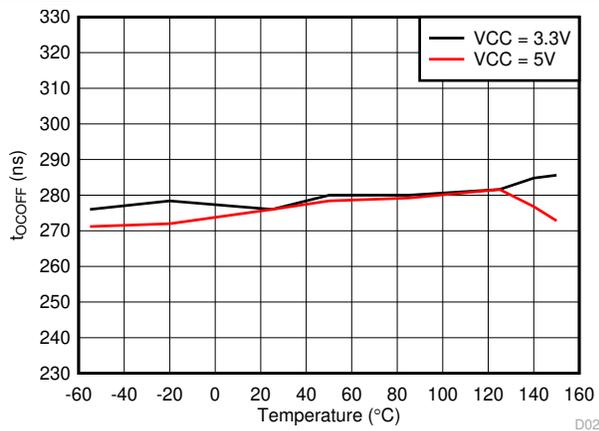


图 5-24. t_{OCOff} OC Propagation Delay vs. Temperature

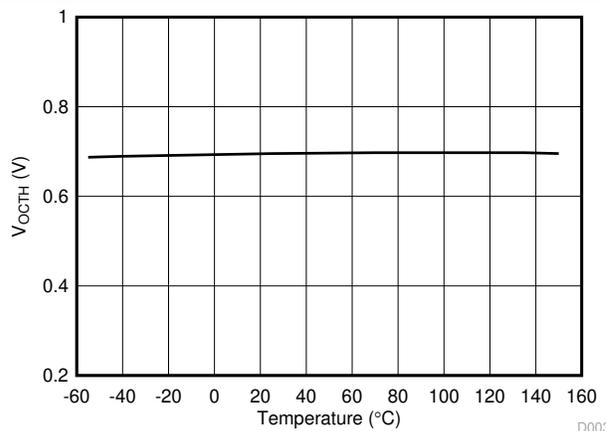


图 5-25. V_{OCTh} OC Detection Threshold vs. Temperature

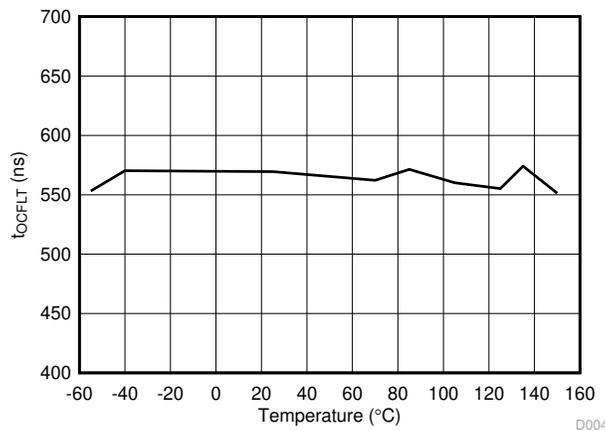


图 5-26. t_{OCFLT} OC to \overline{FLT} Low Delay Time vs. Temperature

6 Parameter Measurement Information

6.1 Propagation Delay

6.1.1 Non-Inverting and Inverting Propagation Delay

图 6-1 shows the propagation delay measurement for non-inverting configurations. 图 6-2 shows the propagation delay measurement with the inverting configurations.

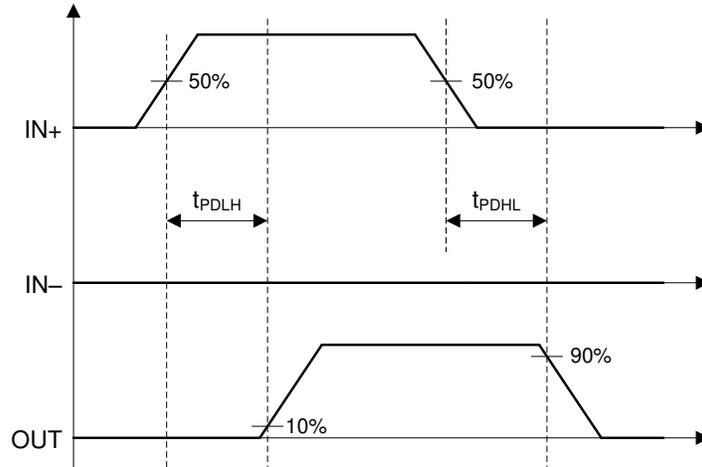


图 6-1. Non-Inverting Logic Propagation Delay Measurement

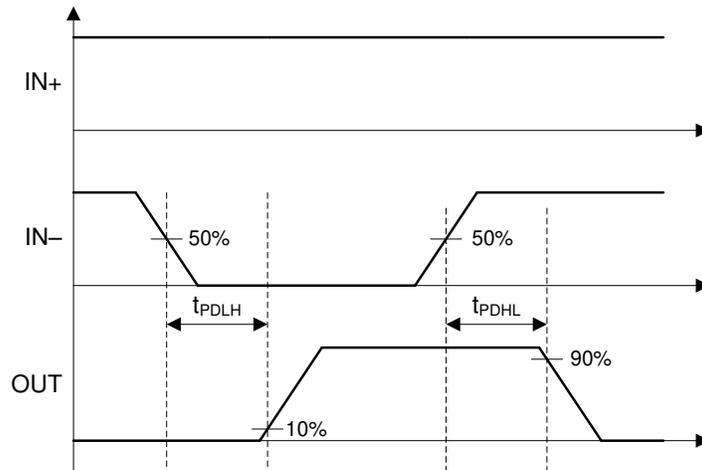


图 6-2. Inverting Logic Propagation Delay Measurement

6.2 Input Deglitch Filter

In order to increase the robustness of gate driver over noise transient and accidental small pulses on the input pins, for example IN+, IN-, $\overline{\text{RST/EN}}$, a 40-ns deglitch filter is designed to filter out the transients and make sure there is no faulty output responses or accidental driver malfunctions. When the IN+ or IN- PWM pulse is smaller than the input deglitch filter width, T_{INFIL} , there will be no responses on the OUT drive signal. 图 6-3 and 图 6-4 shows the IN+ pin ON and OFF pulse deglitch filter effect. 图 6-5 and 图 6-6 shows the IN- pin ON and OFF pulse deglitch filter effect.

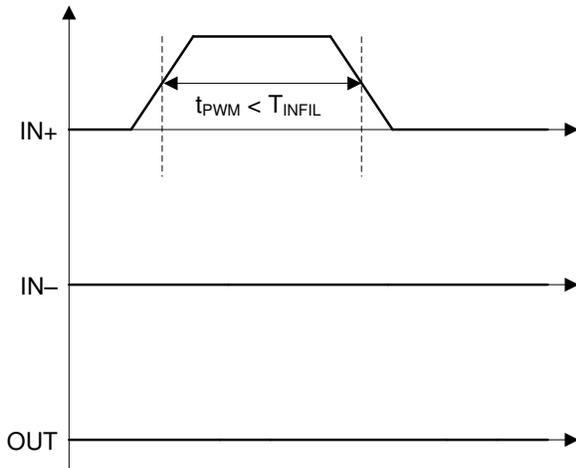


图 6-3. IN+ ON Deglitch Filter

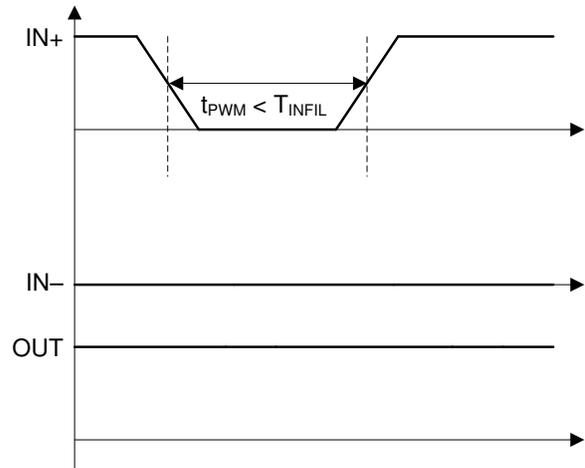


图 6-4. IN+ OFF Deglitch Filter

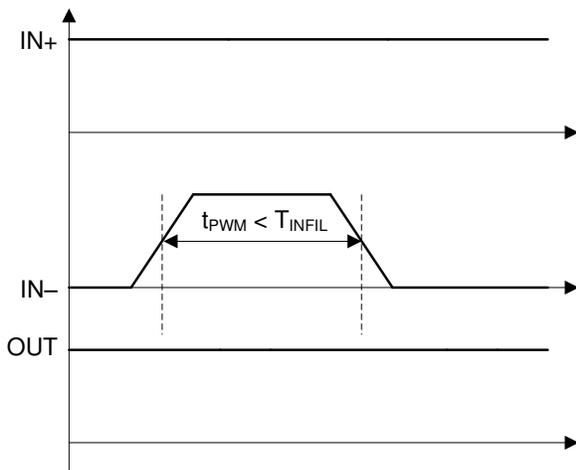


图 6-5. IN- ON Deglitch Filter

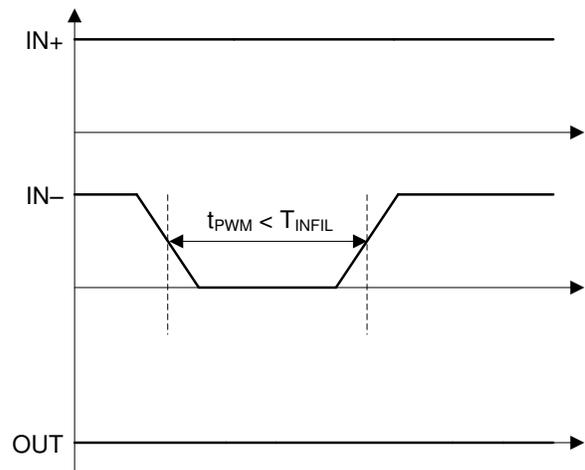


图 6-6. IN- OFF Deglitch Filter

6.3 Active Miller Clamp

6.3.1 Internal Active Miller Clamp

For gate driver application with unipolar bias supply or bipolar supply with small negative turn-off voltage, active Miller clamp can help add a additional low impedance path to bypass the Miller current and prevent the unintentional turn-on through the Miller capacitance. 图 6-7 shows the timing diagram for the on-chip internal Miller clamp function.

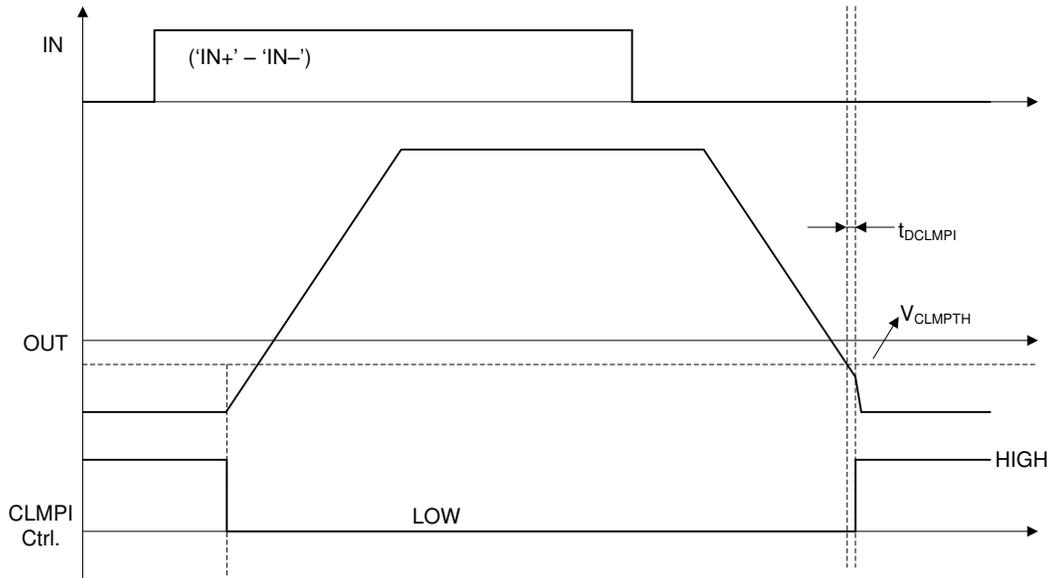


图 6-7. Timing Diagram for Internal Active Miller Clamp Function

6.4 Undervoltage Lockout (UVLO)

UVLO is one of the key protection features designed to protect the system in case of bias supply failures on VCC, primary side power supply, and VDD, secondary side power supply.

6.4.1 VCC UVLO

The VCC UVLO protection details are discussed in this section. 图 6-8 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN - APWM.

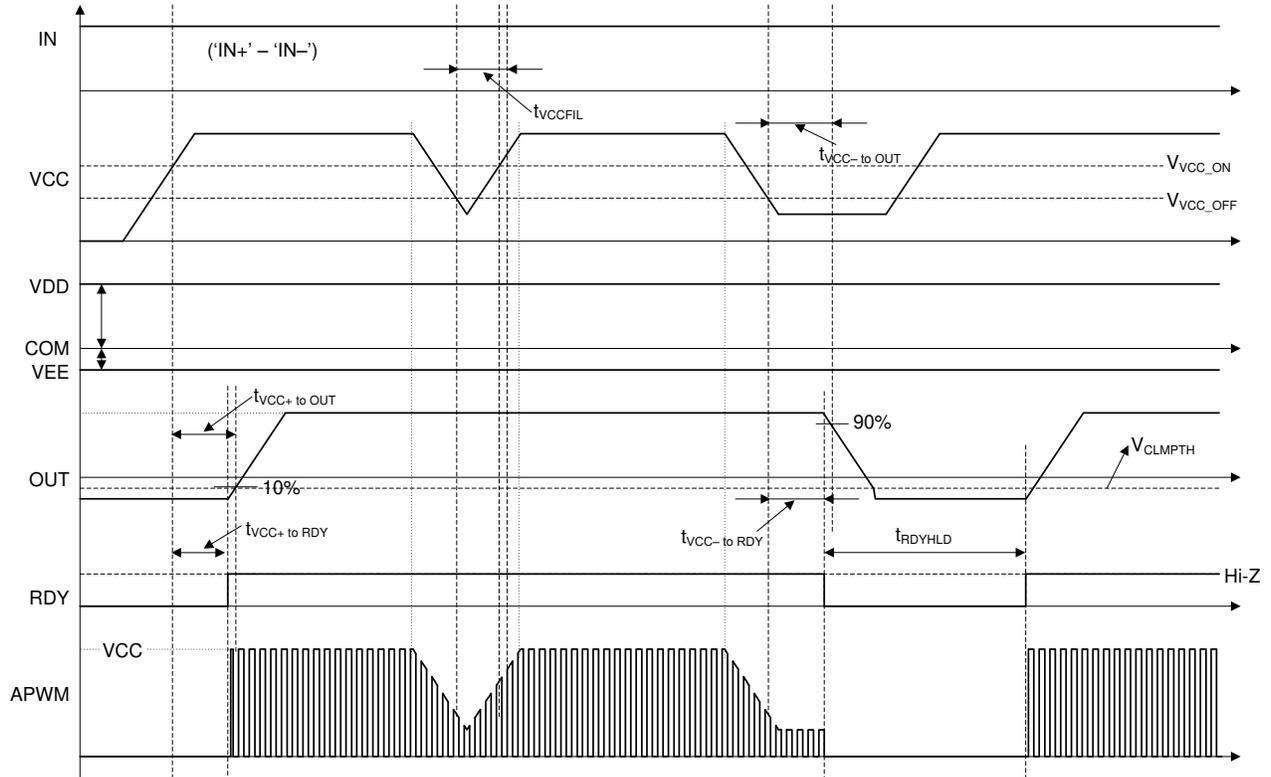


图 6-8. VCC UVLO Protection Timing Diagram

6.4.2 VDD UVLO

The VDD UVLO protection details are discussed in this section. 图 6-9 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN - APWM.

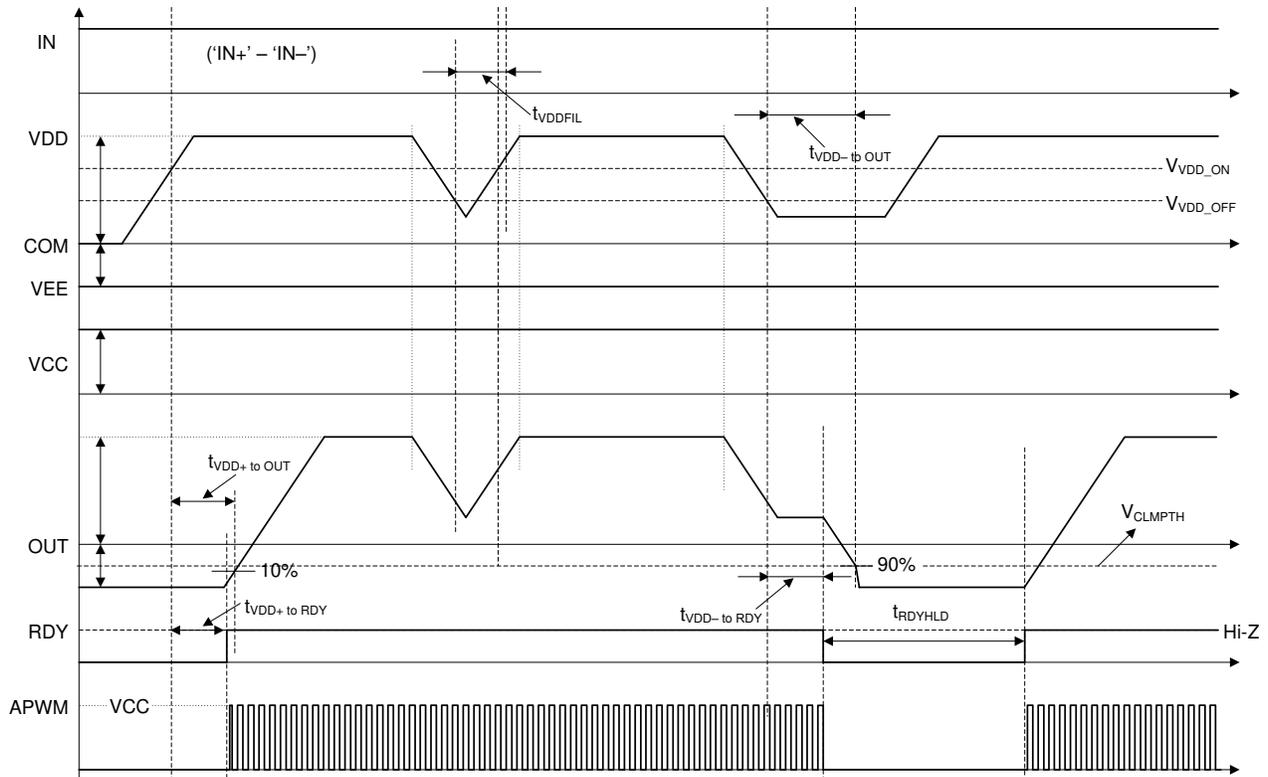


图 6-9. VDD UVLO Protection Timing Diagram

6.5 Overcurrent (OC) Protection

6.5.1 OC Protection with Soft Turn-OFF

OC Protection is used to sense the current of the SiC-MOSFETs and IGBTs under an overcurrent or shoot-through condition. 图 6-10 shows the timing diagram of OC operation with soft turn-off.

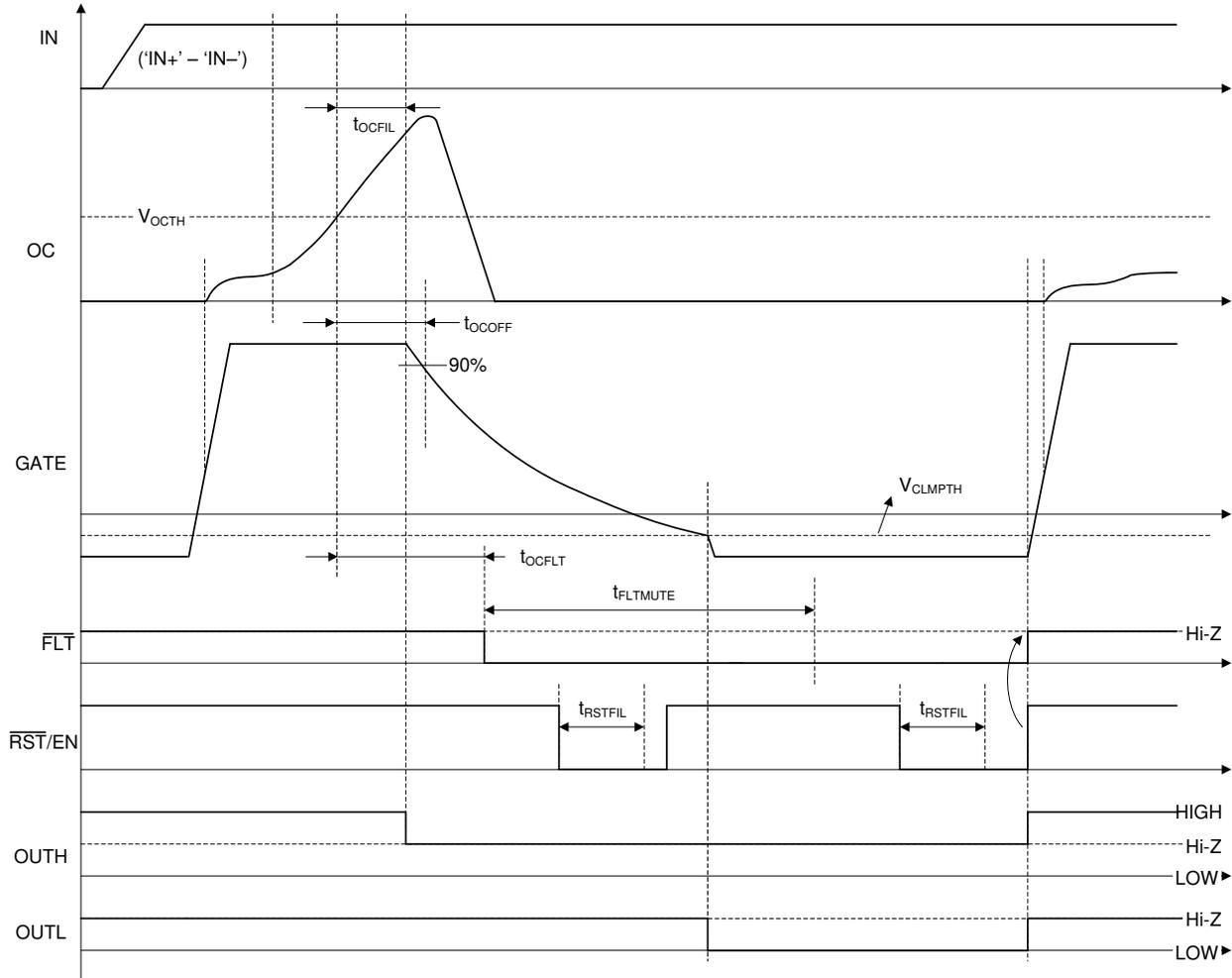


图 6-10. OC Protection with Soft Turn-OFF

6.6 Soft Turn-Off Triggered by $\overline{\text{RST/EN}}$

6.6.1 Soft Turn-Off Triggered by $\overline{\text{RST/EN}}$

图 6-11 shows the timing diagram of a soft turn-off triggered by $\overline{\text{RST/EN}}$ low.

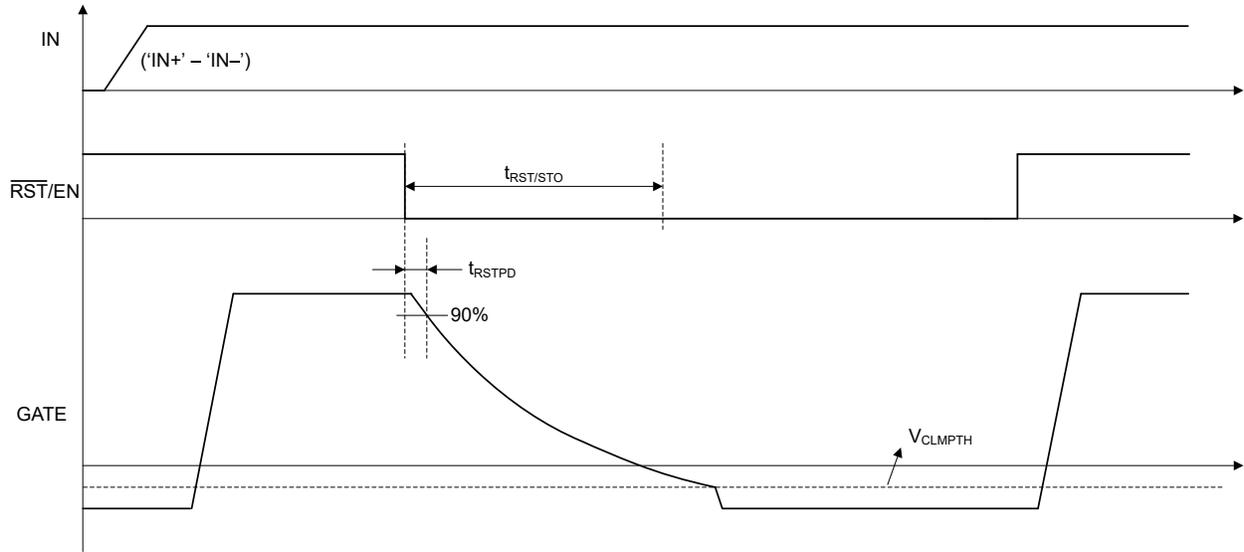


图 6-11. Soft Turn-Off Triggered by $\overline{\text{RST/EN}}$

7 Detailed Description

7.1 Overview

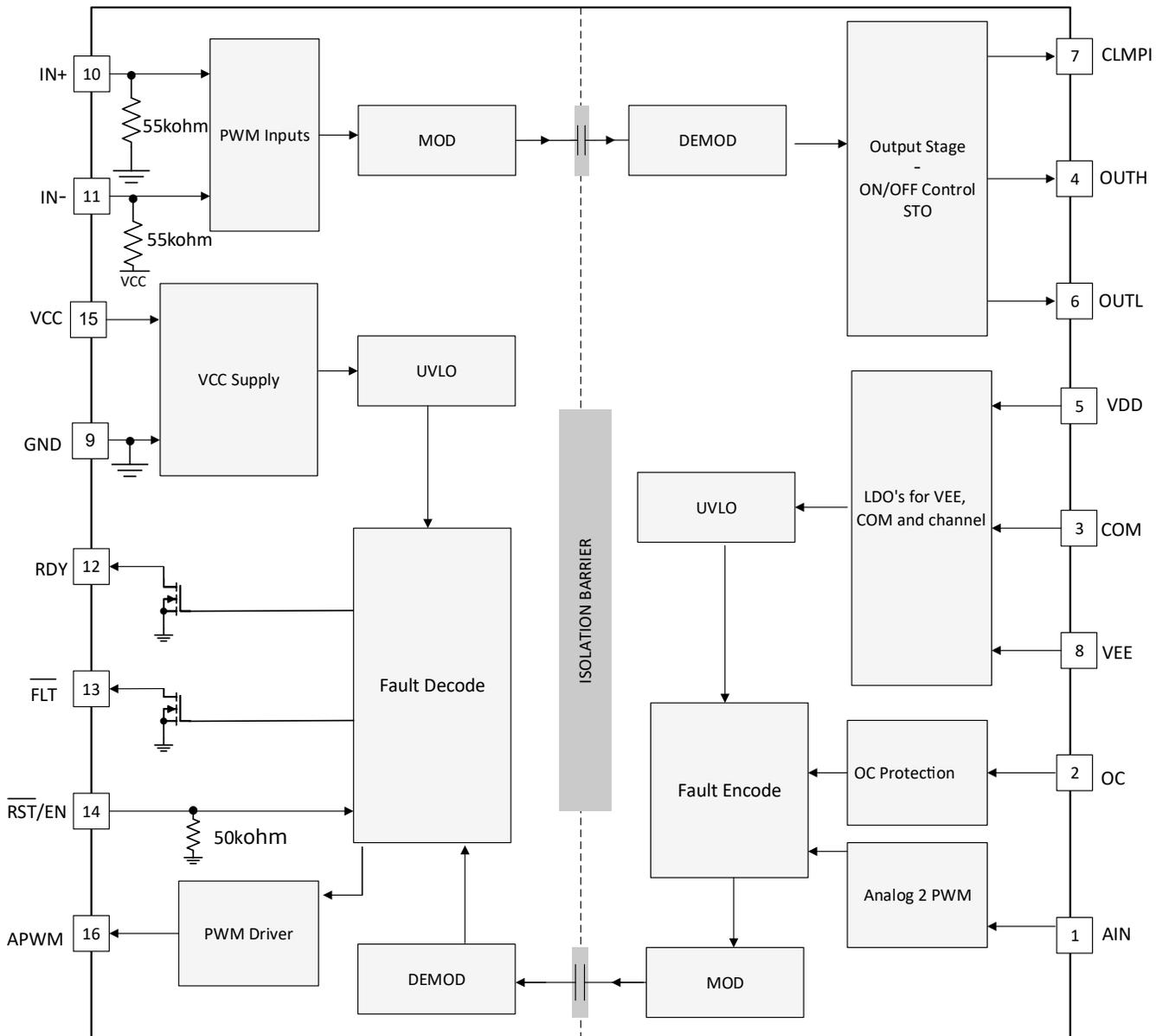
The UCC21717-Q1 device is an advanced isolated gate driver with state-of-art protection and sensing features for SiC MOSFETs and IGBTs. The device can support up to 2121-V DC operating voltage based on SiC MOSFETs and IGBTs, and can be used to above 10-kW applications such as HEV/EV traction inverter, motor drive, on-board and off-board battery charger, solar inverter, and so forth. The galvanic isolation is implemented by the capacitive isolation technology, which can realize a reliable reinforced isolation between the low voltage DSP/MCU and high voltage side.

The ± 10 -A peak sink and source current of the UCC21717-Q1 can drive the SiC MOSFET modules and IGBT modules directly without an extra buffer. The driver can also be used to drive higher power modules or parallel modules with external buffer stage. The device can support up to 1.5-kV_{RMS} working voltage, 12.8-kV_{PK} surge immunity with longer than 40 years isolation barrier life. The strong drive strength helps to switch the device fast and reduce the switching loss. While the 150-V/ns minimum CMTI ensures the reliability of the system with fast switching speed. The small propagation delay and part-to-part skew can minimize the deadtime setting, so the conduction loss can be reduced.

The device includes extensive protection and monitor features to increase the reliability and robustness of the SiC MOSFET and IGBT based systems. The 12-V output side power supply UVLO is suitable for switches with gate voltage ≥ 15 V. The active Miller clamp feature prevents the false turn on causing by Miller capacitance during fast switching. The device has the state-of-art overcurrent and short circuit detection time, and fault reporting function to the low voltage side DSP/MCU. The soft turn-off with soft turn off is triggered when the overcurrent or short circuit fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switches.

The isolated analog to PWM sensor can be used as switch temperature sensing, DC bus voltage sensing, auxiliary power supply sensing, and so forth. The PWM signal can be fed directly to DSP/MCU or through a low-pass-filter as an analog signal.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supply

The input side power supply VCC can support a wide voltage range from 3 V to 5.5 V. The device supports both unipolar and bipolar power supply on the output side, with a wide range from 13 V to 33 V from VDD to VEE. The negative power supply with respect to switch source or emitter is usually adopted to avoid false turn on when the other switch in the phase leg is turned on. The negative voltage is especially important for SiC MOSFET due to its fast switching speed and low threshold voltage.

7.3.2 Driver Stage

The UCC21717-Q1 has ± 10 -A peak drive strength and is suitable for high power applications. The high drive strength can drive a SiC MOSFET module, IGBT module or paralleled discrete devices directly without extra buffer stage. The UCC21717-Q1 can also be used to drive higher power modules or parallel modules with extra buffer stage. Regardless of the values of VDD, the peak sink and source current can be kept at 10 A. The driver

features an important safety function wherein, when the input pins are in floating condition, the OUTH/OUTL is held in LOW state. The split output of the driver stage is depicted in 图 7-1. The driver has rail-to-rail output by implementing a hybrid pull-up structure with a P-Channel MOSFET in parallel with an N-Channel MOSFET, and an N-Channel MOSFET to pulldown. The pull-up NMOS is the same as the pull down NMOS, so the on resistance R_{NMOS} is the same as R_{OL} . The hybrid pull-up structure delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power semiconductor turn-on transient. The R_{OH} in 图 7-1 represents the on-resistance of the pull-up P-Channel MOSFET. However, the effective pull-up resistance is much smaller than R_{OH} . Since the pull-up N-Channel MOSFET has much smaller on-resistance than the P-Channel MOSFET, the pull-up N-Channel MOSFET dominates most of the turn-on transient, until the voltage on OUTH pin is about 3 V below VDD voltage. The effective resistance of the hybrid pull-up structure during this period is about $2 \times R_{OL}$. Then the P-Channel MOSFET pulls up the OUTH voltage to VDD rail. The low pull-up impedance results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

The pull-down structure of the driver stage is implemented solely by a pull-down N-Channel MOSFET. 图 7-1 also shows the on-resistance of the N-Channel MOSFET R_{OL} . This MOSFET can ensure the OUTL voltage be pulled down to VEE rail. The low pull-down impedance not only results in high sink current to reduce the turn-off time, but also helps to increase the noise immunity considering the Miller effect.

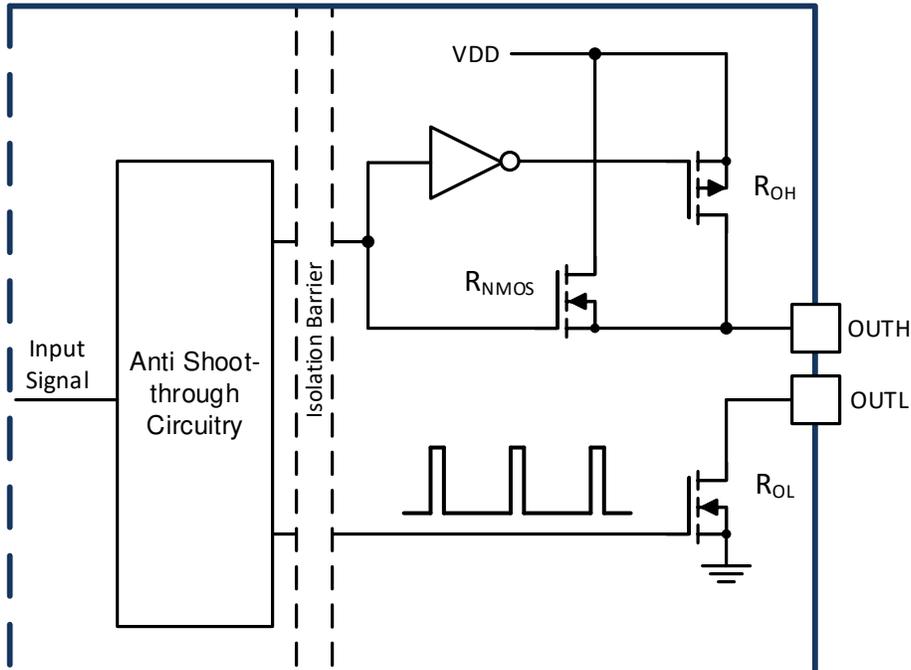


图 7-1. Gate Driver Output Stage

7.3.3 VCC and VDD Undervoltage Lockout (UVLO)

The UCC21717-Q1 implements the internal UVLO protection feature for both input and output power supplies VCC and VDD. When the supply voltage is lower than the threshold voltage, the driver output is held as LOW. The output only goes HIGH when both VCC and VDD are out of the UVLO status. The UVLO protection feature not only reduces the power consumption of the driver itself during low power supply voltage condition, but also increases the efficiency of the power stage. For SiC MOSFET and IGBT, the on-resistance reduces while the gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage. The UCC21717-Q1 implements 12-V threshold voltage of VDD UVLO, with 800-mV hysteresis. This threshold voltage is suitable for both SiC MOSFET and IGBT.

The UVLO protection block features with hysteresis and deglitch filter, which help to improve the noise immunity of the power supply. During the turn on and turn off switching transient, the driver sources and sinks a peak transient current from the power supply, which can result in sudden voltage drop of the power supply. With hysteresis and UVLO deglitch filter, the internal UVLO protection block will ignore small noises during the normal switching transients.

The timing diagrams of the UVLO feature of VCC and VDD are shown in 图 6-8, and 图 6-9. The RDY pin on the input side is used to indicate the power good condition. The RDY pin is open drain. During UVLO condition, the RDY pin is held in low status and connected to GND. Normally the pin is pulled up externally to VCC to indicate the power good. The AIN-APWM function stops working during the UVLO status. The APWM pin on the input side will be held LOW.

7.3.4 Active Pulldown

The UCC21717-Q1 implements an active pulldown feature to ensure the OUTH/OUTL pin clamping to VEE when the VDD is open. The OUTH/OUTL pin is in high-impedance status when VDD is open, the active pulldown feature can prevent the output be false turned on before the device is back to control.

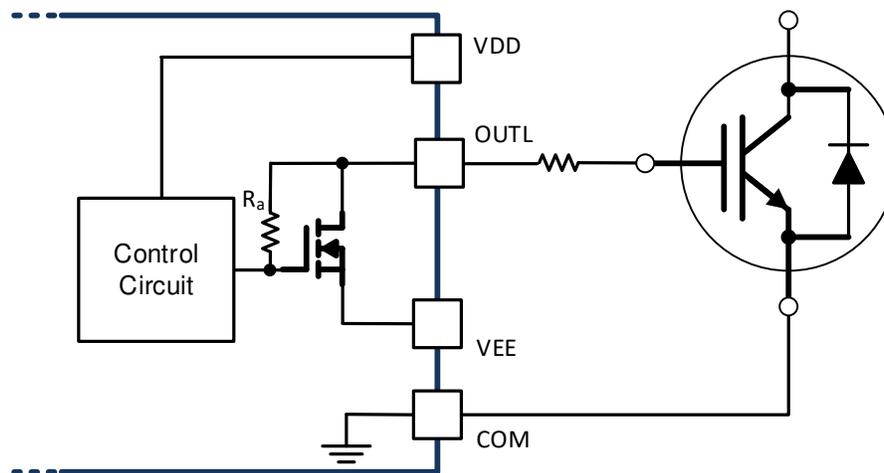


图 7-2. Active Pulldown

7.3.5 Short Circuit Clamping

During short circuit condition, the Miller capacitance can cause a current sinking to the OUTH/OUTL pin due to the high dV/dt and boost the OUTH/OUTL voltage. The short circuit clamping feature of the UCC21717-Q1 can clamp the OUTH/OUTL pin voltage to be slightly higher than VDD, which can protect the power semiconductors from a gate-source and gate-emitter overvoltage breakdown. This feature is realized by an internal diode from the OUTH/OUTL to VDD.

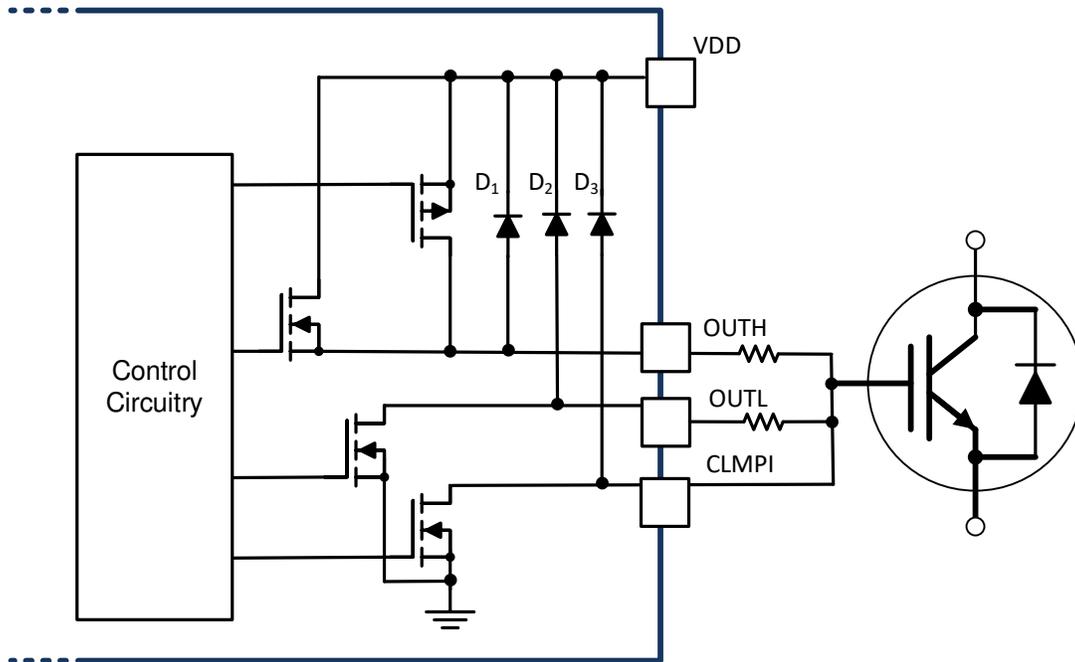


图 7-3. Short Circuit Clamping

7.3.6 Internal Active Miller Clamp

The active Miller clamp feature is important to prevent the false turn-on while the driver is in OFF state. In applications which the device can be in synchronous rectifier mode, the body diode conducts the current during the deadtime while the device is in OFF state, the drain-source or collector-emitter voltage remains the same and the dV/dt happens when the other power semiconductor of the phase leg turns on. The low internal pull-down impedance of the UCC21717-Q1 can provide a strong pulldown to hold the OUTL to VEE. However, external gate resistance is usually adopted to limit the dV/dt . The Miller effect during the turn on transient of the other power semiconductor can cause a voltage drop on the external gate resistor, which boost the gate-source or gate-emitter voltage. If the voltage on V_{GS} or V_{GE} is higher than the threshold voltage of the power semiconductor, a shoot through can happen and cause catastrophic damage. The active Miller clamp feature of the UCC21717-Q1 drives an internal MOSFET, which connects to the device gate. The internal MOSFET is triggered when the gate voltage is lower than V_{CLMPH} , which is 2 V above VEE, and creates a low impedance path to avoid the false turn on issue.

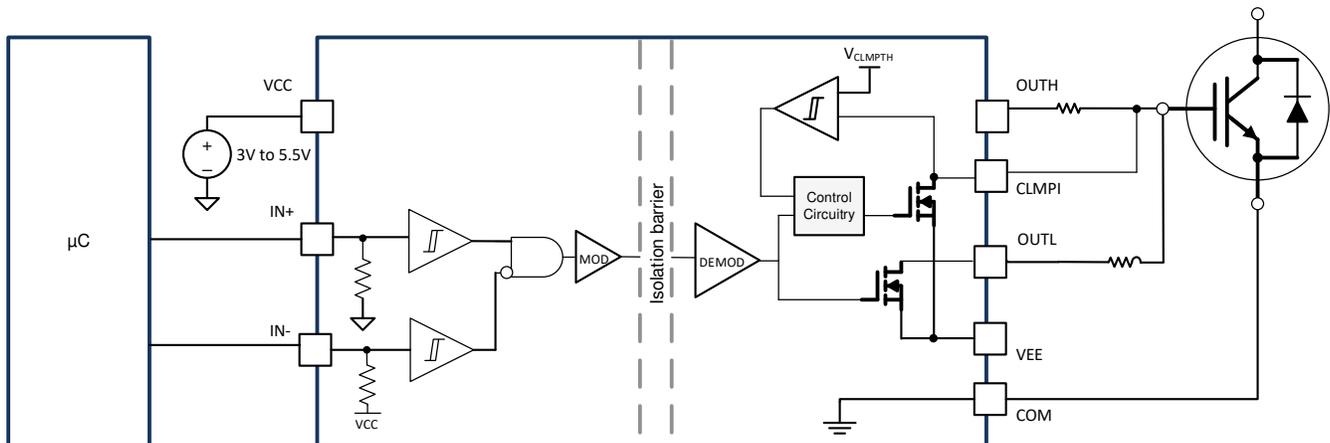


图 7-4. Active Miller Clamp

7.3.7 Overcurrent and Short Circuit Protection

The UCC21717-Q1 implements a fast overcurrent and short circuit protection feature to protect the SiC MOSFET or IGBT from catastrophic breakdown during fault. The OC pin of the device has a typical 0.7-V threshold with respect to COM, source or emitter of the power semiconductor. When the input is in floating condition, or the output is held in low state, the OC pin is pulled down by an internal MOSFET and held in LOW state, which prevents the overcurrent and short circuit fault from false triggering. The OC pin is in high-impedance state when the output is in high state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in on state. The internal pulldown MOSFET helps to discharge the voltage of OC pin when the power semiconductor is turned off.

The overcurrent and short circuit protection feature can be used with SiC MOSFET modules or IGBT modules with SenseFET, traditional desaturation circuit, or shunt resistor in series with the power loop for lower power applications, as shown in 图 7-5. For SiC MOSFET module or IGBT module with SenseFET, the SenseFET integrated in the module can scale down the drain current or collector current. With an external high precision sense resistor, the drain current or collector current can be accurately measured. If the voltage of the sensed resistor higher than the overcurrent threshold V_{OCTH} is detected, the soft turn-off is initiated. A fault will be reported to the input side \overline{FLT} pin to DSP/MCU. The output is held to LOW after the fault is detected, and can only be reset by the $\overline{RST/EN}$ pin. The state-of-art overcurrent and short circuit detection time helps to ensure a short shutdown time for SiC MOSFET and IGBT.

The overcurrent and short circuit protection feature can also be paired with desaturation circuit and shunt resistors. The DESAT threshold can be programmable in this case, which increases the versatility of the device. Detailed application diagrams of desaturation circuit and shunt resistor will be given in 节 8.2.2.6.

- High current and high di/dt during the overcurrent and short circuit fault can cause a voltage bounce on shunt resistor's parasitic inductance and board layout parasitic, which results in false trigger of OC pin. High precision, low ESL and small value resistor must be used in this approach.
- Shunt resistor approach is not recommended for high power applications and short circuit protection of the low power applications.

The detailed applications of the overcurrent and short circuit feature is discussed in 节 8.

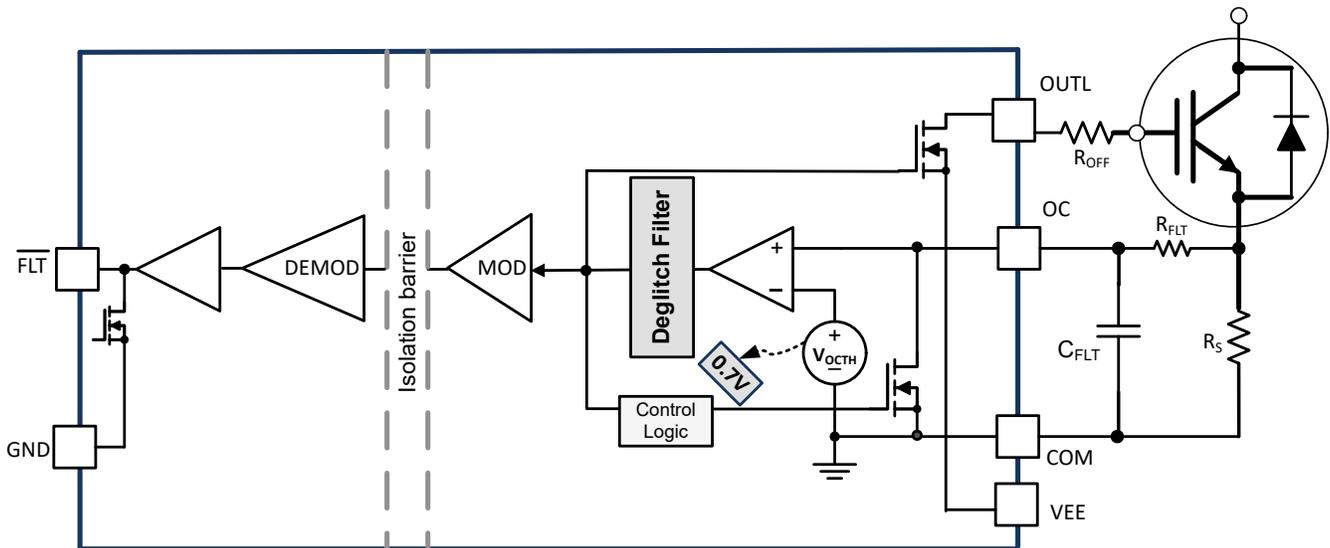


图 7-5. Overcurrent and Short Circuit Protection

7.3.8 Soft Turn-Off

The UCC21717-Q1 initiates a soft turn-off when the overcurrent and short circuit protection are triggered, or when the $\overline{RST/EN}$ is pulled low for longer than t_{RSTPD} . When the overcurrent and short circuit faults occur, the

power semiconductor transitions from the linear region to the saturation region very quickly. The gate voltage controls the channel current. By pulling down the gate voltage with a soft turn-off current, the di/dt of the channel current is controlled by the gate voltage and decreases softly; thus, overshooting the power semiconductor is limited, preventing overvoltage breakdown. 图 6-10 shows the the soft turn-off timing diagram.

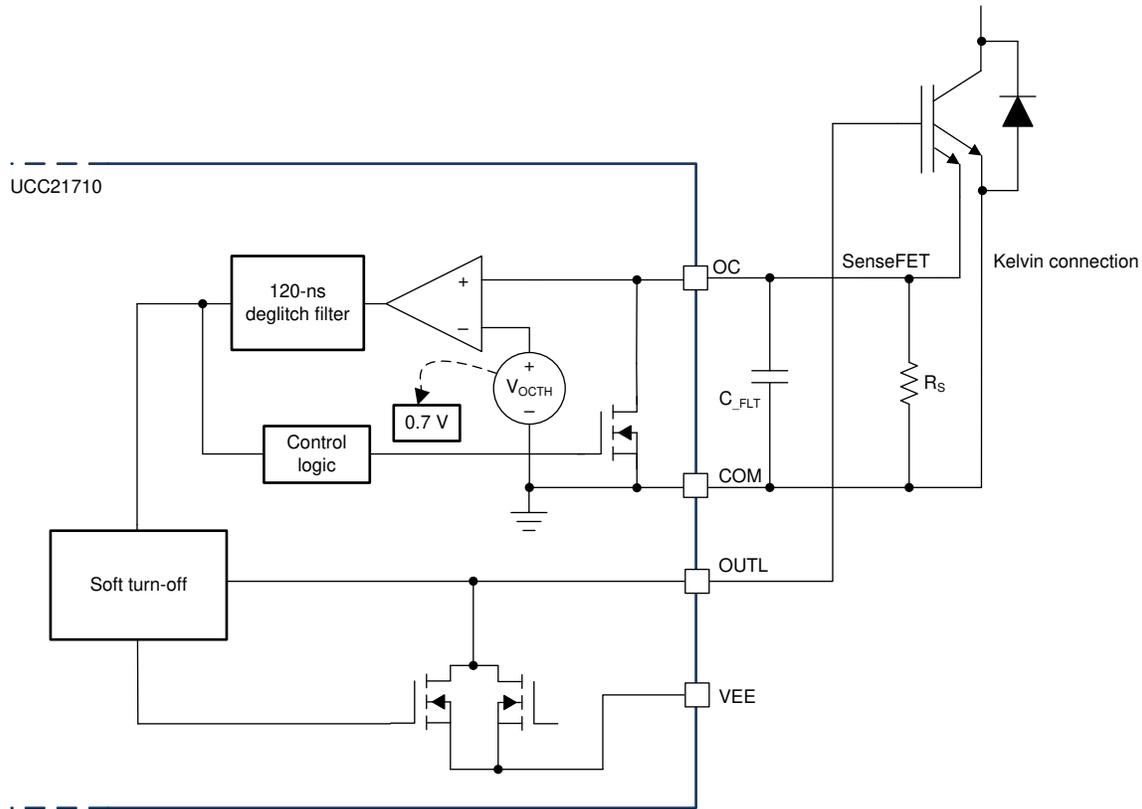


图 7-6. Soft Turn-Off

7.3.9 Fault (\overline{FLT}), Reset and Enable ($\overline{RST/EN}$)

The \overline{FLT} pin of the UCC21717-Q1 is open drain and can report a fault signal to the DSP/MCU when a fault is detected through the OC pin. The \overline{FLT} pin is pulled down to GND after the fault is detected, and is held low until a reset signal is received from $\overline{RST/EN}$. The device has a fault mute time $t_{FLTMUTE}$, within which the device ignores any reset signal.

The $\overline{RST/EN}$ is pulled down internally by a 50-k Ω resistor, and is thus disabled by default when this pin is floating. It must be pulled up externally to enable the driver. The pin has two purposes:

- To reset the \overline{FLT} pin. To reset, then $\overline{RST/EN}$ pin is pulled low; if the pin is set and held in low state for more than t_{RSTFIL} after the mute time $t_{FLTMUTE}$, then the fault signal is reset and \overline{FLT} is reset back to the high impedance status at the rising edge of the input signal at $\overline{RST/EN}$ pin.
- Enable and shutdown the device. If the $\overline{RST/EN}$ pin is pulled low for longer than t_{RSTPD} , the driver is disabled and OUTL is turned off with a soft turn off. The pin must be pulled up externally to enable the part, otherwise the device is disabled by default.

7.3.10 Isolated Analog to PWM Signal Function

The UCC21717-Q1 features an isolated analog to PWM signal function from AIN to APWM pin, which allows the isolated temperature sensing, high voltage dc bus voltage sensing, and so forth. An internal current source I_{AIN} in AIN pin is implemented in the device to bias an external thermal diode or temperature sensing resistor. The UCC21717-Q1 encodes the voltage signal V_{AIN} to a PWM signal, passing through the reinforced isolation

barrier, and output to APWM pin on the input side. The PWM signal can either be transferred directly to DSP/MCU to calculate the duty cycle, or filtered by a simple RC filter as an analog signal. The AIN voltage input range is from 0.6 V to 4.5 V, and the corresponding duty cycle of the APWM output ranges from 88% to 10%. The duty cycle increases linearly from 10% to 88% while the AIN voltage decreases from 4.5 V to 0.6 V. This corresponds to the temperature coefficient of the negative temperature coefficient (NTC) resistor and thermal diode. When AIN is floating, the AIN voltage is 5 V and the APWM operates at 400 kHz with approximately 10% duty cycle. The duty cycle absolute error is $\pm 1.5\%$ at 0.6 V and 2.5 V and is $+1.5\% / -2.5\%$ at 4.5 V across both process and temperature. The in-system accuracy can be improved using calibration to account for any offset. The accuracy of the internal current source I_{AIN} is $\pm 3\%$ across process and temperature.

The isolated analog to PWM signal feature can also support other analog signal sensing, such as the high voltage DC bus voltage, and so forth. The internal current source I_{AIN} should be taken into account when designing the potential divider if sensing a high voltage.

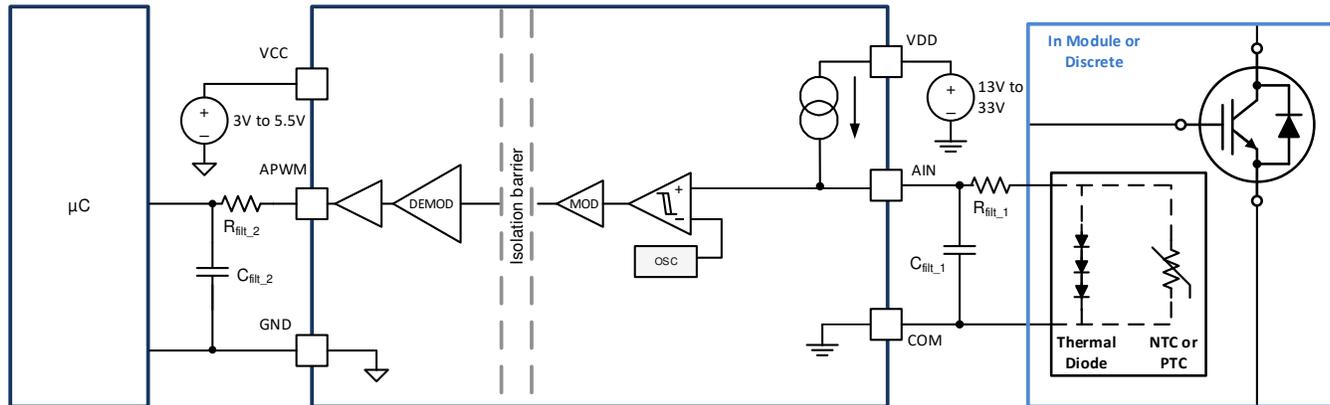


图 7-7. Isolated Analog to PWM Signal

7.4 Device Functional Modes

表 7-1 lists device function.

表 7-1. Function Table

| INPUT | | | | | | | OUTPUT | | | | |
|-------|------|------|------|------|--------|-----|--------|-----|---------------|-------|------|
| VCC | VDD | VEE | IN+ | IN- | RST/EN | AIN | RDY | FLT | OUTH/ OUTL | CLMPI | APWM |
| PU | PD | PU | X | X | X | X | Low | HiZ | Low | Low | Low |
| PD | PU | PU | X | X | X | X | HiZ | HiZ | Low | Low | Low |
| PU | PU | PU | X | X | Low | X | HiZ | HiZ | Low | Low | Low |
| PU | Open | PU | X | X | X | X | Low | HiZ | HiZ | HiZ | HiZ |
| PU | PU | Open | X | X | X | X | Low | HiZ | Low | Low | Low |
| PU | PU | PU | Low | X | High | X | HiZ | HiZ | Low | Low | P* |
| PU | PU | PU | X | High | High | X | HiZ | HiZ | Low | Low | P* |
| PU | PU | PU | High | High | High | X | HiZ | HiZ | Low | Low | P* |
| PU | PU | PU | High | Low | High | X | HiZ | HiZ | High | HiZ | P* |

PU: Power Up ($VCC \geq 2.85V$, $VDD \geq 13.1V$, $VEE \leq 0V$); PD: Power Down ($VCC \leq 2.35V$, $VDD \leq 9.9V$); X: Irrelevant; P*: PWM Pulse; HiZ: High Impedance

8 Applications and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The UCC21717-Q1 device is very versatile because of the strong drive strength, wide range of output power supply, high isolation ratings, high CMTI and superior protection and sensing features. The 1.5-kVRMS working voltage and 12.8-kVPK surge immunity can support both SiC MOSFET and IGBT modules with DC bus voltage up to 2121 V. The device can be used in both low power and high power applications such as the traction inverter in HEV/EV, on-board charger and charging pile, motor driver, solar inverter, industrial power supplies, and so forth. The device can drive the high power SiC MOSFET module, IGBT module, or paralleled discrete device directly without external buffer drive circuit based on NPN/PNP bipolar transistor in totem-pole structure, which allows the driver to have more control to the power semiconductor and saves the cost and space of the board design. The UCC21717-Q1 can also be used to drive very high power modules or paralleled modules with external buffer stage. The input side can support power supply and microcontroller signal from 3.3 V to 5 V, and the device level shifts the signal to output side through reinforced isolation barrier. The device has wide output power supply range from 13 V to 33 V and support wide range of negative power supply. This allows the driver to be used in SiC MOSFET applications, IGBT application and many others. The 12-V UVLO benefits the power semiconductor with lower conduction loss and improves the system efficiency. As a reinforced isolated single channel driver, the device can be used to drive either a low-side or high-side driver.

The UCC21717-Q1 device features extensive protection and monitoring features, which can monitor, report and protect the system from various fault conditions.

- Fast detection and protection for the overcurrent and short circuit fault. The feature is preferable in a split source SiC MOSFET module or a split emitter IGBT module. For the modules with no integrated current mirror or paralleled discrete semiconductors, the traditional desaturation circuit can be modified to implement short circuit protection. The semiconductor is shutdown when the fault is detected and FLT pin is pulled down to indicate the fault detection. The device is latched unless a reset signal is received from the RST/EN pin.
- Soft turn-off feature to protect the power semiconductor from catastrophic breakdown during overcurrent and short circuit fault. The shutdown energy can be controlled while the overshoot of the power semiconductor is limited.
- UVLO detection to protect the semiconductor from excessive conduction loss. Once the device is detected to be in UVLO mode, the output is pulled down and the RDY pin indicates the power supply is lost. The device is back to normal operation mode once the power supply is out of the UVLO status. The power good status can be monitored from the RDY pin.
- Analog signal sensing with isolated analog to PWM signal feature. This feature allows the device to sense the temperature of the semiconductor from the thermal diode or temperature sensing resistor, or dc bus voltage with resistor divider. A PWM signal is generated on the low voltage side with reinforced isolated from the high voltage side. The signal can be fed back to the microcontroller for the temperature monitoring, voltage monitoring, and so forth.
- The active Miller clamp feature protects the power semiconductor from false turn on by driving an external MOSFET. This feature allows flexibility of the board layout design and the pulldown strength of the Miller clamp FET.
- Enable and disable function through the $\overline{\text{RST/EN}}$ pin.
- Short circuit clamping.
- Active pulldown.

8.2 Typical Application

图 8-1 shows the typical application of a half bridge using two UCC21717-Q1 isolated gate drivers. The half bridge is a basic element in various power electronics applications such as a traction inverter in a HEV/EV to convert the DC current of the electric vehicle's battery to AC current to drive the electric motor in the propulsion system. The topology can also be used in motor drive applications to control the operating speed and torque of the AC motors.

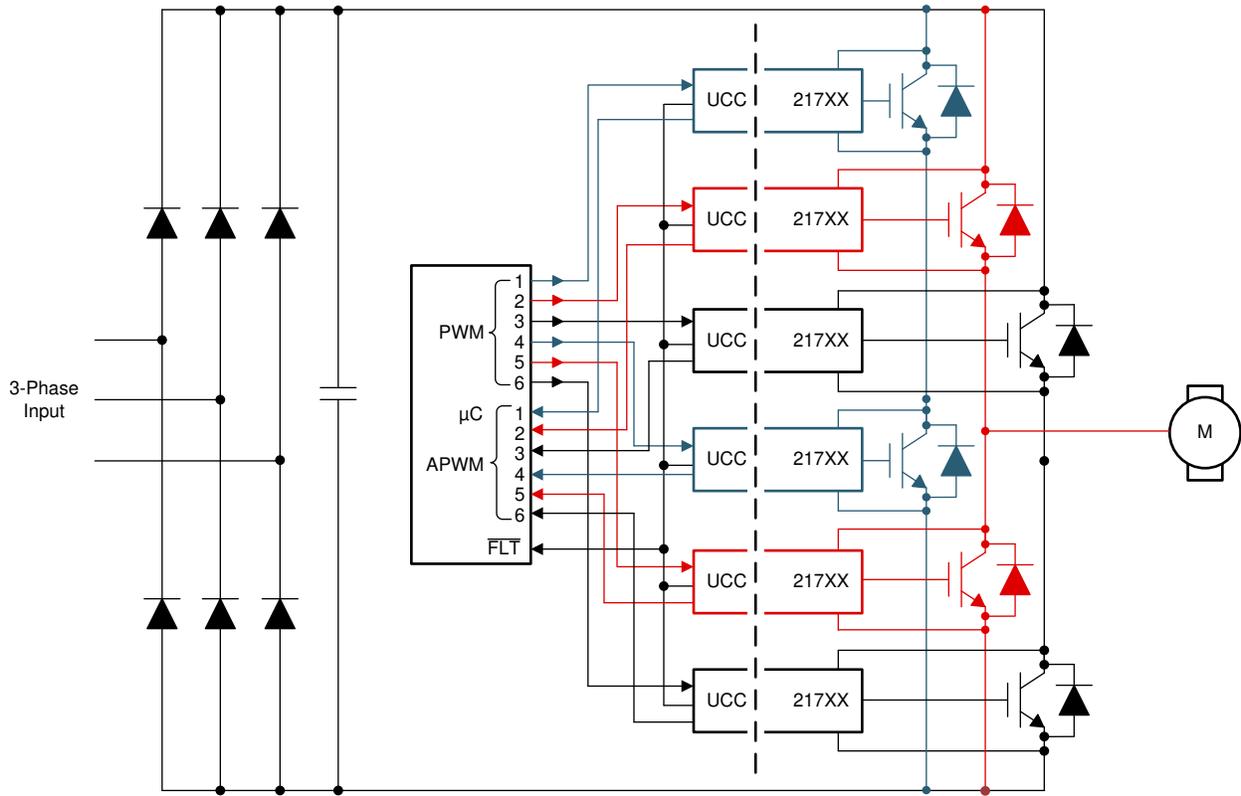


图 8-1. Typical Application Schematic

8.2.1 Design Requirements

The design of the power system for end equipment should consider some design requirements to ensure the reliable operation of the UCC1710 through the load range. Design considerations include peak source and sink currents, power dissipation, overcurrent and short circuit protection, AIN-APWM function for analog signal sensing, and so forth.

A design example for a half bridge based on IGBT is given in this subsection. The design parameters are listed in 表 8-1.

表 8-1. Design Parameters

| PARAMETER | VALUE |
|-----------------------------|--------------|
| Input Supply Voltage | 5 V |
| IN-OUT Configuration | Noninverting |
| Positive Output Voltage VDD | 15 V |
| Negative Output Voltage VEE | - 5 V |
| DC Bus Voltage | 800 V |
| Peak Drain Current | 300 A |
| Switching Frequency | 50 kHz |

表 8-1. Design Parameters (续)

| PARAMETER | VALUE |
|-------------|-------------|
| Switch Type | IGBT Module |

8.2.2 Detailed Design Procedure

8.2.2.1 Input Filters for IN+, IN-, and RST/EN

In the applications of traction inverter or motor drive, the power semiconductors are in hard switching mode. With the strong drive strength of the UCC21717-Q1, the dV/dt can be high, especially for SiC MOSFET. Noise cannot only be coupled to the gate voltage due to the parasitic inductance, but also to the input side as the nonideal PCB layout and coupled capacitance.

The UCC21717-Q1 features a 40-ns internal deglitch filter to the IN+, IN-, and $\overline{RST/EN}$ pins. Any signal less than 40 ns can be filtered out from the input pins. For noisy systems, external low-pass filter can be added externally to the input pins. Adding low-pass filters to IN+, IN-, and $\overline{RST/EN}$ pins can effectively increase the noise immunity and increase the signal integrity. When not in use, the IN+, IN-, and $\overline{RST/EN}$ pins should not be floating. IN- should be tied to GND if only IN+ is used for a noninverting input to output configuration. The purpose of the low-pass filter is to filter out the high frequency noise generated by the layout parasitics. While choosing the low-pass filter resistors and capacitors, both the noise immunity effect and delay time should be considered according to the system requirements.

8.2.2.2 PWM Interlock of IN+ and IN-

The UCC21717-Q1 features a PWM interlock for the IN+ and IN- pins, which can be used to prevent the phase leg shoot through issue. As shown in 表 7-1, the output is logic low while both IN+ and IN- are logic high. When only IN+ is used, IN- can be tied to GND. To utilize the PWM interlock function, the PWM signal of the other switch in the phase leg can be sent to the IN- pin. As shown in 图 8-2, PWM_T is the PWM signal to top side switch, and PWM_B is the PWM signal to bottom side switch. For the top side gate driver, the PWM_T signal is given to the IN+ pin, while the PWM_B signal is given to the IN- pin; for the bottom side gate driver, the PWM_B signal is given to the IN+ pin, while the PWM_T signal is given to the IN- pin. When both PWM_T and PWM_B signals are high, the outputs of both gate drivers are logic low to prevent the shoot through condition.

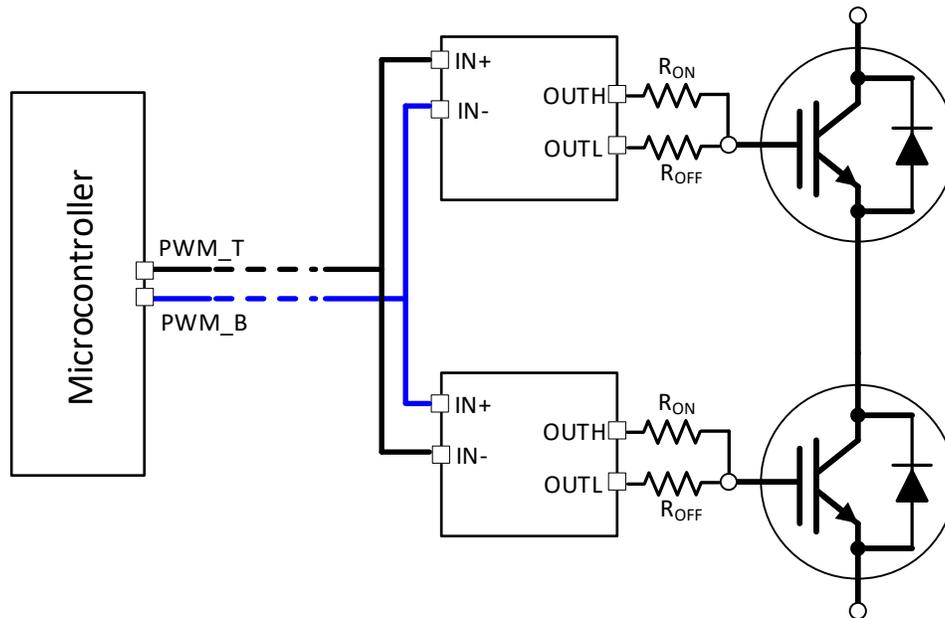


图 8-2. PWM Interlock for a Half Bridge

8.2.2.3 $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST/EN}}$ Pin Circuitry

Both $\overline{\text{FLT}}$ and RDY pins are open-drain outputs. The $\overline{\text{RST/EN}}$ pin has a 50-k Ω internal pulldown resistor, so the driver is in OFF status if the $\overline{\text{RST/EN}}$ pin is not pulled up externally. A 5-k Ω resistor can be used as pullup resistor for the $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST/EN}}$ pins.

To improve the noise immunity due to the parasitic coupling and common-mode noise, low-pass filters can be added between the $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST/EN}}$ pins and the microcontroller. A filter capacitor between 100 pF to 300 pF can be added.

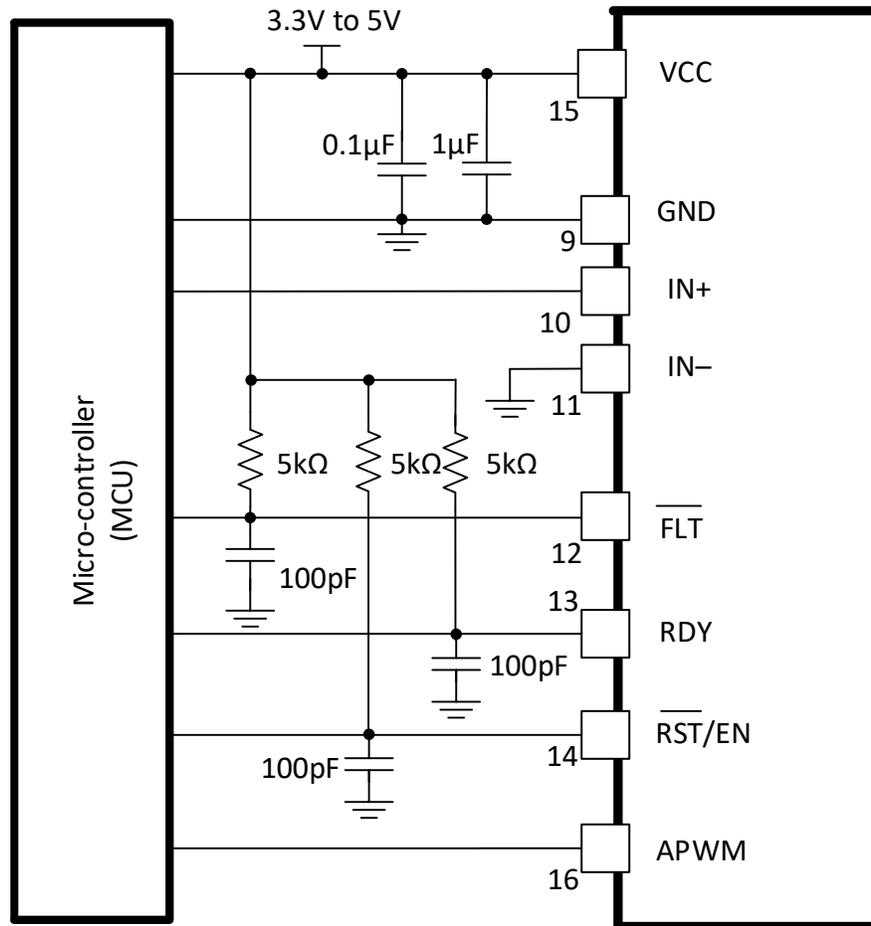


图 8-3. $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST/EN}}$ Pins Circuitry

8.2.2.4 $\overline{\text{RST/EN}}$ Pin Control

The $\overline{\text{RST/EN}}$ pin has two functions. It is used to enable or shutdown the outputs of the driver and to reset the fault signaled on the $\overline{\text{FLT}}$ pin after OC is detected. The $\overline{\text{RST/EN}}$ pin needs to be pulled up to enable the device; when the pin is pulled down, the device is in disabled status. By default the driver is disabled with the internal 50-k Ω pulldown resistor at this pin.

When the driver is latched after overcurrent or a short circuit fault is detected, the $\overline{\text{FLT}}$ pin and output are latched low and need to be reset by the $\overline{\text{RST/EN}}$ pin. The microcontroller must send a signal to the $\overline{\text{RST/EN}}$ pin after the fault to reset the driver. The driver will not respond until after the mute time t_{FLTMUTE} . The reset signal must be held low for at least t_{RSTFIL} after the mute time.

This pin can also be used to automatically reset the driver. The continuous input signal IN+ or IN- can be applied to the $\overline{\text{RST/EN}}$ pin. There is no separate reset signal from the microcontroller when configuring the driver this way. If the PWM is applied to the noninverting input IN+, then IN+ can also be tied to the $\overline{\text{RST/EN}}$ pin. If the

PWM is applied to the inverting input IN-, then a NOT logic is needed between the PWM signal from the microcontroller and the RST/EN pin. Using either configuration results in the driver being reset in every switching cycle without an extra control signal from the microcontroller tied to the RST/EN pin. One must ensure the PWM off-time is greater than t_{RSTFIL} in order to reset the driver in cause of an OC fault.

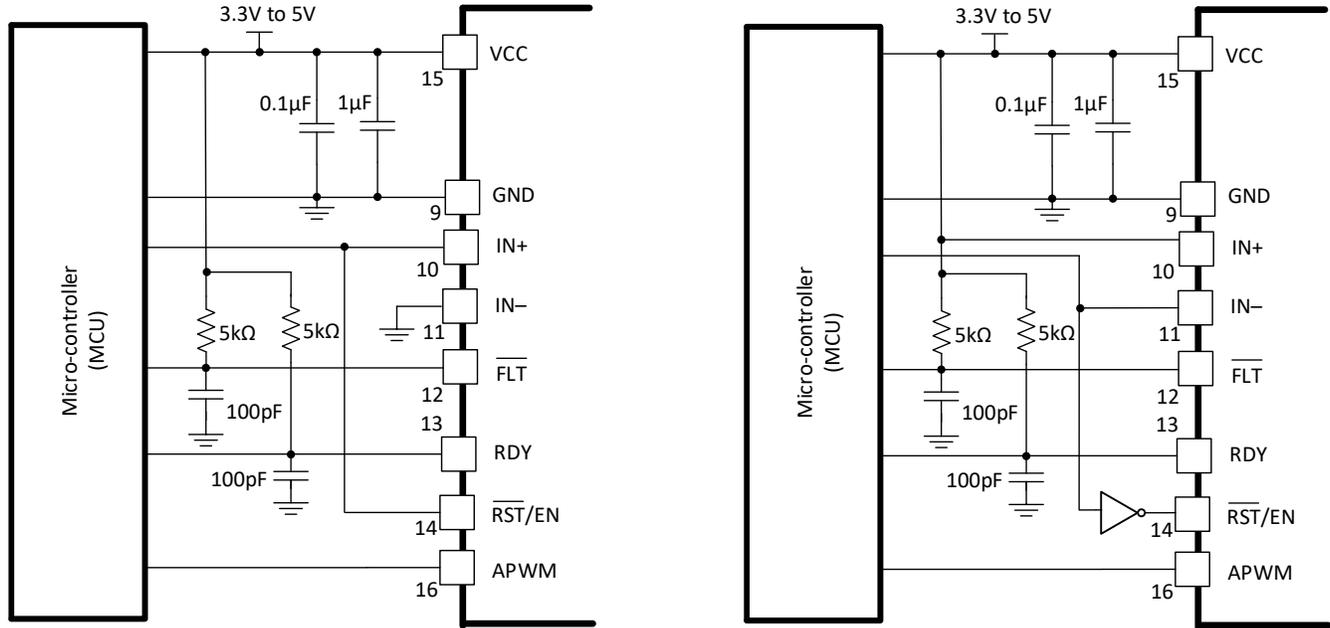


图 8-4. Automatic Reset Control

8.2.2.5 Turn-On and Turn-Off Gate Resistors

The UCC21717-Q1 features split outputs OUTH and OUTL, which enables independent control of the turn on and turn off switching speeds. The turn on and turn off resistances determine the peak source and sink currents, which control the switching speed in turn. Meanwhile, power dissipation in the gate driver should be considered to ensure the device is in the thermal limit. At first, the peak source and sink currents are calculated as:

$$I_{source_pk} = \min\left(10A, \frac{VDD - VEE}{R_{OH_EFF} + R_{ON} + R_{G_Int}}\right)$$

$$I_{sink_pk} = \min\left(10A, \frac{VDD - VEE}{R_{OL} + R_{OFF} + R_{G_Int}}\right) \quad (1)$$

Where

- R_{OH_EFF} is the effective internal pull-up resistance of the hybrid pull-up structure, which is approximately $2 \times R_{OL}$, about 0.7Ω .
- R_{OL} is the internal pulldown resistance, about 0.3Ω .
- R_{ON} is the external turn on gate resistance.
- R_{OFF} is the external turn off gate resistance.
- R_{G_Int} is the internal resistance of the SiC MOSFET or IGBT module.

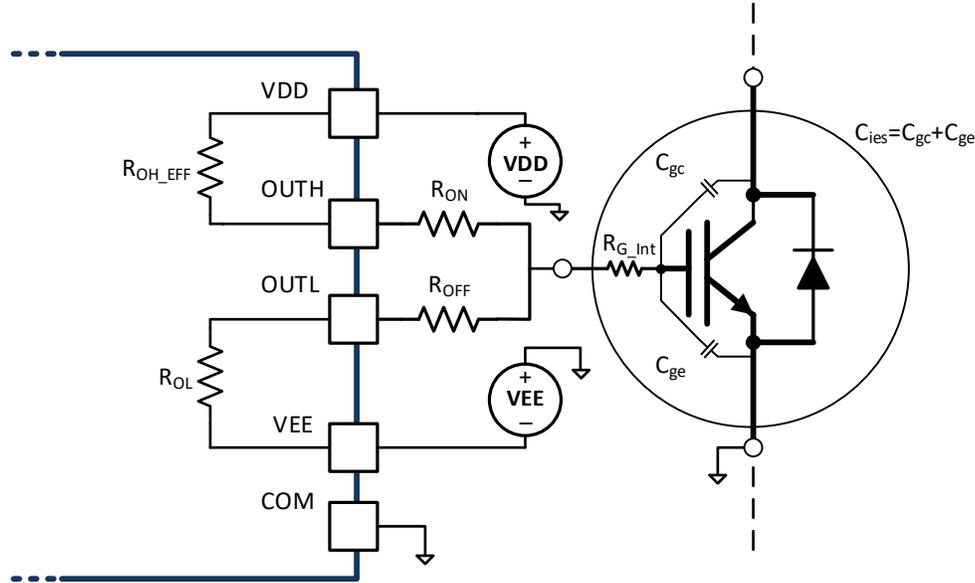


图 8-5. Output Model for Calculating Peak Gate Current

For example, for an IGBT module based system with the following parameters:

- $Q_g = 3300 \text{ nC}$
- $R_{G_Int} = 1.7 \text{ } \Omega$
- $R_{ON} = R_{OFF} = 1 \text{ } \Omega$

The peak source and sink currents in this case are:

$$I_{\text{source_pk}} = \min\left(10\text{A}, \frac{V_{\text{DD}} - V_{\text{VEE}}}{R_{\text{OH_EFF}} + R_{\text{ON}} + R_{\text{G_Int}}}\right) \approx 5.9\text{A}$$

$$I_{\text{sink_pk}} = \min\left(10\text{A}, \frac{V_{\text{DD}} - V_{\text{VEE}}}{R_{\text{OL}} + R_{\text{OFF}} + R_{\text{G_Int}}}\right) \approx 6.7\text{A} \quad (2)$$

Thus by using a 1- Ω external gate resistance, the peak source current is 5.9 A and the peak sink current is 6.7 A. The collector-to-emitter dV/dt during the turn on switching transient is dominated by the gate current at the Miller plateau voltage. The hybrid pullup structure ensures the peak source current at the Miller plateau voltage, unless the turn on gate resistor is too high. The faster the collector-to-emitter, V_{ce} , voltage rises to V_{DC} , the smaller the turn on switching loss is. The dV/dt can be estimated as $Q_{\text{gc}}/I_{\text{source_pk}}$. For the turn off switching transient, the drain-to-source dV/dt is dominated by the load current, unless the turn off gate resistor is too high. After V_{ce} reaches the dc bus voltage, the power semiconductor is in saturation mode and the channel current is controlled by V_{ge} . The peak sink current determines the dI/dt , which dominates the V_{ce} voltage overshoot accordingly. If using relatively large turn off gate resistance, the V_{ce} overshoot can be limited. The overshoot can be estimated by:

$$\Delta V_{\text{ce}} = L_{\text{stray}} \cdot I_{\text{load}} / ((R_{\text{OFF}} + R_{\text{OL}} + R_{\text{G_Int}}) \cdot C_{\text{ies}} \cdot \ln(V_{\text{plat}} / V_{\text{th}})) \quad (3)$$

Where

- L_{stray} is the stray inductance in power switching loop, as shown in 图 8-6
- I_{load} is the load current, which is the turn off current of the power semiconductor.
- C_{ies} is the input capacitance of the power semiconductor.
- V_{plat} is the plateau voltage of the power semiconductor.

- V_{th} is the threshold voltage of the power semiconductor.

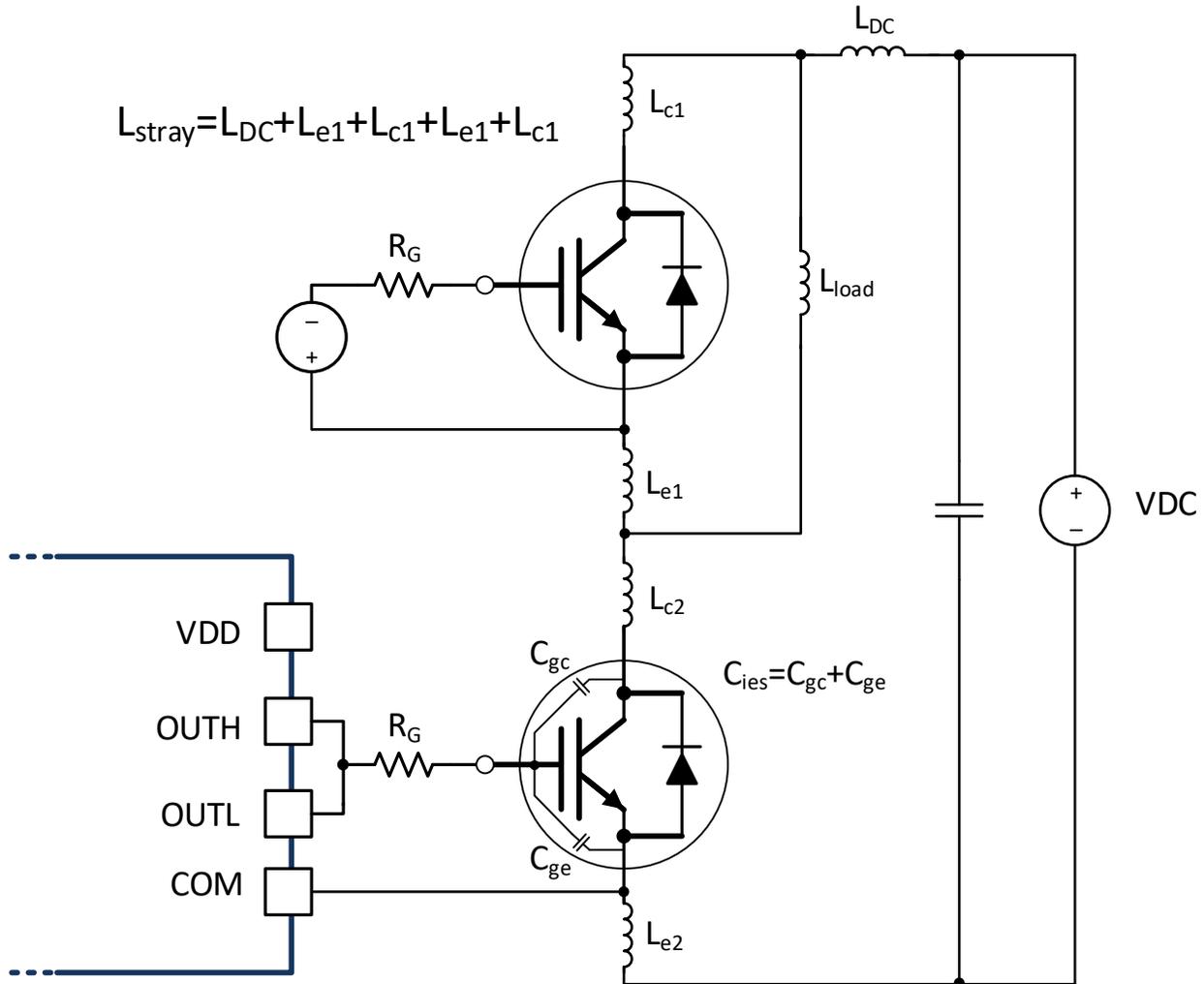


图 8-6. Stray Parasitic Inductance of IGBTs in a Half-Bridge Configuration

Power dissipation should be taken into account to maintain the gate driver within the thermal limit. The power loss of the gate driver includes the quiescent loss and the switching loss, which can be calculated as:

$$P_{DR} = P_Q + P_{SW} \quad (4)$$

P_Q is the quiescent power loss for the driver, which is $I_q \times (V_{DD} - V_{EE}) = 5 \text{ mA} \times 20 \text{ V} = 0.100 \text{ W}$. The quiescent power loss is the power consumed by the internal circuits such as the input stage, reference voltage, logic circuits, protection circuits when the driver is switching when the driver is biased with VDD and VEE, and also the charging and discharging current of the internal circuit when the driver is switching. The power dissipation when the driver is switching can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH_EFF}}{R_{OH_EFF} + R_{ON} + R_{G_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G_Int}} \right) \cdot (V_{DD} - V_{EE}) \cdot f_{sw} \cdot Q_g \quad (5)$$

Where

- Q_g is the gate charge required at the operation point to fully charge the gate voltage from VEE to VDD.
- f_{sw} is the switching frequency.

In this example, the P_{SW} can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH_EFF}}{R_{OH_EFF} + R_{ON} + R_{G_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G_Int}} \right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g = 0.505W \quad (6)$$

Thus, the total power loss is:

$$P_{DR} = P_Q + P_{SW} = 0.10W + 0.505W = 0.605W \quad (7)$$

When the board temperature is 125°C, the junction temperature can be estimated as:

$$T_j = T_b + \psi_{jb} \cdot P_{DR} \approx 150^\circ C \quad (8)$$

Therefore, for the application in this example, with 125°C board temperature, the maximum switching frequency is ~50 kHz to keep the gate driver in the thermal limit. By using a lower switching frequency, or increasing external gate resistance, the gate driver can be operated at a higher switching frequency.

8.2.2.6 Overcurrent and Short Circuit Protection

Fast and reliable overcurrent and short circuit protection is important to protect the catastrophic break down of the SiC MOSFET and IGBT modules, and improve the system reliability. The UCC21717-Q1 features a state-of-art overcurrent and short circuit protection, which can be applied to both SiC MOSFET and IGBT modules with various detection circuits.

8.2.2.6.1 Protection Based on Power Modules with Integrated SenseFET

The overcurrent and short circuit protection function is suitable for SiC MOSFET and IGBT modules with integrated SenseFET. The SenseFET scales down the main power loop current and outputs the current with a dedicated pin of the power module. With an external high precision sensing resistor, the scaled down current can be measured and the main power loop current can be calculated. The value of the sensing resistor R_S sets the protection threshold of the main current. For example, with a ratio of 1:N = 1:50000 of the integrated current mirror, by using R_S of 20 Ω , the threshold protection current is:

$$I_{OC_TH} = \frac{V_{OCTH}}{R_S} \cdot N = 1750A \quad (9)$$

The overcurrent and short circuit protection based on an integrated SenseFET has high precision, as it is sensing the current directly. The accuracy of the method is related to two factors: the scaling down ratio of the main power loop current and the SenseFET, and the precision of the sensing resistor. Since the current is sensed from the SenseFET, which is isolated from the main power loop, and the current is scaled down significantly with much less di/dt , the sensing loop has good noise immunity. To further improve the noise immunity, a low-pass filter can be added. A 100-pF to 10-nF filter capacitor can be added. The delay time caused by the low-pass filter should also be considered for the protection circuitry design.

detection threshold voltage of the driver. A parallel schottky diode can be connected between OC and COM pins to prevent the negative voltage on the OC pin in a noisy system. Since the desaturation circuit measures the V_{CE} of the IGBT or V_{DS} of the SiC MOSFET, not directly the current, the accuracy of the protection is not as high as the SenseFET based protection method. The current threshold cannot be accurately controlled in the protection.

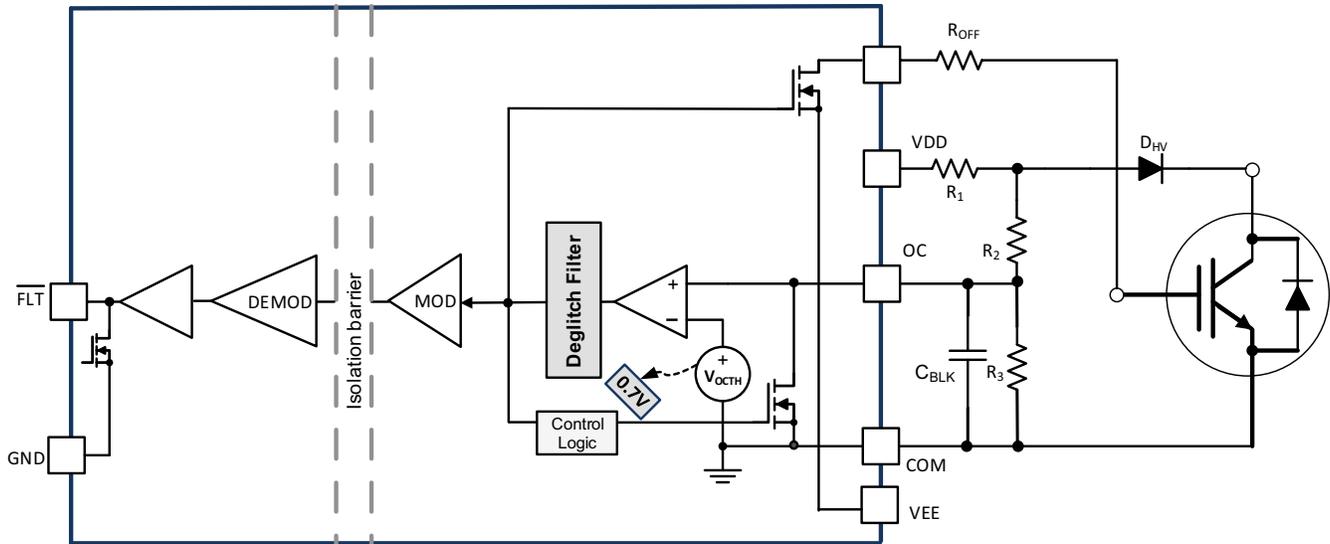


图 8-8. Overcurrent and Short Circuit Protection Based on Desaturation Circuit

8.2.2.6.3 Protection Based on Shunt Resistor in Power Loop

In lower power applications, to simplify the circuit and reduce the cost, a shunt resistor can be used in series in the power loop and measure the current directly. Since the resistor is in series in the power loop, it directly measures the current and can have high accuracy by using a high precision resistor. The resistance needs to be small to reduce the power loss, and should have large enough voltage resolution for the protection. Since the sensing resistor is also in series in the gate driver loop, the voltage drop on the sensing resistor can cause the voltage drop on the gate voltage of the IGBT or SiC MOSFET module. The parasitic inductance of the sensing resistor and the PCB trace of the sensing loop also causes a noise voltage source during the switching transient, which makes the gate voltage oscillate. Thus, this method is not recommended for a high power application, or when di/dt is high. To use it in a low power application, the shunt resistor loop should be designed to have optimal voltage drop and minimum noise injection to the gate loop.

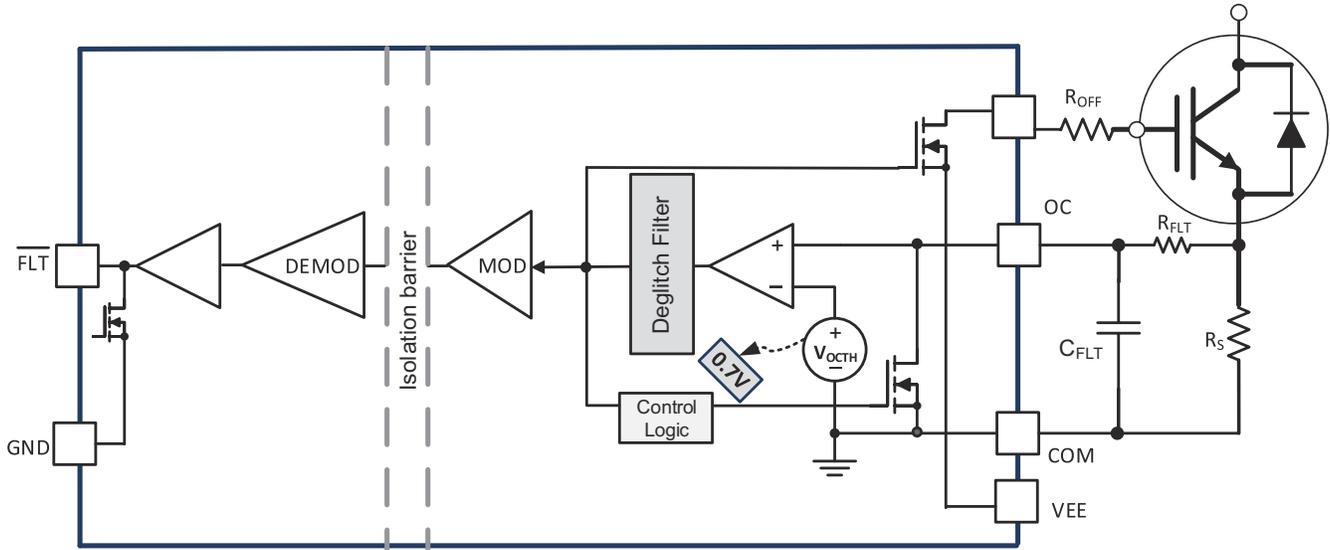


图 8-9. Overcurrent and Short Circuit Protection Based on Shunt Resistor

8.2.2.7 Isolated Analog Signal Sensing

The isolated analog signal sensing feature provides a simple isolated channel for isolated temperature detection, voltage sensing, and so forth. One typical application of this function is a temperature monitor of the power semiconductor. Thermal diodes or temperature sensing resistors are integrated in the SiC MOSFET or IGBT module close to the dies to monitor the junction temperature. The UCC21717-Q1 has an internal 203- μ A current source with $\pm 3\%$ accuracy across temperature, which can forward bias the thermal diodes or create a voltage drop on the temperature sensing resistors. The sensed voltage from the AIN pin is passed through the isolation barrier to the input side and transformed to a PWM signal. The duty cycle of the PWM changes linearly from 10% to 88% when the AIN voltage changes from 4.5 V to 0.6 V and can be represented using 方程式 12.

$$D_{APWM}(\%) = -20 * V_{AIN} + 100 \quad (12)$$

8.2.2.7.1 Isolated Temperature Sensing

A typical application circuit is shown in 图 8-10. To sense temperature, the AIN pin is connected to the thermal diode or thermistor which can be discrete or integrated within the power module. A low-pass filter is recommended for the AIN input. Since the temperature signal does not have a high bandwidth, the low-pass filter is mainly used for filtering the noise introduced by the switching of the power device, which does not require stringent control for propagation delay. The filter capacitance for C_{filt} can be chosen between 1 nF to 100 nF and the filter resistance R_{filt} between 1 Ω to 10 Ω according to the noise level.

The output of APWM is directly connected to the microcontroller to measure the duty cycle dependent on the voltage input at AIN, using 方程式 12.

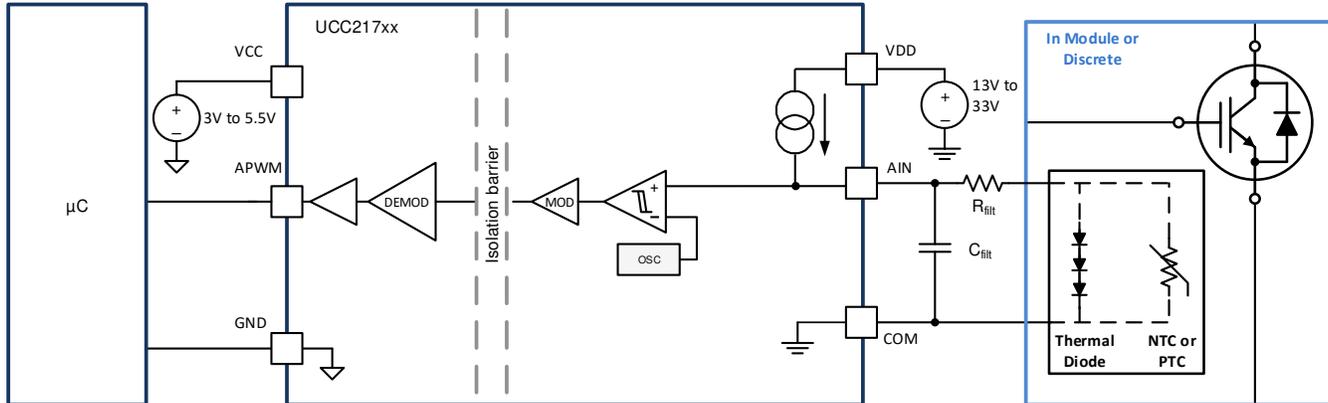


图 8-10. Thermal Diode or Thermistor Temperature Sensing Configuration

When a high-precision voltage supply for VCC is used on the primary side of the UCC21717-Q1 the duty cycle output of APWM may also be filtered and the voltage measured using the microcontroller's ADC input pin, as shown in 图 8-11. The frequency of APWM is 400 kHz, so the value for R_{filt_2} and C_{filt_2} should be such that the cutoff frequency is below 400 kHz. Temperature does not change rapidly, thus the rise time due to the RC constant of the filter is not under a strict requirement.

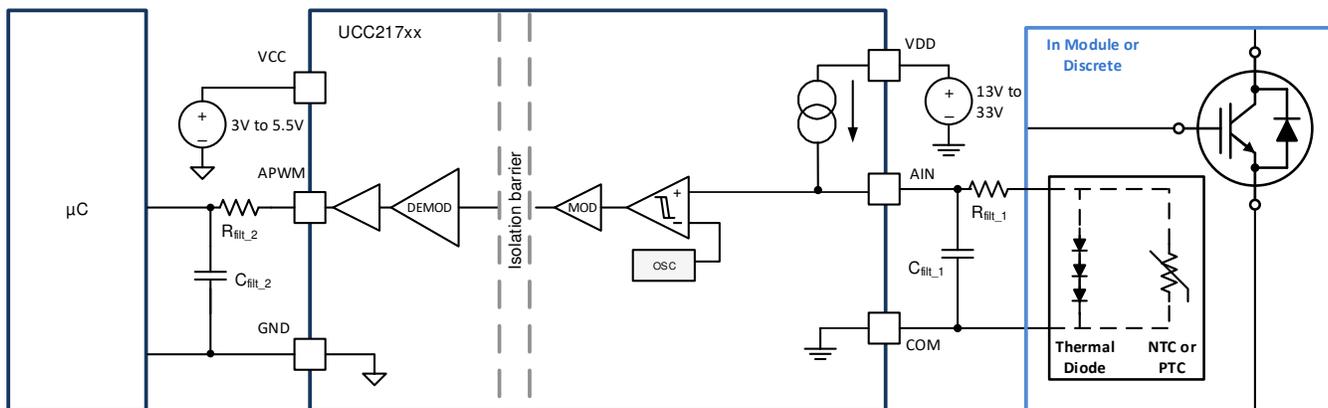


图 8-11. APWM Channel with Filtered Output

The example below shows the results using a 4.7-k Ω NTC, NTCS0805E3472FMT, in series with a 3-k Ω resistor and also the thermal diode using four diode-connected MMBT3904 NPN transistors. The sensed voltage of the four MMBT3904 thermal diodes connected in series ranges from about 2.5 V to 1.6 V from 25°C to 135°C, corresponding to 50% to 68% duty cycle. The sensed voltage of the NTC thermistor connected in series with the 3-k Ω resistor ranges from about 1.5 V to 0.6 V from 25°C to 135°C, corresponding to 70% to 88% duty cycle. The voltage at VAIN of both sensors and the corresponding measured duty cycle at APWM is shown in 图 8-12.

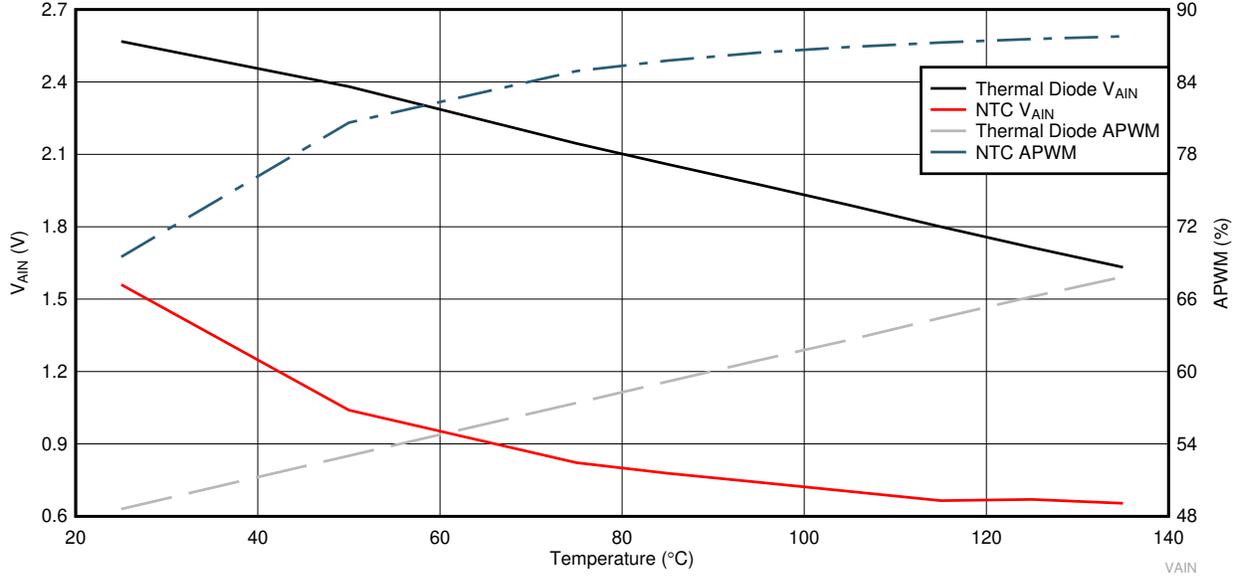


图 8-12. Thermal Diode and NTC V_{AIN} and Corresponding Duty Cycle at APWM

The duty cycle output has an accuracy of $\pm 3\%$ throughout temperature without any calibration, as shown in 图 8-13 but with single-point calibration at 25°C, the duty accuracy can be improved to $\pm 1\%$, as shown in 图 8-14.

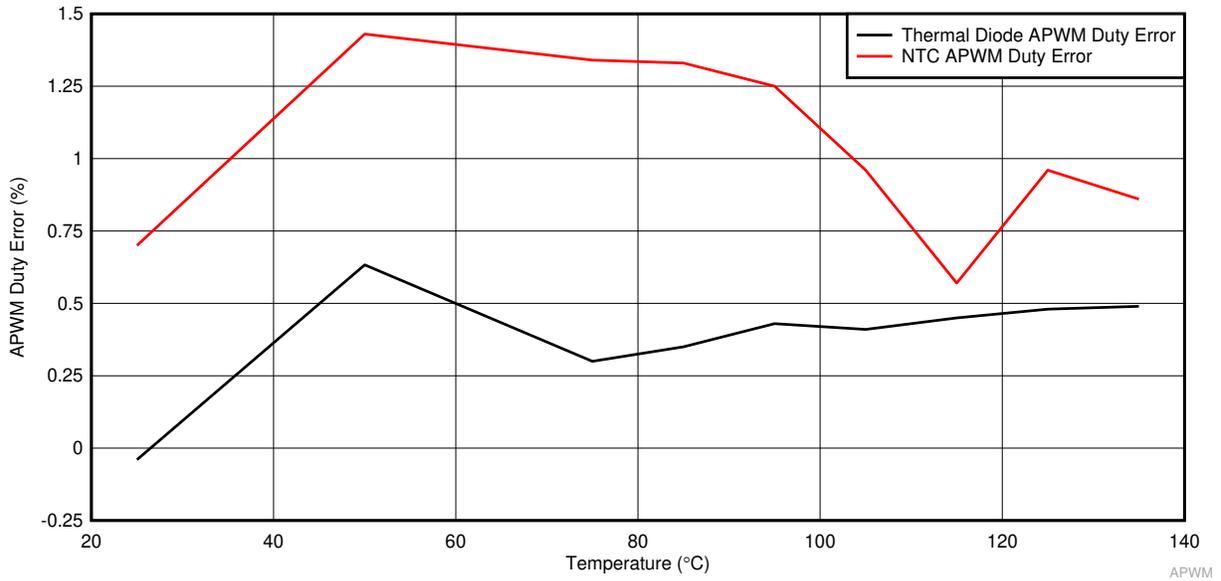


图 8-13. APWM Duty Error without Calibration

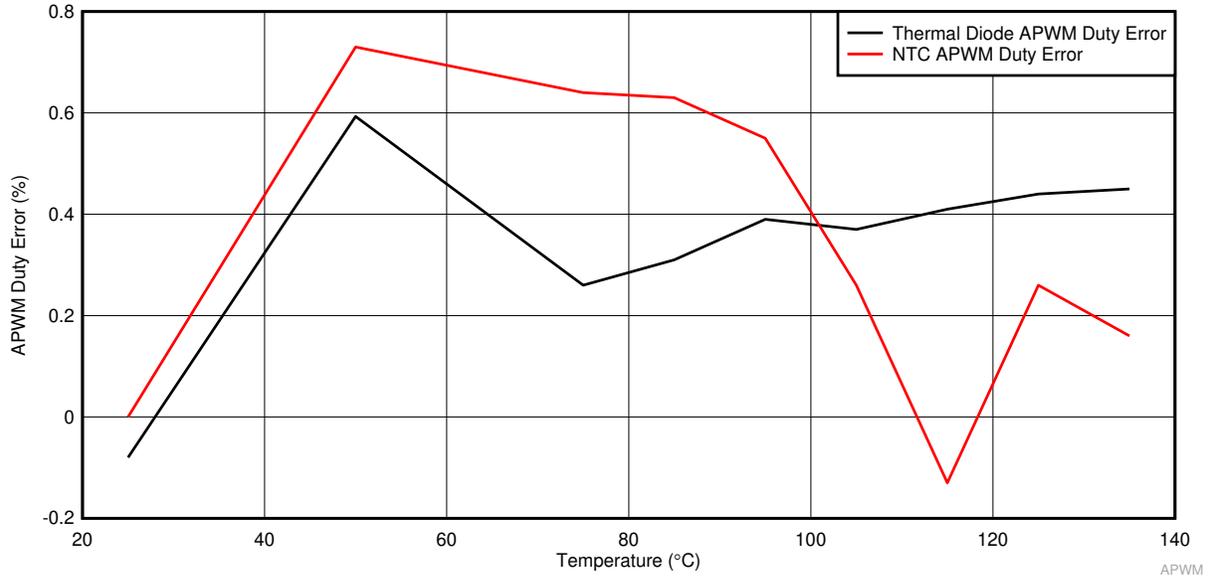


图 8-14. APWM Duty Error with Single-Point Calibration

8.2.2.7.2 Isolated DC Bus Voltage Sensing

The AIN to APWM channel may be used for other applications such as the DC-link voltage sensing, as shown in 图 8-15. The same filtering requirements as given above may be used in this case, as well. The number of attenuation resistors, R_{atten_1} through R_{atten_n} , is dependent on the voltage level and power rating of the resistor. The voltage is finally measured across R_{LV_DC} to monitor the stepped-down voltage of the HV DC-link which must fall within the voltage range of AIN from 0.6 V to 4.5 V. The driver should be referenced to the same point as the measurement reference, thus in the case shown below the UCC21717-Q1 is driving the lower IGBT in the half bridge and the DC-link voltage measurement is referenced to COM. The internal current source I_{AIN} should be taken into account when designing the resistor divider. The AIN pin voltage is:

$$V_{AIN} = \frac{R_{LV_DC}}{R_{LV_DC} + \sum_{i=1}^n R_{atten_i}} \cdot V_{DC} + R_{LV_DC} \cdot I_{AIN} \quad (13)$$

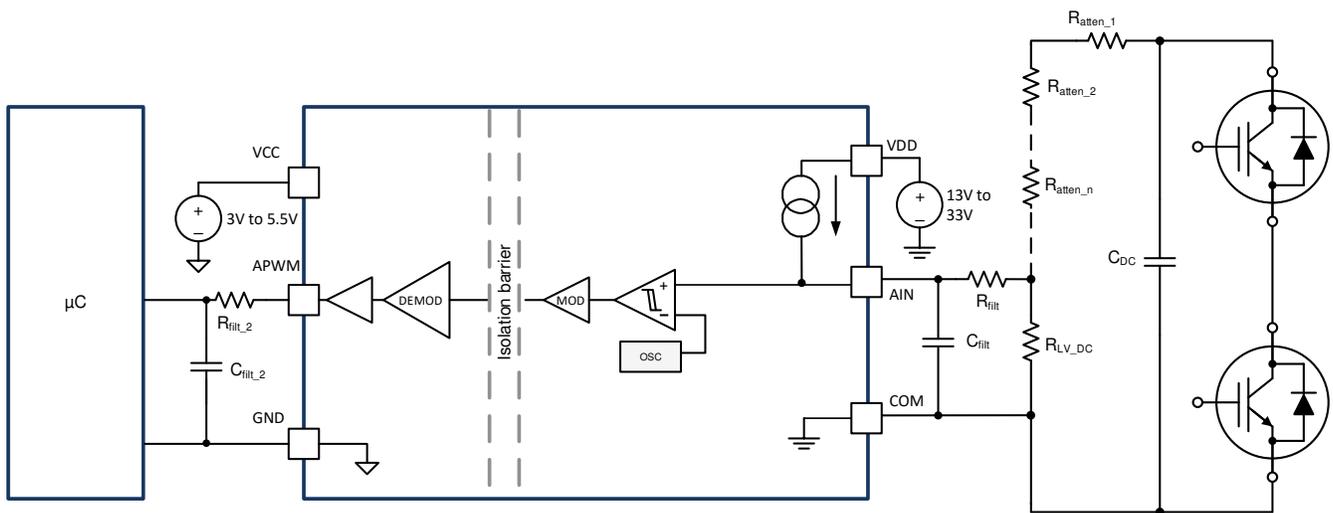


图 8-15. DC-Link Voltage Sensing Configuration

8.2.2.8 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a noninverting current buffer (such as the NPN/PNP buffer shown in 图 8-16) can be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for peak currents up to 15 A, the D44VH10/ D45VH10 pair is up to 20-A peak.

In the case of an overcurrent detection, the soft turn off (STO) is activated. External components must be added to implement STO instead of normal turn off speed when an external buffer is used. C_{STO} sets the timing for soft turn off and R_{STO} limits the inrush current to below the current rating of the internal FET (10 A). R_{STO} should be at least $(VDD-VEE)/10$. The soft turn off timing is determined by the internal current source of 400 mA and the capacitor C_{STO} . C_{STO} is calculated using 方程式 14.

$$C_{STO} = \frac{I_{STO} \cdot t_{STO}}{VDD - VEE} \quad (14)$$

- I_{STO} is the the internal STO current source, 400 mA
- t_{STO} is the desired STO timing

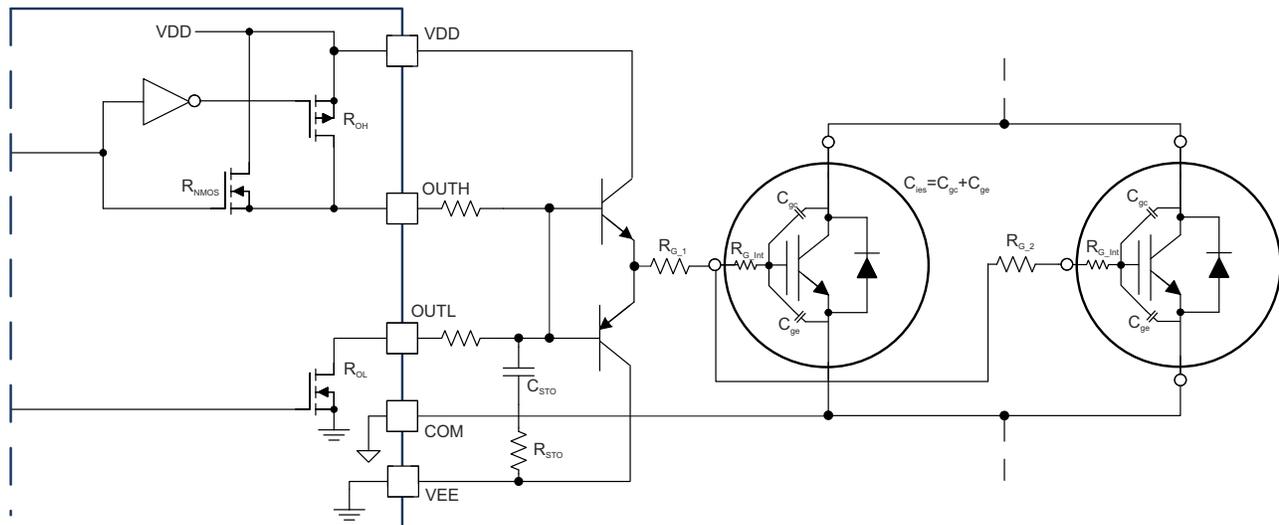


图 8-16. Current Buffer for Increased Drive Strength

9 Power Supply Recommendations

During the turn on and turn off switching transient, the peak source and sink currents are provided by the VDD and VEE power supply. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and ensure a reliable operation, a set of decoupling capacitors are recommended at the power supplies. Considering the UCC21717-Q1 has ± 10 -A peak drive strength and can generate high dV/dt , a 10- μ F bypass capacitor is recommended between VDD and COM, VEE and COM. A 1- μ F bypass capacitor is recommended between VCC and GND due to less current comparing with output side power supplies. A 0.1- μ F decoupling capacitor is also recommended for each power supply to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC, VDD, and VEE pins to prevent noise coupling from the system parasitics of the PCB layout.

10 Layout

10.1 Layout Guidelines

Due to the strong drive strength of the UCC21717-Q1, careful considerations must be taken in the PCB design. Below are some key points:

- The driver should be placed as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
- The decoupling capacitors of the input and output power supplies should be placed as close as possible to the power supply pins. The peak current generated at each switching transient can cause high di/dt and voltage spike on the parasitic inductance of the PCB traces.
- The driver COM pin should be connected to the Kelvin connection of the SiC MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- Use a ground plane on the input side to shield the input signals. The input signals can be distorted by the high frequency noise generated by the output side switching transients. The ground plane provides a low-inductance filter for the return current flow.
- If the gate driver is used for the low-side switch, which the COM pin is connected to the dc bus negative, use the ground plane on the output side to shield the output signals from the noise generated by the switch node. If the gate driver is used for the high-side switch, which the COM pin is connected to the switch node, the ground plane is not recommended.
- If the ground plane is not used on the output side, separate the return path of the OC and AIN ground loop from the gate loop ground which has large peak source and sink currents.
- No PCB trace or copper is allowed under the gate driver. A PCB cutout is recommended to avoid any noise coupling between the input and output side which can contaminate the isolation barrier.

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- [Isolation Glossary](#)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 支持资源

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

12 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision A (June 2023) to Revision B (June 2024) | Page |
|---|------|
| • 更改了器件温度等级..... | 1 |
| • 从“特性”中删除了 ESD 分类..... | 1 |
| • Deleted ESD classifications from Specifications..... | 4 |

| Changes from Revision * (April 2022) to Revision A (June 2023) | Page |
|--|------|
| • 将销售状态从“预告信息”更改为“量产数据”..... | 1 |

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| UCC21717QDWRQ1 | Active | Production | SOIC (DW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC21717Q |
| UCC21717QDWRQ1.A | Active | Production | SOIC (DW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC21717Q |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

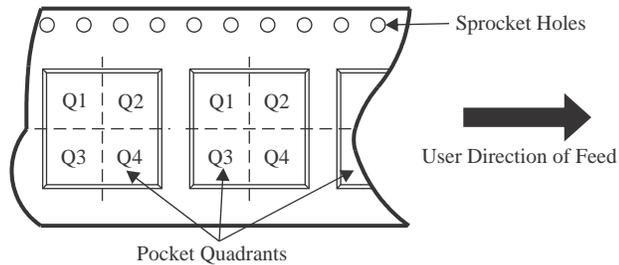
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UCC21717QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UCC21717QDWRQ1 | SOIC | DW | 16 | 2000 | 353.0 | 353.0 | 32.0 |

GENERIC PACKAGE VIEW

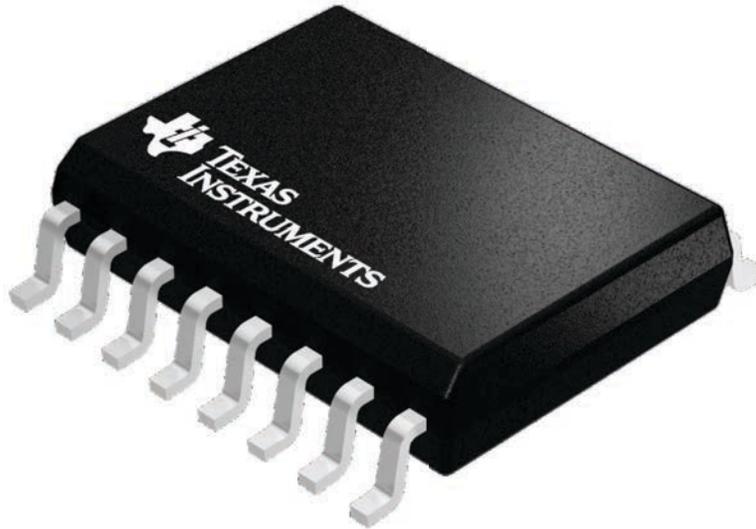
DW 16

SOIC - 2.65 mm max height

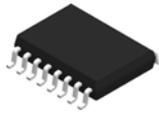
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



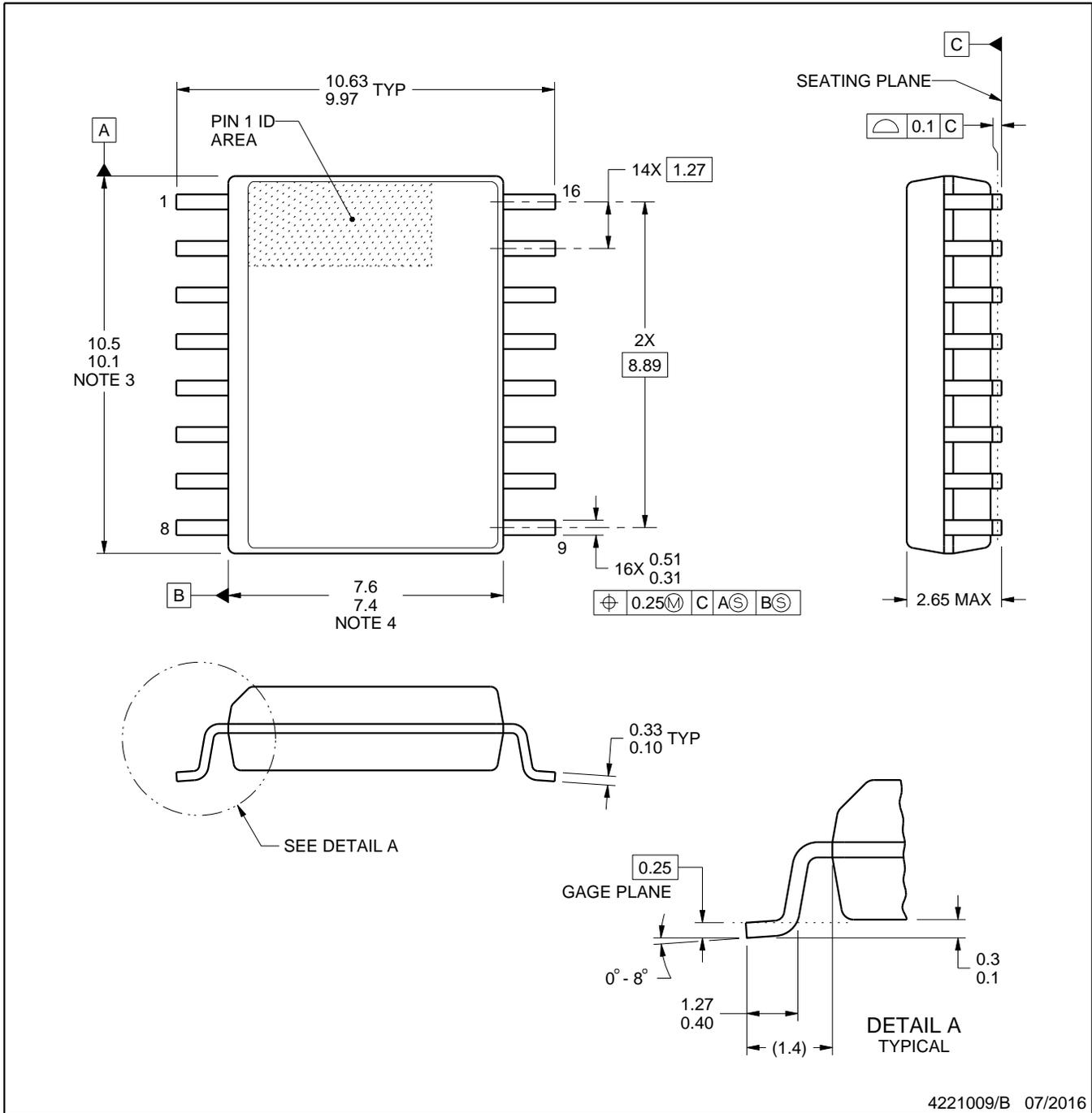
4224780/A



DW0016B

PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

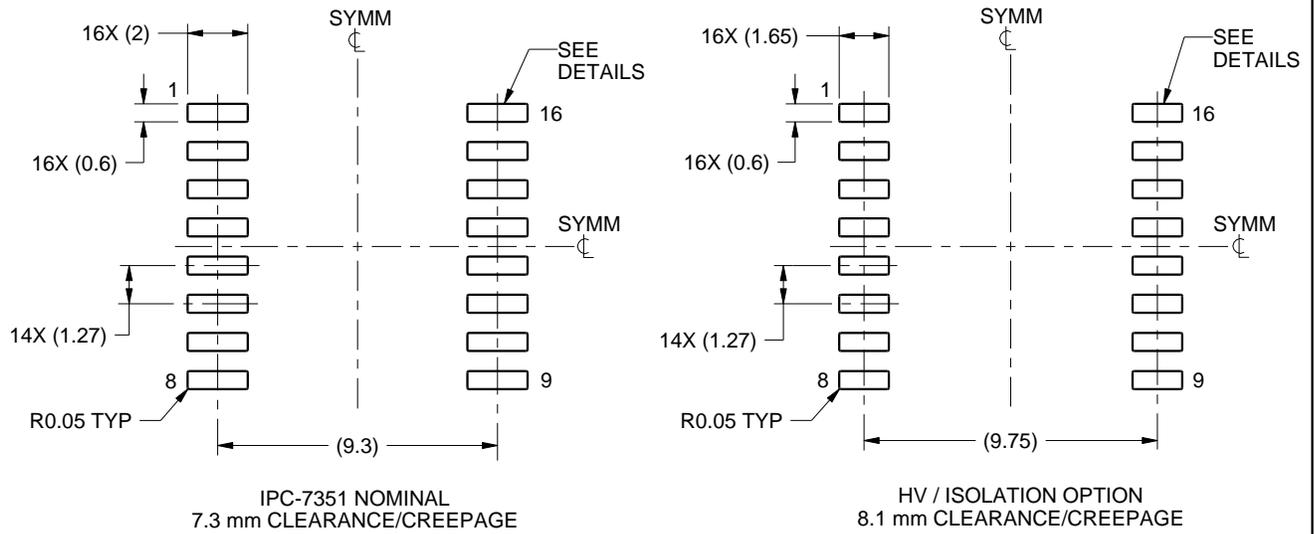
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

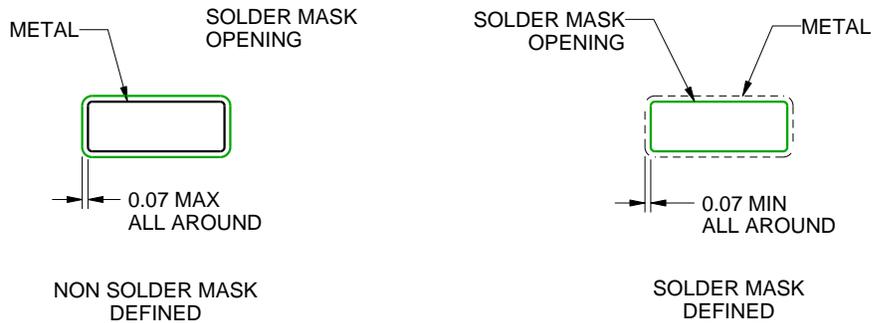
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

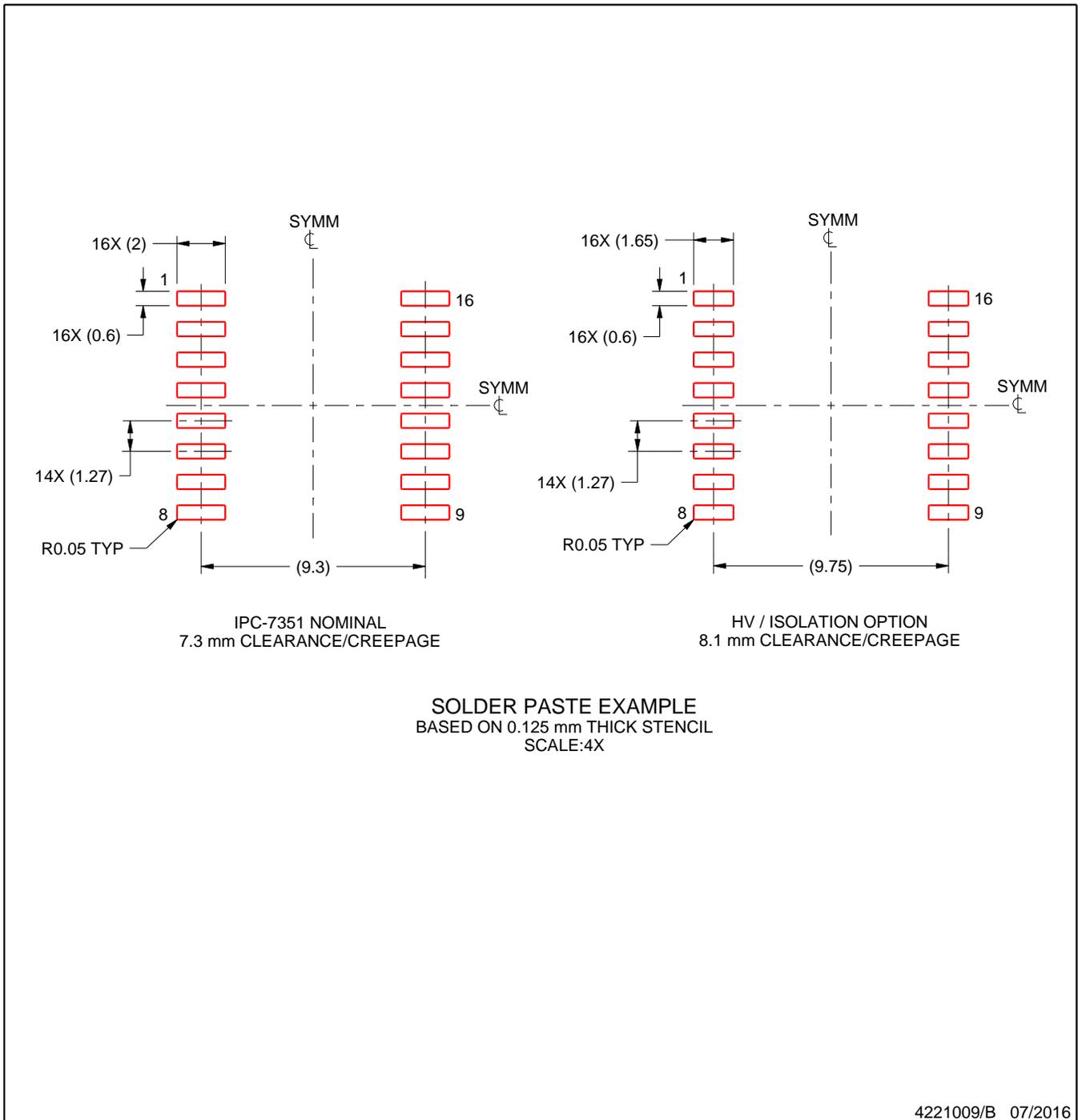
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月