

UC184xA-SP QML V 类电流模式 PWM 控制器

1 特性

- 符合 QML V 类 (QMLV) 标准, SMD 5962-86704
- 抗辐射能力: 30kRad (Si) 总电离剂量 (TID) ^{(1) (2)}
- 经过优化适用于离线和 DC-DC 转换器
- 低启动电流 (< 0.5mA)
- 修整的振荡器放电电流
- 自动前馈补偿
- 逐脉冲电流限制
- 增强型负载响应特性
- 带滞后的欠压闭锁 (UVLO) 保护
- 双脉冲抑制
- 高电流推挽式输出
- 内部调整的带隙参考
- 500kHz 工作频率
- 低 R_O 误差放大器

2 应用

- DC-DC 转换器
- 支持多种拓扑结构:
 - 反激、正激、降压、升压
 - 推挽、半桥、全桥 (采用外部接口电路时)
- 支持军用温度范围 (-55°C 至 125°C)

3 说明

UC184xA-SP 系列控制 IC 是与 UC184x 系列引脚兼容的改进版。该器件提供了控制电流模式开关电源所必需的特性, 并改进了多种功能。额定启动电流低于 0.5mA, 振荡器放电电流调整为 8.3mA。UVLO 期间, 输出级在低于 1.2V 的电压下至少具有 10mA 的灌电流能力 (V_{CC} 高于 5V)。

器件比较表显示了该系列各成员器件间的不同之处。要订购辐射改进型版本 (如已提供), 请参考相应的产品数据表。

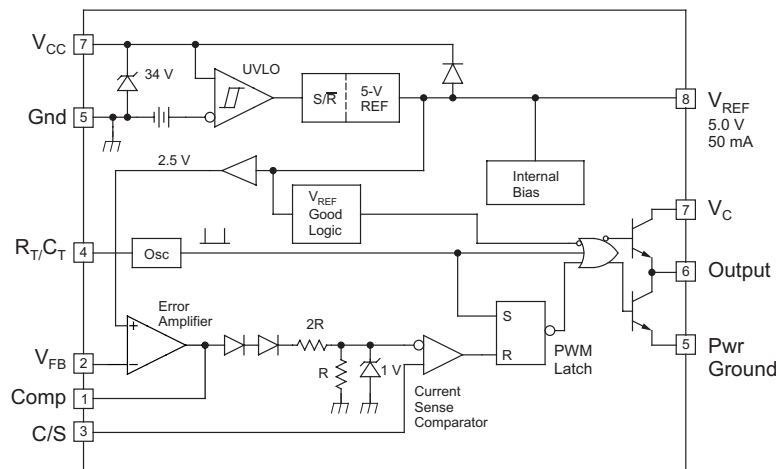
器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
UC1842A-SP	CDIP (8)	6.67mm x 9.60mm
UC1844A-SP	LCCC (20)	8.89mm x 8.89mm

- (1) 仅 UC1843A-SP (订货编号: 5962-8670409VPA) 提供低剂量率 (LDR) 改进型芯片。要获取 UC1842A-SP 或 UC1844A-SP 的 LDR 改进型版本, 请与厂家联系。
- (2) 抗辐射能力是基于初始器件认证 (剂量率 = 10mrads(Si)/s) 获得的典型值。提供辐射批次验收测试 - 详细信息请联系厂家。

- (1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

简化原理图



目录

1	特性	1	8.3	Feature Description	9
2	应用	1	8.4	Device Functional Modes	14
3	说明	1	9	Application and Implementation	15
4	修订历史记录	2	9.1	Application Information	15
5	Device Comparison Table	3	9.2	Typical Application	15
6	Pin Configuration and Functions	3	10	Power Supply Recommendations	23
7	Specifications	4	11	Layout	23
7.1	Absolute Maximum Ratings	4	11.1	Layout Guidelines	23
7.2	ESD Ratings	4	11.2	Layout Example	24
7.3	Recommended Operating Conditions	4	12	器件和文档支持	25
7.4	Thermal Information	4	12.1	相关链接	25
7.5	Electrical Characteristics	5	12.2	接收文档更新通知	25
7.6	Electrical Characteristics (Radiation-Improved Devices)	7	12.3	社区资源	25
7.7	Typical Characteristics	8	12.4	商标	25
8	Detailed Description	9	12.5	静电放电警告	25
8.1	Overview	9	12.6	术语表	25
8.2	Functional Block Diagram	9	13	机械、封装和可订购信息	25

4 修订历史记录

Changes from Revision D (May 2015) to Revision E	Page
• 该数据表删除了 UC1843A-SP 器件	1
• Changed the <i>Pin Configuration</i> images	3
• Changed CT (pF) To: CT (μF) in Equation 1	17

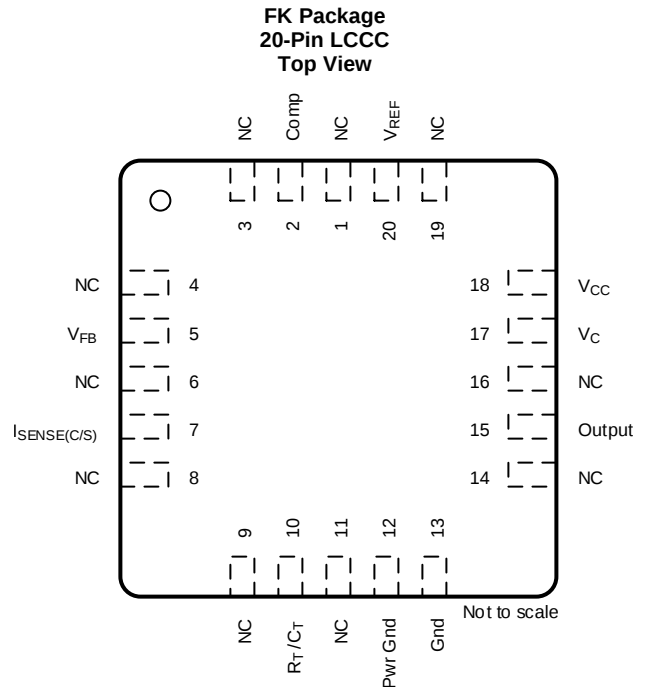
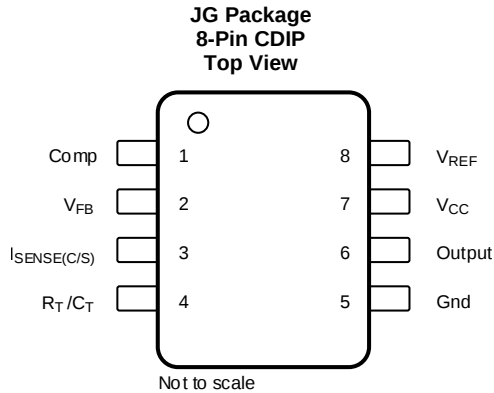
Changes from Revision C (March 2015) to Revision D	Page
• 已更新 特性 以移除抗辐射加固保障	1
• Updated table notes for Electrical Characteristics	5
• Updated table note in Electrical Characteristics (Radiation-Improved Devices)	7
• Corrected minimum discharge current in Electrical Characteristics (Radiation-Improved Devices)	7
• Corrected input voltage unit to V and MIN and MAX values	7
• Decreased set point variation over temperature from ±10% to ±2%	13

Changes from Revision B (October 2013) to Revision C	Page
• 已添加 ESD 额定值表, 典型特性, 详细 说明, 应用和实施, 电源相关建议, 布局以及器件和文档支持部分	1
• 已从本数据表中移除 UC1845A-SP 部件	1

5 Device Comparison Table

PART NO.	UVLO ON	UVLO OFF	MAXIMUM DUTY CYCLE
UC1842A	16 V	10 V	<100%
UC1843A	8.5 V	7.9 V	<100%
UC1844A	16 V	10 V	<50%

6 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	CDIP	LCCC		
Comp	1	2	I	Error amplifier output.
V _{FB}	2	5	I	Voltage feedback input to error amplifier.
I _{SENSE(C/S)}	3	7	I	Current sense comparator input pin.
R _T /C _T	4	10	I	RC time constant input to oscillator.
NC	—	1, 3, 4, 6, 8, 9, 11, 14, 16, 19	—	No connect.
Pwr Gnd	—	12	—	Output section ground.
Gnd	5	13	—	Ground.
Output	6	15	O	Regulated output.
V _C	—	17	—	Output section supply voltage.
V _{CC}	7	18	—	Unregulated supply voltage.
V _{REF}	8	20	O	5-V internally generated reference.

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage, low-impedance source		30	V
V _I	Input voltage (V _{FB} , I _{SENSE})	–0.3	6.3	V
	Supply current	Self limiting		
I _O	Output current		±1	A
	Error amplifier output sink current		10	mA
	Output energy (capacitive load)		5	μJ
P _D	Power dissipation (T _A = 25°C)		1	W
T _{stg}	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground. Currents are positive in, negative out of the specified terminal.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (T_A = T_J = –55°C to 125°C), unless otherwise noted

		MIN	MAX	UNIT
V _{CC}	Supply voltage	12	25	V
	Sink/source output current (continuous or time average)	0	200	mA
	Reference load current	0	20	mA

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UC184xA-SP		UNIT
		JG (CDIP)	FK (LCCC)	
		8 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	103	—	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	9.6	9.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	69.2	—	°C/W
ψ _{JT}	Junction-to-top characterization parameter	13.9	—	°C/W
ψ _{JB}	Junction-to-board characterization parameter	73	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

 $V_{CC} = 15\text{ V}^{(1)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, $T_A = T_J = -55^\circ\text{C}$ to 125°C (unless otherwise noted) ⁽²⁾

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	$T_J = 25^{\circ}\text{C}$, $I_O = 1\text{ mA}$		4.95	5	5.06	V
Line regulation	$V_{IN} = 12\text{ to }25\text{ V}$			6	20	mV
Load regulation	$I_O = 1\text{ to }20\text{ mA}$			6	25	mV
Temperature stability ⁽³⁾⁽⁴⁾				0.2	0.4	mV/ $^{\circ}\text{C}$
Total output variation ⁽³⁾	Over line, load, and temperature		4.9		5.1	V
Output noise voltage	$10\text{ Hz} \leq f \leq 10\text{ kHz}$, $T_J = 25^{\circ}\text{C}$			50		μV
Long-term stability	1000 hours, $T_A = 125^{\circ}\text{C}$ ⁽³⁾			5	25	mV
Short-circuit output current			−30	−100	−180	mA
OSCILLATOR						
Initial accuracy	$T_J = 25^{\circ}\text{C}$ ⁽⁵⁾		47	52	57	kHz
Voltage stability	$V_{CC} = 12\text{ to }25\text{ V}$			0.2%	1%	
Temperature stability	$T_A = \text{MIN to MAX}$ ⁽³⁾			5%		
Amplitude peak-to-peak	$V_{\text{pin }4}$ ⁽³⁾			1.7		V
Discharge current	$V_{\text{pin }4} = 2\text{ V}$ ⁽⁶⁾	$T_J = 25^{\circ}\text{C}$	7.8	8.3	8.8	mA
		$T_J = \text{Full range}$	7.5		8.8	mA
ERROR AMPLIFIER						
Input voltage	$V_{\text{Comp}} = 2.5\text{ V}$		2.45	2.50	2.55	V
Input bias current				−0.3	−1	μA
Open-loop voltage gain	$V_O = 2\text{ to }4\text{ V}$		65	90		dB
Unity-gain bandwidth	$T_J = 25^{\circ}\text{C}$ ⁽³⁾		0.7	1		MHz
PSRR	$V_{CC} = 12\text{ to }25\text{ V}$		60	70		dB
Output sink current	$V_{FB} = 2.7\text{ V}$, $V_{\text{Comp}} = 1.1\text{ V}$		2	6		mA
Output source current	$V_{FB} = 2.3\text{ V}$, $V_{\text{Comp}} = 5\text{ V}$		−0.5	−0.8		mA
High-level output voltage	$V_{FB} = 2.3\text{ V}$, $R_L = 15\text{ k}\Omega$ to ground		5	6		V
Low-level output voltage	$V_{FB} = 2.7\text{ V}$, $R_L = 15\text{ k}\Omega$ to V_{REF}			0.7	1.1	V
CURRENT SENSE						
Gain ⁽⁷⁾⁽⁸⁾			2.85	3	3.15	V/V
Maximum input signal	$V_{\text{Comp}} = 5\text{ V}$ ⁽⁷⁾		0.9	1	1.1	V
PSRR	$V_{CC} = 12\text{ to }25\text{ V}$ ⁽⁷⁾			70		dB
Input bias current				−2	−10	μA
Delay to output	$V_{\text{ISENSE}} = 0\text{ to }2\text{ V}$ ⁽³⁾			150	300	ns

(1) Adjust V_{CC} above the start threshold before setting at 15 V.

(2) Electrical table applicable to 5962-8670405, 5962-8670406, and 5962-8670407 device types.

(3) Parameters ensured by design and/or characterization, if not production tested.

(4) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:
Temperature Stability = $(V_{REF}(\text{max}) - V_{REF}(\text{min})) / (T_J(\text{max}) - T_J(\text{min}))$. $V_{REF}(\text{max})$ and $V_{REF}(\text{min})$ are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

(5) Output frequency equals oscillator frequency for the UC1842A-SP and UC1843A-SP. Output frequency is one-half oscillator frequency for UC1844A.

(6) This parameter is measured with $R_T = 10\text{ k}\Omega$ to V_{REF} . This contributes approximately 300 μA of current to the measurement. The total current flowing into the R_T or C_T pin will be approximately 300 μA higher than the measured value.

(7) Parameter measured at trip point of latch with $V_{FB} = 0\text{ V}$.

(8) Gain defined as: $G = \Delta V_{Comp} / \Delta V_{ISENSE}$; $V_{ISENSE} = 0\text{ to }0.8\text{ V}$.

Electrical Characteristics (continued)
 $V_{CC} = 15\text{ V}^{(1)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, $T_A = T_J = -55^\circ\text{C}$ to 125°C (unless otherwise noted) ⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT					
Output low-level voltage	I _{SINK} = 20 mA		0.1	0.4	V
	I _{SINK} = 200 mA		1.5	2.2	
Output high-level voltage	I _{SOURCE} = −20 mA	13	13.5		V
	I _{SOURCE} = −200 mA	12	13.5		
Rise time	C _L = 1 nF, T _J = 25°C ⁽³⁾		50	150	ns
Fall time	C _L = 1 nF, T _J = 25°C ⁽³⁾		50	150	ns
UVLO saturation	V _{CC} = 5 V, I _{SINK} = 10 mA		0.7	1.2	V
UNDERVOLTAGE LOCKOUT					
Start threshold	UC1842A, UC1844A	15	16	17	V
	UC1843A	7.8	8.4	9	
Minimum operation voltage after turnon	UC1842A, UC1844A	9	10	11	V
	UC1843A	7	7.6	8.2	
PWM					
Maximum duty cycle	UC1842A, UC1843A	94%	96%	100%	
	UC1844A	47%	48%	50%	
Minimum duty cycle				0%	
TOTAL STANDBY CURRENT					
Start-up current			0.3	0.5	mA
Operating supply current	V _{FB} = V _{ISENSE} = 0 V		11	17	mA
V _{CC} Zener voltage	I _{CC} = 25 mA	30	34		V

7.6 Electrical Characteristics (Radiation-Improved Devices)

 $V_{CC} = 15\text{ V}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, $T_A = T_J = -55^\circ\text{C}$ to 125°C (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE					
Output voltage	T _J = 25°C, I _O = 1 mA	4.94	5	5.06	V
Line regulation	V _{CC} = 12 to 25 V		6	20	mV
Load regulation	I _L = 1 to 20 mA		6	25	mV
Total output variation	Over line, load, and temperature	4.9		5.1	V
Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T _J = 25°C		50		μV
Short-circuit output current		−30	−100	−180	mA
OSCILLATOR					
Initial accuracy	T _J = 25°C	47	52	57	kHz
Voltage stability	V _{CC} = 12 to 25 V		0.2%	1%	
Temperature stability	T _J = −55°C to 125°C		5%		
Amplitude	V _{RT/CT} peak to peak		1.7		V
Discharge current ⁽²⁾	T _J = 25°C, V _{RT/CT} = 2 V	7.8	8.3	8.8	mA
	V _{RT/CT} = 2 V	7.5		8.8	
ERROR AMPLIFIER					
Input voltage	V _{Comp} = 2.5 V	2.45	2.50	2.55	V
Input bias current			−0.3	−1	μA
Open-loop voltage gain	V _O = 2 to 4 V	65	90		dB
Unity-gain bandwidth	T _J = 25°C ⁽³⁾	0.7	1		MHz
PSRR	V _{CC} = 12 to 25 V	60	70		dB
Output sink current	V _{FB} = 2.7 V, V _{Comp} = 1.1 V	2	6		mA
Output source current	V _{FB} = 2.3 V, V _{Comp} = 5 V	−0.5	−0.8		mA
High-level output voltage	V _{FB} = 2.3 V, R _L = 15 kΩ to ground	5	6		V
Low-level output voltage	V _{FB} = 2.7 V, R _L = 15 kΩ to V _{REF}		0.7	1.1	V
CURRENT SENSE					
Gain ⁽⁴⁾ ⁽⁵⁾		2.85	3	3.15	V/V
Maximum input signal	V _{Comp} = 5 V ⁽⁴⁾	0.9	1	1.1	V
PSRR	V _{CC} = 12 to 25 V ⁽⁴⁾		70		dB
Input bias current			−2	−10	μA
Delay to output	V _{ISENSE} = 0 to 2 V ⁽³⁾		150	300	ns
OUTPUT					
Output low-level voltage	I _{SINK} = 20 mA		0.1	0.4	V
	I _{SINK} = 200 mA		1.5	2.2	
Output high-level voltage	I _{SOURCE} = 20 mA	13	13.5		V
	I _{SOURCE} = 200 mA	12	13.0		
Rise time	C _L = 1 nF, T _J = 25°C ⁽³⁾		50	150	ns
Fall time	C _L = 1 nF, T _J = 25°C ⁽³⁾		50	150	ns
UVLO saturation	V _{CC} = 5 V, I _{SINK} = 10 mA		0.7	1.2	V
UNDERVOLTAGE LOCKOUT					
Start threshold		7.8	8.4	9	V
Minimum operation voltage after turnon		7	7.6	8.2	V

(1) Electrical table applicable to radiation-improved 5962-8670409 device type

(2) This parameter is measured with $R_T = 10\text{ k}\Omega$ to V_{REF} . This contributes approximately 300 μA of current to the measurement. The total current flowing into the R_T or C_T pin will be approximately 300 μA higher than the measured value.

(3) Parameters ensured by design and/or characterization, if not production tested.

(4) Parameter measured at trip point of latch with $V_{FB} = 0\text{ V}$.

(5) Gain defined as: $G = \Delta V_{Comp} / \Delta V_{ISENSE}$; $V_{ISENSE} = 0\text{ to }0.8\text{ V}$.

Electrical Characteristics (Radiation-Improved Devices) (continued)

$V_{CC} = 15\text{ V}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, $T_A = T_J = -55^\circ\text{C}$ to 125°C (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM					
Maximum duty cycle		94%	96%	100%	
Minimum duty cycle				0%	
TOTAL STANDBY CURRENT					
Start-up current			0.3	0.5	mA
Operating supply current	$V_{FB} = V_{ISENSE} = 0\text{ V}$		11	17	mA
V_{CC} Zener voltage	$I_{CC} = 25\text{ mA}$	30	34		V

7.7 Typical Characteristics

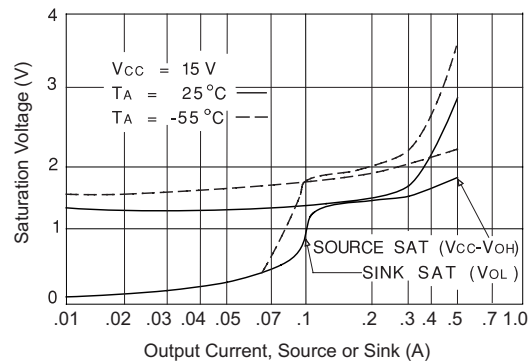


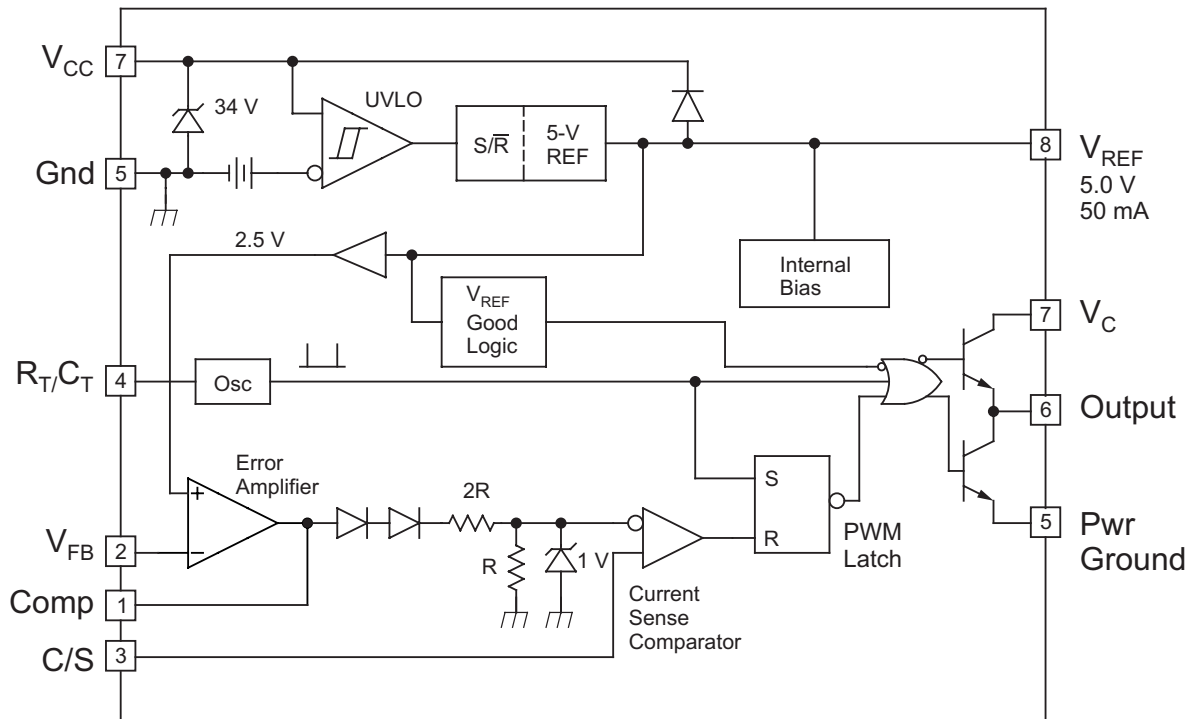
Figure 1. Output Saturation Characteristics

8 Detailed Description

8.1 Overview

The UC184xA-SP control IC is a pin-for-pin compatible improved version of the UC184x family. Providing the necessary characteristics to control current-mode switched-mode power supplies, this device has improved features. Start-up current is specified to be less than 0.5 mA and oscillator discharge is trimmed to 8.3 mA. During UVLO, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

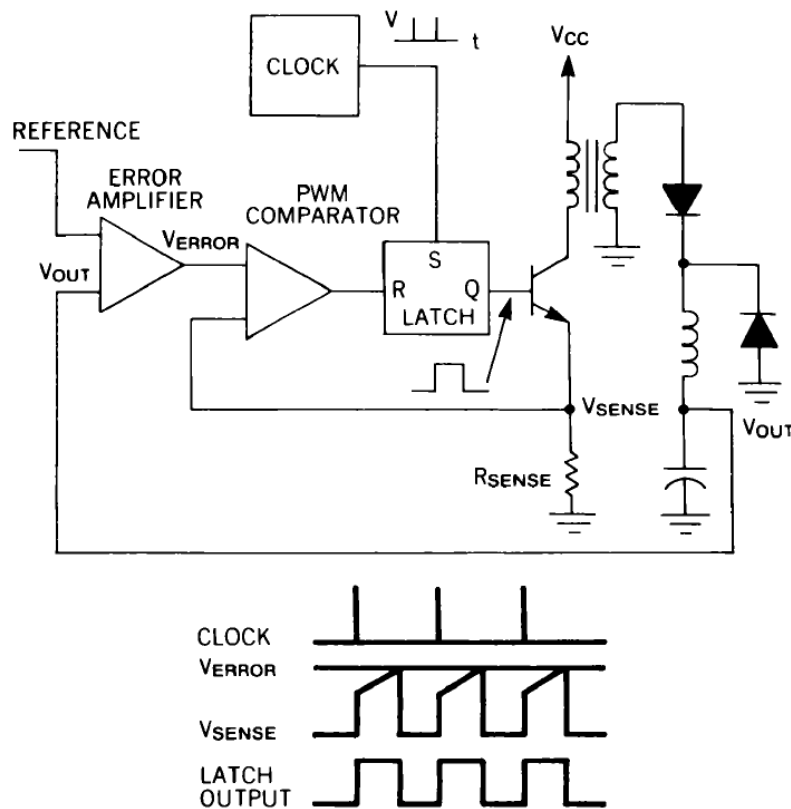
8.3 Feature Description

UC184xA-SP is a current mode controller, used to support various topologies such as forward, flyback, buck, boost and using an external interface circuit will also support half-bridge, full-bridge, and push-pull configurations.

Figure 2 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way, the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; that is, the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

Feature Description (continued)



0019–1

Figure 2. Two-Loop Current-Mode Control System

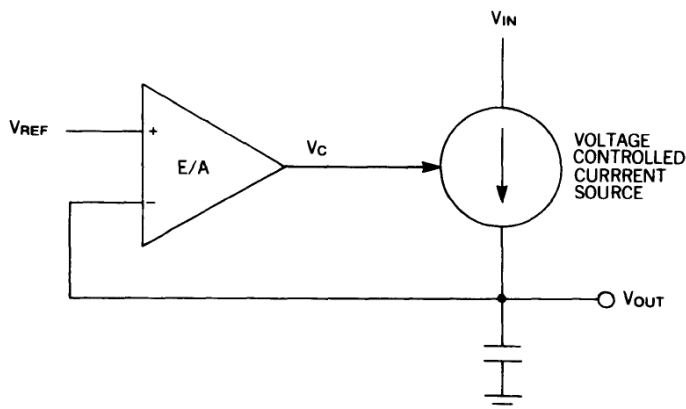
For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an error-voltage-controlled-current-source for the purposes of small-signal analysis (see [Figure 3](#)). The two-pole control-to-output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain bandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as shown in [Figure 4](#).

Capacitor C_i and resistor R_i , in [Figure 4\(A\)](#), add a low-frequency zero, which cancels one of the two control-to-output poles of non-current-mode converters. For large signal load changes, in which converter response is limited by inductor slew rate, the error amplifier saturates while the inductor is catching up with the load. During this time, C_i charges to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is $R_{iz}C_i$, which may be long. However, the compensation network of [Figure 4\(B\)](#) can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i .

Current limiting is greatly simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

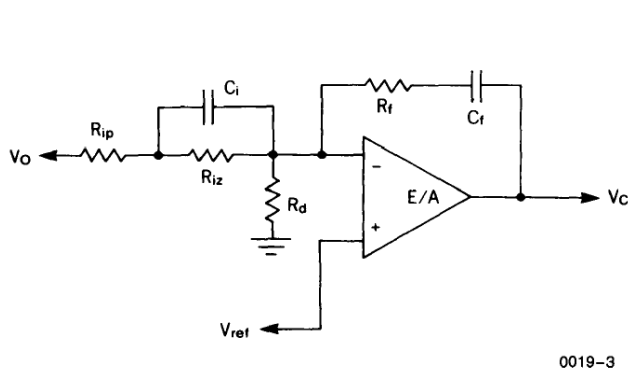
Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

Feature Description (continued)



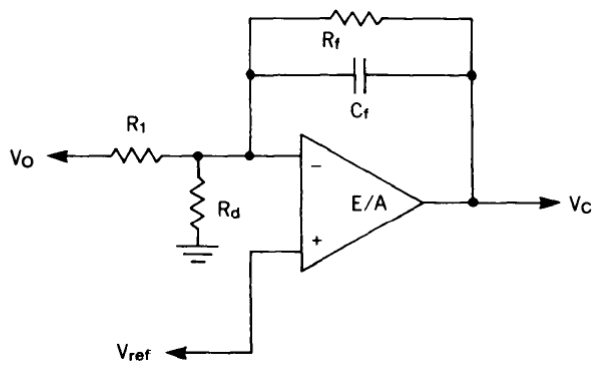
0019-2

Figure 3. Inductor Looks Like a Current Source to Small Signals



0019-3

A. Direct duty cycle control



0019-4

B. Current mode control

Figure 4. Required Error Amplifier Compensation for Continuous Inductor Current Designs

8.3.1 UVLO

The UVLO circuit ensures that V_{CC} is adequate to make the UC184xA-SP fully operational before enabling the output stage. Figure 5 shows that the UVLO turnon and turnoff thresholds are fixed internally at 16 V and 10 V, respectively. The 6-V hysteresis prevents V_{CC} oscillations during power sequencing.

Figure 6 shows supply current requirements. Start-up current is < 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as shown in Figure 7. During normal circuit operation, V_{CC} is developed from auxiliary winding, $WAux$, with D_1 and C_{IN} . However, at start-up, C_{IN} must be charged to 16 V through R_{IN} . With a start-up current of 1 mA, R_{IN} can be as large as 100 k Ω and still charge C_{IN} when $V_{AC} = 90$ -V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line ($V_{AC} = 130$ -V RMS) conditions.

During UVLO, the output driver is in a low state. While it does not exhibit the same saturation characteristics as normal operation, it can easily sink 1 mA, enough to ensure the MOSFET is held off.

Feature Description (continued)

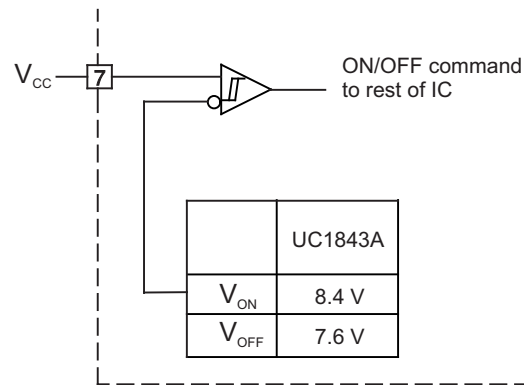
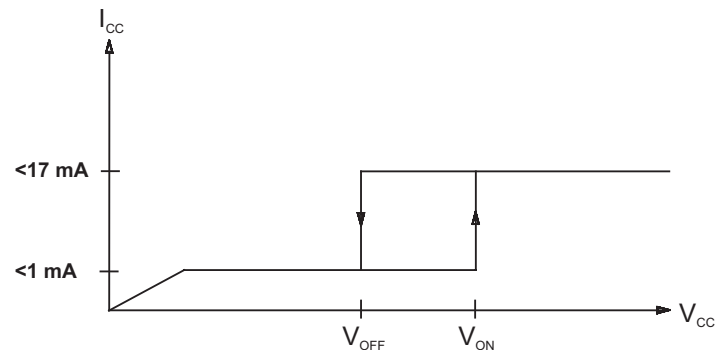
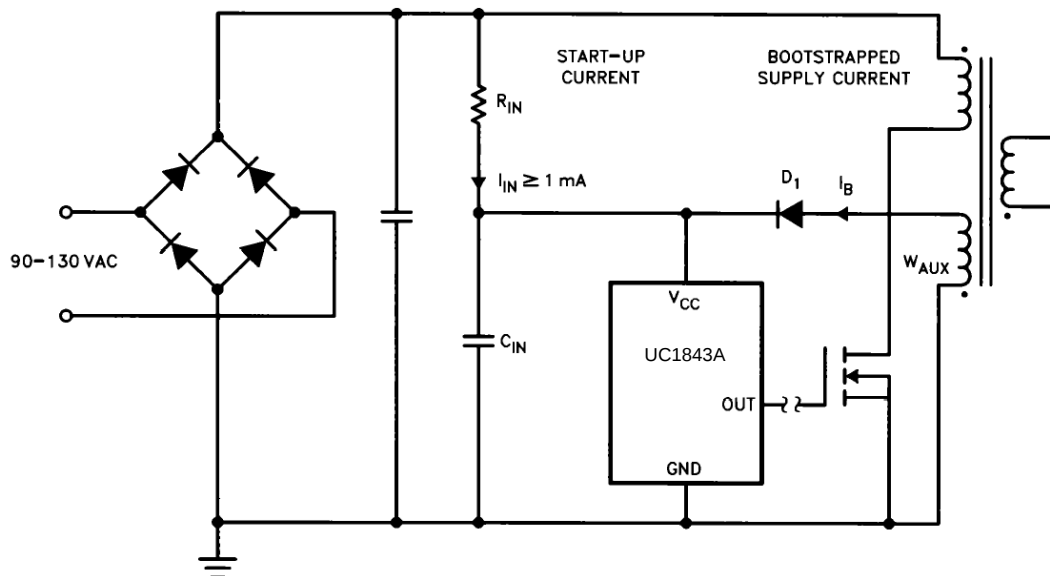


Figure 5. UVLO Turnon TurnOff Threshold



During UVLO, the output driver is biased to sink minor amounts of current.

Figure 6. Supply Current Requirements



0019-8

Figure 7. Providing Power to the UC184xA-SP

Feature Description (continued)

8.3.2 Reference

As highlighted in the [Functional Block Diagram](#), UC184xA-SP incorporates a 5-V internal reference regulator with $\pm 2\%$ set point variation over temperature.

8.3.3 Totem-Pole Output

The UC184xA-SP PWM has a single totem-pole output which can be operated to ± 1 -A peak for driving MOSFET gates, and a +200 mA average current for bipolar power U-100A transistors. Cross conduction between the output transistors is minimal, the average added power with $V_{IN} = 30$ V is only 80 mW at 200 kHz.

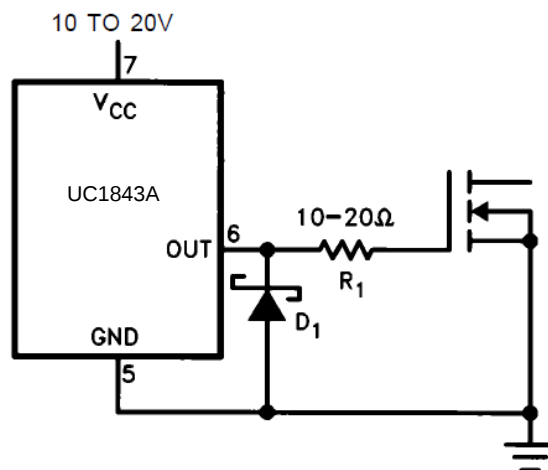
Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage V_C by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole switching and the FET gate capacitance.

The use of a Schottky diode from the PWM output to ground prevents the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3 V at 200 mA. Most 1- to 3-A Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible enhances circuit performance. Implementation of the complete drive scheme is shown in [Figure 8](#) through [Figure 10](#). Transformer-driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

[Figure 8](#) through [Figure 10](#) show suggested circuits for driving MOSFETs and bipolar transistors with the UC184xA-SP output. The simple circuit of [Figure 8](#) can be used when the control IC is not electrically isolated from the MOSFET turnon and turnoff to ± 1 A. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode, D_1 , prevents the output of the IC from going far below ground during turnoff.

[Figure 9](#) shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of [Figure 10](#). Resistors R_1 and R_2 fix the on-state base current while capacitor C_1 provides a negative base current pulse to remove stored charge at turnoff.

Because the UC184xA-SP series has only a single output, an interface circuit is needed to control push-pull, half-bridge, or full-bridge topologies. The UC1706 dual output driver with internal toggle flip-flop performs this function. [Typical Application](#) shows a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC1705/6/7 driver ICs.



0019-19

Figure 8. Direct MOSFET Drive

Feature Description (continued)

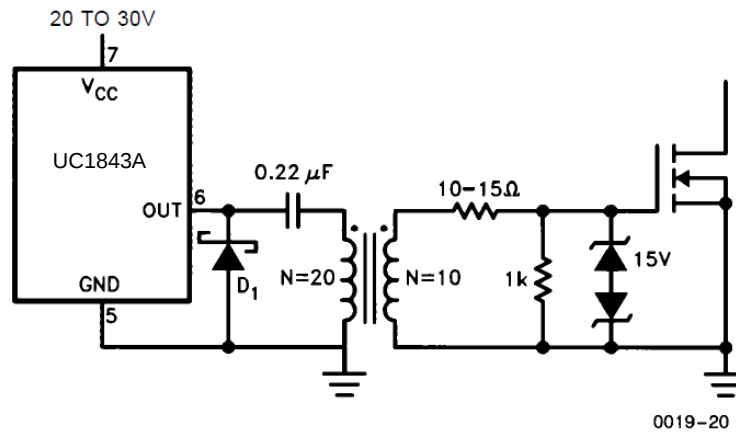


Figure 9. Isolated MOSFET Drive

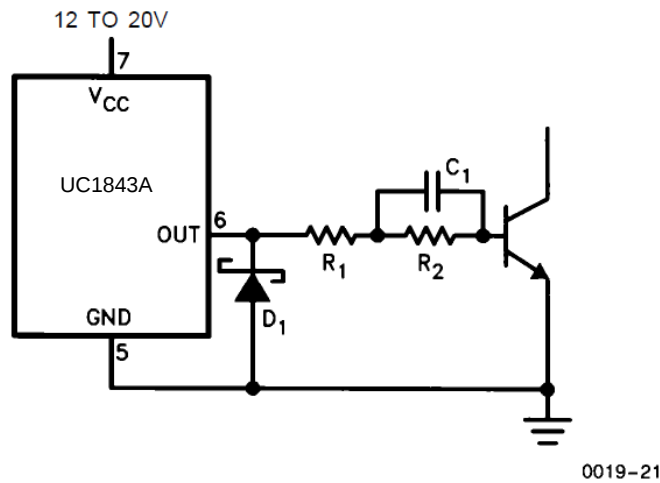


Figure 10. Bipolar Drive With Negative turnoff Bias

8.4 Device Functional Modes

The UC184xA-SP uses fixed frequency, peak current mode control. An internal oscillator initiates the turn on of the driver to high-side power switch. The external power switch current is sensed through an external resistor and is compared via internal comparator. The voltage generated at the COMP pin is stepped down via internal resistors (as shown in the functional block diagram). When the sensed current reaches the stepped down COMP voltage, the high-side power switch is turned off.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

UC184xA-SP can be used as a controller to design various topologies such as buck, boost, flyback, and forward. Using an external interphase circuit can also support push-pull, half-bridge and full-bridge topologies.

9.2 Typical Application

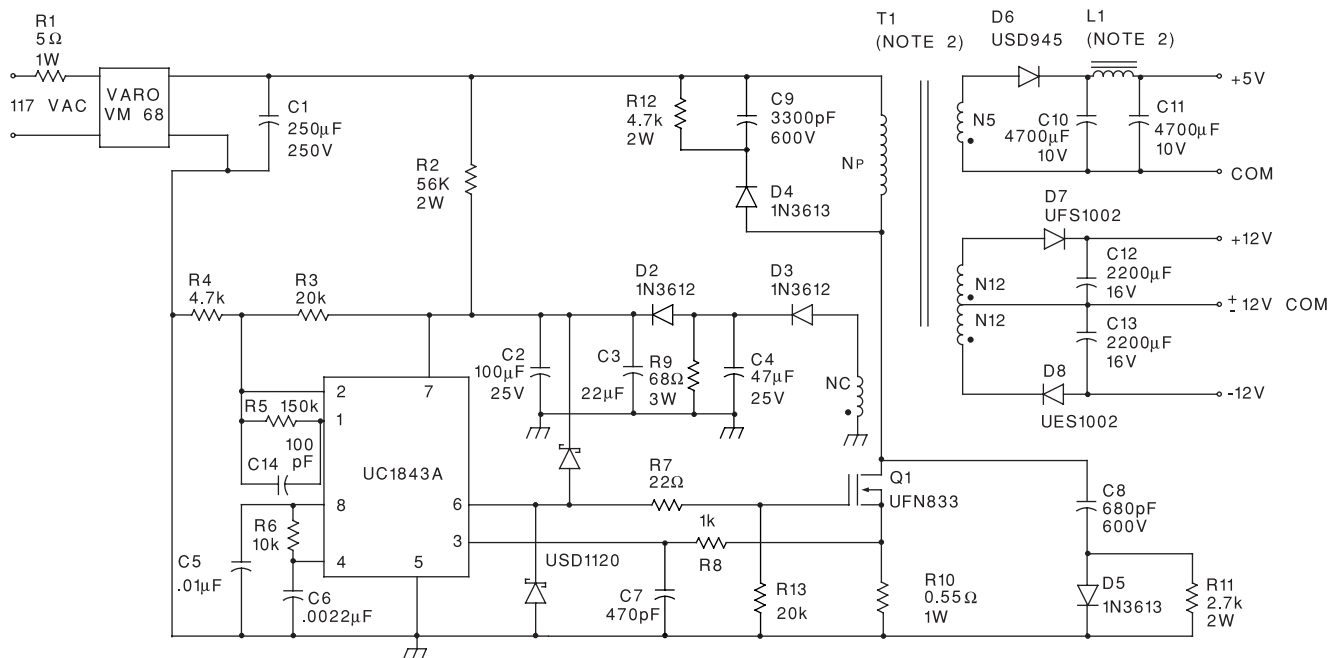


Figure 11. Typical Application Schematic

9.2.1 Design Requirements

See Table 1 for parameter values.

Table 1. Design Parameters⁽¹⁾

DESIGN PARAMETER	VALUE
Input voltage	95 VAC to 130 VAC
Line isolation	3750 V
Switching frequency	40 kHz
Efficiency (full load)	70%
Output voltage (A)	+5 V, ±5%; 1-A to 4-A load; Ripple voltage: 50-mV P-P max
Output voltage (B)	+12 V, ±3%; 0.1-A to 0.3-A load; Ripple voltage: 100-mV P-P max
Output voltage (C)	-12 V, ±3%; 0.1-A to 0.3-A load; Ripple voltage: 100-mV P-P max

(1) See Figure 11 for reference.

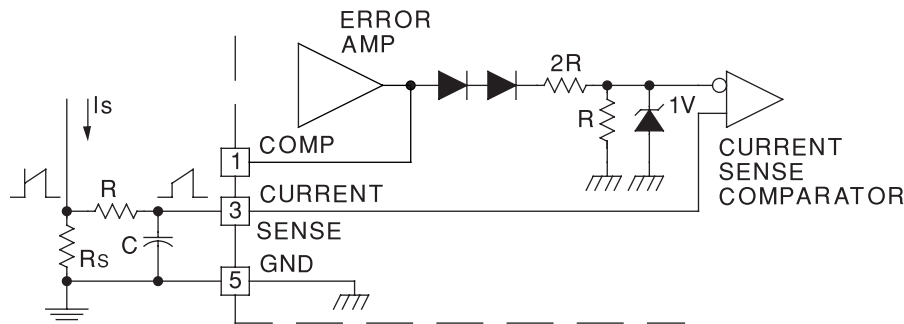
9.2.2 Detailed Design Procedure

See [Table 2](#) for component values.

Table 2. Components⁽¹⁾

COMPONENT	VALUE
R1	5 Ω , 1 W
R2	56 k Ω , 2 W
R3	20 k Ω
R4	4.7 k Ω
R5	150 k Ω
R6	10 k Ω
R7	22 Ω
R8	1 k Ω
R9	68 Ω
R10	0.55 Ω , 1 W
R11	2.7 k Ω , 2 W
R12	4.7 k Ω , 2 W
R13	20 k Ω
C1	250 μ F, 250 V
C2	100 μ F, 25 V
C3	22 μ F
C4	47 μ F, 25 V
C5	0.1 μ F
C6	0.0022 μ F
C7	470 pF
C8	680 pF, 600 V
C9	3300 pF, 600 V
C10	4700 μ F, 10 V
C11	4700 μ F, 10 V
C12	2200 μ F, 10 V
C13	2200 μ F, 10 V
C14	100 pF
D2	1N3612
D3	1N3612
D4	1N3613
D5	1N3613
D6	USD945
D7	UFS1002
D8	UES1002
Q1	UFN833

(1) See [Figure 11](#) for reference.

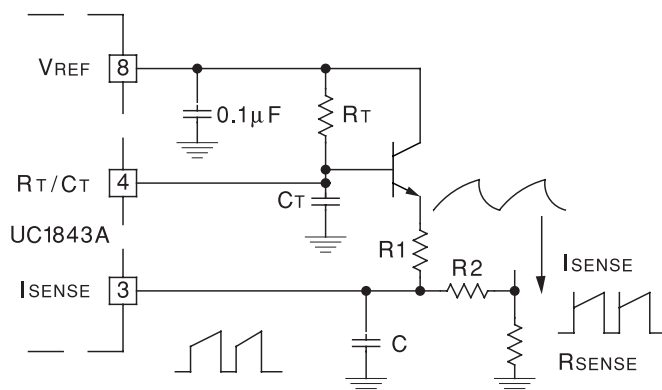


Peak Current (I_s) is determined by the formula:

$$I_{S\text{MAX}} = \frac{1.0 \text{ V}}{R_s}$$

A small RC filter may be required to suppress switch transients.

Figure 12. Current-Sense Circuit



NOTE: A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

Figure 13. Slope Compensation

9.2.2.1 Oscillator

The UC184xA-SP oscillator is programmed as shown in [Figure 15](#). Timing capacitor C_T is charged from VREF (5 V) through the timing resistor R_T , and discharged by an internal current source. The first step in selecting the oscillator components is to determine the required circuit dead time. Once obtained, [Figure 16](#) is used to pinpoint the nearest standard value of C_T for a given dead time. Next, the appropriate R_T value is interpolated using the parameters for C_T and oscillator frequency. [Figure 17](#) shows the R_T/C_T combinations versus oscillator frequency. The timing resistor can be calculated from the following formula.

$$f_{\text{osc}} \text{ (kHz)} = \frac{1.72}{R_T \text{ (k}\Omega) \times C_T \text{ (}\mu\text{F)}} \quad (1)$$

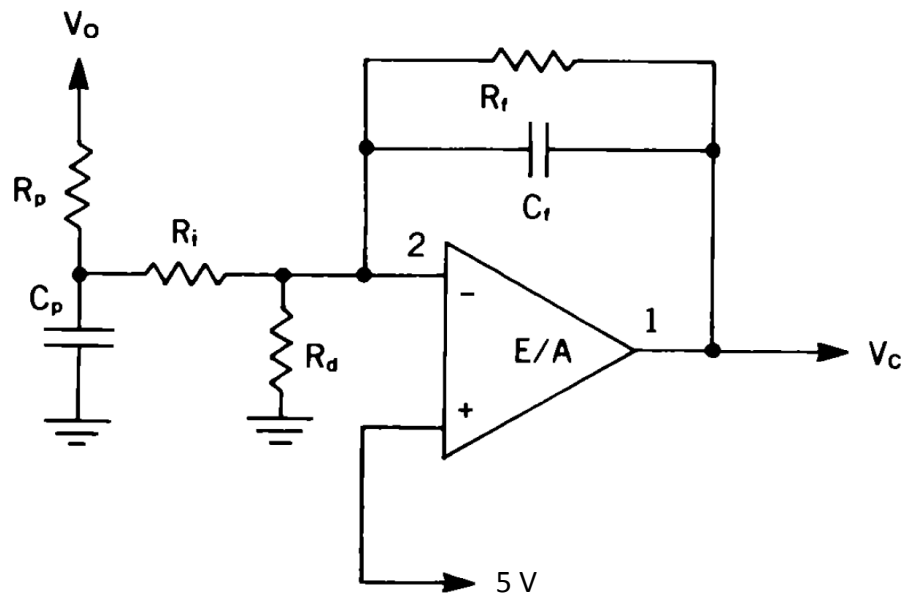


Figure 14. E/A Compensation Circuit for Continuous Boost and Flyback Topologies

The UC184xA-SP has an internal divide-by-two flip-flop driven by the oscillator for a 50% maximum duty cycle. Therefore, their oscillators must be set to run at twice the desired power supply switching frequency.

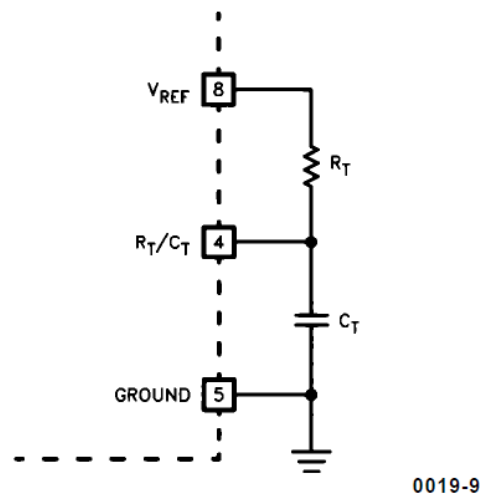


Figure 15. Oscillator Programming

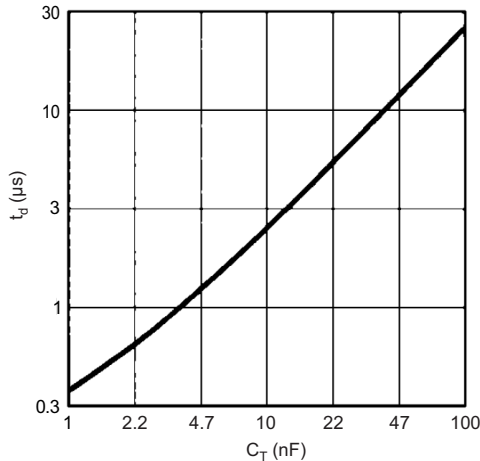


Figure 16. Dead Time vs C_T ($R_T > 5 \text{ k}\Omega$)

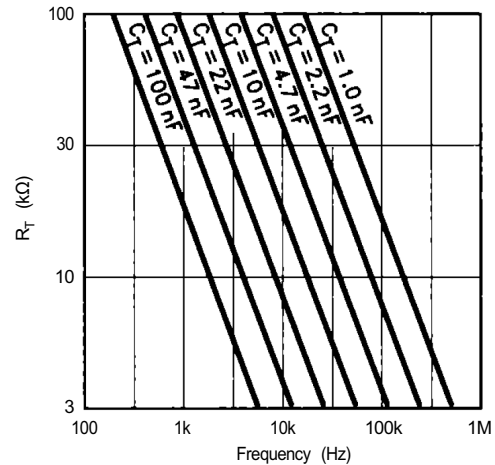


Figure 17. Timing Resistance vs Frequency

9.2.2.2 Current Sensing and Limiting

The UC184xA-SP current sense input is configured as shown in Figure 18. Current-to-voltage conversion is done externally with ground-referenced resistor R_S . Under normal operation, the peak voltage across R_S is controlled by the E/A according to the following relation:

$$I_P = \frac{V_C - 1.4 \text{ V}}{3 R_S}$$

where

- V_C = Control voltage = E/A output voltage (2)

R_S can be connected to the power circuit directly or through a current transformer, as Figure 18 shows. While a direct connection is simpler, a transformer can reduce power dissipation in R_S , reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V_C and peak current in the power stage is given by:

$$I_{(pk)} = N \left(\frac{V_{R_S(pk)}}{R_S} \right) = \frac{N}{3 R_S} (V_C - 1.4 \text{ V})$$

where

- N = Current sense transformer turns ratio = 1 when transformer not used. (3)

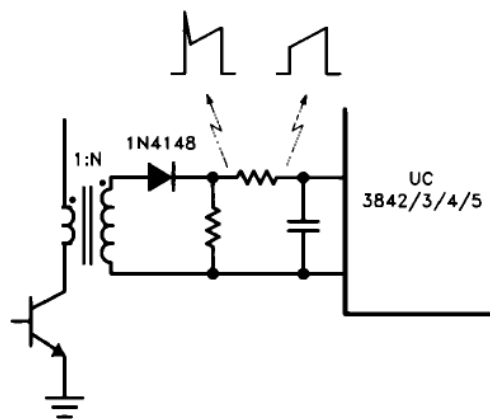
For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{I_{(pk)}}{V_C} = \frac{N}{3 R_S} \quad (4)$$

When sensing current in series with the power transistor, as shown in Figure 18, the current waveform often has a large spike at its leading edge. This spike is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC184xA-SP current-sense comparator is internally clamped to 1 V (Figure 18). Current limiting occurs if the voltage at pin 3 reaches this threshold value, that is, the current limit is defined by:

$$I_{max} = \frac{N \times 1 \text{ V}}{R_S} \quad (5)$$



0019-13

Figure 18. Transformer-Coupled Current Sensing

9.2.2.3 Error Amplifier

The error amplifier (E/A) configuration is shown in Figure 19. The non-inverting input is not brought out to a pin, but is internally biased to 5 V $\pm 2\%$. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 20 shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with inductor current. The feedback components add a pole to the loop transfer function at $f_p = \frac{1}{2\pi R_F C_F}$. R_F and C_F are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_1 and R_F fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0 dB) at $f \approx f_{\text{SWITCHING}} / 4$. This technique ensures converter stability while providing good dynamic response.

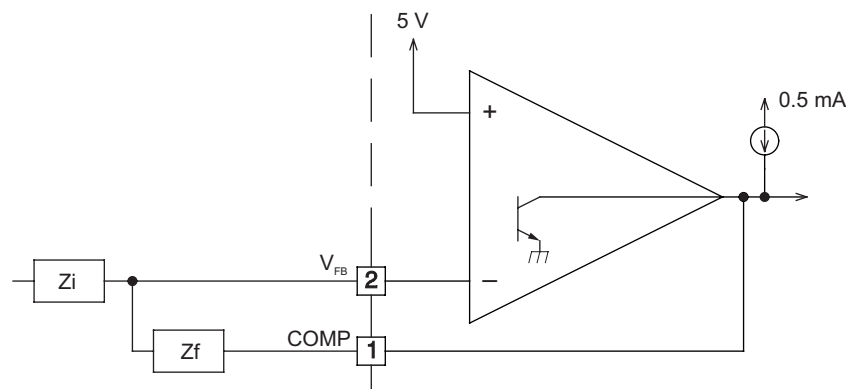
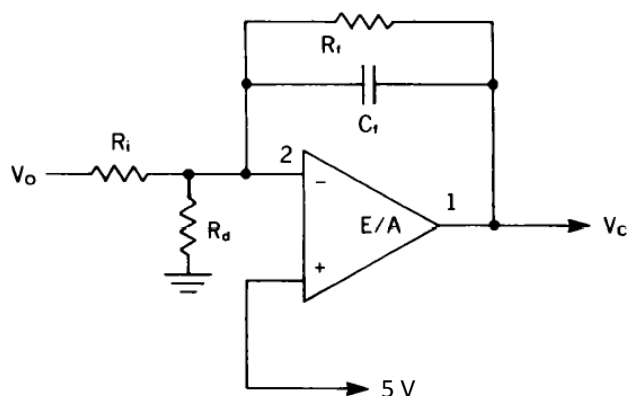


Figure 19. E/A Configuration



0019-15

Figure 20. Compensation

The E/A output sources 0.5 mA and sinks 2 mA. A lower limit for RF is given by:

$$R_{F(MIN)} \approx \frac{V_{EA OUT (MAX)} - 2.5 V}{0.5 \text{ mA}} = \frac{6 V - 2.5 V}{0.5 \text{ mA}} = 7 \text{ k}\Omega \quad (6)$$

E/A input bias current (2-μA max) flows through Ri, resulting in a DC error in output voltage (VO) given by:

$$\Delta V_{O(MAX)} = (2 \text{ }\mu\text{A}) R_i \quad (7)$$

Therefore, the designer should keep the value of Ri, as low as possible.

Figure 21 shows the open-loop frequency response of the UC184xA-SP E/A. The gain represents an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at about 10 MHz and above.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. Rp and Cp in the circuit of Figure 14 provide this pole.

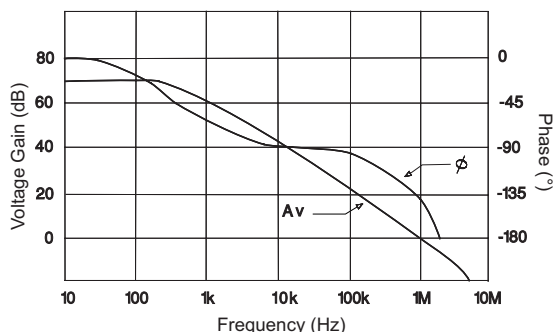


Figure 21. Error Amplifier Open-Loop Frequency Response

9.2.3 Application Curves

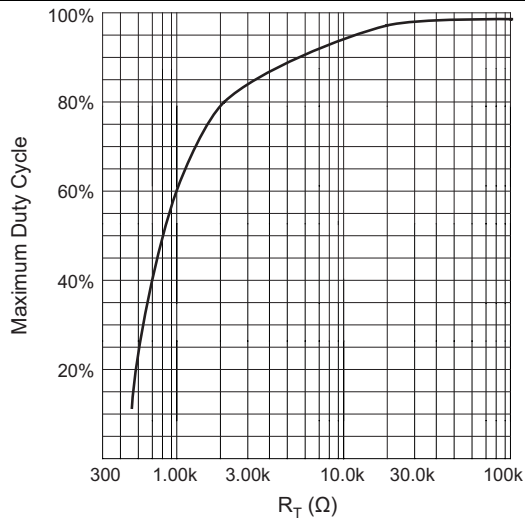


Figure 22. Oscillator Frequency vs Timing Resistance

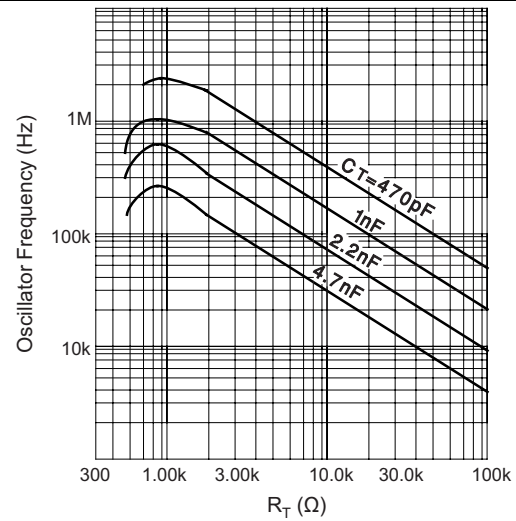
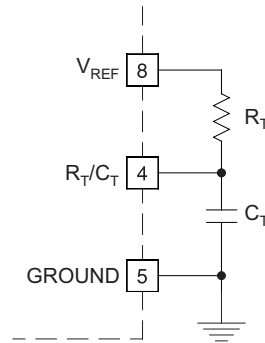


Figure 23. Maximum Duty Cycle vs Timing Resistor



For $R_T > 5k$ $f \approx 1.72 / (R_T C_T)$

Figure 24. Oscillation Schematic

Layout Guidelines (continued)

11.1.2 Input/Output Capacitors

When using a low-value ceramic input filter capacitor, locate it as close as possible to the VIN pin of the IC. This eliminates as much trace inductance effects as possible and gives the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case, it should also be positioned as close as possible to the IC. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

11.1.3 Compensation Components

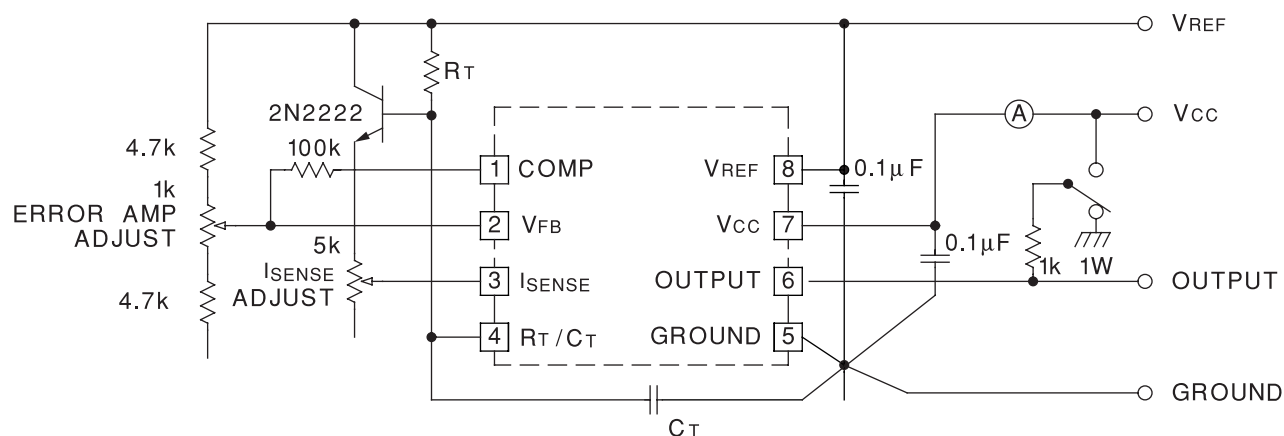
External compensation components for stability should also be placed close to the IC. TI recommends to also use surface mount components for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor either.

11.1.4 Traces and Ground Planes

Make all of the power (high-current) traces as short, direct, and thick as possible. It is good practice on a standard PCB to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere. The inductor, output capacitors, and output diode should be as close as possible to each other. This helps reduce the EMI radiated by the power traces due to the high-switching currents through them. This also reduces lead inductance and resistance, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This reduces noise by reducing ground loop errors and absorbing more of the EMI radiated by the inductor.

For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multi-layer boards, vias are required to connect traces and different planes. It is a good practice to use one standard via per 200 mA of current if the trace needs to conduct a significant amount of current from one plane to the other. Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states: one state when the switch is on and one when the switch is off. During each state there is a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

11.2 Layout Example



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 26. Open-Loop Laboratory Test Fixture

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 3. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
UC1842A-SP	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UC1844A-SP	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](#) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8670405VPA	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670405VPA UC1842A
5962-8670405VPA.A	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670405VPA UC1842A
5962-8670407VPA	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670407VPA UC1844A
5962-8670407VPA.A	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670407VPA UC1844A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1842A-SP, UC1844A-SP :

- Catalog : [UC1842A](#), [UC1844A](#)
- Enhanced Product : [UC1842A-EP](#), [UC1844A-EP](#)

NOTE: Qualified Version Definitions:

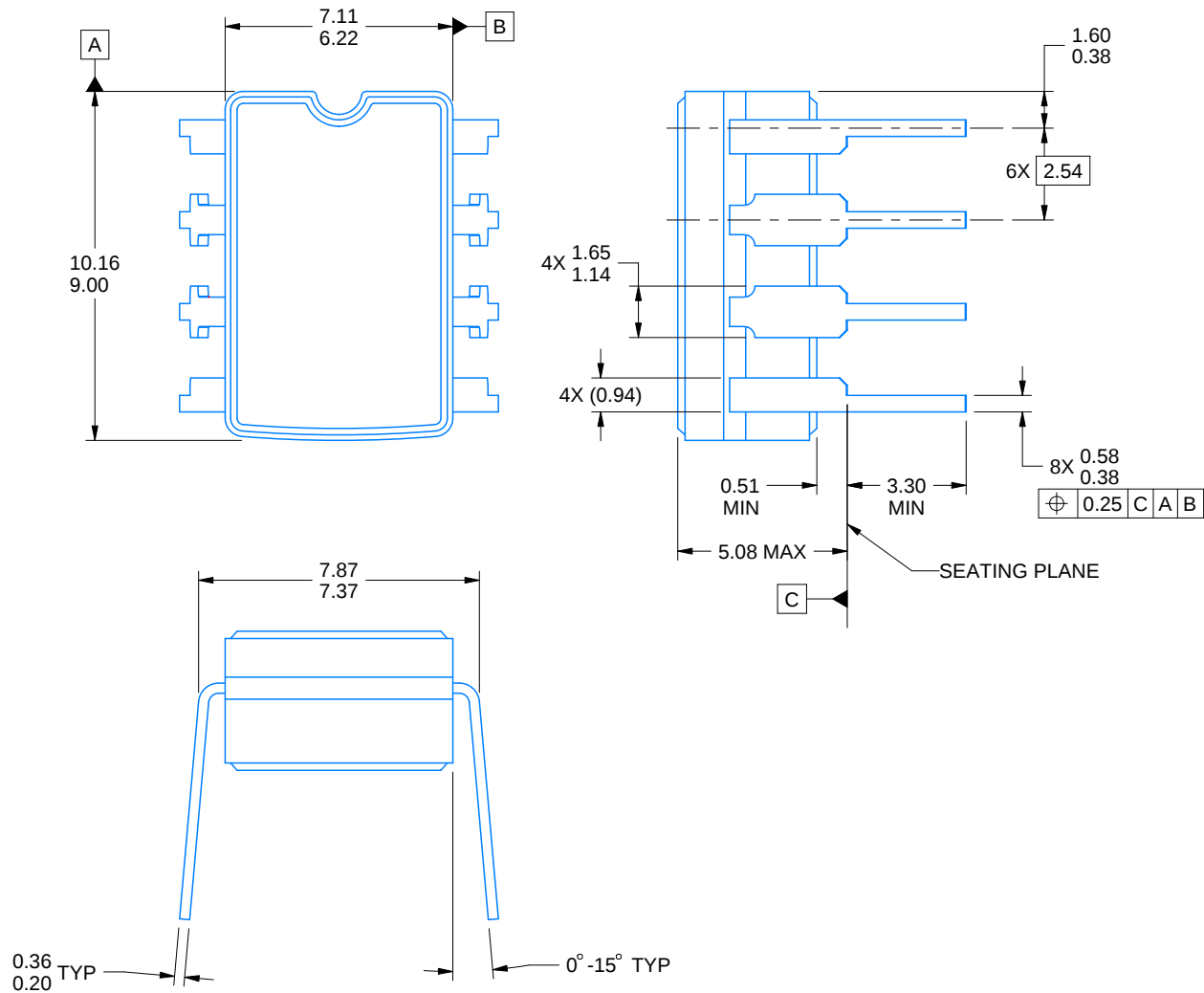
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

JG0008A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

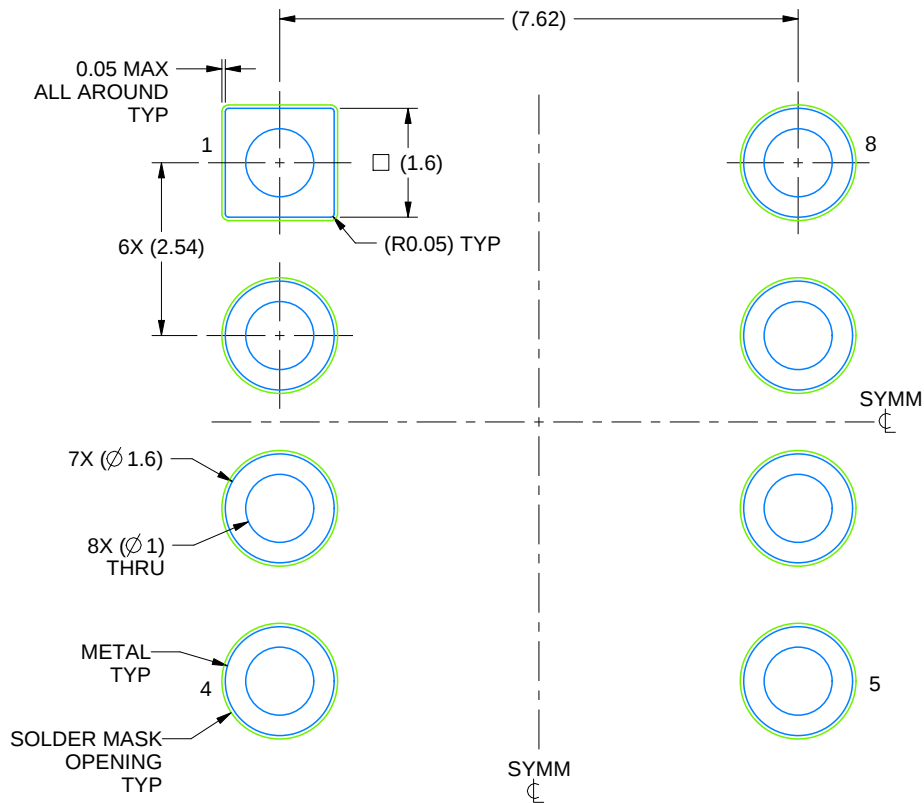
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司