



TUSB551 1.8V USB 3.0 单通道转接驱动器，具有均衡功能

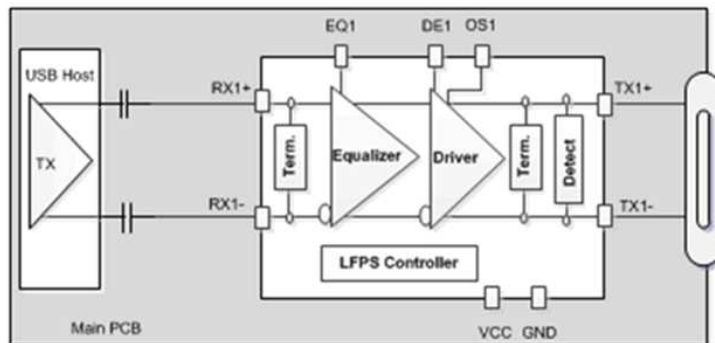
1 特性

- 由 1.8V 电源供电运行的 USB 3.0 超高速 (SuperSpeed) 转接驱动器
- 超低功率架构：
 - 有源时：< 130mW
 - U2/U3：< 22mW
 - 无连接时 < 8mW
- 最优接收器均衡：
 - 3/6/9dB
- 出色的驱动性能
- 自动低频率周期信号 (LFPS) 去加重控制，以满足 USB 3.0 技术规格要求
- 对主机/器件端没有要求
- 小封装选项
- 支持热插拔
- 静电放电 (ESD) 保护超过 $\pm 4\text{kV}$ 人体模型 (HBM)
- 40°C 至 85°C 工业温度范围

2 应用范围

- 手机
- 平板电脑
- 扩展坞
- 电视
- 通电的线缆
- 背板

4 简化电路原理图

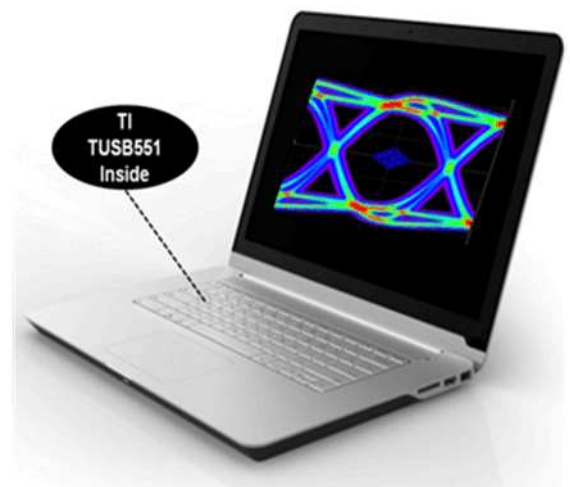


3 说明

TUSB551 是一款第四代 USB 3.0 SuperSpeed (SS) 转接驱动器，此转接驱动器特有低功耗 1.8V 电源，出色输出驱动性能，以及针对完全 USB3.0 兼容性的自动 LFPS 去加重控制。此转接驱动器在均衡器中提供可选增益设置，以解决通道损耗问题。这些设置由 EQ 端子控制。为了补偿下行传输线路损耗，此输出驱动器支持去加重和输出摆动（端子 DE 和 OS）。这些设置可实现最佳性能、增加信号传输距离，以及在 SuperSpeed USB 路径上灵活放置 TUSB551。

器件信息

订货编号	封装	封装尺寸
TUSB551RWBR	X2QFN (12)	1.6mm x 1.6mm



目录

1	特性	1	8	Detailed Description	9
2	应用范围	1	8.1	Overview	9
3	说明	1	8.2	Functional Block Diagram	9
4	简化电路原理图	1	8.3	Feature Description	9
5	修订历史记录	2	8.4	Device Functional Modes	10
6	Terminal Configuration and Functions	3	9	Applications and Implementation	11
7	Specifications	4	9.1	Application Information	11
7.1	Absolute Maximum Ratings	4	9.2	Typical Application	11
7.2	Handling Ratings	4	10	Power Supply Recommendations	13
7.3	Recommended Operating Conditions	4	11	Layout	13
7.4	Thermal Information	4	11.1	Layout Guidelines	13
7.5	Power Supply Electrical Characteristics	5	11.2	Layout Example	14
7.6	DC Electrical Characteristics	5	12	器件和文档支持	15
7.7	AC Electrical Characteristics	5	12.1	Trademarks	15
7.8	Timing Requirements/Timing Diagrams	6	12.2	Electrostatic Discharge Caution	15
7.9	Switching Characteristics	8	12.3	Glossary	15
7.10	Typical Characteristics	8	13	机械封装和可订购信息	15

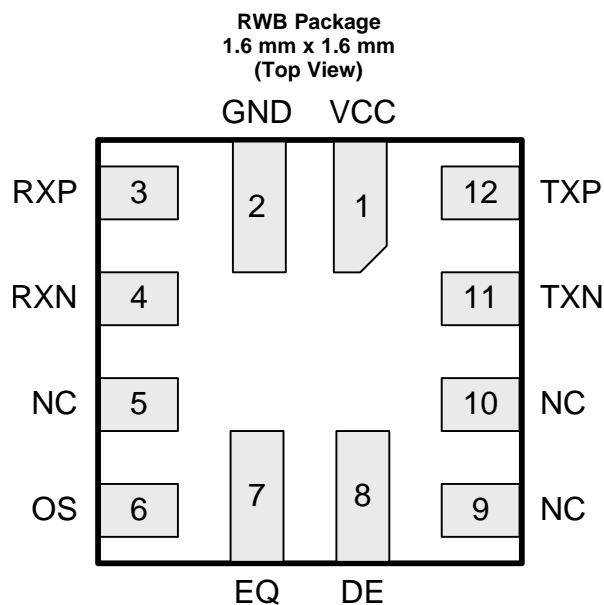
5 修订历史记录

Changes from Original (March 2014) to Revision A

Page

• 已更改 从产品预览更改为生产数据	1
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6 Terminal Configuration and Functions



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VCC	1	Power	1.8 V Power Supply.
GND	2	GND	Ground.
RXP	3	Differential input	Differential input for 5Gbps SuperSpeed positive signals.
RXN	4	Differential input	Differential input for 5Gbps SuperSpeed negative signals.
NC	5, 9, 10		Not internally connected
OS	6	CMOS Input	Sets output swing on the TX. 2-state input with integrated pull-up and pull-down resistors.
EQ	7	CMOS Input	Sets equalizer gain on the RX. 3-state input with integrated pull-up and pull-down resistors.
DE	8	CMOS Input	Sets output de-emphasis on the TX. 3-state input with integrated pull-up and pull-down resistors.
TXN	11	Differential output	Differential output for 5Gbps SuperSpeed negative signals.
TXP	12	Differential output	Differential output for 5Gbps SuperSpeed positive signals.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	−0.3	2.3	V
	Voltage range at any input or output terminal	Differential I/O	−0.3	1.5
		CMOS Inputs	−0.3	2.3
T _J	Maximum junction temperature		105	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{STG}	Storage temperature	−65	150	°C
ESD	Electrostatic discharge	Human Body Model (all terminals) ⁽¹⁾	±4	kV
		Charged-device model (all terminals) ⁽²⁾	±1250	V

- (1) Tested in accordance with JEDEC Standard 22, Test Method A114-B.

- (2) Tested in accordance with JEDEC Standard 22, Test Method C101-A.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Main power supply	1.62	1.8	1.98	V
T _A	Operating free-air temperature	−40		85	°C
C _{AC}	AC coupling capacitor	75	100	200	nF

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TUSB551	UNIT
		RWB PACKAGE	
		12 TERMINALS	
θ _{JA}	Junction-to-ambient thermal resistance ⁽²⁾	175.2	°C/W
θ _{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	71.5	
θ _{JB}	Junction-to-board thermal resistance ⁽⁴⁾	40.5	
ψ _{JT}	Junction-to-top characterization parameter ⁽⁵⁾	2.5	
ψ _{JB}	Junction-to-board characterization parameter ⁽⁶⁾	40.5	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

- (5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

- (6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

7.5 Power Supply Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC-ACTIVE}$	Average active current	Link in U0 with SuperSpeed data transmission; OS = Low; DE = Low	71.65		mA
		Link in U0 with SuperSpeed data transmission; OS = Floating; DE = Low	82.35		
$I_{CC-IDLE}$	Average current in idle state	Link has some activity, not in U1; OS = Low	35		mA
$I_{CC-U2U3}$	Average current in U2/U3	Link in U2 or U3	12.20		mA
I_{CC-NC}	Average current with no connection	No SuperSpeed device is connected to TXP/TXN	4.3		mA

7.6 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
3-State CMOS Inputs (EQ, DE)					
V_{IH}	High-level input voltage	$V_{CC} * 0.8$			V
V_{IM}	Mid-level input voltage		$V_{CC} / 2$		V
V_{IL}	Low-level input voltage			$V_{CC} * 0.2$	V
V_F	Floating voltage	$V_{IN} = \text{High impedance}$	$V_{CC} / 2$		V
R_{PU}	Internal pull-up resistance		105		k Ω
R_{PD}	Internal pull-down resistance		105		k Ω
I_{IH}	High-level input current	$V_{IN} = 1.98V$		26	μA
I_{IL}	Low-level input current	$V_{IN} = GND$	-26		μA
2-State CMOS Inputs (OS)					
V_{IL}	Low-level input voltage	$V_{CC} * 0.8$			V
V_{IM}	Mid-level input voltage		$V_{CC}/2$		V
V_F	Floating voltage	$V_{IN} = \text{High Impedance}$	$V_{CC}/2$		V
R_{PD}	Internal pull-down resistance		105		Ω
I_{IM}	Mid-level input current			26	μA
I_{IL}	Low-level input current	$V_{IN} = GND$	-26		μA

7.7 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Receiver (RXP, RXN)						
V _{CM-RX}	Common-mode voltage bias in the receiver (DC)		0			V
Z _{RX-DIFF}	Differential input impedance (DC)	Present after a SuperSpeed device is detected on TXP/TXN	72	91	120	Ω
Z _{RX-CM}	Common-mode input impedance (DC)	Present after a SuperSpeed device is detected on TXP/TXN	18	24	30	Ω
Z _{RX-HIGH-IMP-DC-POS}	Common-mode input impedance with termination disabled (DC)	Present when no SuperSpeed device is detected on TXP/TXN. Measured over the range of 0-500mV with respect to GND.	25	150		kΩ
V _{RX-LFPS-DET-DIFF-PP}	Low Frequency Periodic Signaling (LFPS) detect threshold	Below the minimum is squelched.	100		300	mVpp
C _{RX}	RX input capacitance to GND	At 2.5GHz	400			fF

AC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Transmitter (TXP, TXN)						
$V_{TX-DIFF-PP}$	Transmitter differential voltage swing (transition-bit) ⁽¹⁾	OS = Low, DE=Low		1050		mVpp
		OS = Floating, DE=Low		1200		
$V_{TX-DIFF-PP-LFPS}$	LFPS differential voltage swing	OS = Low, Floating	800		1200	mVpp
$V_{TX-DE-RATIO}$	Transmitter de-emphasis	DE = Low, OS = Floating		0		dB
		DE = Floating, OS = Floating	-3	-3.5	-4	
		DE = High, OS = Floating		-6		
C_{TX}	TX input capacitance to GND	At 2.5GHz			1.25	pF
$Z_{TX-DIFF}$	Differential impedance of the driver		80		120	Ω
Z_{TX-CM}	Common-mode impedance of the driver	Measured with respect to AC ground over 0-500mV	20		30	Ω
I_{TX-SC}	TX short circuit current	TX+/- shorted to GND			60	mA
V_{CM-TX}	Common-mode voltage bias in the transmitter (DC)		0.6		0.8	V
$V_{CM-TX-AC}$	AC common-mode voltage swing in active mode	Within U0 and within LFPS			100	mVpp
$V_{TX-IDLE-DIFF-AC-PP}$	Differential voltage swing during electrical idle	Tested with a high-pass filter	0		10	mVpp
$V_{TX-CM-\Delta U1-U0}$	Absolute delta of DC CM voltage during active and idle states				100	mV
$V_{TX-IDLE-DIFF-DC}$	DC electrical idle differential output voltage	Voltage must be low pass filtered to remove any AC component	0		10	mV
V_{detect}	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV

(1) $V_{TX-DIFF-PP}$ is measured at the TX output with no load and no trace.

7.8 Timing Requirements/Timing Diagrams

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{READY}	Time from power applied until RX termination	Apply 0V to VCC, connect SuperSpeed termination to TX \pm , apply 1.8V to VCC, and measure when ZRX-DIFF is enabled.		52		ms
Differential Transmitter (TXP, TXN)						
t_r, t_f	Output rise/fall times (see Figure 3)	20%-80% of differential voltage measured 1 inch from the output terminal		56		ps
t_{RF-MM}	Output rise/fall time mismatch	20%-80% of differential voltage measured 1 inch from the output terminal			2.6	ps

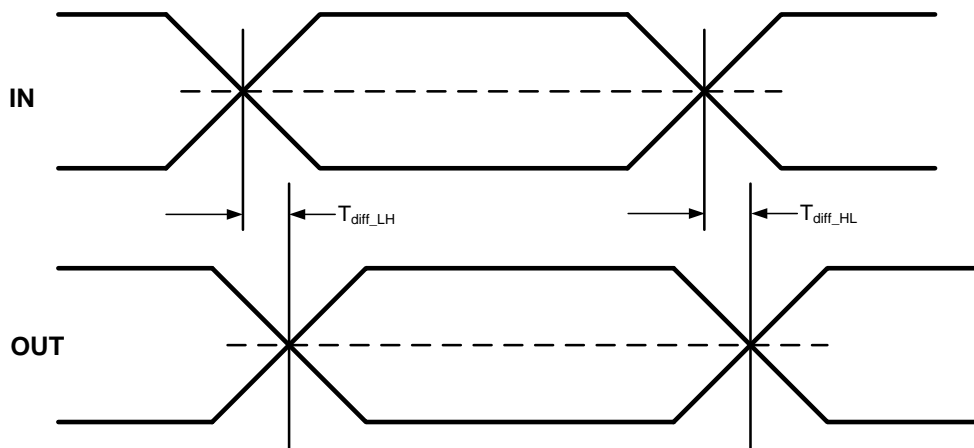


Figure 1. Propagation Delay Timing

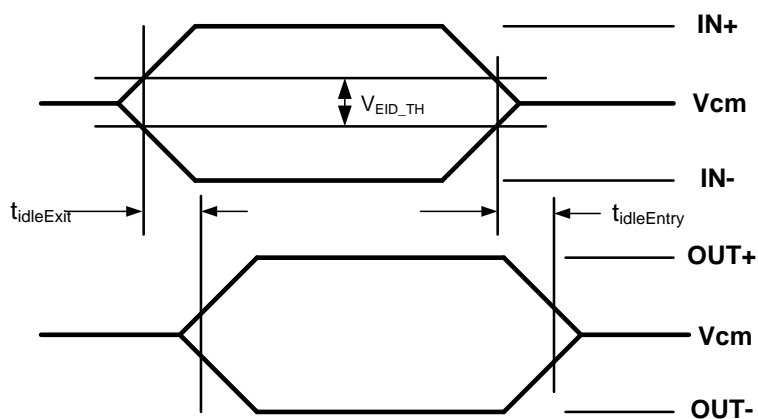


Figure 2. Electrical Idle Mode Exit and Entry Delay Timing

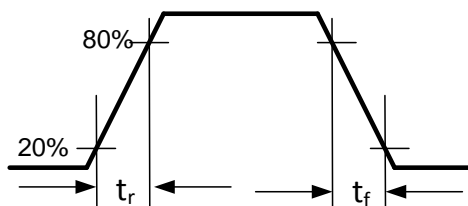


Figure 3. Output Rise and Fall Times

7.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Transmitter (TXP, TXN)					
$T_{diff-LH}$, $T_{diff-HL}$	Differential propagation delay times (see Figure 1)	De-Emphasis = -3.5dB Propagation delay between 50% level at input and output		278	ps
$t_{idleEntry}$, $t_{idleExit}$	Idle entry and exit times (see Figure 2)		6		ns

7.10 Typical Characteristics

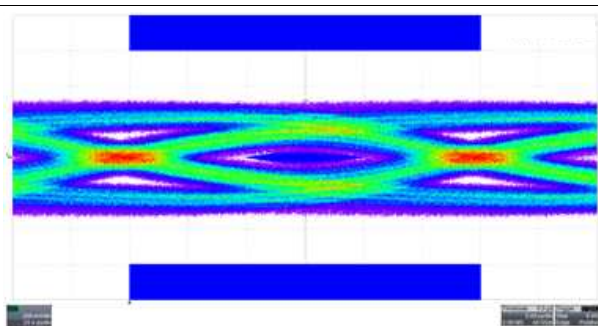


Figure 4. No Re-Driver, Trace Length = 16" + 3m Cable

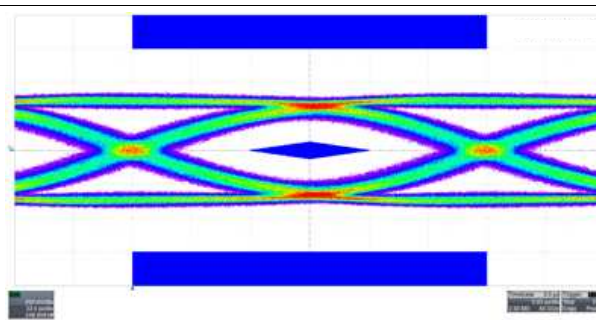


Figure 5. After Re-Driver EQ(3dB), Input = 12", Output = 4" + 3m Cable

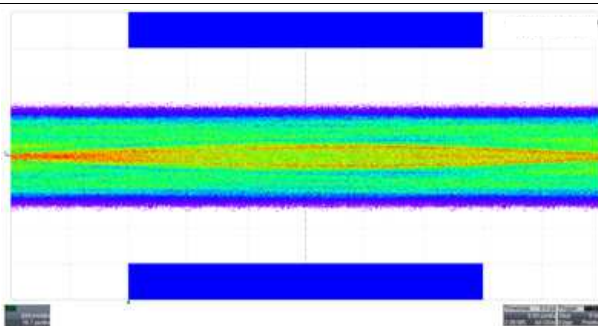


Figure 6. No Re-Driver, Trace Length = 24" + 3m Cable

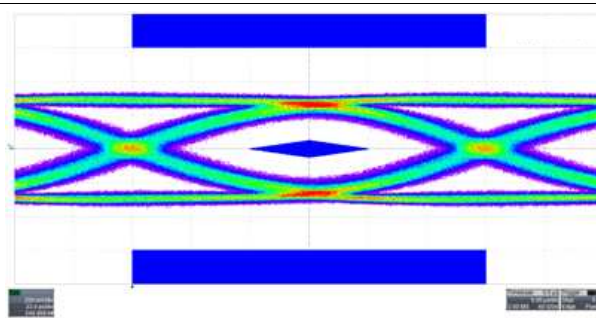


Figure 7. After Re-Driver EQ(6dB), Input = 20", Output = 4" + 3m Cable

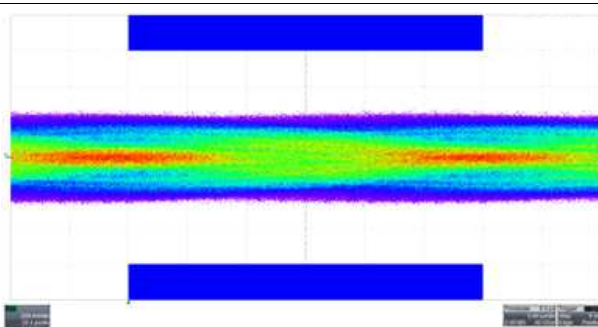


Figure 8. No Re-Driver, Trace Length = 36" + 3m Cable

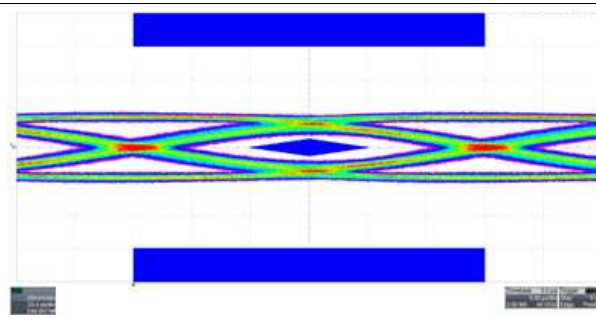


Figure 9. After Re-Driver De = 3.5dB, EQ = 3dB, Input = 16", Output = 20" + 3m Cable

8 Detailed Description

8.1 Overview

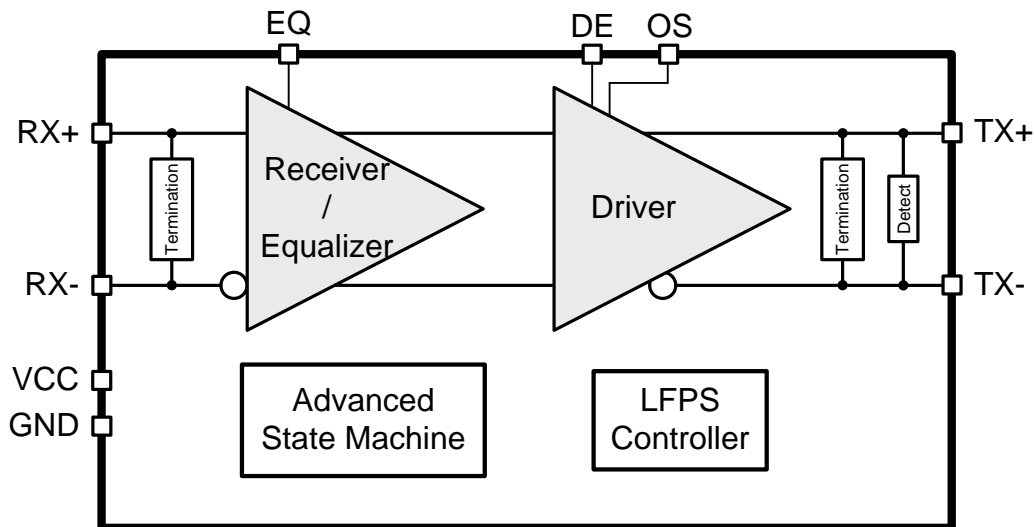
When 5Gbps SuperSpeed USB signals travel across a PCB or cable, signal integrity degrades due to loss and inter-symbol interference. The TUSB551 recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. This extends the possible channel length, and enables systems to pass USB 3.0 compliance.

The TUSB551 advanced state machine makes it transparent to hosts and devices. After power up, the TUSB551 periodically performs receiver detection on the TX pair. If it detects a SuperSpeed USB receiver, the RX termination is enabled, and the TUSB551 is ready to re-drive.

The device's ultra low-power architecture operates at a 1.8V power supply and achieves enhanced performance. The receiver equalizer has three gain settings that are controlled by terminal EQ: 3 dB, 6 dB, and 9 dB. The equalization should be set based on amount of insertion loss in the channel before the TUSB551. Likewise, the output driver supports configuration of De-Emphasis and Output Swing (terminals DE and OS). The automatic LFPS De-Emphasis control further enables the system to be USB3.0 compliant.

The TUSB551 operates over the industrial temperature range of -40°C to 85°C in the 1.6mm x 1.6mm X2QFN package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Receiver Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TUSB551. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss before the input of the TUSB551.

8.3.2 De-Emphasis Control and Output Swing

The differential driver output provides selectable de-emphasis and output swing control in order to achieve USB3.0 compliance. The TUSB551 offers a unique way to adjust output de-emphasis and transmitter swing based on the OS and DE terminals. The level of de-emphasis required in the system depends on the channel length after the output of the re-driver.

Feature Description (continued)

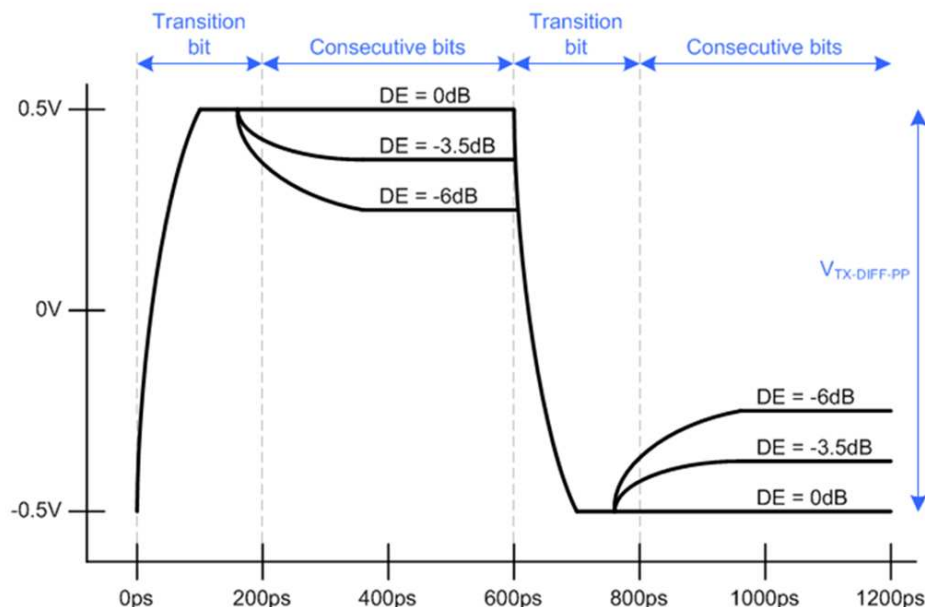


Figure 10. Transmitter Differential Voltage, OS=Floating

8.3.3 Automatic LFPS Detection

The TUSB551 features an intelligent low frequency periodic signaling (LFPS) controller. The controller senses the low frequency signals and automatically disables the driver de-emphasis, for full USB3.0 compliance.

8.4 Device Functional Modes

8.4.1 Receiver Equalization Settings

TERMINAL	DESCRIPTION	LOGIC STATE	GAIN
EQ	Equalization amount	Low	3 dB
		Floating (NC)	6 dB
		High	9 dB

8.4.2 De-Emphasis Control Settings

TERMINAL	INTERNAL TIE	LOGIC STATE	DE-EMPHASIS RATIO	
			FOR OS = LOW	FOR OS = FLOATING
DE	De-emphasis amount	Low	0 dB	0 dB
		Floating (NC)	-2 dB	-3.5 dB
		High	-4 dB	-6 dB

8.4.3 Output Swing Control Settings

TERMINAL	INTERNAL TIE	LOGIC STATE	OUTPUT DIFFERENTIAL VOLTAGE
OS	Output swing amplitude, DE = Low	Low	1050 mVpp
		Floating (NC)	1200 mVpp

9 Applications and Implementation

9.1 Application Information

One example of the TUSB551 used in a Host application on transmit and receive channels is shown below. The re-driver is needed on the transmit path to pass transmitter compliance due to loss between the Host and connector. The re-driver uses its equalization to recover the insertion loss and re-drive the signal with boosted swing down the remaining channel, through the USB3.0 cable, and into the device PCB. Additionally, the TUSB551 is needed on the receive channel for the Host to pass receiver jitter tolerance. The re-driver recovers the loss from the Device PCB, connector, and USB 3.0 cable and re-drives the signal going into the Host receiver. The equalization, output swing, and de-emphasis settings are dependent upon the type of USB3.0 signal path and end application.

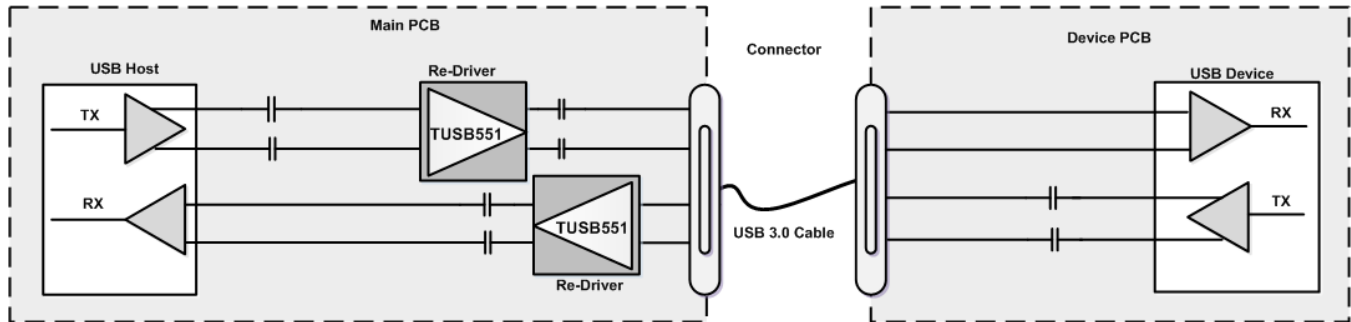


Figure 11. Application for Host Systems

9.2 Typical Application

9.2.1 Transmit and Receive Channels

The TUSB551 is placed in the transmitter channel and connected to a USB3 Type-A connector. This particular example shows the polarity swapped on the RXP/N and TXP/N differential pairs. The positive signal may be routed to RXN as long as the corresponding output, TXN, is routed to the positive terminal on the connector (SSTXP). This allows routing to be done without crossing the differential pair signals and using extra vias. The EQ and DE terminals must be pulled up, pulled down, or left floating depending on the amount of equalization or de-emphasis that is desired. The OS terminal must be pulled down or left floating depending on the required output swing. In this example, the EQ terminal is pulled low through a resistor and the OS and DE terminals are left floating.

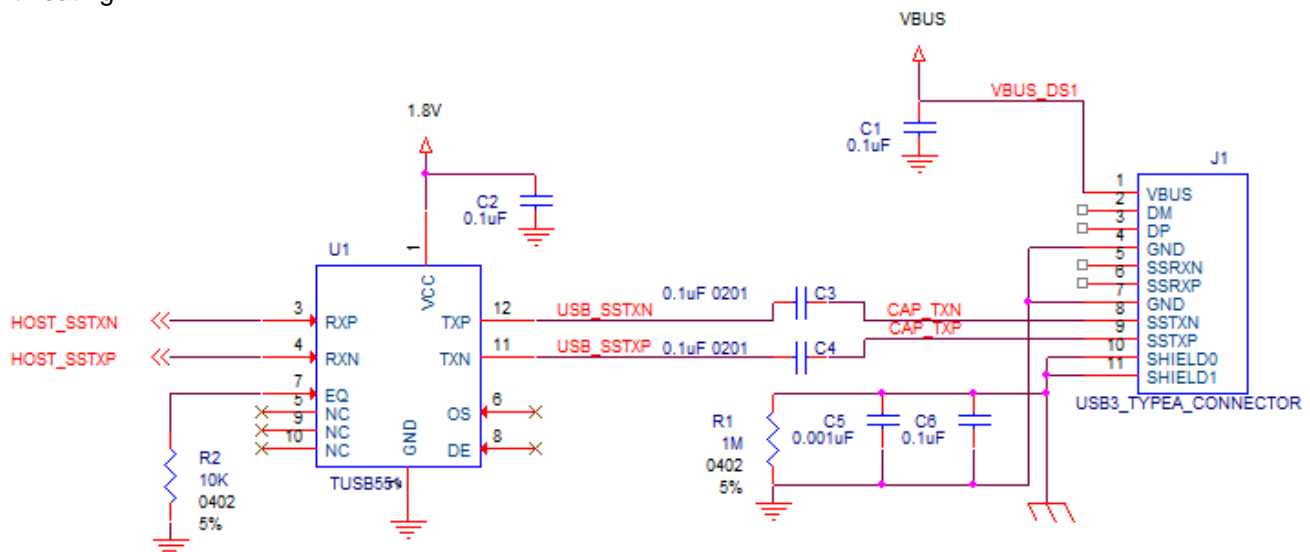


Figure 12. Transmitter Channel Implementation with Differential Pair Polarity Swapped

Typical Application (continued)

The TUSB551 is placed in the receiver channel and connected to a USB3 Type-A connector. This example shows the polarity matched, and the TUSB551 footprint is rotated so the trace routing of the differential pairs will not overlap. The EQ and DE terminals must be pulled up, pulled down, or left floating depending on the amount of equalization or de-emphasis that is desired. The OS terminal must be pulled down or left floating depending on the required output swing. In this example, the EQ and OS terminals are left floating and the DE terminal is pulled up through a resistor.

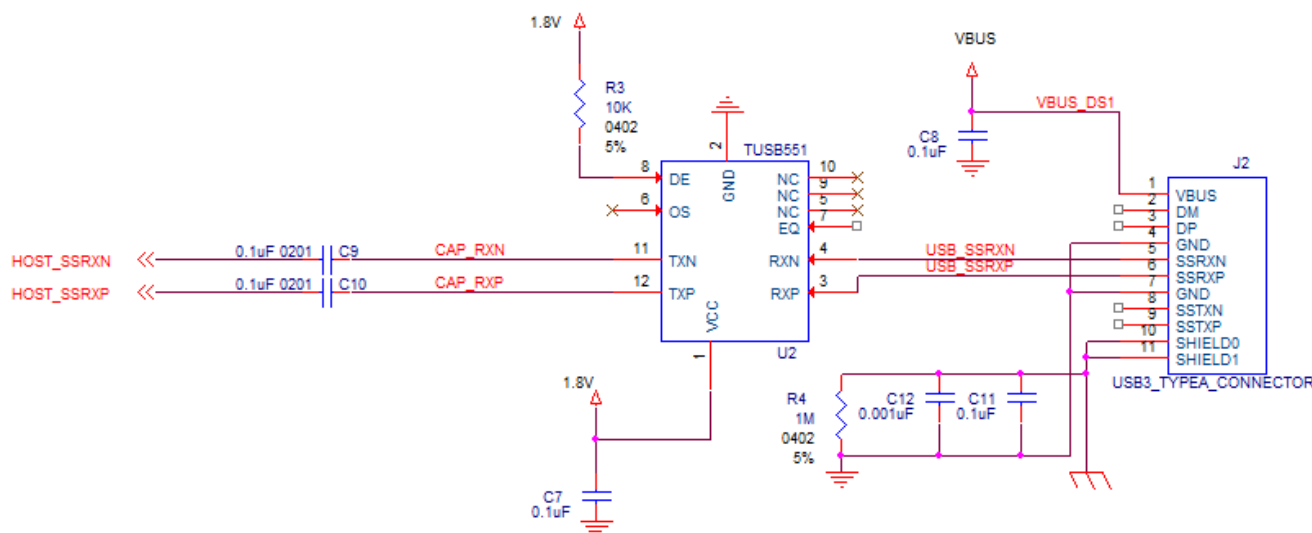


Figure 13. Receive Channel Implementation

9.2.1.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	100 mV to 1200 mV
Output Voltage Range	1050 mV to 1200 mV
Equalization	3, 6, 9 dB
De-Emphasis	0, -3.5, -6 dB (OS Floating)
VCC	1.8 V nominal supply

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

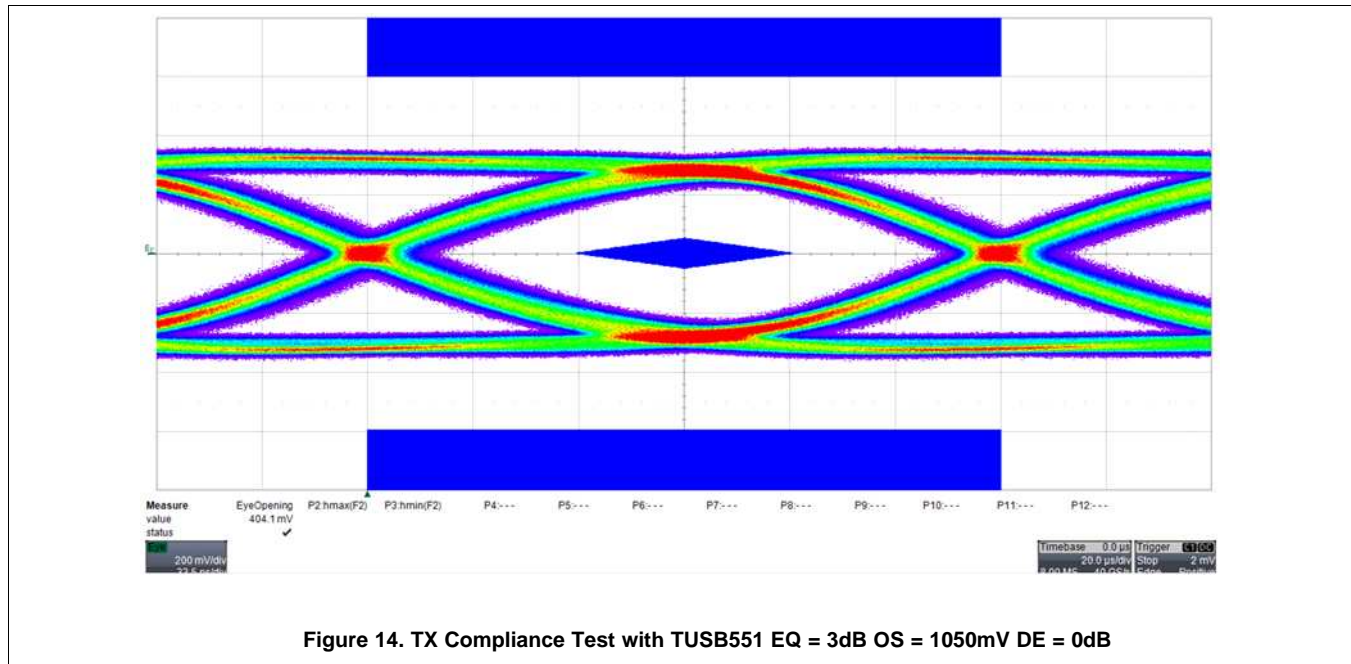
- Equalization (EQ) setting
- De-Emphasis (DE) setting
- Output Swing Amplitude (OS) setting

The equalization should be set based on the insertion loss in the pre-channel (channel before the TUSB551 device). The input voltage to the device is able to have a large range because of the receiver sensitivity and the available EQ settings. The EQ terminal can be pulled high through a resistor to VCC, low through a resistor to ground, or left floating. The application schematic above shows the implementation. See [Device Functional Modes](#) section for EQ values.

The De-Emphasis setting should be set based on the length and characteristics of the post channel (channel after the TUSB551 device). Output de-emphasis can be tailored using the DE terminal. This terminal should be pulled high through a resistor to VCC, low through a resistor to ground, or left floating. The application schematic above shows the implementation. See [Device Functional Modes](#) section for DE values.

The output swing setting can also be configured based on the amplitude needed to pass the compliance test. This setting will also be based on the length of interconnect or cable the TUSB551 is driving. This terminal should be pulled low through a resistor to ground or left floating. The application schematic above shows the implementation. See [Device Functional Modes](#) section for OS values.

9.2.1.3 Application Performance Plot



10 Power Supply Recommendations

This device is designed to operate with a 1.8V supply. If using a higher voltage system power supply such as VBUS, a voltage regulator can be used to step down to 1.8V. Decoupling capacitors may be used to reduce noise and improve power supply integrity.

11 Layout

11.1 Layout Guidelines

- The 100nF capacitors on the TXP and SSTXN nets should be placed close to the USB connector (Type A, Type B, and so forth).
- The ESD and EMI protection devices (if used) should also be placed as close as possible to the USB connector.
- Place voltage regulators as far away as possible from the differential pairs.
- In general, the large bulk capacitors associated with each power rail should be placed as close as possible to the voltage regulators.
- It is recommended that small decoupling capacitors for the 1.8V power rail be placed close to the TUSB551 as shown below.
- The SuperSpeed differential pair traces for RXP/N and TXP/N must be designed with a characteristic impedance of $90\Omega \pm 10\%$. The PCB stack-up and materials will determine the width and spacing needed for a characteristic impedance of 90Ω .
- The SuperSpeed differential pair traces should be routed parallel to each other as much as possible. It is recommended the traces be symmetrical.
- In order to minimize cross talk, it is recommended to keep high speed signals away from each other. Each pair should be separated by at least 5 times the signal trace width. Separating with ground will also help.

Layout Guidelines (continued)

minimize cross talk.

- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.
- Adding test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
- Avoid 90 degree turns in traces. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.
- Match the etch lengths of the differential pair traces. There should be less than 5 mils difference between a SS differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.
- The etch lengths of the differential pair groups do not need to match (i.e. the length of the RXP/N pair to that of the TXP/N pair), but all trace lengths should be minimized.
- Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible to the TUSB551 device.
- To ease routing, the polarity of the SS differential pairs can be swapped. This means that TXP can be routed to TXN or RXN can be routed to RXP.
- Do not place power fuses across the differential pair traces.

11.2 Layout Example

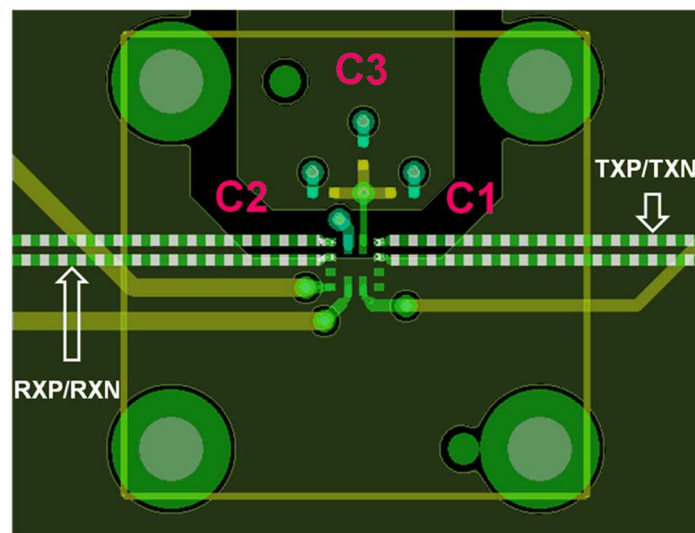


Figure 15. TUSB551 PCB Layout Example

12 器件和文档支持

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB551RWBR	Active	Production	X2QFN (RWB) 12	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	51
TUSB551RWBR.A	Active	Production	X2QFN (RWB) 12	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	51

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB551RWBR	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.61	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB551RWBR	X2QFN	RWB	12	3000	213.0	191.0	35.0



RWB0012A



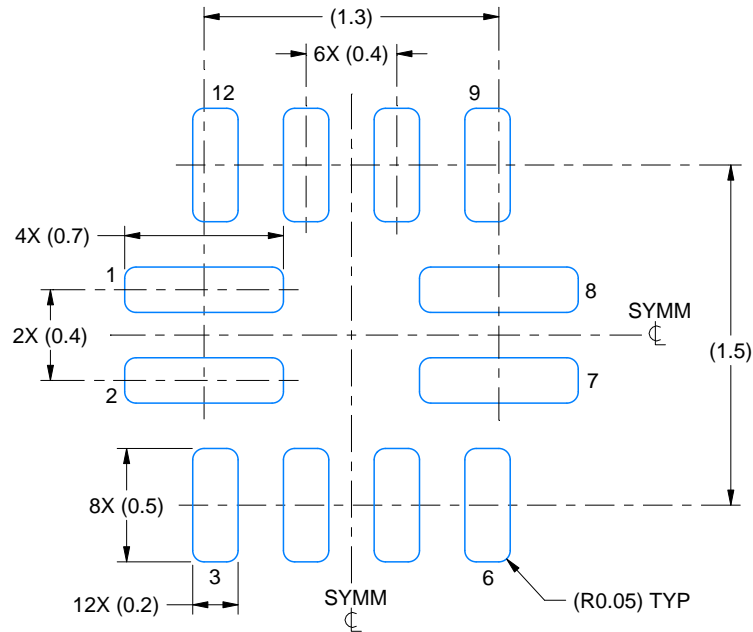
- 
- TEXAS
INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

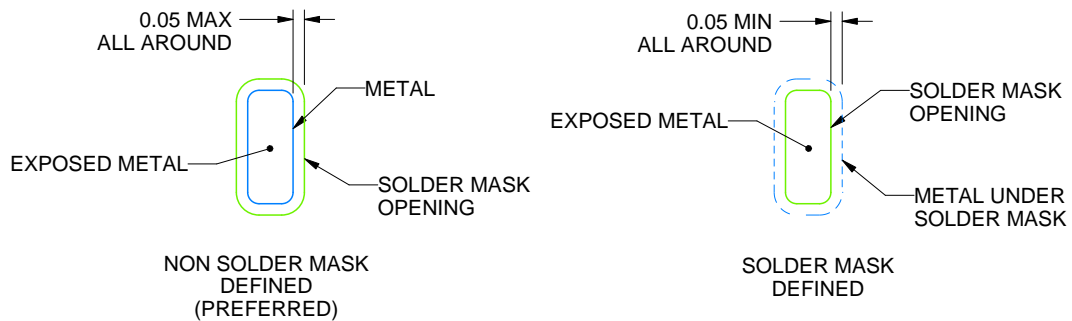
RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

4221631/B 07/2017

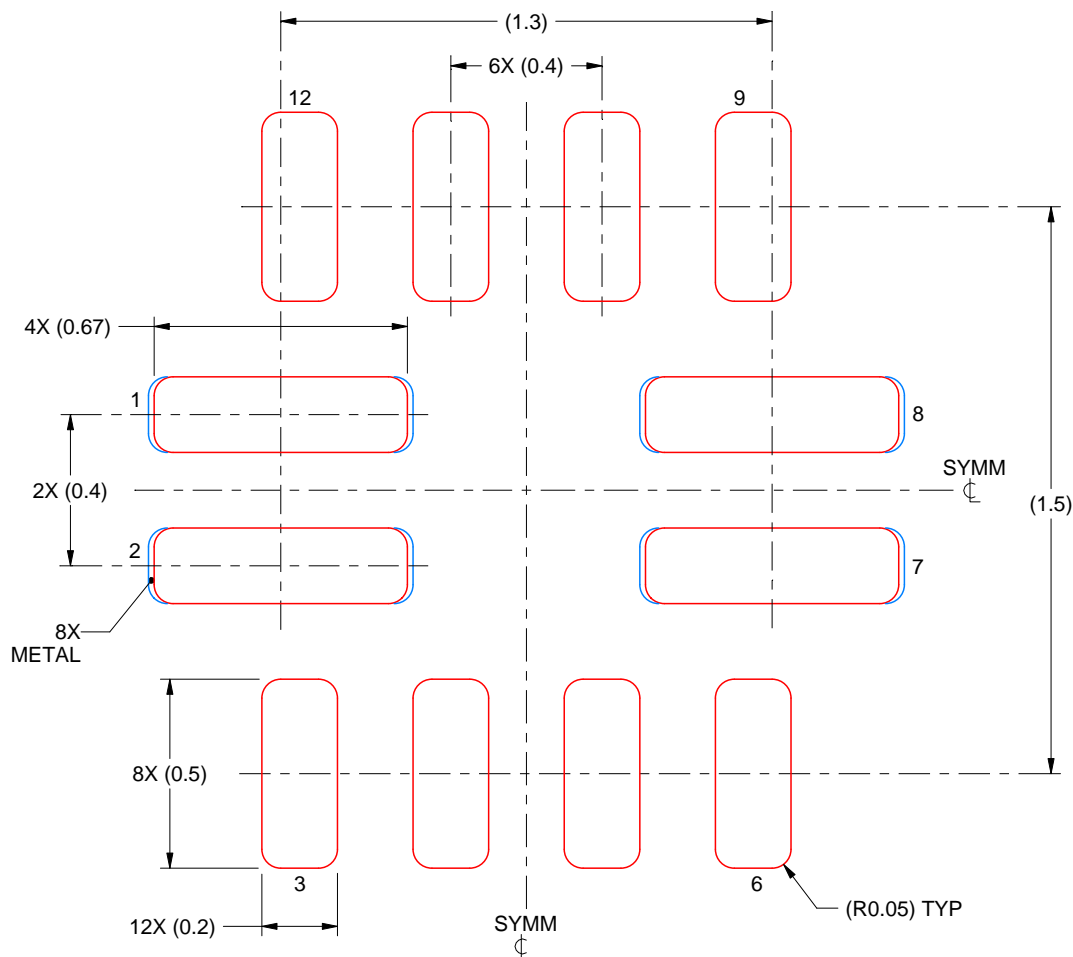
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

4221631/B 07/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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