支持均衡的 **USB 3.0** 单通道转接驱动器

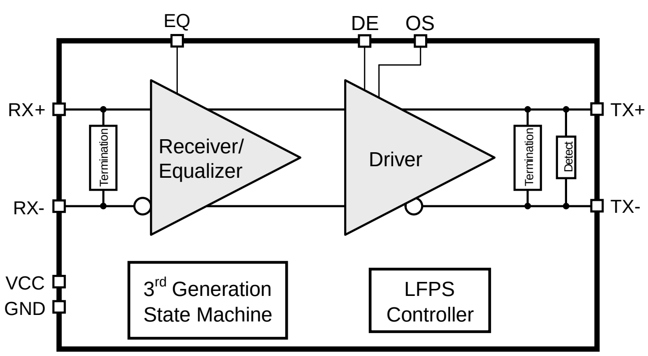
查询样品: **TUSB501**

特性

- 积极低功耗架构（典型值）：
  - **126mW** 有源功耗
  - 在 **U2/U3** 中为 **20mW**
  - 无连接时为 **3mW**
- 自动低频率周期信号 **(LFPS)** 去加重 **(DE)** 控制
- 出色的抖动与损耗补偿
  - **32** 英寸的 **FR4 4** 毫英寸带状线
  - 长度 **3m** 的 **30** 美制电线标准 **(AWG)** 电缆
- 集成型终端
- 小型 **2mm × 2mm** 四方扁平无引线 **(QFN)** 封装
- 可选接收器均衡、发射器去加重和输出摆动
- 支持热插拔
- 静电放电 **(ESD)** 保护 **±5kV** 人体模型 **(HBM)**

应用范围

- 手机、计算机、扩展坞、电视、有源电缆、背板



说明

TUSB501 是一款 3rd代 3.3V USB 3.0 单通道转接驱动器。 当 5Gbps 超高速 USB 信号由印刷电路板 (PCB) 或电缆传播时，信号完整性会由于损耗和符号间干扰而降级。 TUSB501 通过采用补偿通道损耗的均衡来恢复进入的数据，并且使用一个高差分电压来向外驱动信号。 这样扩展了可能的通道长度，并且使系统能够符合 USB3.0 兼容性。 TUSB501 高级状态机使得它对于主机和器件透明。

加电后，TUSB501 在 TX 对上定期执行接收器检测。 如果它检测到一个超高速 USB 接收器，RX 端接被启用，TUSB501 为转接驱动做好准备。

接收器均衡器具有三个由引脚 EQ 控制的增益设置：3dB，6dB 和 9dB。 这应该在 TUSB501 之前根据损耗量设定。 相似地，输出驱动器支持去加重和输出摆动配置（引脚 DE 和 OS）。 这些设置使得 TUSB501 可被灵活地放置在超高速 USB 路径上，并具有最优性能。

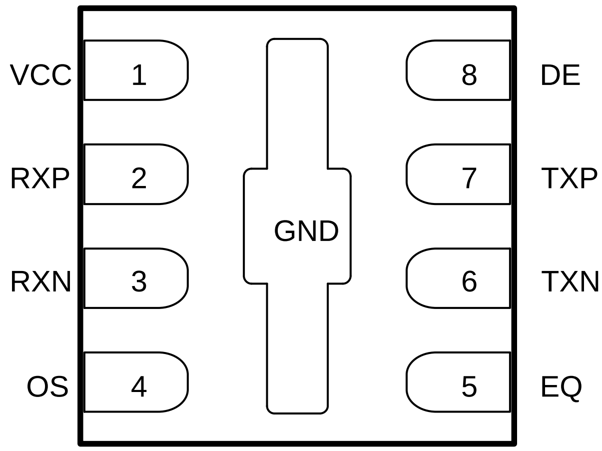
与之前几代产品相比，TUSB501 在全部链路状态下功耗减少，一个更加强大的 OS 选项，经改进的接收器均衡设置和一个智能 LFPS 控制器。 这个控制器感测低频信号，并且自动禁用驱动器去加重，以实现 USB 3.0 兼容性。

TUSB501 被封装在小型 2mm x 2mm 四方扁平无引线 (QFN) 封装内，并在 –40°C 至 85°的工业用温度范围内运行。

English Data Sheet: SLLSEG5

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DRF PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
RXP	2	Differential I/O	Differential input pair for 5 Gbps SuperSpeed USB signals.
RXN	3		
TXN	6		Differential output pair for 5 Gbps SuperSpeed USB signals.
TXP	7		
EQ	5	CMOS Input	Sets the receiver equalizer gain. 3-state input with integrated pull-up and pull-down resistors.
DE	8		Sets the output de-emphasis gain. 3-state input with integrated pull-up and pull-down resistors.
OS	4		Sets the output swing (differential voltage amplitude). 2-state input with an integrated pull-down resistor.
VCC	1	Power	3.3-V power supply
GND	Thermal Pad		Reference ground

DEVICE CONFIGURATION

Table 1. Control Pin Effects (Typical Values)

PIN	DESCRIPTION	LOGIC STATE	GAIN
EQ	Equalization Amount	Low	3 dB
		Floating	6 dB
		High	9 dB

PIN	DESCRIPTION	LOGIC STATE	OUTPUT DIFFERENTIAL VOLTAGE FOR THE TRANSITION BIT
OS	Output Swing Amplitude	Low	930 mV_{pp}
		High	1300 mV_{pp}

PIN	DESCRIPTION	LOGIC STATE	DE-EMPHASIS RATIO	
			FOR OS = LOW	FOR OS = HIGH
DE	De-Emphasis Amount	Low	0 dB	–2.6 dB
		Floating	–3.5 dB	–5.9 dB
		High	–6.2 dB	–8.3 dB

(1) Typical values

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range (2)	V_{CC}	–0.5	4	V
Voltage range at any input or output terminal	Differential I/O	–0.5	4	V
	CMOS inputs	–0.5	V_{CC} + 0.5	V
Electrostatic discharge	Human body model (all pins) (3)		±5	kV
	Charged-device model (all pins) (4)		±1.5	
Storage temperature, T_{STG}		–65	150	°C
Maximum junction temperature, T_J		-40	105	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.

THERMAL INFORMATION

THERMAL METRIC (1)		TUSB501	UNITS
		DRF	
θ_{JA}	Junction-to-ambient thermal resistance	102.4	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	90.3	
θ_{JB}	Junction-to-board thermal resistance	21.2	
ψ_{JT}	Junction-to-top characterization parameter	70	
ψ_{JB}	Junction-to-board characterization parameter	3.6	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	70.2	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Main power supply	3	3.3	3.6	V
T_A	Operating free-air temperature	–40		85	°C
C_{AC}	AC coupling capacitor	75	100	200	nF

POWER SUPPLY CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
$I_{CC\text{-}ACTIVE}$	Average active current	Link in U0 with SuperSpeed USB data transmission, OS = Low		38.1		mA
		Link in U0 with SuperSpeed USB data transmission, OS = High		43.8	65	
$I_{CC\text{-}IDLE}$	Average current in idle state	Link has some activity, not in U0, OS = Low		29.8		mA
$I_{CC\text{-}U2U3}$	Average current in U2/U3	Link in U2 or U3		6.1		mA
$I_{CC\text{-}NC}$	Average current with no connection	No SuperSpeed USB device is connected to TXP, TXN		1.3		mA
P_D	Power Dissipation in U0	OS = Low		126		mW
		OS = High		145	234	

(1) TYP values use V_{CC} = 3.3 V, T_A = 25°C.
(2) MAX values use V_{CC} = 3.6 V, T_A = –40°C.

DC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3-State CMOS Inputs (EQ, DE)						
V_{IH}	High-level input voltage		2.8			V
V_{IM}	Mid-level input voltage			V_{CC} / 2		V
V_{IL}	Low-level input voltage				0.6	V
V_F	Floating voltage	V_{IN} = High impedance		V_{CC} / 2		V
R_{PU}	Internal pull-up resistance			190		kΩ
R_{PD}	Internal pull-down resistance			190		kΩ
I_{IH}	High-level input current	V_{IN} = 3.6 V			36	µA
I_{IL}	Low-level input current	V_{IN} = GND, V_{CC} = 3.6 V	-36			µA
2-State CMOS Input (OS)						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.5	V
V_F	Floating voltage	V_{IN} = High impedance		GND		V
R_{PD}	Internal pull-down resistance			270		kΩ
I_{IH}	High-level input current	V_{IN} = 3.6 V			26	µA
I_{IL}	Low-level input current	V_{IN} = GND	-1			µA

AC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Receiver (RXP, RXN)						
$V_{DIFF\text{-}pp}$	Input differential voltage swing	AC-coupled differential peak-to-peak signal	100		1200	mV_{pp}
$V_{CM\text{-}RX}$	Common-mode voltage bias in the receiver (DC)			3.3		V
$Z_{RX\text{-}DIFF}$	Differential input impedance (DC)	Present after a SuperSpeed USB device is detected on TXP/TXN	72	91	120	Ω
$Z_{RX\text{-}CM}$	Common-mode input impedance (DC)	Present after a SuperSpeed USB device is detected on TXP, TXN	18	22.8	30	Ω
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	Common-mode input impedance with termination disabled (DC)	Present when no SuperSpeed USB device is detected on TXP, TXN. Measured over the range of 0-500 mV with respect to GND.	25	35		kΩ
$V_{RX\text{-}LFPS\text{-}DET\text{-}DIFF\text{-}pp}$	Low Frequency Periodic Signaling (LFPS) Detect Threshold	Below the minimum is squelched	100		300	mV_{pp}
Differential Transmitter (TXP, TXN)						
$V_{TX\text{-}DIFF\text{-}PP}$	Transmitter differential voltage swing (transition-bit)	OS = Low, No load		930		mV_{pp}
		OS = High, No load		1300		
$V_{TX\text{-}DE\text{-}RATIO}$	Transmitter de-emphasis	DE = Floating, OS = Low		-3.5		dB
C_{TX}	TX input capacitance to GND	At 2.5 GHz		1.25		pF
$Z_{TX\text{-}DIFF}$	Differential impedance of the driver		75	93	125	Ω
$Z_{TX\text{-}CM}$	Common-mode impedance of the driver	Measured with respect to AC ground over 0-500 mV	18.75		31.25	Ω
$I_{TX\text{-}SC}$	TX short circuit current	TX ± shorted to GND			60	mA
$V_{CM\text{-}TX}$	Common-mode voltage bias in the transmitter (DC)		1.2		2.5	V
$V_{CM\text{-}TX\text{-}AC}$	AC common-mode voltage swing in active mode	Within U0 and within LFPS			100	mV_{pp}
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}AC\text{-}pp}$	Differential voltage swing during electrical idle	Tested with a high-pass filter	0		10	mV_{pp}
$V_{TX\text{-}CM\text{-}DeltaU1\text{-}U0}$	Absolute delta of DC CM voltage during active and idle states	Restrict the test condition to meet 100 mV			100	mV
$V_{TX\text{-}idle\text{-}diff\text{-}DC}$	DC electrical idle differential output voltage	Voltage must be low pass filtered to remove any AC component	0		12	mV
Differential Transmitter (TXP, TXN)						
t_R, t_F	Output rise, fall time see Figure 4	20%-80% of differential voltage measured 1 inch from the output pin		80		ps
$t_{RF\text{-}MM}$	Output Rise, Fall time mismatch	20%-80% of differential voltage measured 1 inch from the output pin			20	ps
$t_{diff\text{-}LH}$, $t_{diff\text{-}HL}$	Differential propagation delay see Figure 2	De-emphasis = -3.5 dB propagation delay between 50% level at input and output		290		ps
$t_{idleEntry}$, $t_{idleExit}$	Idle entry and exit times see Figure 3			3.6		ns

AC ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing						
t_{READY}	Time from power applied until RX termination	Apply 0 V to VCC, connect SuperSpeed USB termination to TX±, apply 3.3 V to VCC, and measure when $Z_{RX\text{-}DIFF}$ is enabled.		9		ms
Jitter						
$T_{JTX\text{-}EYE}$	Total jitter (1) (2)	EQ = Floating, OS = High, DE = High See Figure 1.		0.213		UI (3)
D_{JTX}	Deterministic jitter (2)			0.197		UI (3)
R_{JTX}	Random jitter (2) (4)			0.016		UI (3)

(1) Includes R_J at 10^{-12}.
(2) Measured at the ends of reference channel in Figure 1 with K28.5 pattern, V_{ID} = 1000 mV_{pp}, 5 Gbps, -3.5 dB de-emphasis from source.
(3) UI = 200 ps.
(4) R_j calculated as 14.069 times the RMS random jitter for 10^{-12} BER.

PARAMETER MEASUREMENT INFORMATION

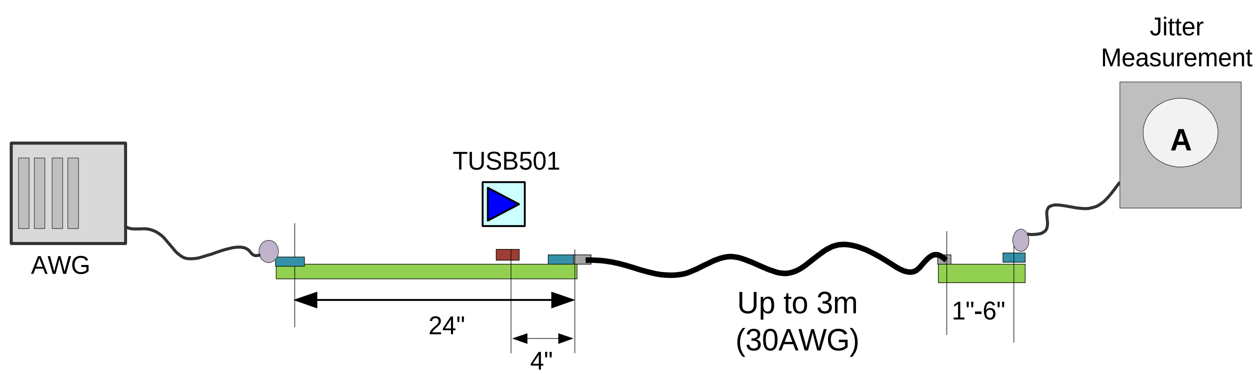


Figure 1. Jitter Measurement Setup

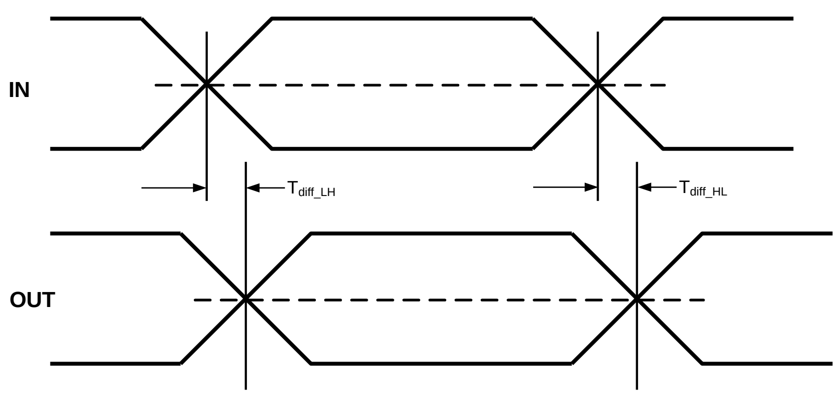


Figure 2. Propagation Delay

PARAMETER MEASUREMENT INFORMATION (continued)

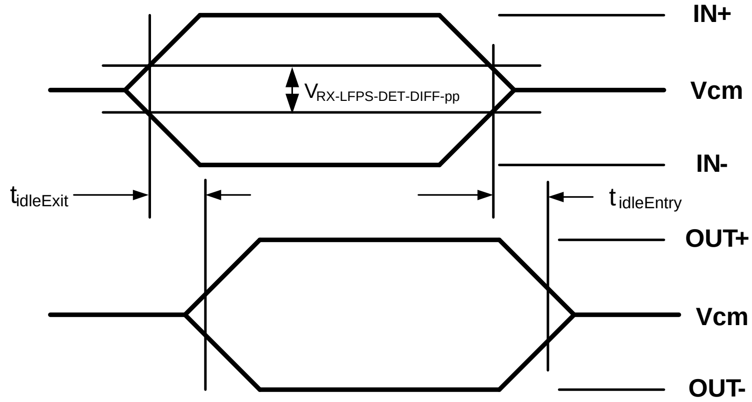


Figure 3. Electrical Idle Mode Exit and Entry Delay

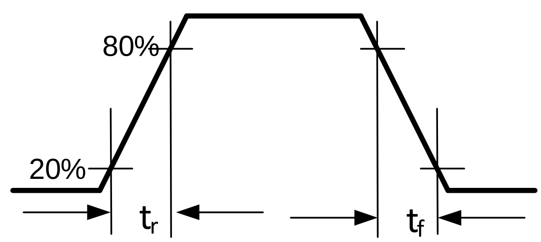


Figure 4. Output Rise and Fall Times

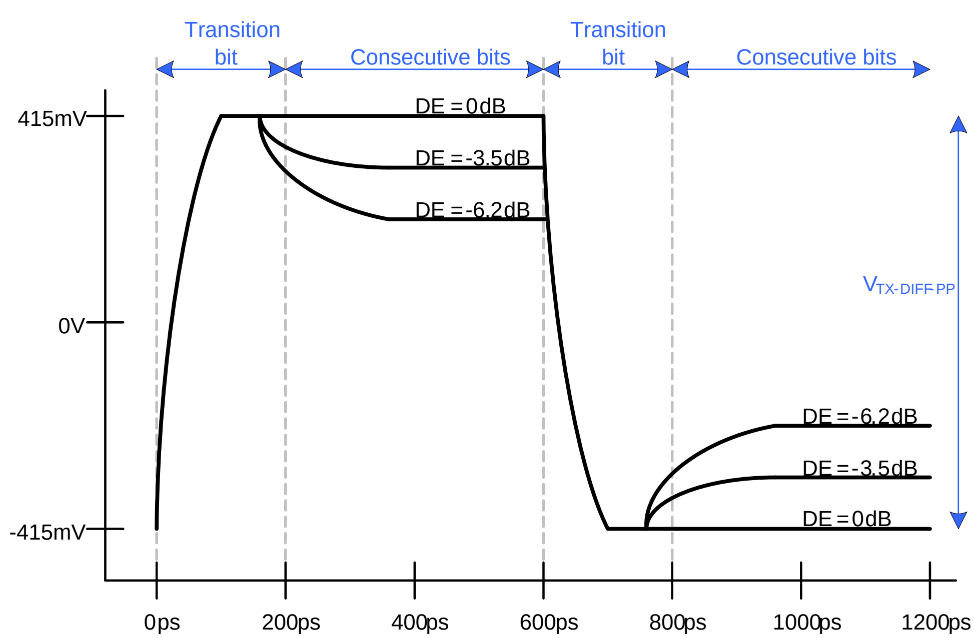


Figure 5. Transmitter Differential Voltage, OS = L

PARAMETER MEASUREMENT INFORMATION (continued)

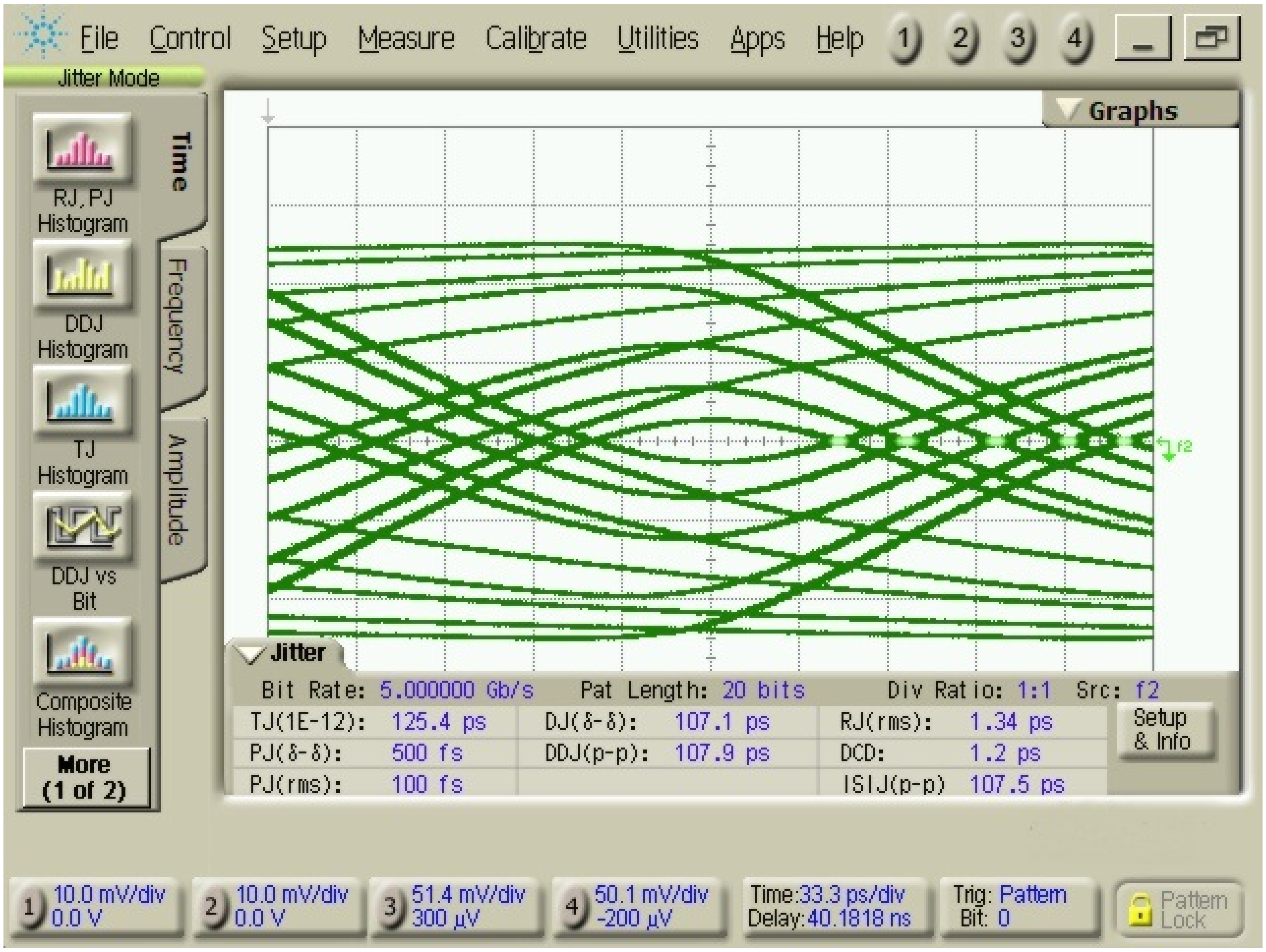


Figure 6. Input for Typical Output Measurement at TUSB501 at T_A = 25°C

PARAMETER MEASUREMENT INFORMATION (continued)

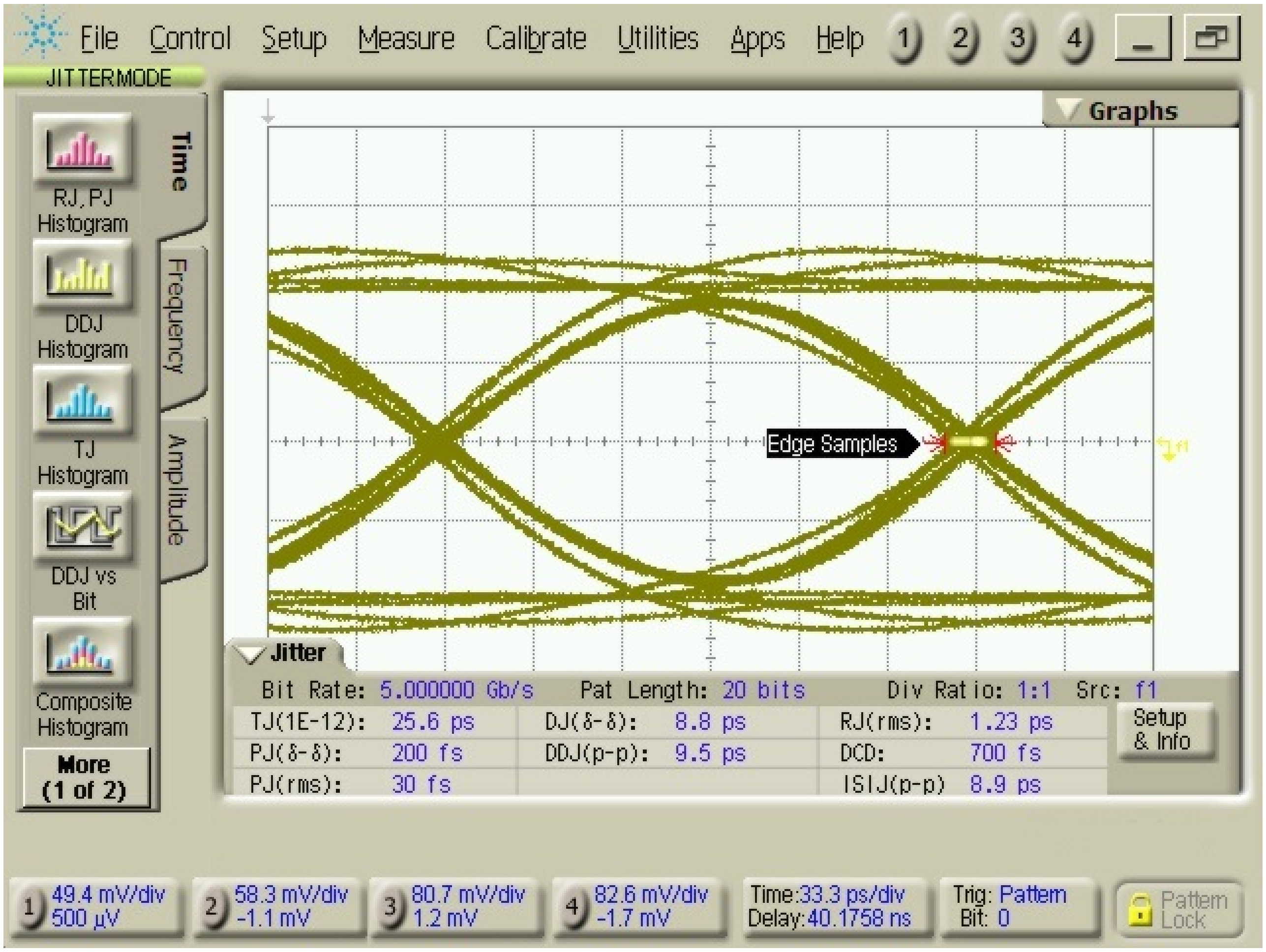


Figure 7. Typical Output Eye for Jitter Measurement Setup in Figure 1 at T_A = 25°C, DE = HIGH, OS = HIGH, EQ = NC

REVISION HISTORY

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB501DRFR	Active	Production	WSON (DRF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T501
TUSB501DRFR.B	Active	Production	WSON (DRF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T501
TUSB501DRFRG4	Active	Production	WSON (DRF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T501
TUSB501DRFRG4.B	Active	Production	WSON (DRF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T501

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TUSB501 :

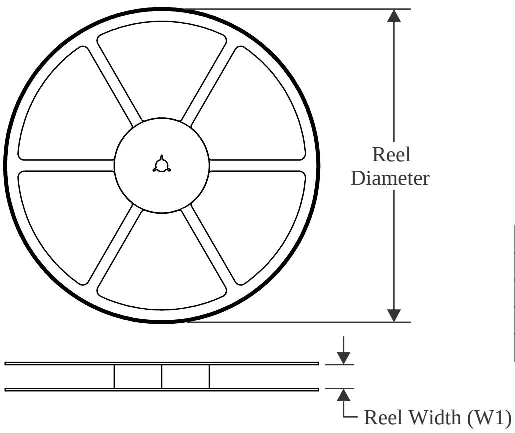
- Automotive : TUSB501-Q1

NOTE: Qualified Version Definitions:

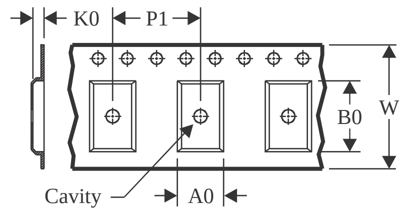
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

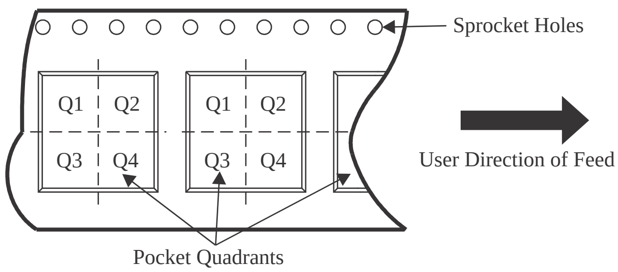


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

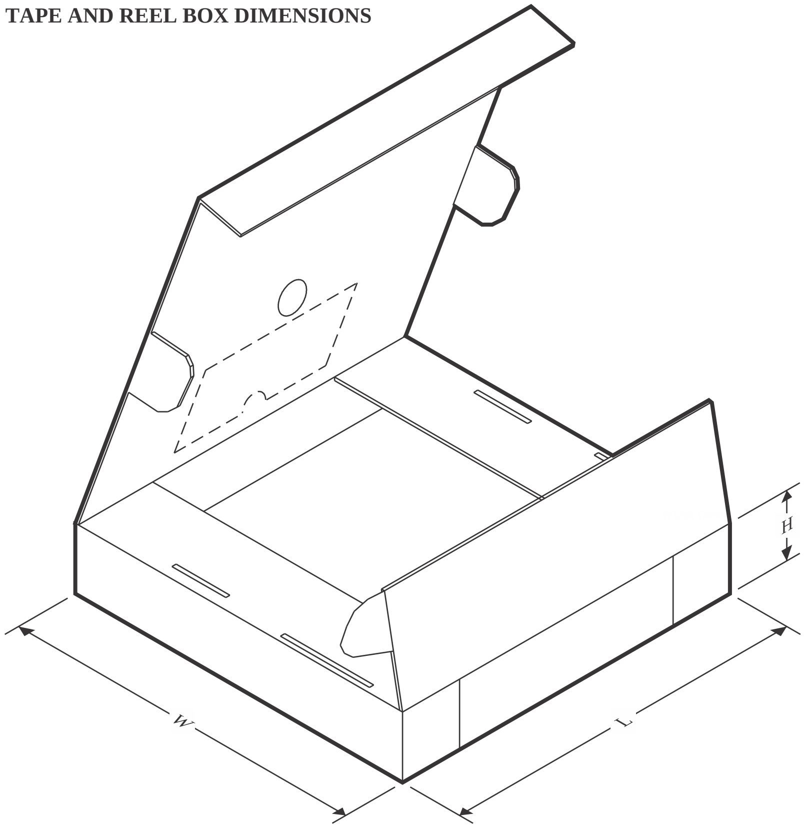
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB501DRFR	WSON	DRF	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TUSB501DRFRG4	WSON	DRF	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

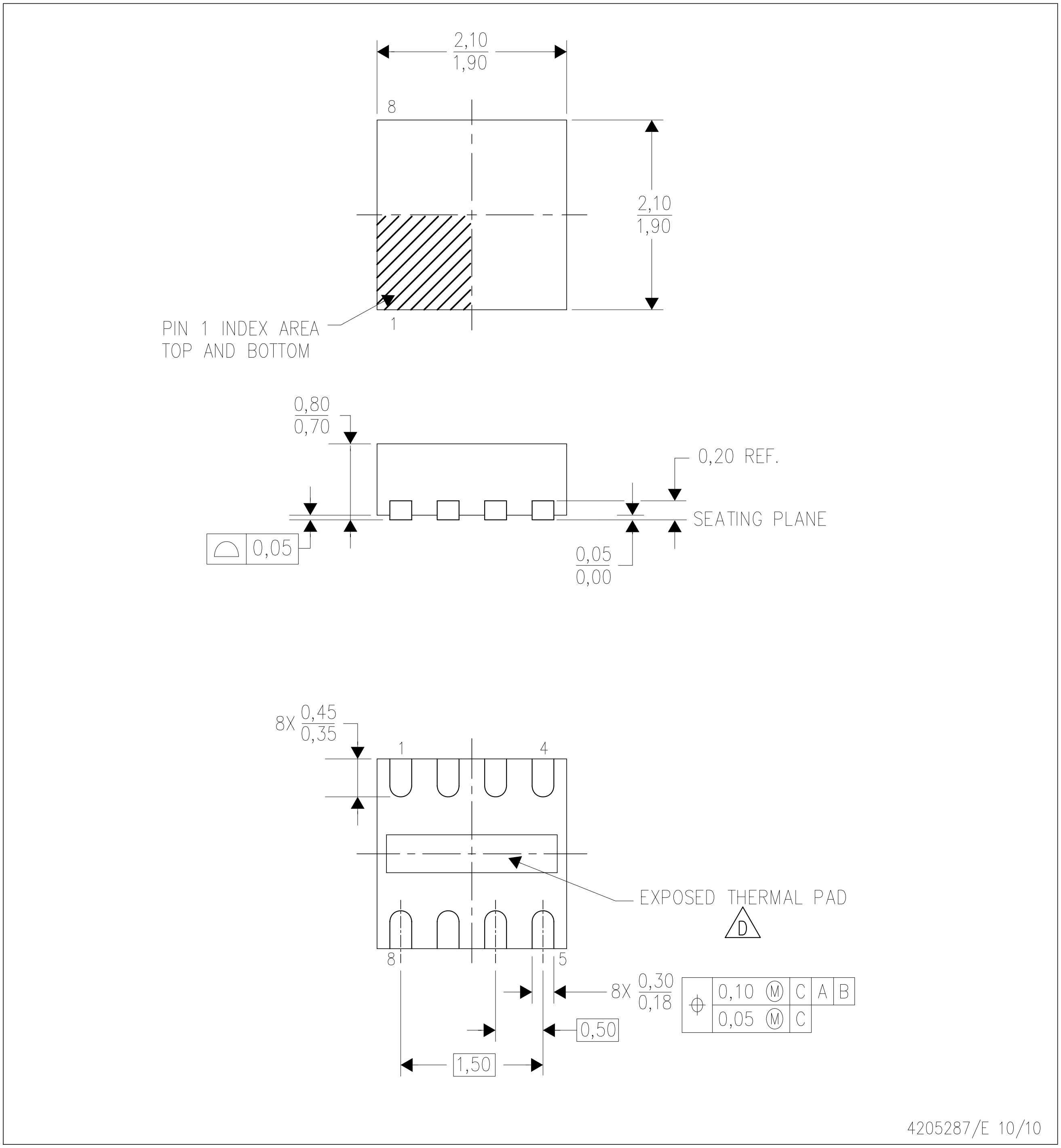
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB501DRFR	WSON	DRF	8	3000	210.0	185.0	35.0
TUSB501DRFRG4	WSON	DRF	8	3000	210.0	185.0	35.0

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

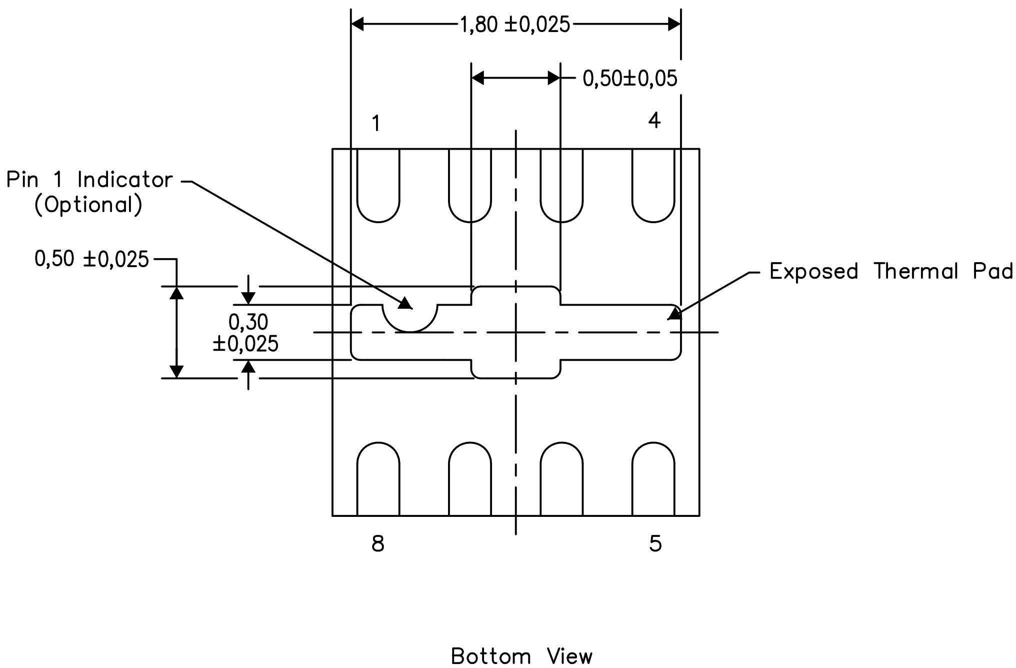
DRF (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

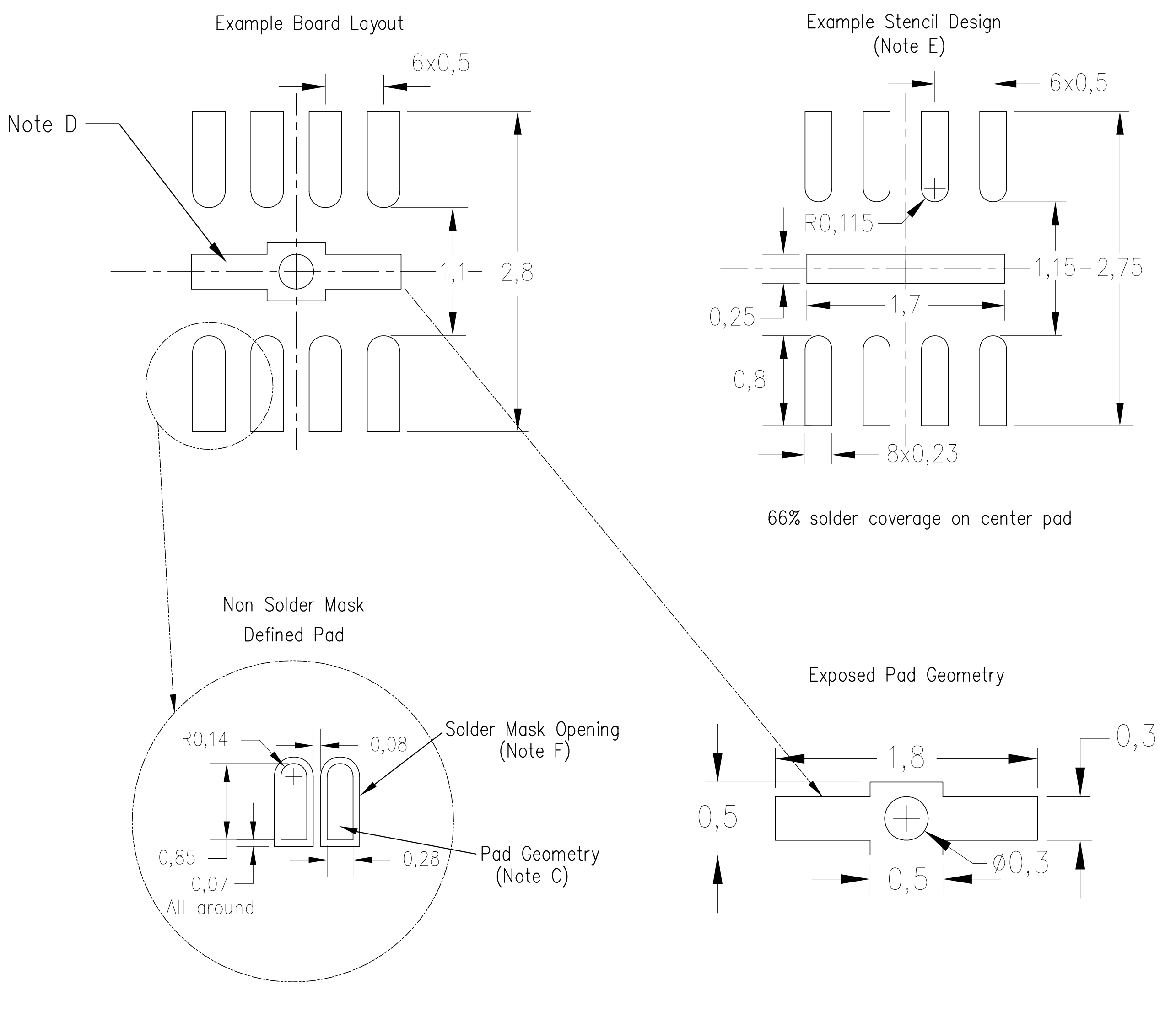


Exposed Thermal Pad Dimensions

4206840/H 12/14

NOTE: A. All linear dimensions are in millimeters

DRF (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



4209166/C 03/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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