

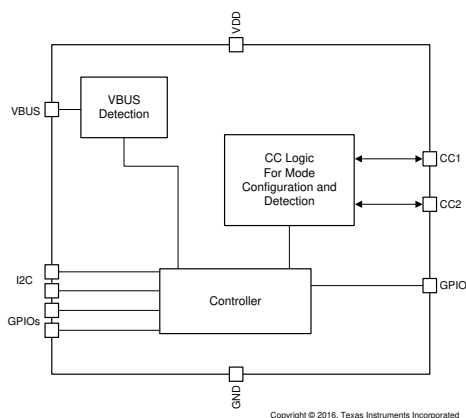
## TUSB320 USB Type-C™ 配置通道逻辑和端口控制 ( )

### 1 特性

- USB Type-C™ 规范 1.1
- 向后兼容 USB Type-C 规范 1.0
- 支持高达 3A 的电流广播和检测
- 模式配置
  - 仅主机 - DFP (拉电流)
  - 仅器件 - UFP (灌电流)
  - 双角色端口 - DRP
- 通道配置 (CC)
  - USB 端口连接检测
  - 电缆方向检测
  - 角色检测
  - Type-C 电流模式 (默认、中等和高)
- V<sub>BUS</sub> 检测
- I<sup>2</sup>C 或 GPIO 控制
- 通过 I<sup>2</sup>C 实现角色配置控制
- 电源电压: 2.7V 至 5V
- 低电流消耗
- 工业温度范围: -40°C 至 85°C

### 2 应用

- 主机、器件、双角色端口应用
- [手机](#)
- [平板电脑](#)和[笔记本电脑](#)
- [USB 外设](#)



简化版原理图

### 3 说明

TUSB320 器件可在 USB Type-C 端口上实现 Type-C 生态系统所需的配置通道 (CC) 逻辑。TUSB320 器件使用 CC 引脚来确定端口的连接状态和电缆方向, 以及进行角色检测和 Type-C 电流模式控制。TUSB320 器件可配置为下行端口 (DFP)、上行端口 (UFP) 或双角色端口 (DRP), 是任何应用的理想之选。

根据 Type-C 规范, TUSB320 器件会交替配置为 DFP 或 UFP。CC 逻辑块通过监视 CC1 和 CC2 引脚上的上拉或下拉电阻来确定 USB 端口的连接时间、电缆的方向以及检测到的角色。CC 逻辑根据检测到的角色来确定 Type-C 电流模式为默认、中等还是高。该逻辑通过实施 V<sub>BUS</sub> 检测来确定端口在 UFP 和 DRP 模式下是否连接成功。

该器件能够在宽电源范围内工作, 并且具有较低功耗。TUSB320 器件适用于工业级和商业级温度范围。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TUSB320	X2QFN (12)	1.60mm × 1.60mm
TUSB320I	X2QFN (12)	1.60mm × 1.60mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



示例应用



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision E (May 2017) to Revision F (March 2022)</b> .....	<b>Page</b>
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 在整个数据表中将术语 <i>主机</i> 更改为 <i>控制器</i> ，以便与 MIPI I3C 规范和 NXP 的包容性语言项目保持一致.....	1
• Added the Junction Temperature to the <i>Absolute Maximum Ratings</i> section.....	5
• Changed the tCCCB_DEFAULT typical parameter from 168 ms to 133 ms.....	7
• Added <i>Functional Block Diagram</i> section.....	9
<b>Changes from Revision D (October 2016) to Revision E (May 2017)</b> .....	<b>Page</b>
• Changed R <sub>VBUS</sub> values From: MIN = 891, TYP = 900, MAX = 909 K $\Omega$ To: MIN = 855, TYP = 887, MAX = 920 K $\Omega$ .....	6
<b>Changes from Revision C (September 2016) to Revision D (October 2016)</b> .....	<b>Page</b>
• Changed text for Pin 7 in the <i>Pin Functions</i> table From: "default current mode detected (H); medium or high current mode detected (L)." To: "Refer to 表 7-3 for more details.".....	4
• Changed text for Pin 8 in the <i>Pin Functions</i> table From: "default or medium current mode detected (H); high current mode detected (L)." To: "Refer to 表 7-3 for more details.".....	4
<b>Changes from Revision B (March 2016) to Revision C (September 2016)</b> .....	<b>Page</b>
• Changed pins CC1 and CC2 values From: MIN = -0.3 MAX = V <sub>DD</sub> + 0.3 To: MIN -0.3 MAX = 6 in the 节 6.1 ...	5
<b>Changes from Revision A (June 2015) to Revision B (March 2016)</b> .....	<b>Page</b>
• Added Note 1 and 2 to the <i>Pin Functions</i> table.....	4
• Changed the DESCRIPTION of pin EN_N pin in the <i>Pin Functions</i> table.....	4
• Changed the DESCRIPTION of pin V <sub>DD</sub> in the <i>Pin Functions</i> table.....	4
• Changed the MIN, TYP, and MAX values for V <sub>TH_UFP_CC_USB</sub> , V <sub>TH_UFP_CC_MED</sub> , and V <sub>TH_UFP_CC_HIGH</sub> in the 节 6.5 table.....	6
• Added Test Condition "See 图 6-1" to V <sub>BUS_THR</sub> in the 节 6.5 .....	6

• Added Note 2 to the <a href="#">节 6.5</a> table .....	<a href="#">6</a>
• Updated <a href="#">节 6.6</a> table with new values.....	<a href="#">7</a>
• Added <i>Data hold time</i> , <i>Data valid time</i> , <i>Data valid acknowledge time</i> , and $C_{bus\_400kHz}$ values to <a href="#">节 6.6</a> table....	<a href="#">7</a>
• Changed the <a href="#">节 6.7</a> table .....	<a href="#">7</a>
• Added Note: "SW must make sure..." to the Description of INTERRUPT_STATUS in <a href="#">表 7-7</a> .....	<a href="#">16</a>
• Added text to list item 2 in the <a href="#">节 8.3</a> section.....	<a href="#">27</a>

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**Changes from Revision \* (May 2015) to Revision A (June 2015)**
**Page**

• 将 TUSB320 的器件状态从产品预发布更改为量产数据 .....	<a href="#">1</a>
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## 5 Pin Configuration and Functions

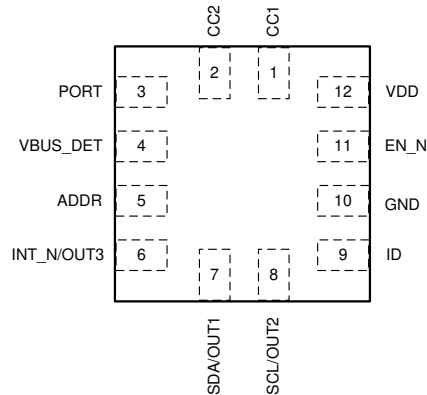


图 5-1. RWB Package, 12-Pin X2QFN (Top View)

表 5-1. Pin Functions

PIN		TYPE <sup>(3)</sup>	DESCRIPTION
NAME	NO.		
CC1	1	I/O	Type-C configuration channel signal 1
CC2	2	I/O	Type-C configuration channel signal 2
PORT <sup>(1)</sup>	3	I	Tri-level input pin to indicate port mode. The state of this pin is sampled when EN_N is asserted low and VDD is active. This pin is also sampled following a I2C_SOFT_RESET. H - DFP (Pull-up to VDD if DFP mode is desired) NC - DRP (Leave unconnected if DRP mode is desired) L - UFP (Pull-down or tie to GND if UFP mode is desired)
VBUS_DET <sup>(1)</sup>	4	I	5- to 28-V VBUS input voltage. VBUS detection determines UFP attachment. One 900-kΩ external resistor required between system VBUS and VBUS_DET pin.
ADDR <sup>(1)</sup>	5	I	Tri-level input pin to indicate I2C address or GPIO mode: H - I2C is enabled and I2C 7-bit address is 0x61. NC - GPIO mode (I2C is disabled) L - I2C is enabled and I2C 7-bit address is 0x60. ADDR pin should be pulled up to VDD if high configuration is desired
INT_N/OUT3 <sup>(1)</sup>	6	O	The INT_N/OUT3 is a dual-function pin. When used as the INT_N, the pin is an open drain output in I2C control mode and is an active low interrupt signal for indicating changes in I2C registers. When used as OUT3, the pin is in audio accessory detect in GPIO mode: no detection (H), audio accessory connection detected (L).
SDA/OUT1 <sup>(1) (2)</sup>	7	I/O	The SDA/OUT1 is a dual-function pin. When I2C is enabled (ADDR pin is high or low), this pin is the I2C communication data signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the TUSB320 device is in UFP mode: Refer to 表 7-3 for more details.
SCL/OUT2 <sup>(1) (2)</sup>	8	I/O	The SCL/OUT2 is a dual function pin. When I2C is enabled (ADDR pin is high or low), this pin is the I2C communication clock signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the TUSB320 device is in UFP mode: Refer to 表 7-3 for more details.
ID <sup>(1)</sup>	9	O	Open drain output; asserted low when the CC pins detect device attachment when port is a source (DFP), or dual-role (DRP) acting as source (DFP).
GND	10	G	Ground
EN_N	11	I	Enable signal; active low. Pulled up to VDD internally to disable the TUSB320 device. If controlled externally, must be held high at least for 50 ms after VDD has reached its valid voltage level.
VDD	12	P	Positive supply voltage. VDD must ramp within 25 ms or less

- (1) When VDD is off, the TUSB320 non-failsafe pins (VBUS\_DET, ADDR, PORT, ID, OUT[3:1] pins) could back-drive the TUSB320 device if not handled properly. When necessary to pull these pins up, it is recommended to pullup PORT, ADDR, INT\_N/OUT3, and ID to the device VDD supply. The VBUS\_DET must be pulled up to VBUS through a 900-kΩ resistor.
- (2) When using the 3.3 V supply for I2C, the end user must ensure that the VDD is 3 V and above. Otherwise the I2C may back power the device.
- (3) I = input, O = output, P = power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	V <sub>DD</sub>	-0.3	6	V
Control pins	PORT, ADDR, ID, EN_N, INT_N/OUT3	-0.3	V <sub>DD</sub> + 0.3	V
	CC1, CC2	-0.3	6	
	SDA/OUT1, SCL/OUT2	-0.3	V <sub>DD</sub> + 0.3	
	VBUS_DET	-0.3	4	
Storage temperature, T <sub>stg</sub>		-65	150	°C
Junction temperature		-40	105	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±7000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage range	2.7		5	V
V <sub>BUS</sub>	System V <sub>BUS</sub> voltage	4	5	28	V
VBUS_DET	VBUS_DET threshold voltage on the pin			4	V
T <sub>A</sub>	TUSB320I Operating free air temperature range	-40	25	85	°C
	TUSB320 Operating free air temperature range	0	25	70	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TUSB320	UNIT
		RWB (X2QFN)	
		12 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	169.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	68.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	83.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	83.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and C Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Power Consumption</b>						
$I_{UNATTACHED\_UFP}$	Current consumption in unattached mode when port is unconnected and waiting for connection. ( $V_{DD} = 4.5\text{ V}$ , $EN\_N = L$ , $ADDR = NC$ , $PORT = L$ )			100		$\mu\text{A}$
$I_{ACTIVE\_UFP}$	Current consumption in active mode. ( $V_{DD} = 4.5\text{ V}$ , $EN\_N = L$ , $ADDR = NC$ , $PORT = L$ )			100		$\mu\text{A}$
$I_{SHUTDOWN}$	Leakage current when $V_{DD}$ is supplied but the TUSB320 device is not enabled. ( $V_{DD} = 4.5\text{ V}$ , $EN\_N = H$ )				1.7	$\mu\text{A}$
<b>CC1 and CC2 Pins</b>						
$R_{CC\_DB}$	Pulldown resistor when in dead-battery mode.		4.1	5.1	6.1	$k\Omega$
$R_{CC\_D}$	Pulldown resistor when in UFP or DRP mode.		4.6	5.1	5.6	$k\Omega$
$V_{UFP\_CC\_USB}$	Voltage level range for detecting a DFP attach when configured as an UFP and DFP is advertising default current source capability.		0.25		0.61	V
$V_{UFP\_CC\_MED}$	Voltage level range for detecting a DFP attach when configured as an UFP and DFP is advertising medium (1.5 A) current source capability.		0.7		1.16	V
$V_{UFP\_CC\_HIGH}$	Voltage level range for detecting a DFP attach when configured as an UFP and DFP is advertising high (3 A) current source capability.		1.31		2.04	V
$V_{TH\_DFP\_CC\_USB}$	Voltage threshold for detecting an UFP attach when configured as a DFP and advertising default current source capability.		1.51	1.6	1.64	V
$V_{TH\_DFP\_CC\_MED}$	Voltage threshold for detecting an UFP attach when configured as a DFP and advertising medium current (1.5 A) source capability.		1.51	1.6	1.64	V
$V_{TH\_DFP\_CC\_HIGH}$	Voltage threshold for detecting an UFP attach when configured as a DFP and advertising high current (3.0 A) source capability.		2.46	2.6	2.74	V
$I_{CC\_DEFAULT\_P}$	Default mode pullup current source when operating in DFP or DRP mode.		64	80	96	$\mu\text{A}$
$I_{CC\_MED\_P}$	Medium (1.5 A) mode pullup current source when operating in DFP or DRP mode.		166	180	194	$\mu\text{A}$
$I_{CC\_HIGH\_P}$	High (3 A) mode pullup current source when operating in DFP or DRP mode. <sup>(1)</sup>		304	330	356	$\mu\text{A}$
<b>Control Pins: PORT, ADDR, INT/OUT3, EN_N, ID</b>						
$V_{IL}$	Low-level control signal input voltage, (PORT, ADDR, EN_N)				0.4	V
$V_{IM}$	Mid-level control signal input voltage (PORT, ADDR)		$0.28 \times V_{DD}$	$0.56 \times V_{DD}$		V
$V_{IH}$	High-level control signal input voltage (PORT, ADDR, EN_N)		$V_{DD} - 0.3$			V
$I_{IH}$	High-level input current		- 20		20	$\mu\text{A}$
$I_{IL}$	Low-level input current		- 10		10	$\mu\text{A}$
$R_{EN\_N}$	Internal pullup resistance for EN_N			1.1		$M\Omega$
$R_{pu}^{(2)}$	Internal pullup resistance (PORT, ADDR)			588		$k\Omega$
$R_{pd}^{(2)}$	Internal pulldown resistance (PORT, ADDR)			1.1		$M\Omega$
$V_{OL}$	Low-level signal output voltage (open-drain) (INT_N/OUT3, ID)	$I_{OL} = -1.6\text{ mA}$			0.4	V
$R_{p\_ODext}$	External pullup resistor on open drain IOs (INT_N/OUT3, ID)			200		$k\Omega$
$R_{p\_TLezt}$	Tri-level input external pullup resistor (PORT, ADDR)			4.7		$k\Omega$

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>I<sup>2</sup>C - SDA/OUT1, SCL/OUT2 can operate from 1.8 or 3.3 V (±10%)<sup>(3)</sup></b>						
V <sub>DD_I2C</sub>	Supply range for I <sup>2</sup> C (SDA/OUT1, SCL/OUT2)		1.65	1.8	3.6	V
V <sub>IH</sub>	High-level signal voltage		1.05			V
V <sub>IL</sub>	Low-level signal voltage				0.4	V
V <sub>OL</sub>	Low-level signal output voltage (open drain)	I <sub>OL</sub> = -1.6 mA			0.4	V
<b>VBUS_DET IO Pins (Connected to System V<sub>BUS</sub> signal)</b>						
V <sub>BUS_THR</sub>	V <sub>BUS</sub> threshold range	See 图 6-1	2.95	3.30	3.80	V
R <sub>VBUS</sub>	External resistor between V <sub>BUS</sub> and VBUS_DET pin		855	887	920	KΩ
R <sub>VBUS_PD</sub>	Internal pulldown resistance for VBUS_DET			95		KΩ

- (1) V<sub>DD</sub> must be 3.5 V or greater to advertise 3 A current.
- (2) Internal pullup and pulldown for PORT and ADDR are removed after the device has sampled EN = high or EN\_N = low.
- (3) When using 3.3 V for I<sup>2</sup>C, customer must ensure V<sub>DD</sub> is above 3.0 V at all times.

## 6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>I<sup>2</sup>C (SDA, SCL)</b>					
t <sub>SU:DAT</sub>	Data setup time	100			ns
t <sub>HD:DAT</sub>	Data hold time	10			ns
t <sub>SU:STA</sub>	Set-up time, SCL to start condition	0.6			μs
t <sub>HD:STA</sub>	Hold time, (repeated) start condition to SCL	0.6			μs
t <sub>SU:STO</sub>	Set up time for stop condition	0.6			μs
t <sub>BUF</sub>	Bus free time between a stop and start condition	1.3			μs
t <sub>VD:DAT</sub>	Data valid time			0.9	ns
t <sub>VD:ACK</sub>	Data valid acknowledge time			0.9	ns
f <sub>SCL</sub>	SCL clock frequency; I <sup>2</sup> C mode for local I <sup>2</sup> C control			400	kHz
t <sub>r</sub>	Rise time of both SDA and SCL signals			300	ns
t <sub>f</sub>	Fall time of both SDA and SCL signals			300	ns
C <sub>bus_100kHz</sub>	Total capacitive load for each bus line when operating at ≤ 100 kHz			400	pF
C <sub>bus_400kHz</sub>	Total capacitive load for each bus line when operating at ≤ 400 kHz			100	pF

## 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>CCCB_DEFAULT</sub>	Power on default of CC1 and CC2 voltage debounce time	DEBOUCE register = 2'b00		133		ms
t <sub>VBUS_DB</sub>	Debounce of VBUS_DET pin after valid V <sub>BUS_THR</sub>			2		ms
t <sub>DRP_DUTY_CYCLE</sub>	Power-on default of percentage of time DRP advertises DFP during a t <sub>DRP</sub>	DRP_DUTY_CYCLE register = 2'b00		30%		
t <sub>DRP</sub>	The period during which the TUSB320 or the TUSB320I in DFP mode completes a DFP to UFP and back advertisement.		50	75	100	ms
t <sub>I2C_EN</sub>	Time from TUSB320 EN_N low or TUSB320I EN high and V <sub>DD</sub> active to I <sup>2</sup> C access available				100	ms
t <sub>SOFT_RESET</sub>	Soft reset duration		26	49	95	ms

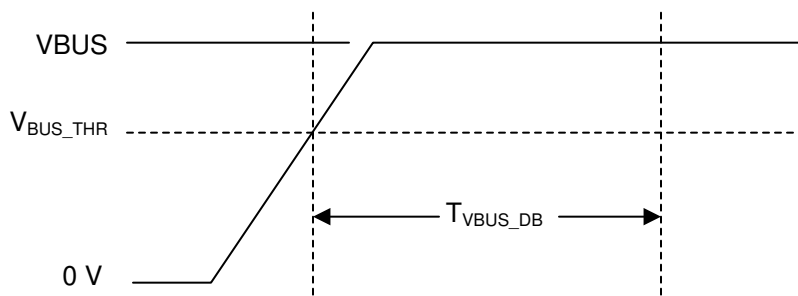


图 6-1. VBUS Detect and Debounce

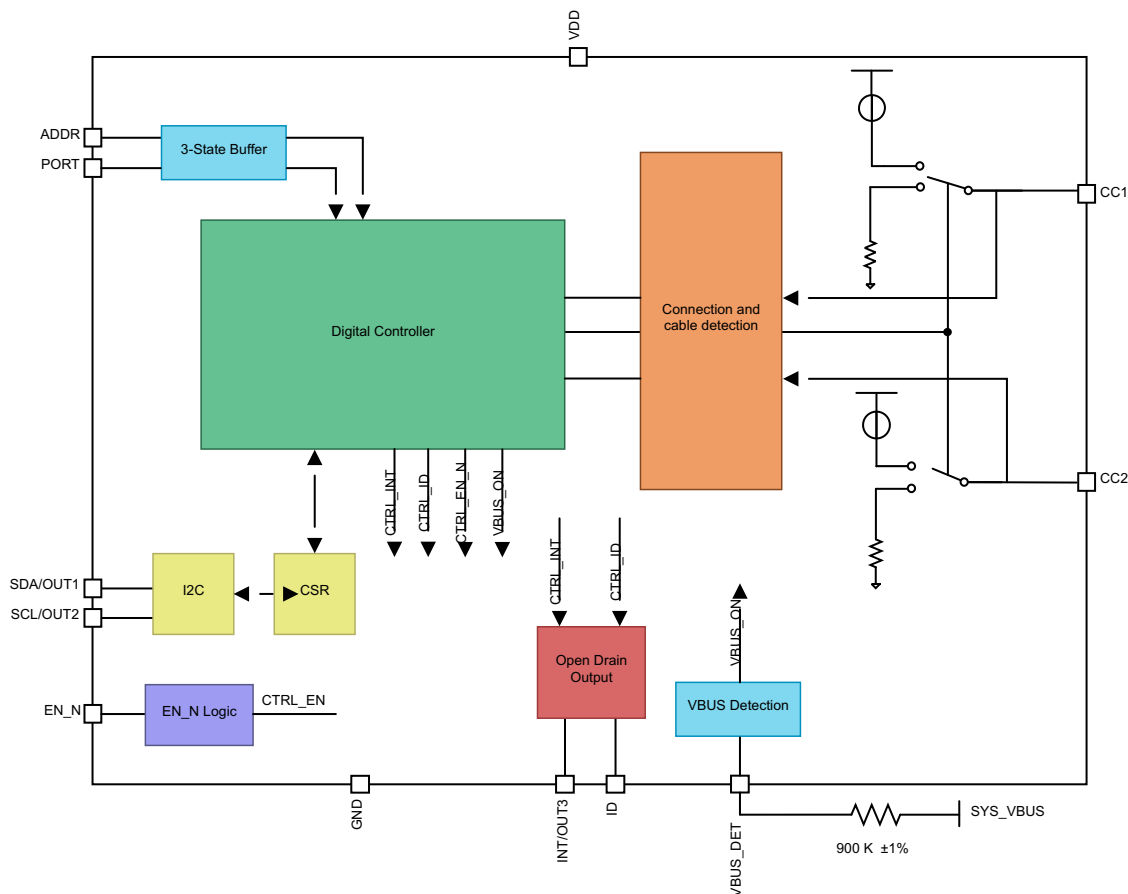


## 7 Detailed Description

### 7.1 Overview

The USB Type-C ecosystem operates around a small form factor connector and cable that is flippable and reversible. Because of the nature of the connector, a scheme is needed to determine the connector orientation. Additional schemes are needed to determine when a USB port is attached and the acting role of the USB port (DFP, UFP, and DRP), as well as to communicate Type-C current capabilities. These schemes are implemented over the CC pins according to the USB Type-C specifications. The TUSB320 device provides Configuration Channel (CC) logic for determining USB port attach and detach, role detection, cable orientation, and Type-C current mode. The TUSB320 device also contains several features such as mode configuration and low standby current which make this device ideal for source or sinks in USB 2.0 applications.

### 7.2 Functional Block Diagram



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图 7-1. Functional Block Diagram of TUSB320

#### 7.2.1 Cables, Adapters, and Direct Connect Devices

*Type-C Specification 1.1* defines several cables, plugs and receptacles to be used to attach ports. The TUSB320 device supports all cables, receptacles, and plugs. The TUSB320 device does not support e-marking.

##### 7.2.1.1 USB Type-C Receptacles and Plugs

Below is list of Type-C receptacles and plugs supported by the TUSB320 device:

- USB Type-C receptacle for USB 2.0 platforms and devices
- USB full-featured Type-C plug
- USB 2.0 Type-C plug

### 7.2.1.2 USB Type-C Cables

Below is a list of Type-C cable types supported by the TUSB320 device:

- USB full-featured Type-C cable
- USB 2.0 Type-C cable with USB 2.0 plug
- Captive cable with either a USB full-featured plug or USB 2.0 plug

### 7.2.1.3 Legacy Cables and Adapters

The TUSB320 device supports legacy cable adapters as defined by the Type-C specification. The cable adapter must correspond to the mode configuration of the TUSB320 device.

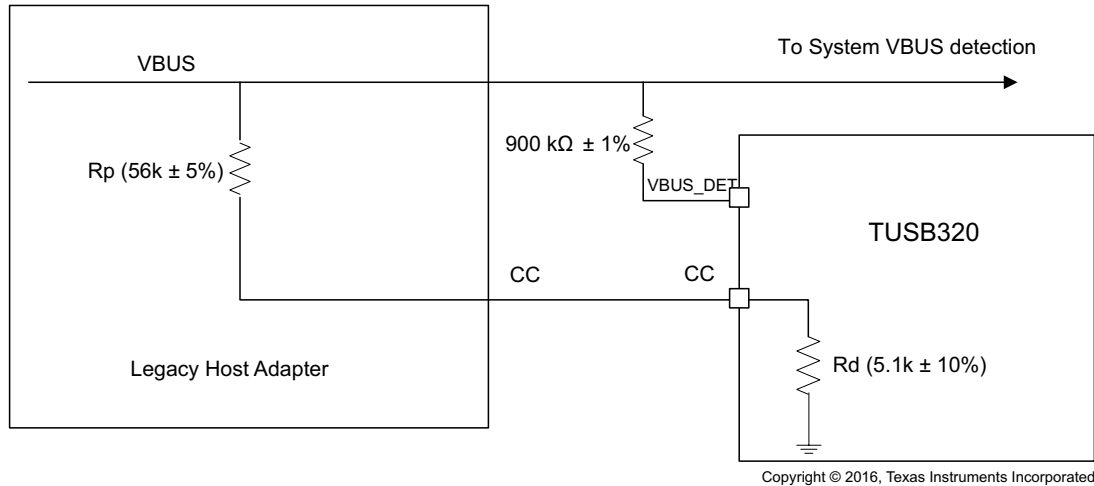


图 7-2. Legacy Adapter Implementation Circuit

### 7.2.1.4 Direct Connect Devices

The TUSB320 device supports the attaching and detaching of a direct-connect device.

### 7.2.1.5 Audio Adapters

Additionally, the TUSB320 device supports audio adapters for audio accessory mode, including:

- Passive audio adapter
- Charge through audio adapter

## 7.3 Feature Description

### 7.3.1 Port Role Configuration

The TUSB320 device can be configured as a downstream facing port (DFP), upstream facing port (UFP), or dualrole port (DRP) using the tri-level PORT pin. The PORT pin should be pulled high to  $V_{DD}$  using a pullup resistance, low to GND or left as floated on the PCB to achieve the desired mode. This flexibility allows the TUSB320 device to be used in a variety of applications. The TUSB320 device samples the PORT pin after reset and maintains the desired mode until the TUSB320 device is reset again. 表 7-1 lists the supported features in each mode.

**表 7-1. Supported Features for the TUSB320 Device by Mode**

PORT PIN	HIGH (DFP ONLY)	LOW (UFP ONLY)	NC (DRP)
SUPPORTED FEATURES			
Port attach and detach	Yes	Yes	Yes
Cable orientation (through I <sup>2</sup> C)	Yes	Yes	Yes
Current advertisement	Yes	—	Yes (DFP)
Current detection	—	Yes	Yes (UFP)
Accessory modes (audio and debug)	Yes	—	Yes
Active cable detection	Yes	—	Yes (DFP)
I <sup>2</sup> C / GPIO	Yes	Yes	Yes
Legacy cables	Yes	Yes	Yes
V <sub>BUS</sub> detection	—	Yes	Yes (UFP)

### 7.3.1.1 Downstream Facing Port (DFP) - Source

The TUSB320 device can be configured as a DFP only by pulling the PORT pin high through a resistance to V<sub>DD</sub>. In DFP mode, the TUSB320 device constantly presents R<sub>ps</sub> on both CC. In DFP mode, the TUSB320 device initially advertises default USB Type-C current. The Type-C current can be adjusted through I<sup>2</sup>C if the system needs to increase the amount advertised. The TUSB320 device adjusts the R<sub>ps</sub> to match the desired Type-C current advertisement. In GPIO mode, the TUSB320 device only advertises default Type-C current.

When configured as a DFP, the TUSB320 can operate with older USB Type-C 1.0 devices except for a USB Type-C 1.0 DRP device. The TUSB320 can not operate with a USB Type-C 1.0 DRP device. This limitation is a result of a backwards compatibility problem between USB Type-C 1.1 DFP and a USB Type-C 1.0 DRP.

### 7.3.1.2 Upstream Facing Port (UFP) - Sink

The TUSB320 device can be configured as an UFP only by pulling the PORT pin low to GND. In UFP mode, the TUSB320 device constantly presents pulldown resistors (R<sub>d</sub>) on both CC pins. The TUSB320 device monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The TUSB320 device debounces the CC pins and wait for V<sub>BUS</sub> detection before successfully attaching. As an UFP, the TUSB320 device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs (if in GPIO mode) or through the I<sup>2</sup>C CURRENT\_MODE\_DETECT register one time in the Attached.SNK state.

After initial connection, the advertised current by the connected DFP could change due to changes in its system power resource. For example, a DFP could advertise high current on initial connection but then decide to reduce to default current because user removed external power adapter from their notebook. Because the TUSB320 will only advertise on OUT1 and OUT2 the initial advertised current, it is recommend to monitor the advertised current through the TUSB320's I<sup>2</sup>C interface from the CURRENT\_MODE\_DETECT register. System software must periodically perform a I2C\_SOFT\_RESET in order for the CURRENT\_MODE\_DETECT register to be updated based on the state of the CC pins.

### 7.3.1.3 Dual Role Port (DRP)

The TUSB320 device can be configured to operate as a DRP when the PORT pin is left floated on the PCB. In DRP mode, the TUSB320 device toggles between operating as a DFP and an UFP. When functioning as a DFP in DRP mode, the TUSB320 device complies with all operations as defined for a DFP according to the Type-C specification. When presenting as an UFP in DRP mode, the TUSB320 device operates as defined for an UFP according to the Type-C specification.

### 7.3.2 Type-C Current Mode

When a valid cable detection and attach have been completed, the DFP has the option to advertise the level of Type-C current an UFP can sink. The default current advertisement for the TUSB320 device is 500 mA (for USB 2.0) or 900 mA (for USB 3.1). If a higher level of current is available, the I<sup>2</sup>C registers can be written to provide medium current at 1.5 A or high current at 3 A. When the CURRENT\_MODE\_ADVERTISE register has been written to advertise higher than default current, the DFP adjusts the Rps for the specified current level. If a DFP advertises 3 A, it ensures that the V<sub>DD</sub> of the TUSB320 device is 3.5 V or greater. 表 7-2 lists the Type-C current advertisements in GPIO and I<sup>2</sup>C modes.

**表 7-2. Type-C Current Advertisement for GPIO and I<sup>2</sup>C Modes**

TYPE-C CURRENT		GPIO MODE (ADDR PIN IN NC)		I <sup>2</sup> C MODE (ADDR PIN H, L)	
		UFP (PORT PIN L)	DFP (PORT PIN H)	UFP	DFP
Default	500 mA (USB 2.0) 900 mA (USB 3.1)	Current mode detected and output through OUT1 / OUT2	Only advertisement	Current mode detected and read through I <sup>2</sup> C register	I <sup>2</sup> C register default is 500 or 900 mA
Medium - 1.5 A			N/A		Advertisement selected through writing I <sup>2</sup> C register
High - 3 A					

### 7.3.3 Accessory Support

The TUSB320 device supports audio and debug accessories in DFP mode and DRP mode. Audio and debug accessory support is provided through reading of I<sup>2</sup>C registers. Audio accessory is also supported through GPIO mode with INT\_N/OUT3 pin (audio accessory is detected when INT\_N/OUT3 pin is low).

#### 7.3.3.1 Audio Accessory

Audio accessory mode is supported through two types of adapters. First, the passive audio adapter can be used to convert the Type-C connector into an audio port. To effectively detect the passive audio adapter, the TUSB320 device must detect a resistance < R<sub>a</sub> on both of the CC pins.

Secondly, a charge through audio adapter may be used. The primary difference between a passive and charge through adapter is that the charge through adapter supplies 500 mA of current over V<sub>BUS</sub>. The charge through adapter contains a receptacle and a plug. The plug acts as a DFP and supply V<sub>BUS</sub> when the plug detects a connection.

When the TUSB320 device is configured in GPIO mode, OUT3 pin determines if an audio accessory is connected. When an audio accessory is detected, the OUT3 pin is pulled low.

#### 7.3.3.2 Debug Accessory

Debug is an additional state supported by USB Type-C. The specification does not define a specific user scenario for this state, but it is important because the end user could use debug accessory mode to enter a test state for production specific to the application. Charge through debug accessory is not supported by TUSB320 when in DRP or UFP mode.

### 7.3.4 I<sup>2</sup>C and GPIO Control

The TUSB320 device can be configured for I<sup>2</sup>C communication or GPIO outputs using the ADDR pin. The ADDR pin is a tri-level control pin. When the ADDR pin is left floating (NC), the TUSB320 device is in GPIO output mode. When the ADDR pin is pulled high or pulled low, the TUSB320 device is in I<sup>2</sup>C mode.

All outputs for the TUSB320 device are open drain configuration.

The OUT1 and OUT2 pins are used to output the Type-C current mode when in GPIO mode. Additionally, the OUT3 pin is used to communicate the audio accessory mode in GPIO mode. 表 7-3 lists the output pin settings. See the [Pin Functions](#) table for more information.

**表 7-3. Simplified Operation for OUT1 and OUT2**

OUT1	OUT2	ADVERTISEMENT
H	H	Default Current in Unattached State
H	L	Default Current in Attached State
L	H	Medium Current (1.5 A) in Attached State
L	L	High Current (3.0 A) in Attached State

When operating in I<sup>2</sup>C mode, the TUSB320 device uses the SCL and SDA lines for clock and data and the INT\_N pin to communicate a change in I<sup>2</sup>C registers, or an interrupt, to the system. The INT\_N pin is pulled low when the TUSB320 device updates the registers with new information. The INT\_N pin is open drain. The INTERRUPT\_STATUS register should be set when the INT\_N pin is pulled low. To clear the INTERRUPT\_STATUS register, the end user writes to I<sup>2</sup>C.

When operating in GPIO mode, the OUT3 pin is used in place of the INT\_N pin to determine if an audio accessory is detected and attached. The OUT3 pin is pulled low when an audio accessory is detected.

**备注**

When using the 3.3 V supply for I<sup>2</sup>C, the end user must ensure that the V<sub>DD</sub> is 3 V and above. Otherwise the I<sup>2</sup>C may back power the device.

### 7.3.5 V<sub>BUS</sub> Detection

The TUSB320 device supports V<sub>BUS</sub> detection according to the Type-C specification. V<sub>BUS</sub> detection is used to determine the attachment and detachment of an UFP and to determine the entering and exiting of accessory modes. V<sub>BUS</sub> detection is also used to successfully resolve the role in DRP mode.

The system V<sub>BUS</sub> voltage must be routed through a 900-k $\Omega$  resistor to the VBUS\_DET pin on the TUSB320 device if the PORT pin is configured as a DRP or an UFP. If the TUSB320 device is configured as a DFP and only ever used in DFP mode, the VBUS\_DET pin can be left unconnected.

## 7.4 Device Functional Modes

The TUSB320 device has four functional modes. 表 7-4 lists these modes:

**表 7-4. USB Type-C States According to TUSB320 Functional Modes**

MODES	GENERAL BEHAVIOR	PORT PIN	STATES <sup>(1)</sup>
Unattached	USB port unattached. ID, PORT operational. I <sup>2</sup> C on. CC pins configure according to PORT pin.	UFP	Unattached.SNK
			AttachWait.SNK
		DRP	Toggle Unattached.SNK → Unattached.SRC
			AttachedWait.SRC or AttachedWait.SNK
		DFP	Unattached.SRC
			AttachWait.SRC
Active	USB port attached. All GPIOs operational. I <sup>2</sup> C on.	UFP	Attached.SNK
			Attached.SNK
		DRP	Attached.SRC
			Audio accessory
			Debug accessory
			Attached.SRC
		DFP	Audio accessory
			Debug accessory
			Attached.SRC
Dead battery	No operation. V <sub>DD</sub> not available.	UFP/DRP/DFP	Default device state to UFP/SNK with Rd.

**表 7-4. USB Type-C States According to TUSB320 Functional Modes (continued)**

MODES	GENERAL BEHAVIOR	PORT PIN	STATES <sup>(1)</sup>
Shutdown	V <sub>DD</sub> available. EN_N pin high.	UFP/DRP/DFP	Default device state to UFP/SNK with Rd.

(1) Required; not in sequential order.

#### 7.4.1 Unattached Mode

Unattached mode is the primary mode of operation for the TUSB320 device, because a USB port can be unattached for a lengthy period of time. In unattached mode, V<sub>DD</sub> is available, and all IOs and I<sup>2</sup>C are operational. After the TUSB320 device is powered up, the part enters unattached mode until a successful attach has been determined. Initially, right after power up, the TUSB320 device comes up as an Unattached.SNK. The TUSB320 device checks the PORT pin and operates according to the mode configuration. The TUSB320 device toggles between the UFP and the DFP if configured as a DRP. In unattached mode, I<sup>2</sup>C can be used to change the mode configuration or port role if the board configuration of the PORT pin is not the desired mode. Writing to the I<sup>2</sup>C MODE\_SELECT register can override the PORT pin only in unattached mode. The PORT pin is only sampled at reset or power up. I<sup>2</sup>C must be used after reset to change the device mode configuration.

#### 7.4.2 Active Mode

Active mode is defined as the port being attached. In active mode, all GPIOs are operational, and I<sup>2</sup>C is read / write (R/W). When in active mode, the TUSB320 device communicates to the AP that the USB port is attached. This happens through the ID pin if TUSB320 is configured as a DFP or DRP connect as source. If TUSB320 is configured as an UFP or a DRP connected as a sink, the OUT1/OUT2 and INT\_N/OUT3 pins are used. The TUSB320 device exits active mode under the following conditions:

- Cable unplug
- V<sub>BUS</sub> removal if attached as an UFP
- Dead battery; system battery or supply is removed
- EN\_N pin floated or pulled high

During active mode, I<sup>2</sup>C cannot be used to change the mode configuration. This can only be done if TUSB320 is in an unattached state.

#### 7.4.3 Dead Battery Mode

During dead battery mode, V<sub>DD</sub> is not available. CC pins always default to pulldown resistors in dead battery mode. Dead battery mode means:

- TUSB320 in UFP with 5.1-k $\Omega$   $\pm$  20% Rd; cable connected and providing charge
- TUSB320 in UFP with 5.1-k $\Omega$   $\pm$  20% Rd; nothing connected (application could be off or have a discharged battery)

Upon exiting dead battery mode (V<sub>DD</sub> is active), the software must perform the following sequence in order for Rp to be presented on both CC pins:

1. Write a 0x04 to I<sup>2</sup>C address 0x45.
2. Wait 30ms.
3. Write a 0x00 to I<sup>2</sup>C address 0x45.

Between steps 1 and 3, the status flags will be set. The software must ignore these flags when performing the three steps.

#### 备注

When V<sub>DD</sub> is off, the TUSB320 non-failsafe pins (VBUS\_DET, ADDR, PORT, ID, OUT[3:1] pins) could back-drive the TUSB320 device if not handled properly. When necessary to pull these pins up, it is recommended to pullup PORT, ADDR, INT\_N/OUT3, and ID to the device's V<sub>DD</sub> supply. The VBUS\_DET must be pulled up to V<sub>BUS</sub> through a 900-k $\Omega$  resistor.

#### 7.4.4 Shutdown Mode

Shutdown mode for TUSB320 device is defined as follows:

- Supply voltage available and EN\_N pin is pulled high.
- EN\_N pin has internal pullup resistor.
- The TUSB320 device is off, but still maintains the Rd on the CC pins.

#### 7.5 Programming

For further programmability, the TUSB320 device can be controlled using I<sup>2</sup>C. The TUSB320 device local I<sup>2</sup>C interface is available for reading/writing after T<sub>I2C\_EN</sub> when the device is powered up. The SCL and SDA terminals are used for I<sup>2</sup>C clock and I<sup>2</sup>C data respectively. If I<sup>2</sup>C is the preferred method of control, the ADDR pin must be set accordingly.

**表 7-5. TUSB320 I<sup>2</sup>C Addresses**

TUSB320 I <sup>2</sup> C Target Address								
ADDR pin	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
H	1	1	0	0	0	0	1	0/1
L	1	1	0	0	0	0	0	0/1

The following procedure should be followed to write to TUSB320 I<sup>2</sup>C registers:

1. The controller initiates a write operation by generating a start condition (S), followed by the TUSB320 7-bit address and a zero-value R/W bit to indicate a write cycle
2. The TUSB320 device acknowledges the address cycle
3. The controller presents the sub-address (I<sup>2</sup>C register within the TUSB320 device) to be written, consisting of one byte of data, MSB-first
4. The TUSB320 device acknowledges the sub-address cycle
5. The controller presents the first byte of data to be written to the I<sup>2</sup>C register
6. The TUSB320 device acknowledges the byte transfer
7. The controller may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB320 device
8. The controller terminates the write operation by generating a stop condition (P)

The following procedure should be followed to read the TUSB320 I<sup>2</sup>C registers:

1. The controller initiates a read operation by generating a start condition (S), followed by the TUSB320 7-bit address and a one-value R/W bit to indicate a read cycle
2. The TUSB320 device acknowledges the address cycle
3. The TUSB320 device transmits the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the T I<sup>2</sup>C register occurred prior to the read, then the TUSB320 device starts at the sub-address specified in the write.
4. The TUSB320 device waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I<sup>2</sup>C controller acknowledges reception of each data byte transfer
5. If an ACK is received, the TUSB320 device transmits the next byte of data
6. The controller terminates the read operation by generating a stop condition (P)

The following procedure should be followed for setting a starting sub-address for I<sup>2</sup>C reads:

1. The controller initiates a write operation by generating a start condition (S), followed by the TUSB320 7-bit address and a zero-value R/W bit to indicate a read cycle
2. The TUSB320 device acknowledges the address cycle
3. The controller presents the sub-address (I<sup>2</sup>C register within the TUSB320 device) to be read, consisting of one byte of data, MSB-first
4. The TUSB320 device acknowledges the sub-address cycle
5. The controller terminates the read operation by generating a stop condition (P)



## 备注

If no sub-addressing is included for the read procedure, then the reads start at register offset 00h and continue byte-by-byte through the registers until the I<sup>2</sup>C controller terminates the read operation. If a I<sup>2</sup>C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

## 7.6 Register Maps

表 7-6. CSR Registers

ACCESS TAG	NAME	MEANING
R	Read	The field may be read by software.
W	Write	The field may be written by software.
S	Set	The field may be set by a write of one. Writes of zeros to the field have no effect.
C	Clear	The field may be cleared by a write of one. Writes of zeros to the field have no effect.
U	Update	Hardware may autonomously update this field.
NA	No Access	Not accessible or not applicable.

表 7-7. CSR Registers Bit Address and Description

ADDRESS	BIT(S)	BIT NAME	DESCRIPTION	ACCESS
0x00 - 0x07	7:0	DEVICE_ID	For the TUSB320 device these fields return a string of ASCII characters returning TUSB320 Addresses 0x07 - 0x00 = {0x00 0x54 0x55 0x53 0x42 0x33 0x32 0x30}	R



**表 7-7. CSR Registers Bit Address and Description (continued)**

ADDRESS	BIT(S)	BIT NAME	DESCRIPTION	ACCESS
0x08	7:6	CURRENT_MODE_ADVERTISE	These bits are programmed by the application to raise the current advertisement from default.  00 - Default (500 mA / 900 mA) initial value at startup 01 - Medium (1.5 A) 10 - High (3 A) 11 - Reserved	RW
	5:4	CURRENT_MODE_DETECT	These bits are set when an UFP determines the Type-C Current mode.  00 - Default (value at start up) 01 - Medium 10 - Charge through accessory - 500 mA 11 - High	RU
	3:1	ACCESSORY_CONNECTED	These bits are read by the application to determine if an accessory was attached.  000 - No accessory attached (default) 001 - Reserved 010 - Reserved 011 - Reserved 100 - Audio accessory 101 - Audio charged thru accessory 110 - Debug accessory 111 - Reserved	RU
	0	ACTIVE_CABLE_DETECTION	This flag indicates that an active cable has been plugged into the Type-C connector. When this field is set, an active cable is detected.	RU

表 7-7. CSR Registers Bit Address and Description (continued)

ADDRESS	BIT(S)	BIT NAME	DESCRIPTION	ACCESS
0x09	7:6	ATTACHED_STATE	<p>This is an additional method to communicate attach other than the ID pin. These bits can be read by the application to determine what was attached.</p> <p>00 - Not attached (default)</p> <p>01 - Attached.SRC (DFP)</p> <p>10 - Attached.SNK (UFP)</p> <p>11 - Attached to an accessory</p>	RU
	5	CABLE_DIR	<p>Cable orientation. The application can read these bits for cable orientation information.</p> <p>0 - CC1</p> <p>1 - CC2 (default)</p>	RU
	4	INTERRUPT_STATUS	<p>The INT pin is pulled low whenever a CSR changes. When a CSR change has occurred this bit should be held at 1 until the application clears it.</p> <p>0 - Clear</p> <p>1 - Interrupt (When INT_N is pulled low, this bit will be 1. This bit is 1 whenever any CSR are changed)</p> <p>Note: SW must make sure the INTERRUPT_STATUS has been cleared to zero. Rewrites to this register are needed for the INT_N to be correctly asserted for all interrupt events.</p>	RCU
	3		Reserved	R
	2:1	DRP_DUTY_CYCLE	<p>Percentage of time that a DRP advertises DFP during tDRP</p> <p>00 - 30% (default)</p> <p>01 - 40%</p> <p>10 - 50%</p> <p>11 - 60%</p>	RW
	0		Reserved	R

**表 7-7. CSR Registers Bit Address and Description (continued)**

ADDRESS	BIT(S)	BIT NAME	DESCRIPTION	ACCESS
0x0A	7:6	DEBOUNCE	The nominal amount of time the TUSB320 device debounces the voltages on the CC pins.  00 - 133 ms (default) 01 - 116 ms 10 - 151 ms 11 - 168 ms	RW
	5:4	MODE_SELECT	This register can be written to set the TUSB320 device mode operation. The ADDR pin must be set to I <sup>2</sup> C mode. If the default is maintained, the TUSB320 device operates according to the PORT pin levels and modes. The MODE_SELECT can only be changed when in the unattached state.  00 - Maintain mode according to PORT pin selection (default) 01 - UFP mode (unattached.SNK) 10 - DFP mode (unattached.SRC) 11 - DRP mode (start from unattached.SNK)	RW
	3	I <sup>2</sup> C_SOFT_RESET	This resets the digital logic. The bit is self-clearing. A write of 1 starts the reset. The following registers maybe affected after setting this bit:  CURRENT_MODE_DETECT ACTIVE_CABLE_DETECTION ACCESSORY_CONNECTED ATTACHED_STATE CABLE_DIR	RSU
	2:1		Reserved	R
	0		Reserved	R
0x45	7:3		Reserved	R
	2	DISABLE_RD_RP	When this field is set, Rd and Rp are disabled.  0 - Normal operation (default) 1 - Disable Rd and Rp	RW
	1:0		Reserved. For TI internal use only. Do not change default value.	RW

## 8 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TUSB320 device is a Type-C configuration channel logic and port controller. The TUSB320 device can detect when a Type-C device is attached, what type of device is attached, the orientation of the cable, and power capabilities (both detection and broadcast). The TUSB320 device can be used in a source application (DFP) or in a sink application (UFP).

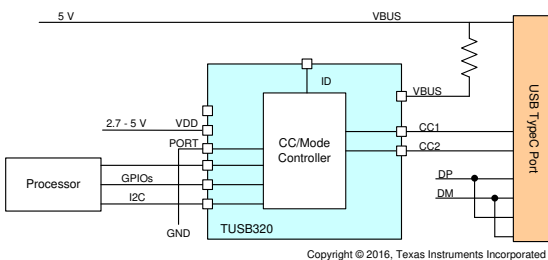


图 8-1. TUSB320 in UFP Mode Supporting Default Implementation

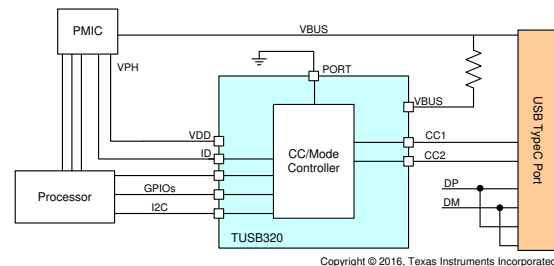


图 8-2. TUSB320 in UFP Mode Supporting Advanced Power Delivery

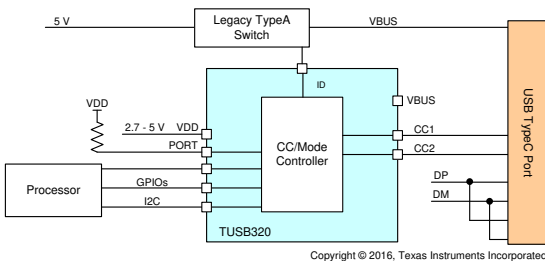


图 8-3. TUSB320 in DFP Mode Supporting Default Implementation

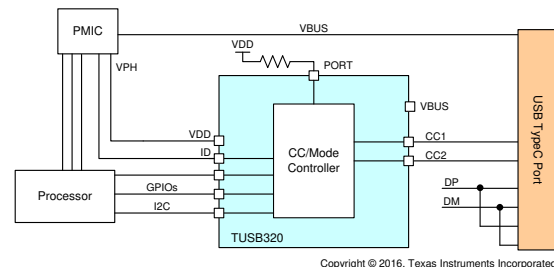


图 8-4. TUSB320 in DFP Mode Supporting Advanced Power Delivery

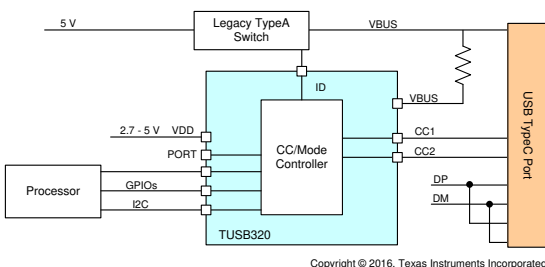


图 8-5. TUSB320 in DRP Mode Supporting Default Implementation

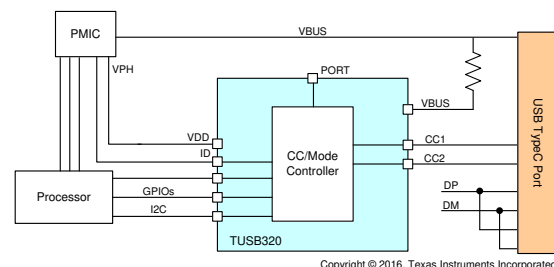


图 8-6. TUSB320 in DRP Mode Supporting Advanced Power Delivery

## 8.2 Typical Application

### 8.2.1 DRP in I<sup>2</sup>C Mode

图 8-7 shows the TUSB320 device configured as a DRP in I<sup>2</sup>C mode.

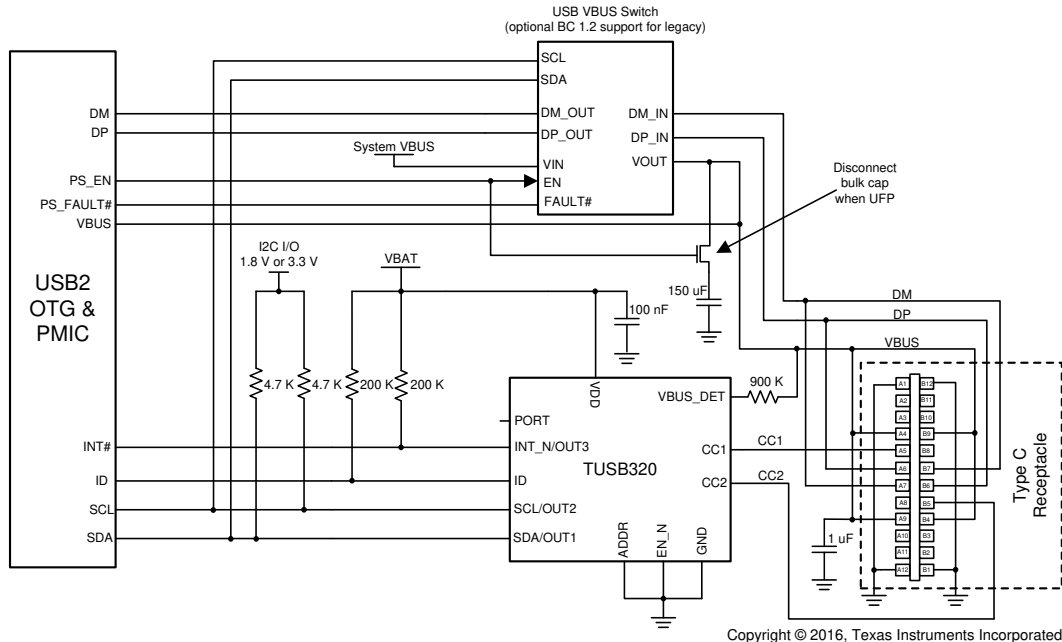


图 8-7. DRP in I<sup>2</sup>C Mode Schematic

#### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 8-1:

表 8-1. Design Requirements for DRP in I<sup>2</sup>C Mode

DESIGN PARAMETER	VALUE
V <sub>DD</sub> (2.75 V to 5 V)	VBAT (less than 5 V)
Mode (I <sup>2</sup> C or GPIO)	I <sup>2</sup> C ADDR pin must be pulled down or pulled up
I <sup>2</sup> C address (0x61 or 0x60)	0x60 ADDR pin must be pulled low or tied to GND
Type-C port type (UFP, DFP, or DRP)	DRP PORT pin is NC
Shutdown support (EN_N control)	No

#### 8.2.1.2 Detailed Design Procedure

The TUSB320 device supports a V<sub>DD</sub> in the range of 2.75 V to 5 V. In this particular use case, VBAT which must be in the required V<sub>DD</sub> range is connected to the V<sub>DD</sub> pin. A 100-nF capacitor is placed near V<sub>DD</sub>.

The TUSB320 device is placed into I<sup>2</sup>C mode by either pulling the ADDR pin high or low. In this case, the ADDR pin is tied to GND which results in a I<sup>2</sup>C address of 0x60. The SDA and SCL must be pulled up to either 1.8 V or 3.3 V. When pulled up to 3.3 V, the V<sub>DD</sub> supply must be at least 3 V to keep from back-driving the I<sup>2</sup>C interface.

The TUSB320 device can enter shutdown mode by pulling the EN\_N pin high, which puts the TUSB320 device into a low power state. In this case, external control of the EN\_N pin is not implemented and therefore the EN\_N pin is tied to GND.

The INT\_N/OUT3 pin is used to notify the PMIC when a change in the TUSB320 I<sup>2</sup>C registers occurs. This pin is an open drain output and requires an external pullup resistor. The pin should be pulled up to V<sub>DD</sub> using a 200-k $\Omega$  resistor.

The ID pin is used to indicate when a connection has occurred if the TUSB320 device is a DFP while configured for DRP. An OTG USB controller can use this pin to determine when to operate as a USB host or USB device. When this pin is driven low, the OTG USB controller functions as a host and then enables V<sub>BUS</sub>. The Type-C standard requires that a DFP should not enable V<sub>BUS</sub> until it is in the Attached.SRC state. If the ID pin is not low but V<sub>BUS</sub> is detected, then OTG USB controller functions as a device. The ID pin is open drain output and requires an external pullup resistor. It should be pulled up to V<sub>DD</sub> using a 200-k $\Omega$  resistor.

The Type-C port mode is determined by the state of the PORT pin. When the PORT pin is not connected, the TUSB320 device is in DRP mode. The Type-C port mode can also be controlled by the MODE\_SELECT register through the I<sup>2</sup>C interface when the TUSB320 device is in the unattached state.

The VBUS\_DET pin must be connected through a 900-k $\Omega$  resistor to V<sub>BUS</sub> on the Type-C that is connected. This large resistor is required to protect the TUSB320 device from large V<sub>BUS</sub> voltage that is possible in present day systems. This resistor along with internal pulldown keeps the voltage observed by the TUSB320 device in the recommended range.

The USB2 specification requires the bulk capacitance on V<sub>BUS</sub> based on UFP or DFP. When operating the TUSB320 device in a DRP mode, it alternates between UFP and DFP. If the TUSB320 device connects as an UFP, the large bulk capacitance must be removed. The FET in 图 8-7 performs this task.

表 8-2. USB2 Bulk Capacitance Requirements

PORT CONFIGURATION	MIN	MAX	UNIT
Downstream facing port (DFP)	120		$\mu$ F
Upstream facing port (UFP)	1	10	$\mu$ F

### 8.2.1.3 Application Curves

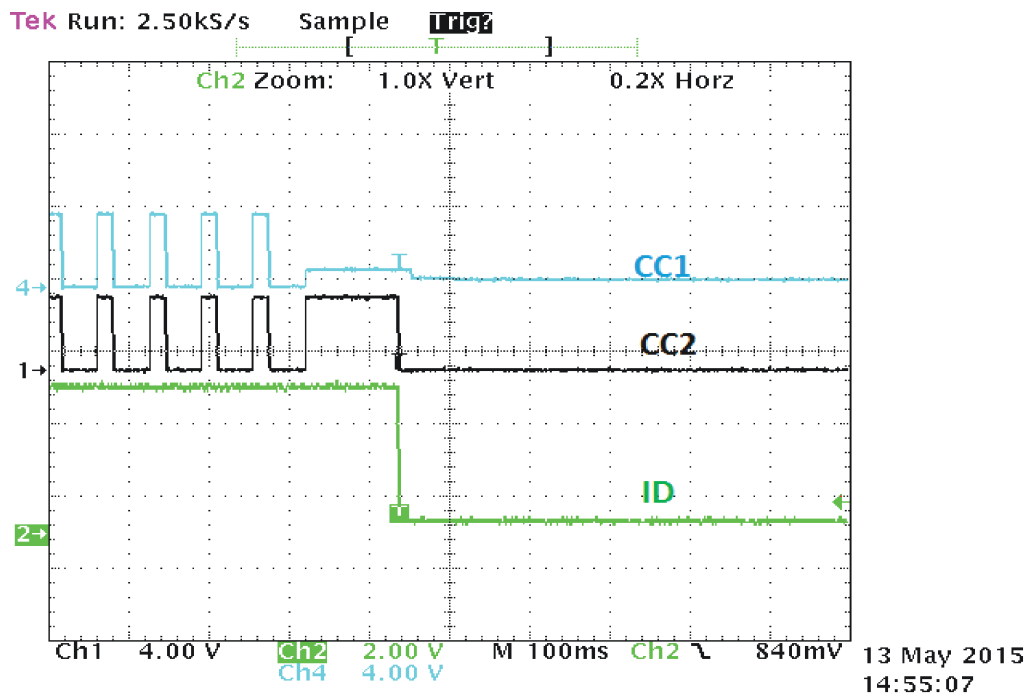
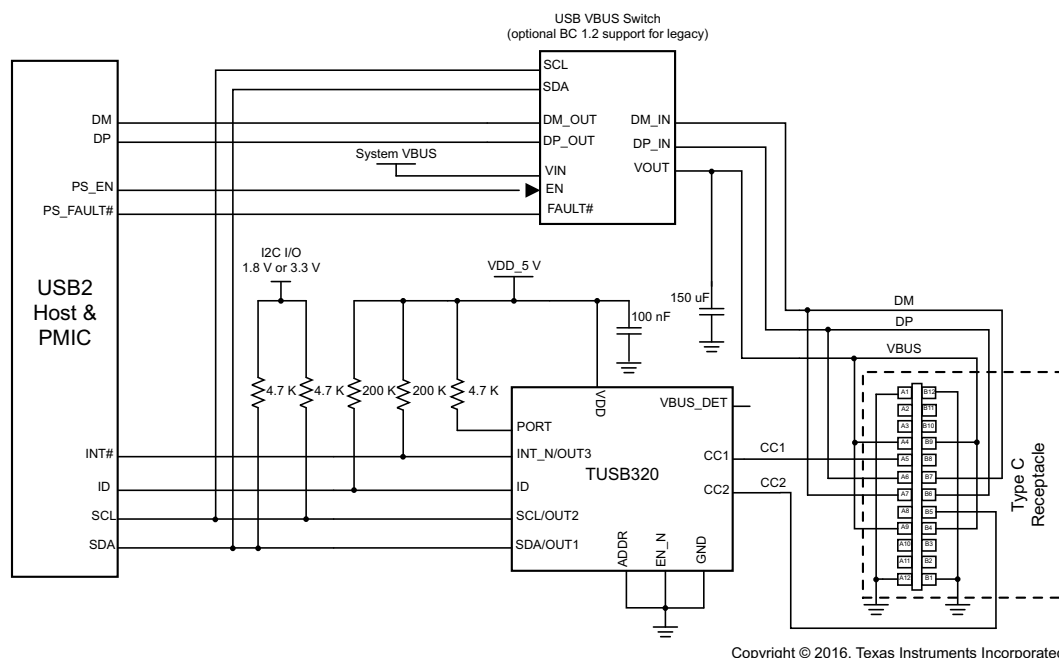


图 8-8. Application Curve for DRP in I<sup>2</sup>C Mode

### 8.2.2 DFP in I<sup>2</sup>C Mode

图 8-9 shows the TUSB320 device configured as a DFP in I<sup>2</sup>C mode.



**图 8-9. DFP in I<sup>2</sup>C Mode Schematic**

#### 8.2.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-3:

### 表 8-3. Design Requirements for DFP in I<sup>2</sup>C Mode

DESIGN PARAMETER	VALUE
V <sub>DD</sub> (2.75 V to 5 V)	5 V
Mode (I <sup>2</sup> C or GPIO)	I <sup>2</sup> C ADDR pin must be pulled down or pulled up
I <sup>2</sup> C address (0x61 or 0x60)	0x60 ADDR pin must be pulled low or tied to GND
Type-C port type (UFP, DFP, or DRP)	DFP PORT pin is pulled up
Shutdown support (EN_N Control)	No

#### 8.2.2.2 Detailed Design Procedure

The TUSB320 device supports a  $V_{DD}$  in the range of 2.75 V to 5 V. In this particular case,  $V_{DD}$  is set to 5 V. A 100-nF capacitor is placed near  $V_{DD}$ .

The TUSB320 device is placed into I<sup>2</sup>C mode by either pulling the ADDR pin high or low. In this particular case, the ADDR pin is tied to GND which results in an I<sup>2</sup>C address of 0x60. The SDA and SCL must be pulled up to either 1.8 V or 3.3 V. When pulled up to 3.3 V, the V<sub>DD</sub> supply must be at least 3 V to keep from back-driving the I<sup>2</sup>C interface.

The TUSB320 device can enter shutdown mode by pulling the EN\_N pin high, which puts the TUSB320 device into a low power state. In this case, external control of the EN\_N pin is not implemented and therefore the EN\_N pin is tied to GND.

The INT\_N/OUT3 pin is used to notify the PMIC when a change in the TUSB320 I<sup>2</sup>C registers occurs. This pin is an open drain output and requires an external pullup resistor. The pin should be pulled up to V<sub>DD</sub> using a 200-k $\Omega$  resistor.

The Type-C port mode is determined by the state of the PORT pin. When the PORT pin is pulled high, the TUSB320 device is in DFP mode. The Type-C port mode can also be controlled by the MODE\_SELECT register through the I<sup>2</sup>C interface when the TUSB320 device is in the unattached state.

The VBUS\_DET pin must be connected through a 900-k $\Omega$  resistor to V<sub>BUS</sub> on the Type-C that is connected. This large resistor is required to protect the TUSB320 device from the largest V<sub>BUS</sub> voltage that is possible in present day systems. This resistor along with internal pulldown keeps the voltage observed by the TUSB320 device in the recommended range.

The USB2 specification requires the bulk capacitance on V<sub>BUS</sub> based on UFP or DFP. When operating the TUSB320 device in a DFP mode, a bulk capacitance of at least 120  $\mu$ F is required. In this particular case, a 150- $\mu$ F capacitor was chosen.

### 8.2.2.3 Application Curves

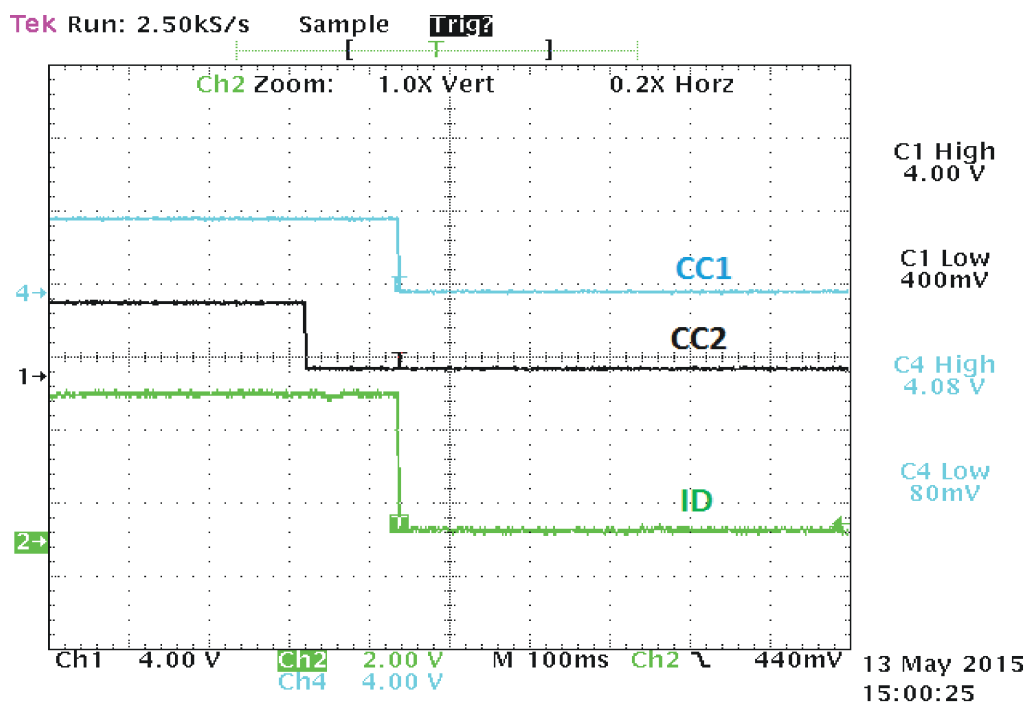


图 8-10. Application Curve for DFP in I<sup>2</sup>C Mode



### 8.2.3 UFP in I<sup>2</sup>C Mode

图 8-11 shows the TUSB320 device configured as a DFP in I<sup>2</sup>C mode.

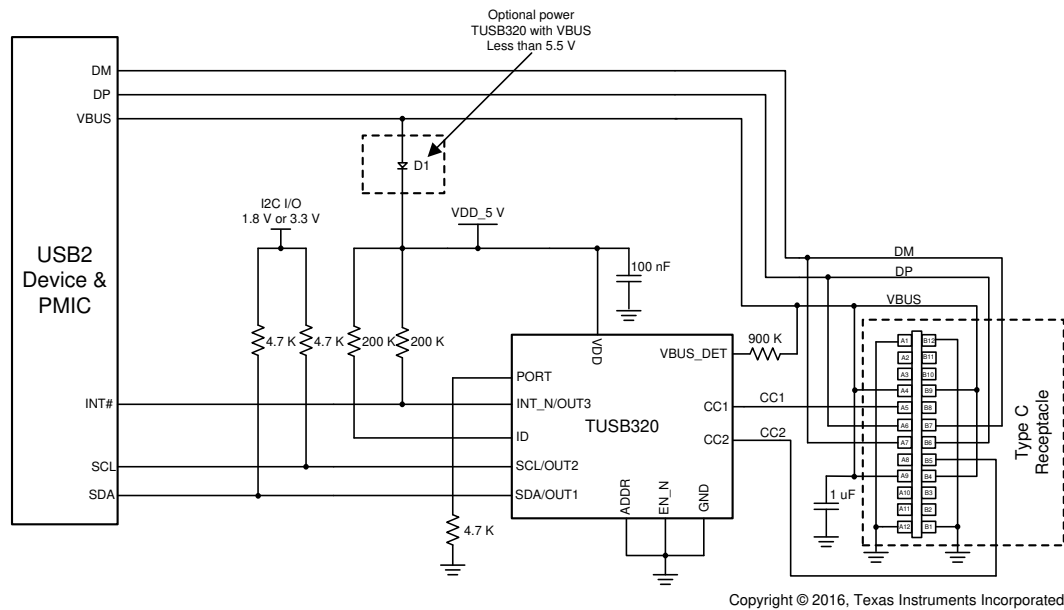


图 8-11. UFP in I<sup>2</sup>C Mode Schematic

#### 8.2.3.1 Design Requirements

For this design example, use the parameters listed in 表 8-4:

表 8-4. Design Requirements for UFP in I<sup>2</sup>C Mode

DESIGN PARAMETER	VALUE
V <sub>DD</sub> (2.75 V to 5 V)	5 V
Mode (I <sup>2</sup> C or GPIO)	I <sup>2</sup> C ADDR pin must be pulled down or pulled up
I <sup>2</sup> C address (0x61 or 0x60)	0x60 ADDR pin must be pulled low or tied to GND
Type-C port type (UFP, DFP, or DRP)	UFP PORT pin is pulled down
Shutdown support (EN_N control)	No

#### 8.2.3.2 Detailed Design Procedure

The TUSB320 device supports a V<sub>DD</sub> in the range of 2.75 V to 5 V. In this particular case, V<sub>DD</sub> is set to 5 V. A 100-nF capacitor is placed near V<sub>DD</sub>. If V<sub>BUS</sub> is guaranteed to be less than 5.5 V, powering the TUSB320 device through a diode can be implemented.

The TUSB320 device is placed into I<sup>2</sup>C mode by either pulling the ADDR pin high or low. In this case, the ADDR pin is tied to GND which results in a I<sup>2</sup>C address of 0x60. The SDA and SCL must be pulled up to either 1.8 V or 3.3 V. When pulled up to 3.3 V, the V<sub>DD</sub> supply must be at least 3 V to keep from back-driving the I<sup>2</sup>C interface.

The TUSB320 device can enter shutdown mode by pulling the EN\_N pin high, which puts the TUSB320 device into a low power state. In this case, external control of the EN\_N pin is not implemented and therefore the EN\_N pin is tied to GND.

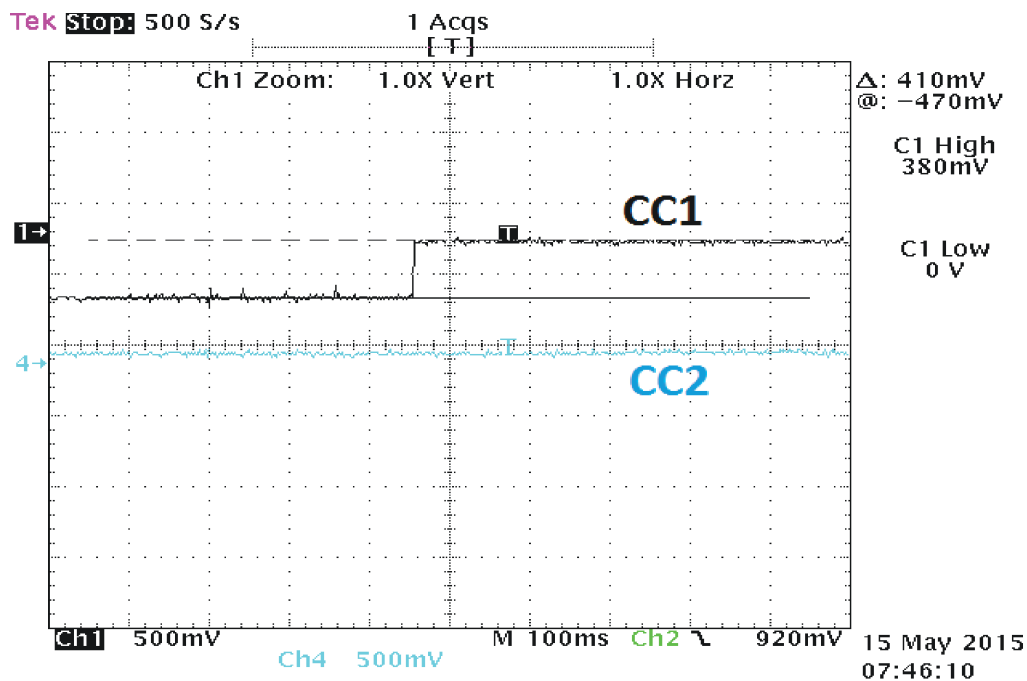
The INT\_N/OUT3 pin is used to notify the PMIC when a change in the TUSB320 I<sup>2</sup>C registers occurs. This pin is an open drain output and requires an external pullup resistor. The pin should be pulled up to V<sub>DD</sub> using a 200-k $\Omega$  resistor.

The Type-C port mode is determined by the state of the PORT pin. When the PORT pin is pulled low, the TUSB320 device is in UFP mode. The Type-C port mode can also be controlled by the MODE\_SELECT register through the I<sup>2</sup>C interface when the TUSB320 device is in the unattached state.

The VBUS\_DET pin must be connected through a 900-k $\Omega$  resistor to V<sub>BUS</sub> on the Type-C that is connected. This large resistor is required to protect the TUSB320 device from large V<sub>BUS</sub> voltage that is possible in present day systems. This resistor along with internal pulldown keeps the voltage observed by the TUSB320 device in the recommended range.

The USB2 specification requires the bulk capacitance on  $V_{BUS}$  based on UFP or DFP. When operating the TUSB320 device in an UFP mode, a bulk capacitance between 1 to 10  $\mu F$  is required. In this particular case, a 1- $\mu F$  capacitor was chosen.

### 8.2.3.3 Application Curves



**图 8-12. Application Curve for UFP in I<sup>2</sup>C Mode**

## 8.3 Initialization Set Up

The general power-up sequence for the TUSB320 device (EN\_N tied to ground) is as follows:

1. System is powered off (device has no  $V_{DD}$ ). The TUSB320 device is configured internally in UFP mode with Rds on CC pins (dead battery).
2.  $V_{DD}$  ramps - POR circuit.  $V_{DD}$  must ramp within 25 ms or less. IO pull-up power rail (for example, pull up on ID, INT, SCL, SDA, ADDR, and PORT) must ramp with  $V_{DD}$  or lag after  $V_{DD}$ .
3. I<sup>2</sup>C supply ramps up.
4. The TUSB320 device enters unattached mode and determines the voltage level from the PORT pin. This determines the mode in which the TUSB320 device operates (DFP, UFP, and DRP).
5. The TUSB320 device monitors the CC pins as a DFP and  $V_{BUS}$  for attach as an UFP.
6. The TUSB320 device enters active mode when attach has been successfully detected.

## 9 Power Supply Recommendations

The TUSB320 device has a wide power supply range from 2.7 to 5 V, and can be powered by a battery system.

## 10 Layout

### 10.1 Layout Guidelines

1. An extra trace (or stub) is created when connecting between more than two points. A trace connecting pin A6 to pin B6 will create a stub because the trace also has to go to the USB Host. Ensure that:
  - A stub created by short on pin A6 (DP) and pin B6 (DP) at Type-C receptacle does not exceed 3.5 mm.
  - A stub created by short on pin A7 (DM) and pin B7 (DM) at Type-C receptacle does not exceed 3.5 mm.
2. A 100-nF capacitor should be placed as close as possible to the TUSB320  $V_{DD}$  pin.

### 10.2 Layout Example

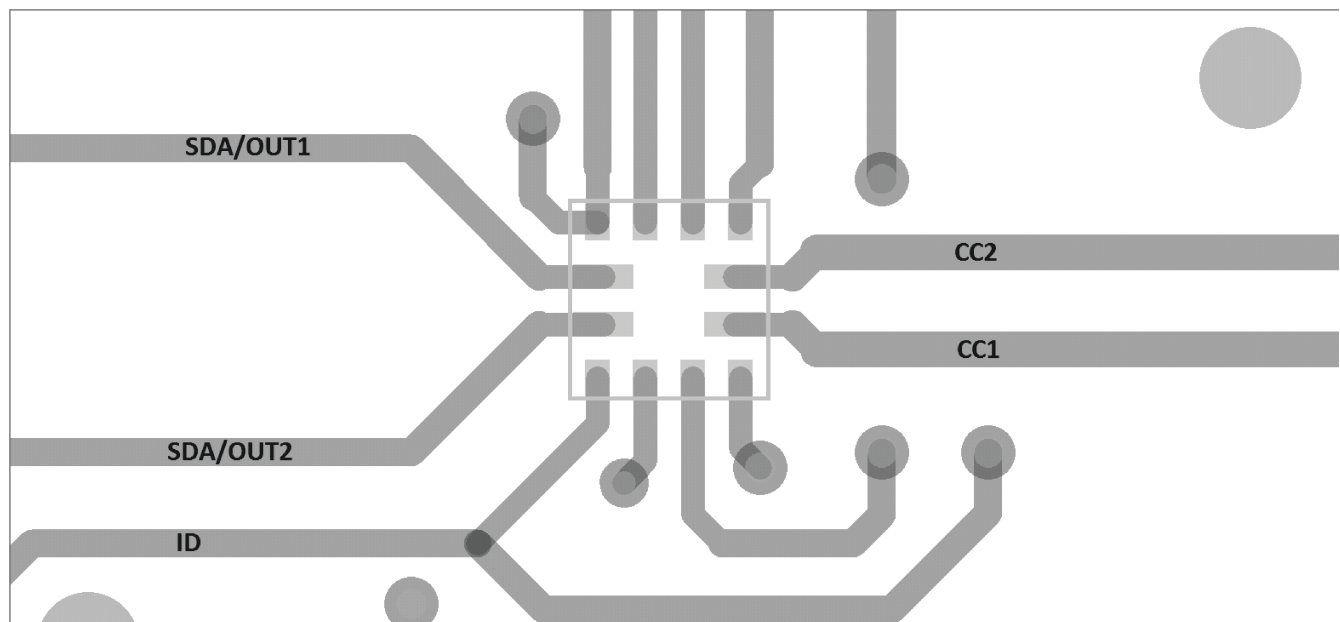


图 10-1. TUSB320 Layout

## 11 Device and Documentation Support

### 11.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.2 支持资源

**TI E2E™ 支持论坛** 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 11.3 Trademarks

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### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TUSB320IRWBR</a>	Active	Production	X2QFN (RWB)   12	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	70
TUSB320IRWBR.A	Active	Production	X2QFN (RWB)   12	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	70
TUSB320IRWBRG4	Active	Production	X2QFN (RWB)   12	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70
TUSB320IRWBRG4.A	Active	Production	X2QFN (RWB)   12	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70
<a href="#">TUSB320RWBR</a>	Active	Production	X2QFN (RWB)   12	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	20
TUSB320RWBR.A	Active	Production	X2QFN (RWB)   12	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	20

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB320IRWBR	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.48	4.0	8.0	Q2
TUSB320IRWBRG4	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.48	4.0	8.0	Q2
TUSB320RWBR	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.48	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS

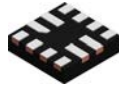


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB320IRWBR	X2QFN	RWB	12	3000	210.0	185.0	35.0
TUSB320IRWBRG4	X2QFN	RWB	12	3000	210.0	185.0	35.0
TUSB320RWBR	X2QFN	RWB	12	3000	210.0	185.0	35.0



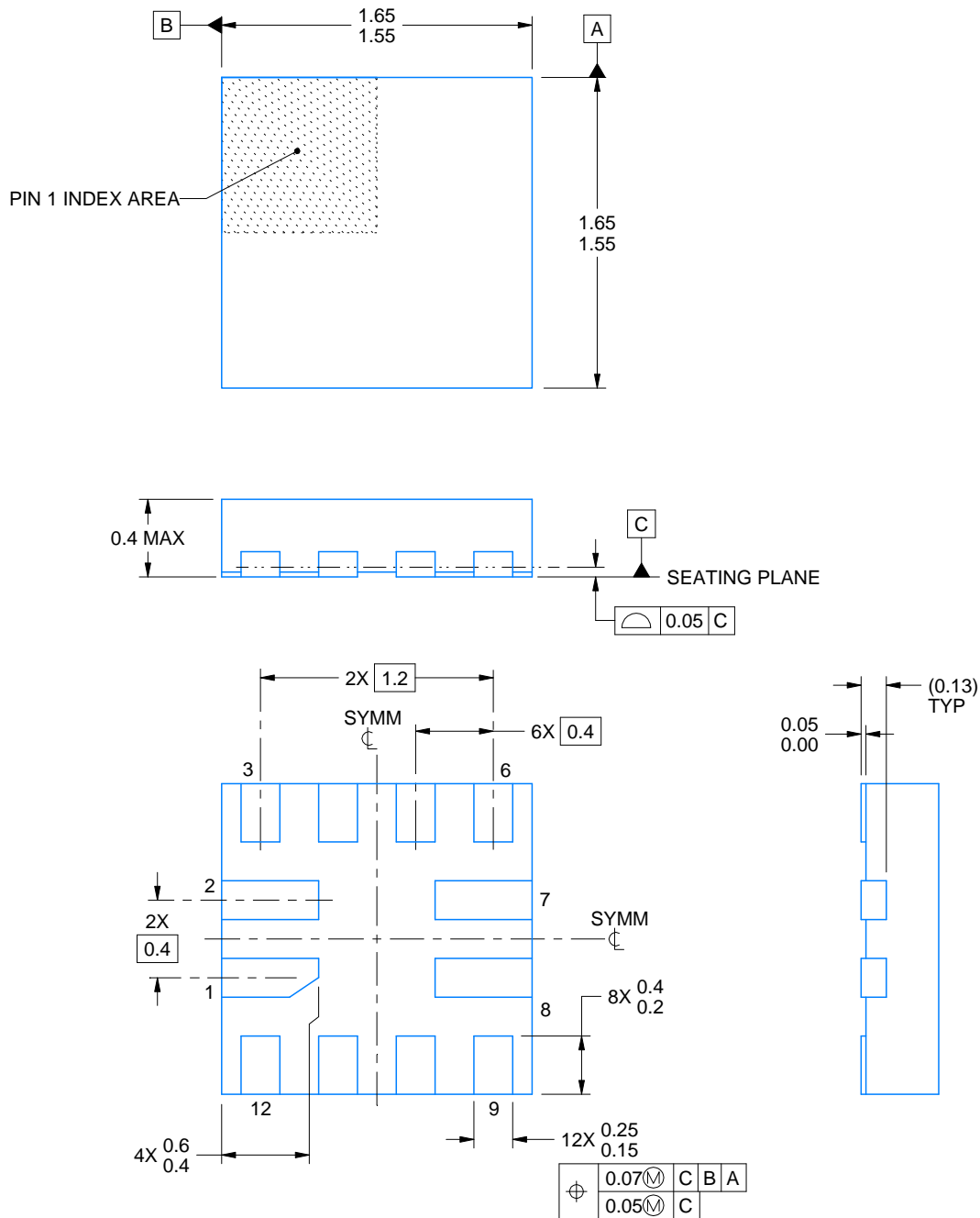
RWB0012A



## PACKAGE OUTLINE

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4221631/B 07/2017

### NOTES:

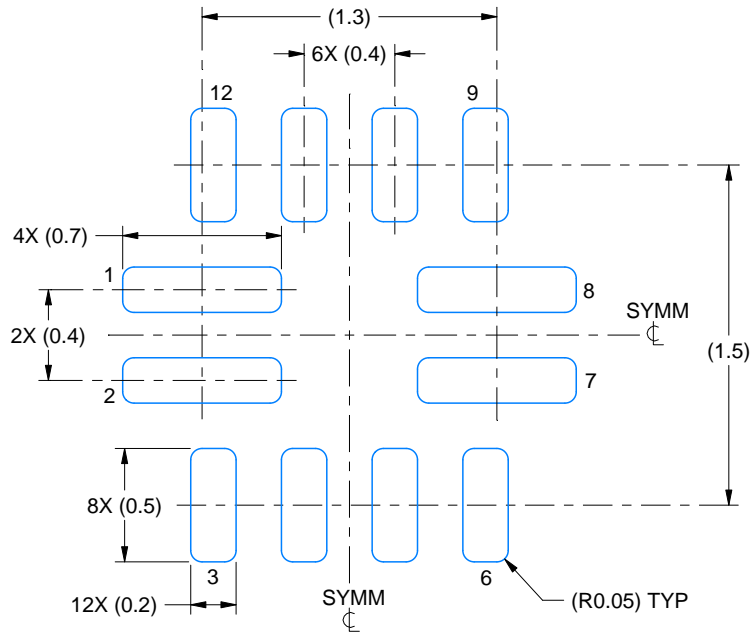
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

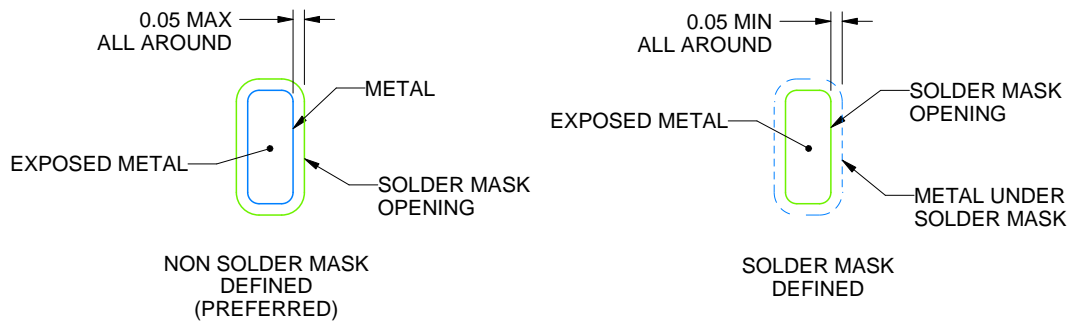
RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:30X



SOLDER MASK DETAILS

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NOTES: (continued)

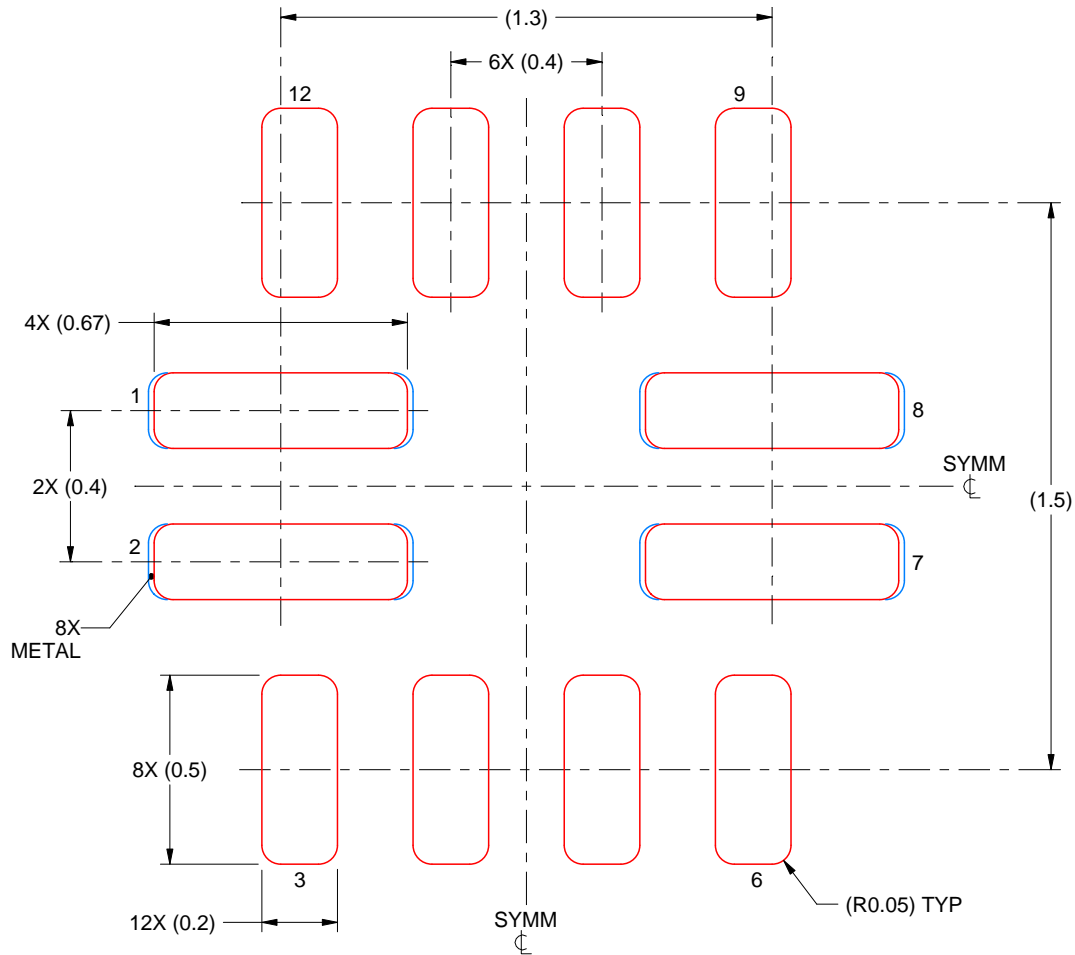
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8  
96% PRINTED SOLDER COVERAGE BY AREA  
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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