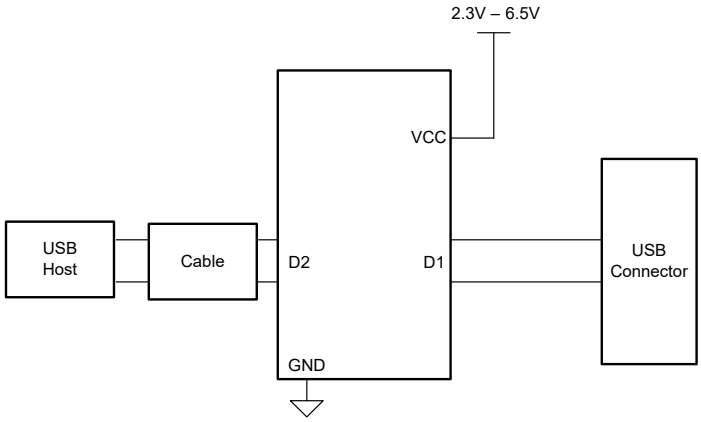
TUSB211A-Q1 汽车类 USB 2.0 480Mbps 高速信号调节器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 2：-40°C 至 105°C
- 宽电源电压范围：2.3V 至 6.5V
- 超低 USB 断开和关断功耗
- 可提供 USB 2.0 高速信号调节
- 兼容 USB 2.0、On-The-Go (OTG) 2.0 和电池充电 (BC) 1.2
- 支持低速、全速和高速信号传输
- 主机或器件无关
- 支持长达 5m 的电缆
  - 通过外部下拉电阻器值实现四种可选的信号 EQ（边沿升压与直流升压）设置
- 支持长达 10m 的电缆和两台 TUSB211A-Q1 器件
- 可扩展解决方案 – 器件可通过菊花链连接用于高损耗应用
- 与 TUSB211/212/214/216/217A 引脚兼容 (3.3V)

2 应用

- 汽车信息娱乐系统与仪表组
- 汽车音响主机
- 有源电缆、电缆扩展器和背板



简化版原理图

3 说明

TUSB211A-Q1 是第三代 USB™ 2.0 高速信号调节器，旨在补偿传输通道中的交流损失（由于容性负载）和直流损失（由于电阻损耗）。

TUSB211A-Q1 采用了专利设计，可通过边缘加速器来对 USB 2.0 高速信号的传输边缘进行加速，并通过直流升压功能来提高静态电平。

此外，TUSB211A-Q1 还具有预均衡功能，可补偿较长电缆应用中的码间串扰 (ISI) 抖动。USB 低速和全速信号特征不受 TUSB211A-Q1 的影响。

TUSB211A-Q1 可在不改变数据包计时或不增加传播延迟的情况下提高信号质量。

TUSB211A-Q1 可使用长达 5 米的线缆帮助系统通过 USB 2.0 高速近端眼图合规性测试。

TUSB211A-Q1 与 USB On-The-Go (OTG) 和电池充电 (BC) 协议兼容。

器件比较

器件型号	封装(1)	OP TEMP (T_A)°C
TUSB211A	RWB（X2QFN，12）	0 至 70
TUSB211AI		-40 至 85
TUSB211A-Q1		-40 至 105

封装信息

器件型号	封装(1)	封装尺寸(2)
TUSB211A-Q1	RWB（X2QFN，12）	1.6mm x 1.6mm

(1) 有关更多信息，请参阅 节 10。
(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。

Table of Contents

4 Pin Configuration and Functions

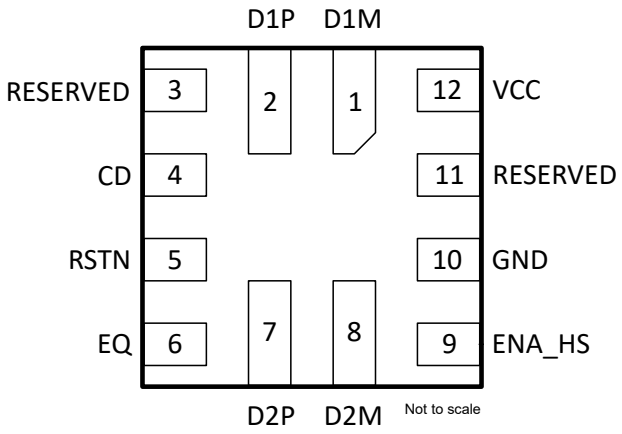


图 4-1. TUSB211A-Q1 RWB 12-Pin X2QFN (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
EQ	6	I	N/A	USB High-speed EQ select via external pull down resistor. Both edge boost and DC boost are controlled by a single pin. Sampled upon power up. Does not recognize real time adjustments. Auto selects EQ LEVEL = 3 when left floating.
RESERVED	11	I	500kΩ PU	Reserved pin for TI test purposes. Leave floating or connect external capacitor to GND for normal operation.
ENA_HS	9	I/O	N/A	After reset: Output signal ENA_HS. Flag indicating that channel is in High-speed mode. Asserted upon: 1. Detection of USB-IF High-speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18µs – 128µs].
D2P	7	I/O	N/A	USB High-speed positive port.
D2M	8	I/O	N/A	USB High-speed negative port.
GND	10	P	N/A	Ground
D1M	1	I/O	N/A	USB High-speed negative port.
D1P	2	I/O	N/A	USB High-speed positive port.
RESERVED	3	I/O	500kΩ PU 1.8 MΩ PD	Reserved pin for TI test purposes. Leave floating for normal operation.
VCC	12	P	N/A	Supply power
RSTN	5	I	500kΩ PU 1.8 MΩ PD	Device disable/enable. Low – Device is at reset and in shutdown, and High - Normal operation. Recommend 0.1µF external capacitor to GND to allow for clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.
CD	4	O	When RSTN asserted there is a 500kΩ PD	After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.

(1) I = input, O = output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range	VCC	–0.3	7	V
Voltage range USB data	DxP, DxM	–0.3	5.5	V
Voltage range on EQ pin	EQ	-0.3	1.98	V
Voltage range other pins	RSTN	-0.3	5.5	V
Storage temperature, T_{stg}		–65	150	°C
Maximum junction temperature, $T_{J\ (max)}$			125	°C

(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011(2)	±750	

(1) AEC Q100-002 HBM ESD Classification Level 2
(2) AEC Q100- 011 CDM ESD Classification Level C4A

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.3	5	6.5	V
T_A	Operating free-air temperature (AEC-Q100)	–40		105	°C
T_J	Junction temperature (AEC-Q100)			115	°C
DxP, DxM	Voltage range USB data	0		3.6	V
EQ	Voltage range EQ pin	0		1.98	V
DIGITAL	Voltage range other pins (RSTN)	0		3.6	V

5.4 Thermal Information

THERMAL METRIC (1)		RWB (X2QFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	137.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
POWER						
I_{ACTIVE_HS}	High Speed Active Current	USB channel = HS mode. 480Mbps traffic. V_{CC} supply stable, with EQ = Max		22	36	mA
I_{IDLE_HS}	High Speed Idle Current	USB channel = HS mode, no traffic. V_{CC} supply stable, EQ = Max		22	36	mA
$I_{HS\_SUSPEND}$	High Speed Suspend Current	USB channel = HS Suspend mode. V_{CC} supply stable		0.75	1.4	mA
I_{FS}	Full-Speed Current	USB channel = FS mode, 12Mbps traffic, V_{cc} supply stable		0.75	1.4	mA
$I_{DISCONN}$	Disconnect Power	Host side application. No device attachment.		0.80	1.4	mA
I_{SHUTDN}	Shutdown Power	RSTN driven low, V_{CC} supply stable		60	115	µA
CONTROL PIN LEAKAGE						
I_{LKG_FS}	Pin failsafe leakage current for RSTN	V_{CC} = 0V, pin at $V_{IH, max}$		10	15	µA
INPUT RSTN						
V_{IH}	High level input voltage		1.5		3.6	V
V_{IL}	Low-level input voltage		0		0.5	V
I_{IH}	High level input current	V_{IH} = 3.6V, R_{PU} enabled			±15	µA
I_{IL}	Low level input current	V_{IL} = 0V, R_{PU} enabled			±20	µA
INPUT EQ						
R_{EQ_LVL0}	External pulldown resistor for EQ Level 0				160	Ω
R_{EQ_LVL1}	External pulldown resistor for EQ Level 1		1.5	1.8	2	kΩ
R_{EQ_LVL2}	External pulldown resistor for EQ Level 2		3.4	3.6	3.96	kΩ
R_{EQ_LVL3}	External pulldown resistor for EQ Level 3 to remove upper limit for resistor value, can be left open		7.5			kΩ
OUTPUTS CD, ENA_HS						
V_{OH}	High level output voltage for CD and ENA_HS	I_O = –50µA, VCC >= 3.0V	2.5			V
V_{OH}	High level output voltage for CD	I_O = –25µA, VCC = 2.3V	1.7			V
V_{OH}	High level output voltage for ENA_HS	I_O = –25µA, VCC = 2.3V	1.8			V
V_{OL}	Low level output voltage for CD and ENA_HS	I_O = 50µA			0.3	V
DxP, DxM						
C_{IO_DXX}	Capacitance to GND	Measured with VNA at 240MHz, V_{CC} supply stable, Redriver off		2.5		pF

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.

5.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
DxP, DxM USB Signals						
F_{BR_DXX}	Bit Rate	USB channel = HS mode. 480Mbps traffic. V_{CC} supply stable			480	Mbps
t_{R/F_DXX}	Rise/Fall time		100			ps

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.

5.7 Timing Requirements

		MIN	NOM	MAX	UNIT
POWER UP TIMING					
T_{RSTN_PW}	Minimum width to detect a valid RSTN signal assert when the pin is actively driven low	100			µs
T_{STABLE}	VCC must be stable before RSTN de-assertion	300			µs
T_{READY}	Maximum time needed for the device to be ready after RSTN is de-asserted.			500	µs
T_{RAMP}	V_{CC} ramp time			100	ms
T_{RAMP}	V_{CC} ramp time	0.2			ms

5.8 Typical Characteristics

The typical characteristics shown in this section apply to near-end eye measurements taken at nominal conditions. The eyes are measured with various pre-channel cable lengths applied at the input or post-channel cable lengths applied at the output of the TUSB211A-Q1 as indicated.

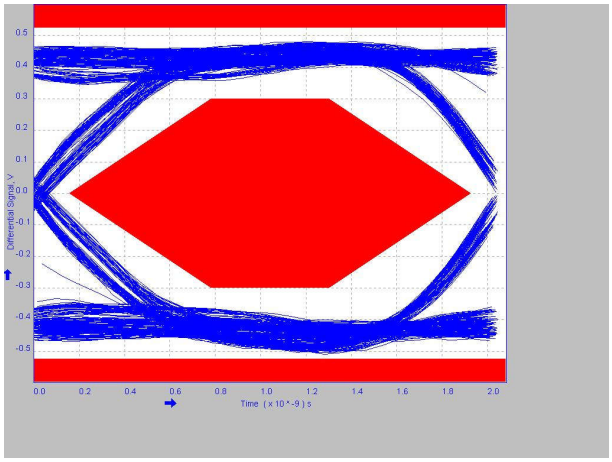


图 5-1. 2 Meter Pre-Channel With TUSB211A-Q1 EQ=1

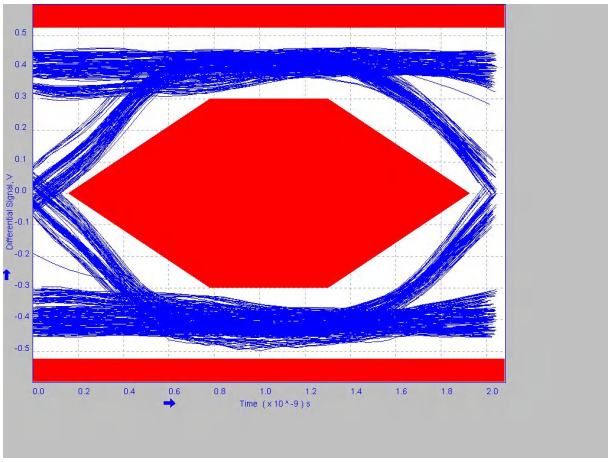


图 5-2. 5 Meter Pre-Channel With TUSB211A-Q1 EQ=2

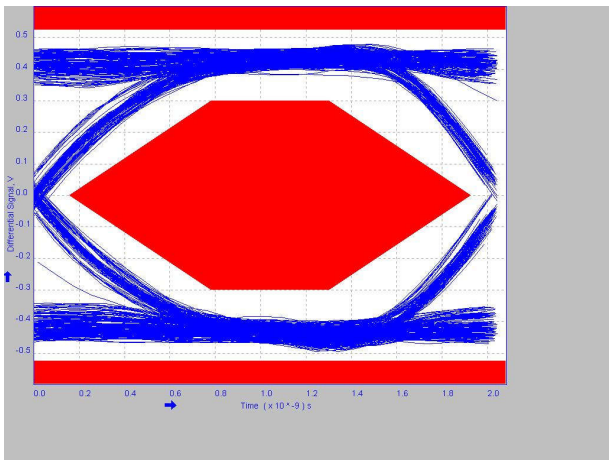


图 5-3. 2 Meter Post-Channel With TUSB211A-Q1 EQ=1

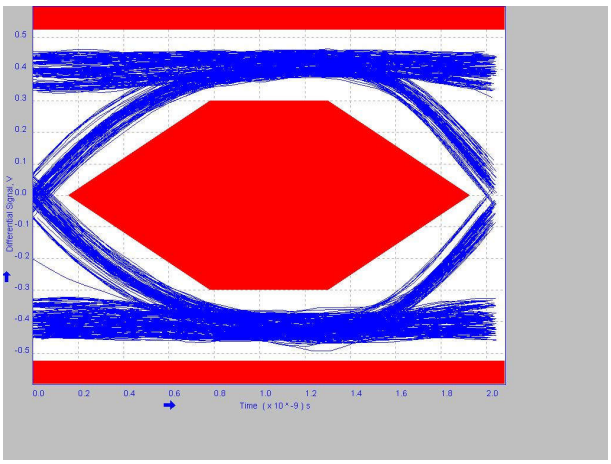


图 5-4. 4 Meter Post-Channel With TUSB211A-Q1 EQ=2

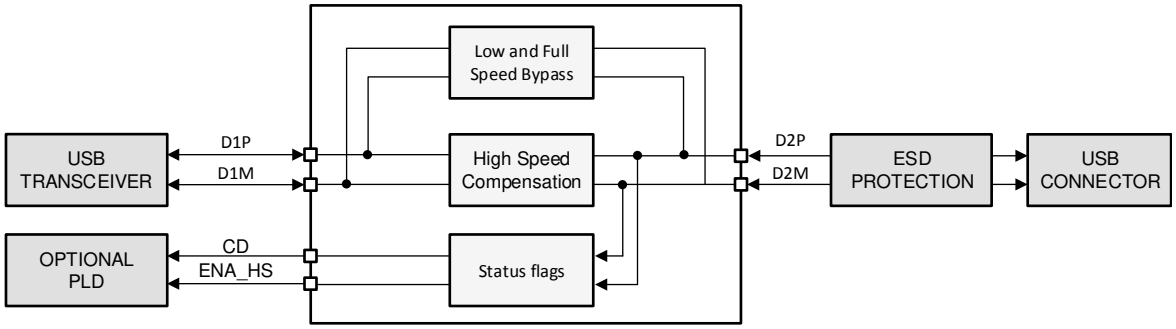
6 Detailed Description

6.1 Overview

The TUSB211A-Q1 is a USB High-Speed (HS) signal conditioner designed to compensate for ISI signal loss in a transmission channel. TUSB211A-Q1 has a patented design for USB Low Speed (LS) and Full Speed (FS) signals. It does not alter the signal characteristics. HS signals are compensated. The design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals. This helps pass USB HS electrical compliance tests at the connector. The TUSB211A-Q1 allows application in series to cover longer distances, or high loss transmission paths. A maximum of 4 devices can be daisy-chained.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 High-Speed EQ

The high-speed EQ (combination of edge boost and DC boost) improves the eye width for USB2.0 high-speed signals. It is direction independent, which makes it compatible to OTG systems. The EQ pin is configuring the EQ strength with different values of pull down resistors to set 4 levels of EQ.

6.4 Device Functional Modes

6.4.1 Low-Speed (LS) Mode

TUSB211A-Q1 automatically detects an LS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low.

6.4.2 Full-Speed (FS) Mode

TUSB211A-Q1 automatically detects an FS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low.

6.4.3 High-Speed (HS) Mode

TUSB211A-Q1 automatically detects an HS connection and will enable signal compensation as determined by the external pull down resistance on its EQ pin.

CD pin and ENA_HS pin are asserted high when high-speed EQ is active.

6.4.4 High-Speed Downstream Port Electrical Compliance Test Mode

TUSB211A-Q1 will detect an HS compliance test fixture and enter the downstream port high-speed eye diagram test mode. CD pin will be low and ENA_HS pin is asserted high when TUSB211A-Q1 is in HS eye compliance test mode.

If the RSTN pin is asserted low and de-asserted high while TUSB211A-Q1 is operating in HS functional mode, then TUSB211A-Q1 will transition to HS eye compliance test mode, the CD asserts low, and ENA_HS remains high. When all this occurs, signal compensation is enabled.

6.4.5 Shutdown Mode

TUSB211A-Q1 can be disabled when its RSTN pin is asserted low. DP, DM traces are continuous through the device in shutdown mode. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin as to the status of the channel.

表 6-1. CD and ENA_HS Pins in Different Modes

MODE	CD	ENA_HS
Low-speed	HIGH	LOW
Full-speed	HIGH	LOW
High-speed	HIGH	HIGH
High-speed downstream port electrical test	LOW	HIGH
Shutdown	LOW	LOW

7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The purpose of the TUSB211A-Q1 is to restore the signal integrity of a USB High-speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB211A-Q1 can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB211A-Q1 to control other blocks on the customer platform, if so desired.

7.2 Typical Application

A typical application for TUSB211A-Q1 is shown in 图 7-1. In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. The orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].

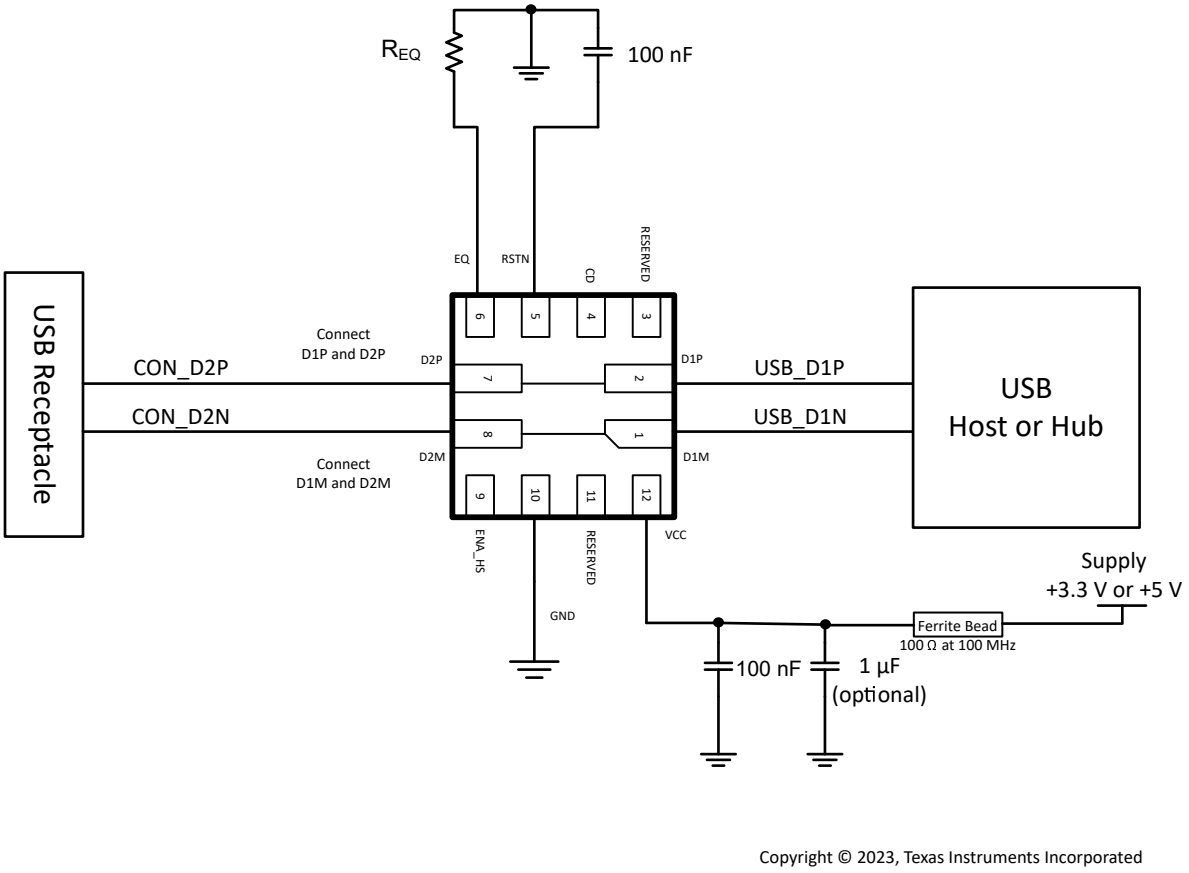


图 7-1. TUSB211A-Q1 Reference Schematic

7.2.1 Design Requirements

TUSB211A-Q1 requires a valid reset signal as described in the *Power Supply Recommendations* section. The capacitor at RSTN pin is not required if a micro controller drives the RSTN pin according to recommendations.

For this design example, use the parameters provided in 表 7-1.

表 7-1. Design Parameters for 3.3V Supply With Low to Medium Loss System

PARAMETER			VALUE(1)
V_{CC}			3.3V ±10%
I^2C support required in system (Yes/No)			No
Edge and DC Boost	R_{EQ}	EQ Level	EQ Level 0: R_{EQ} = 0Ω
	0Ω	0	
	1.8kΩ ±1%	1	
	3.6kΩ ±1%	2	
	Do Not Install (DNI)	3	

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 3.3V supply system and could be applicable to 5V supply system as well.

7.2.2 Detailed Design Procedure

The best EQ setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with EQ Level 0, and then increment to EQ Level 1, and so on.

For the TUSB211A-Q1 to recognize any change to the EQ setting, the RSTN pin must be toggled. This is because the EQ pin is latched on power up and the pin is ignored thereafter.

Placement of the device is also dependent on the application goal. 表 7-2 provides TI recommendations.

表 7-2. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED TUSB211A-Q1 PLACEMENT
Pass USB Near End Mask at the receptacle	Close to measurement point (connector)
Pass USB Far End Eye Mask at the plug	Close to USB PHY
Cascade multiple TUSB211A-Q1s to improve device enumeration	Midway between each USB interconnect

表 7-3. Table of Recommended Settings

EQ settings(1) for channel loss	
Pre-channel cable length (Between USB PHY and TUSB211A-Q1)	**EQ**
0-3 meter	Level 0
2-5 meter	Level 1
Post-channel cable length (Between TUSB211A-Q1 and inter-connect)	**EQ**
0-2 meter	Level 0
1-4 meter	Level 1

(1) These parameters are starting values for different cable lengths. Further tuning might be required based on specific host or device as well as cable length and loss profile.

7.2.2.1 Test Procedure to Construct USB High-Speed Eye Diagram

备注

USB-IF certification tests for High-speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the *Electrical Specifications* section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High-speed Eye Mask:

7.2.2.1.1 For a Host Side Application

1. Configure the TUSB211A-Q1 to the desired EQ setting.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB211A-Q1.
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB211A-Q1.
4. Enable the host to transmit USB TEST_PACKET.
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps to re-test TUSB211A-Q1 with a different EQ setting (must reset to change).

7.2.2.1.2 For a Device Side Application

1. Configure the TUSB211A-Q1 to the desired EQ setting.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB211A-Q1.
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB211A-Q1. Ensure that the USB-IF device test fixture is configured to the ‘INIT’ position.
4. Allow the host to enumerate the device.
5. Enable the device to transmit USB TEST_PACKET.
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the ‘TEST’ position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps to re-test TUSB211A-Q1 with a different EQ setting (must reset to change).

7.2.3 Application Curves

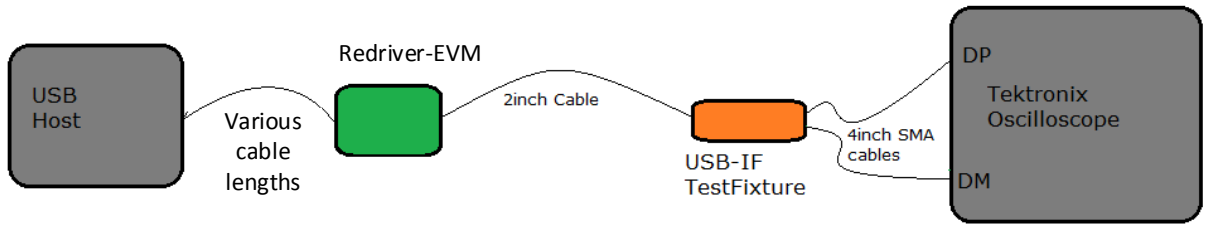


图 7-2. Near End Eye Measurement Set-Up With Pre-Channel Cable

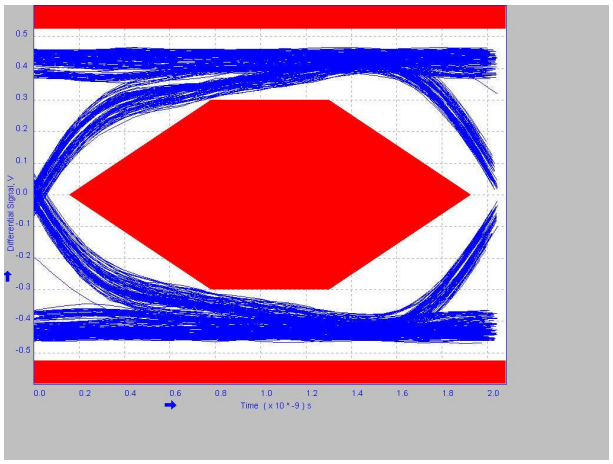


图 7-3. 2 Meter Pre-Channel Without TUSB211A-Q1

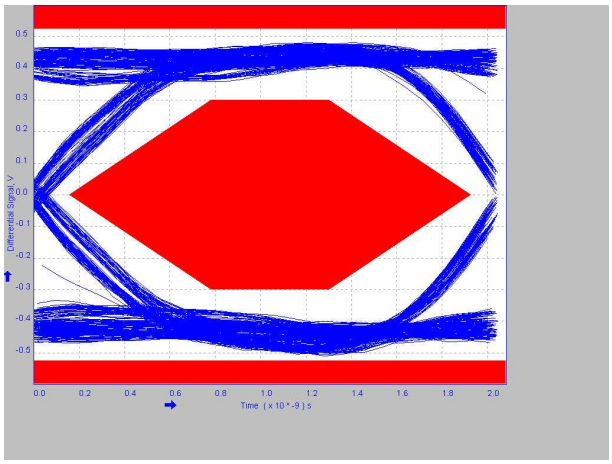


图 7-4. 2 Meter Pre-Channel With TUSB211A-Q1 EQ=1

7.2.3 Application Curves (continued)

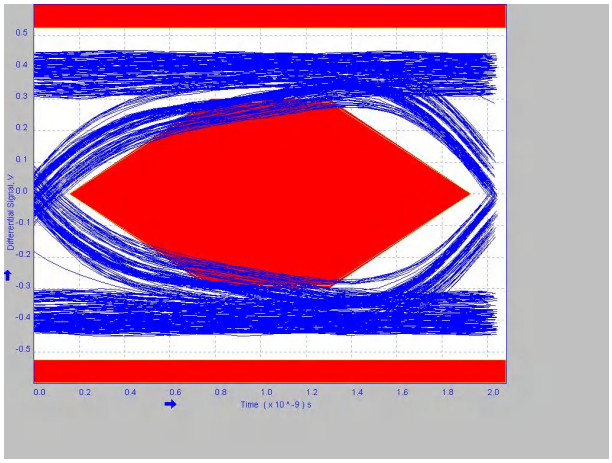


图 7-5. 5 Meter Without TUSB211A-Q1

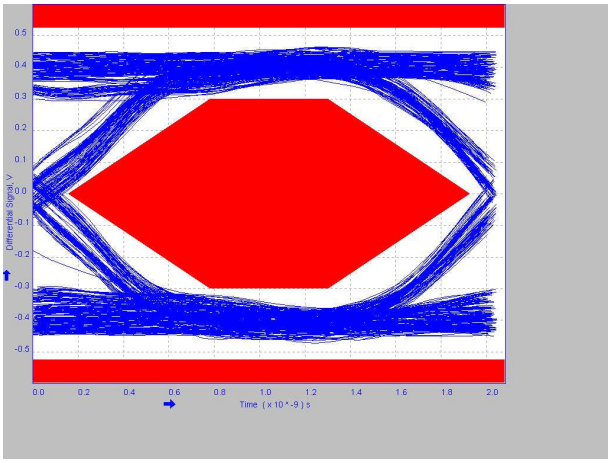


图 7-6. 5 Meter Pre-Channel With TUSB211A-Q1 EQ=1

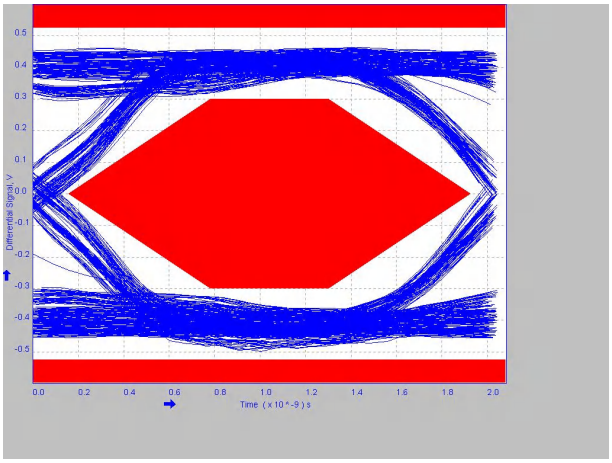


图 7-7. 5 Meter Pre-Channel With TUSB211A-Q1 EQ=2

7.2.3 Application Curves (continued)

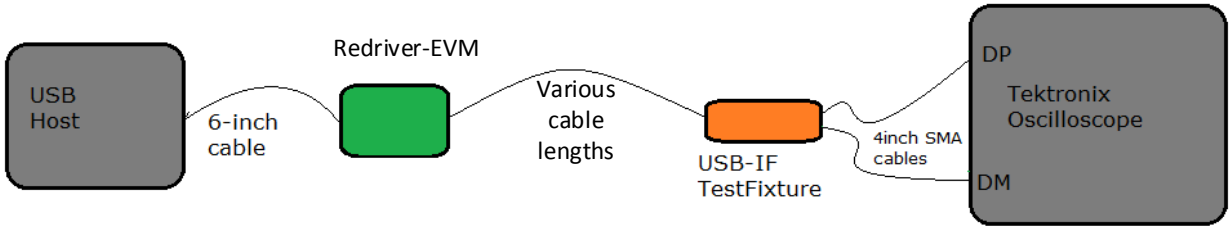


图 7-8. Near End Eye Measurement Set-Up With Post-Channel Cable

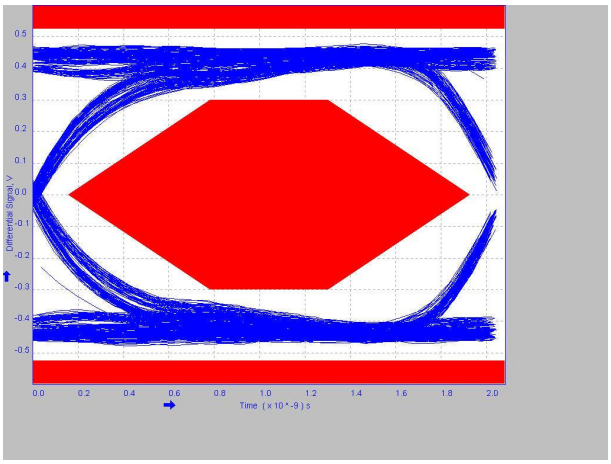


图 7-9. 1 Meter Post-Channel Without TUSB211A-Q1

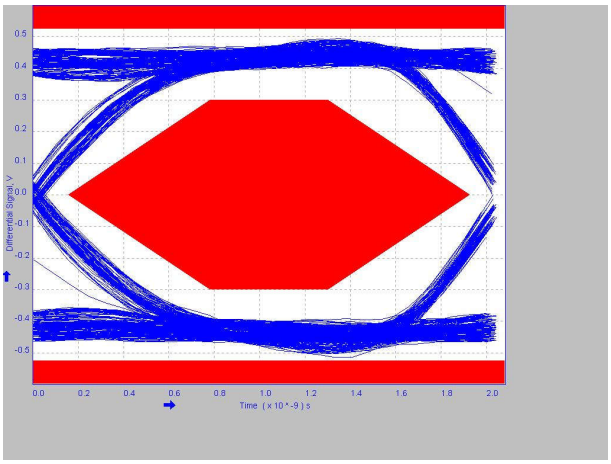


图 7-10. 1 Meter Post-Channel With TUSB211A-Q1 EQ=0

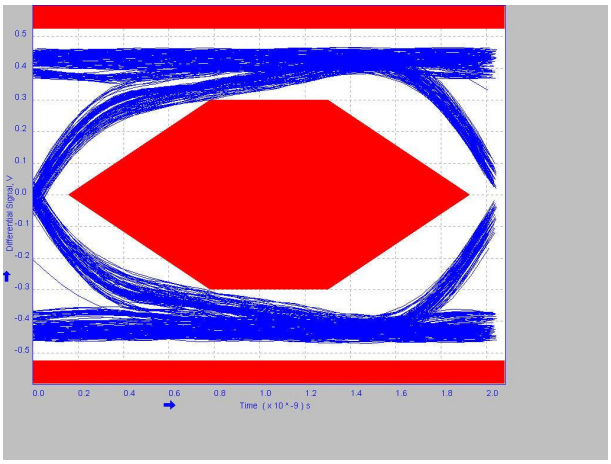


图 7-11. 2 Meter Post-Channel Without TUSB211A-Q1

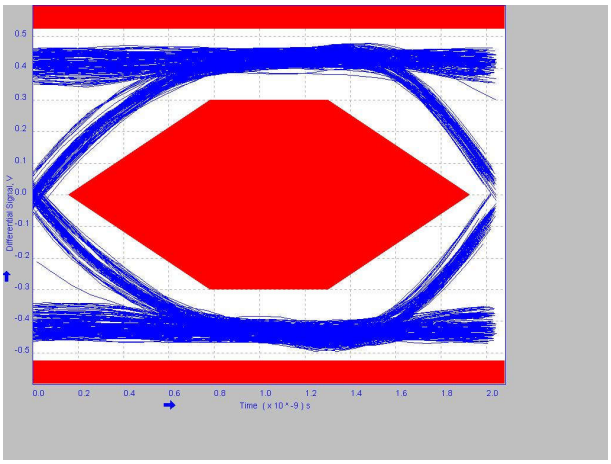


图 7-12. 2 Meter Post-Channel With TUSB211A-Q1 EQ=1

7.2.3 Application Curves (continued)

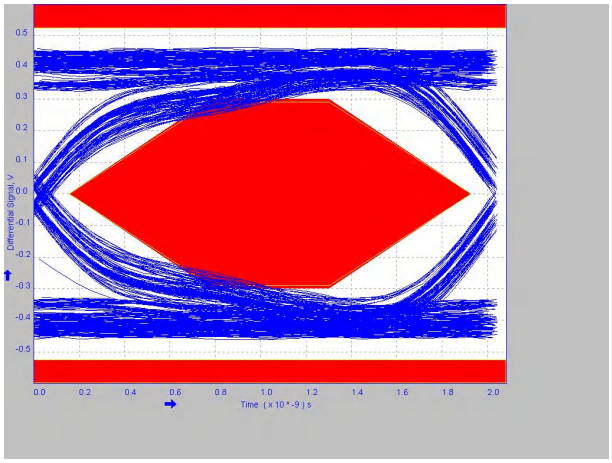


图 7-13. 4 Meter Post-Channel Without TUSB211A-Q1

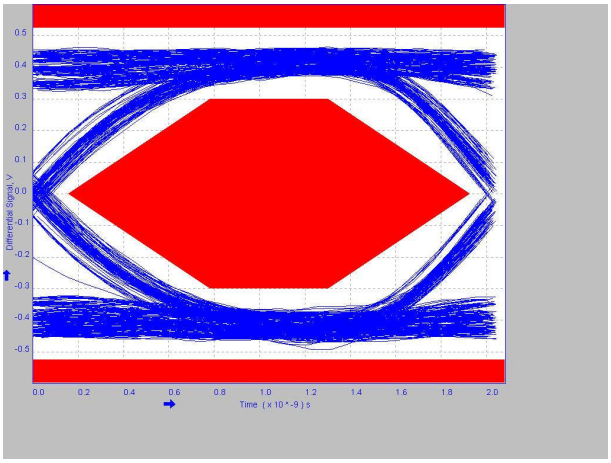


图 7-14. 4 Meter Post-Channel With TUSB211A-Q1 EQ=2

7.3 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to the minimum recommended supply voltage or higher for a correct power on reset of the digital circuitry. If RSTN cannot be held low by the microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500kΩ, the recommended minimum external capacitance is calculated as:

$$[Ramp\ Time\ \times\ 5]\ \div\ [500\ k\Omega] \quad (1)$$

7.4 Layout

7.4.1 Layout Guidelines

Although the land pattern has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. The recommendation is to maintain 90 Ω differential routing underneath the device.

7.4.2 Layout Example

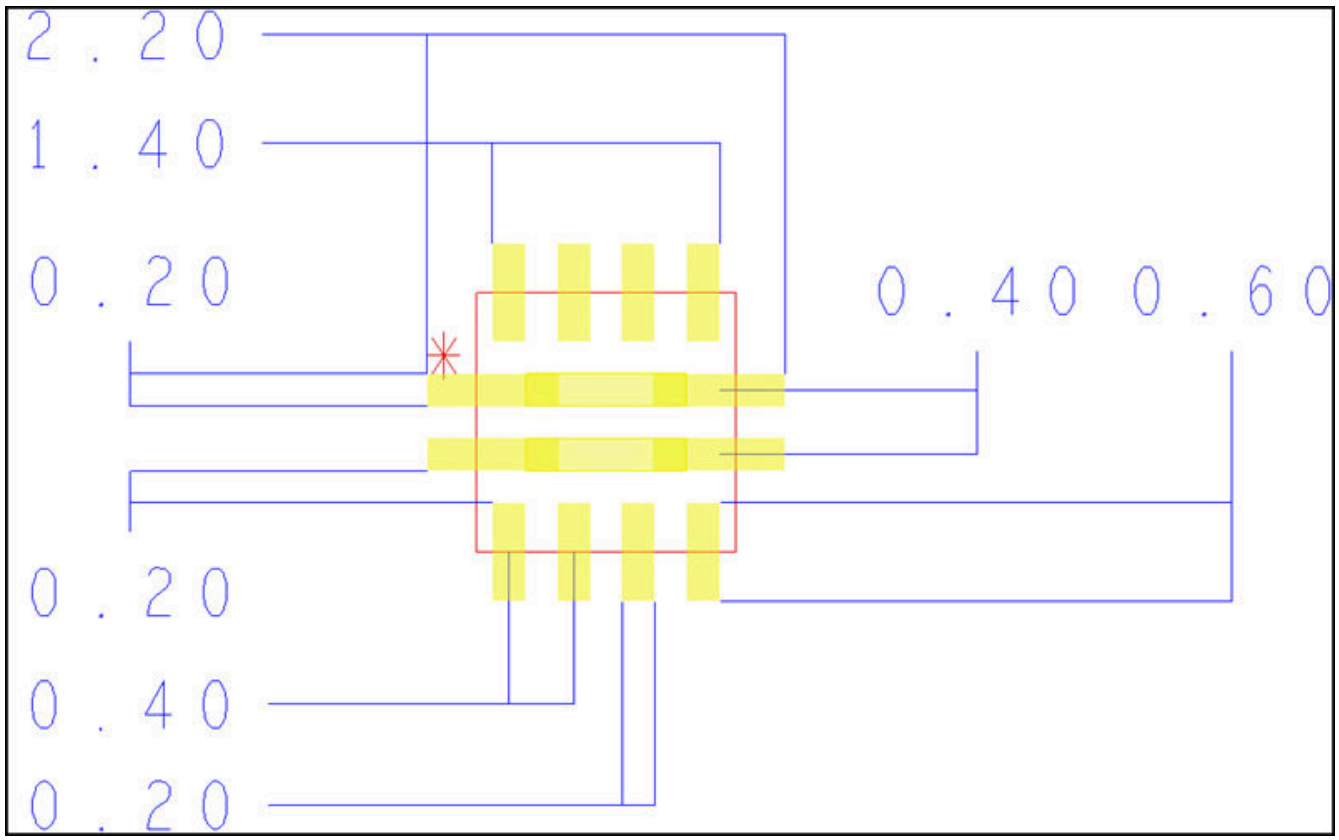


图 7-15. DP and DM Routing Underneath Device Package

8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
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8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

DATE	REVISION	NOTES
February 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB211ARWBRQ1	Active	Production	X2QFN (RWB) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1Q
TUSB211ARWBRQ1.A	Active	Production	X2QFN (RWB) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1Q
TUSB211ARWBTQ1	Active	Production	X2QFN (RWB) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1Q
TUSB211ARWBTQ1.A	Active	Production	X2QFN (RWB) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TUSB211A-Q1 :

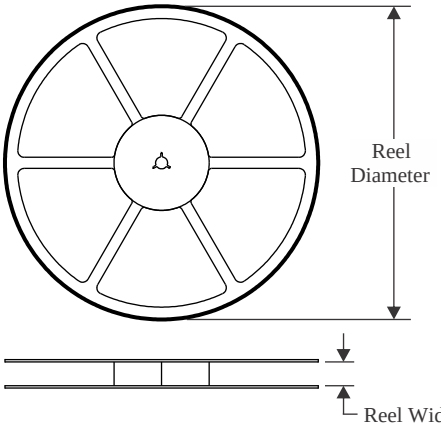
- Catalog : TUSB211A

NOTE: Qualified Version Definitions:

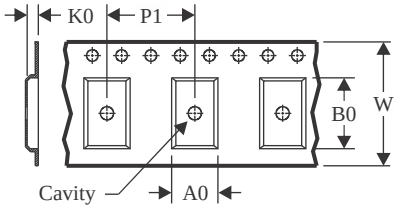
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

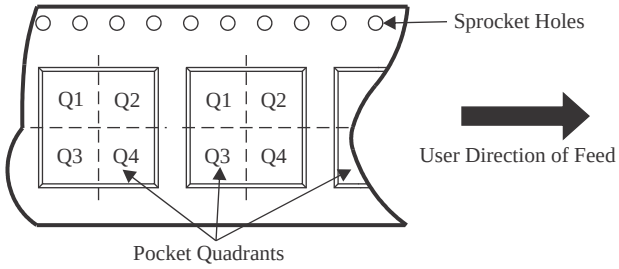


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

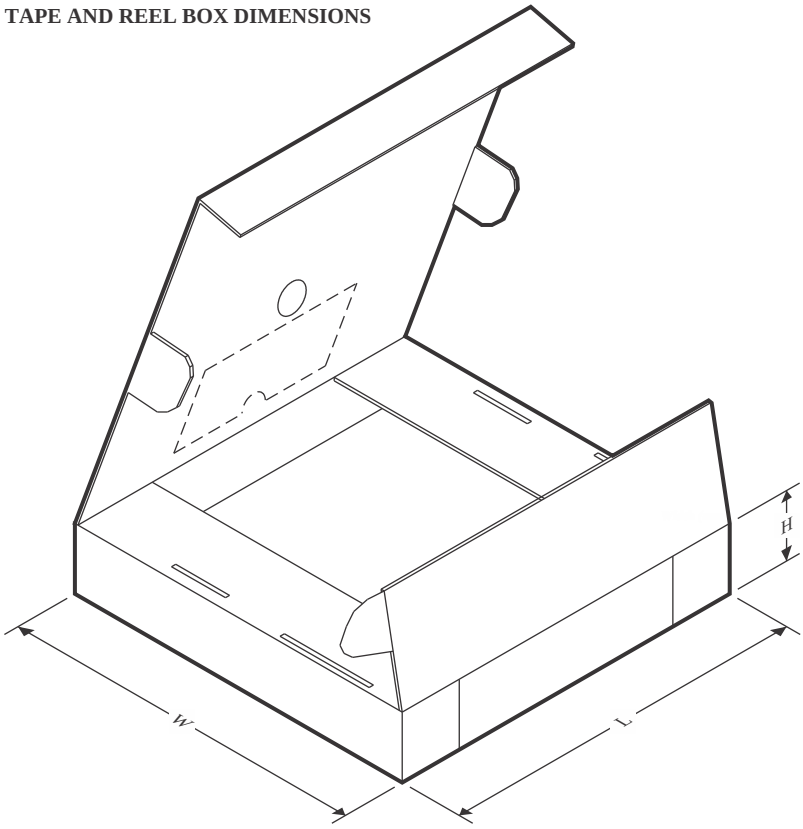
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB211ARWBRQ1	X2QFN	RWB	12	3000	180.0	9.5	1.8	1.8	0.45	4.0	8.0	Q1
TUSB211ARWBTQ1	X2QFN	RWB	12	250	180.0	9.5	1.8	1.8	0.45	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

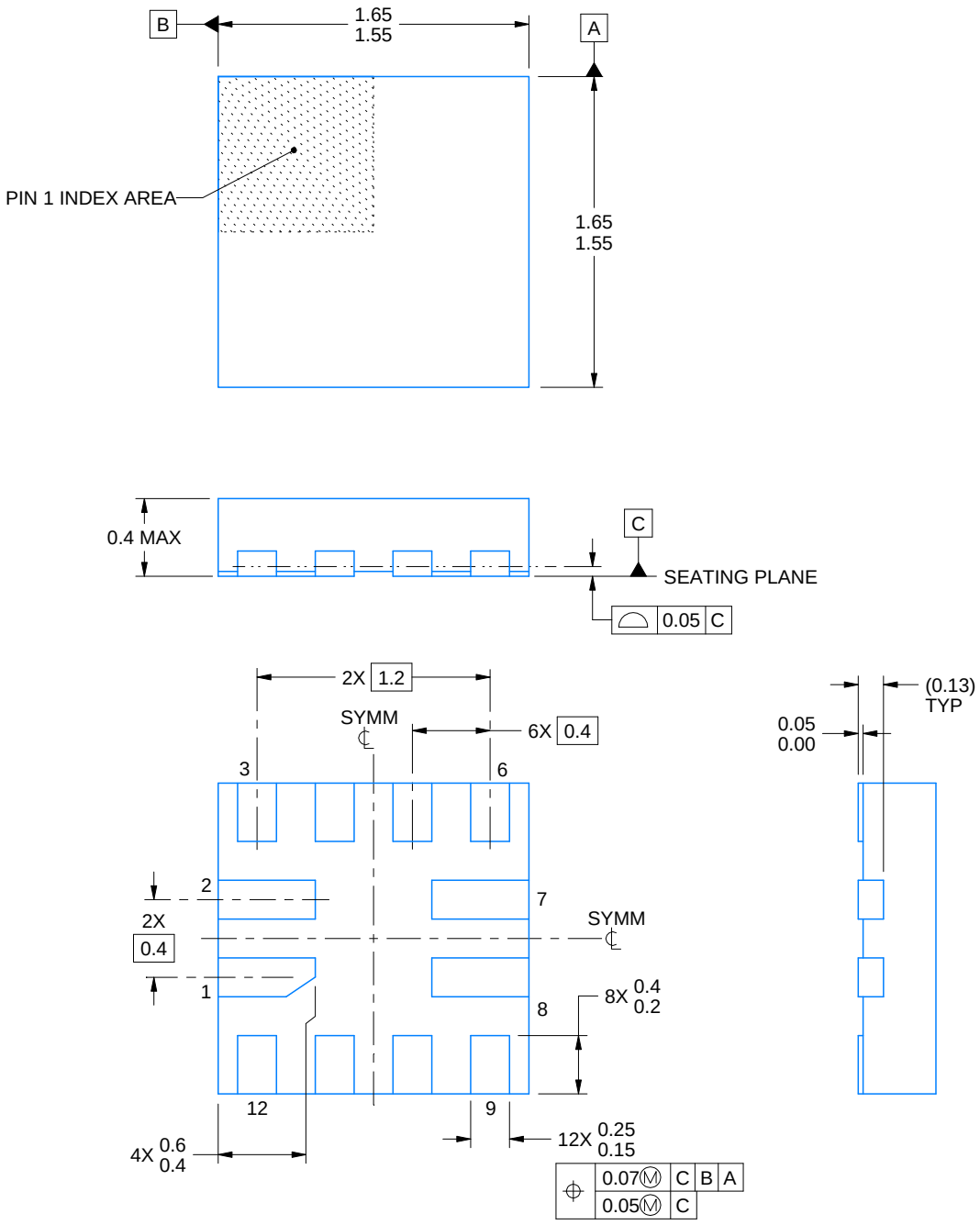
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB211ARWBRQ1	X2QFN	RWB	12	3000	189.0	185.0	36.0
TUSB211ARWBTQ1	X2QFN	RWB	12	250	189.0	185.0	36.0

PACKAGE OUTLINE

RWB0012A

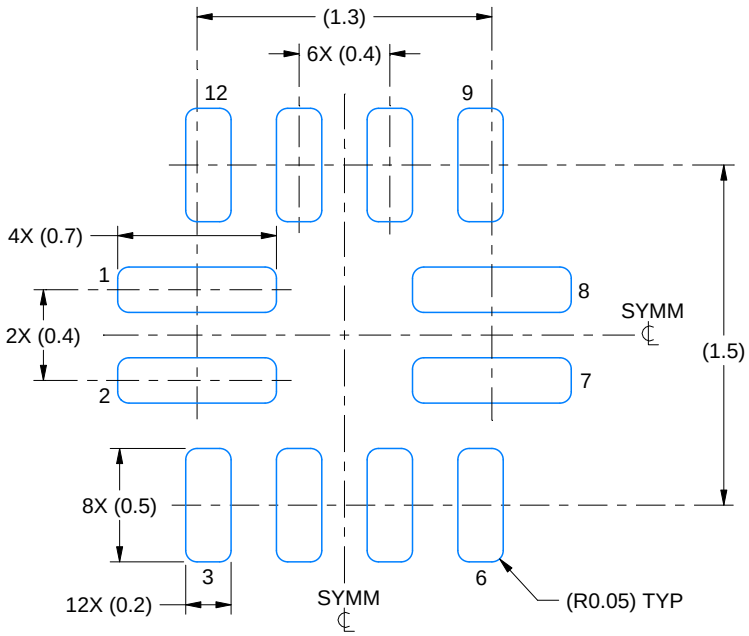
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

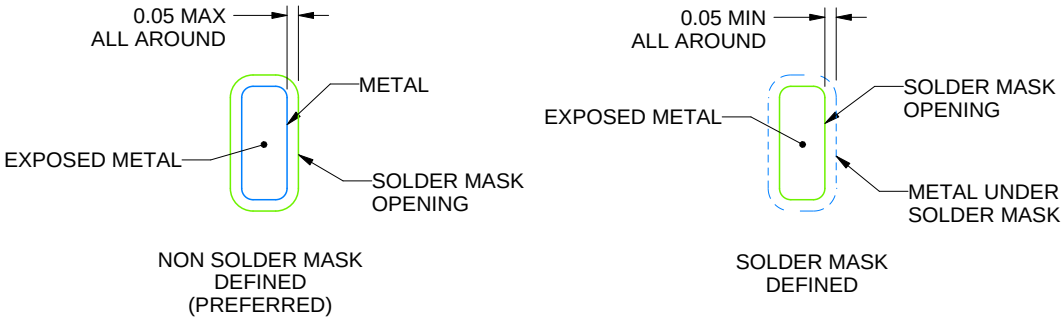


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

4221631/B 07/2017

NOTES: (continued)

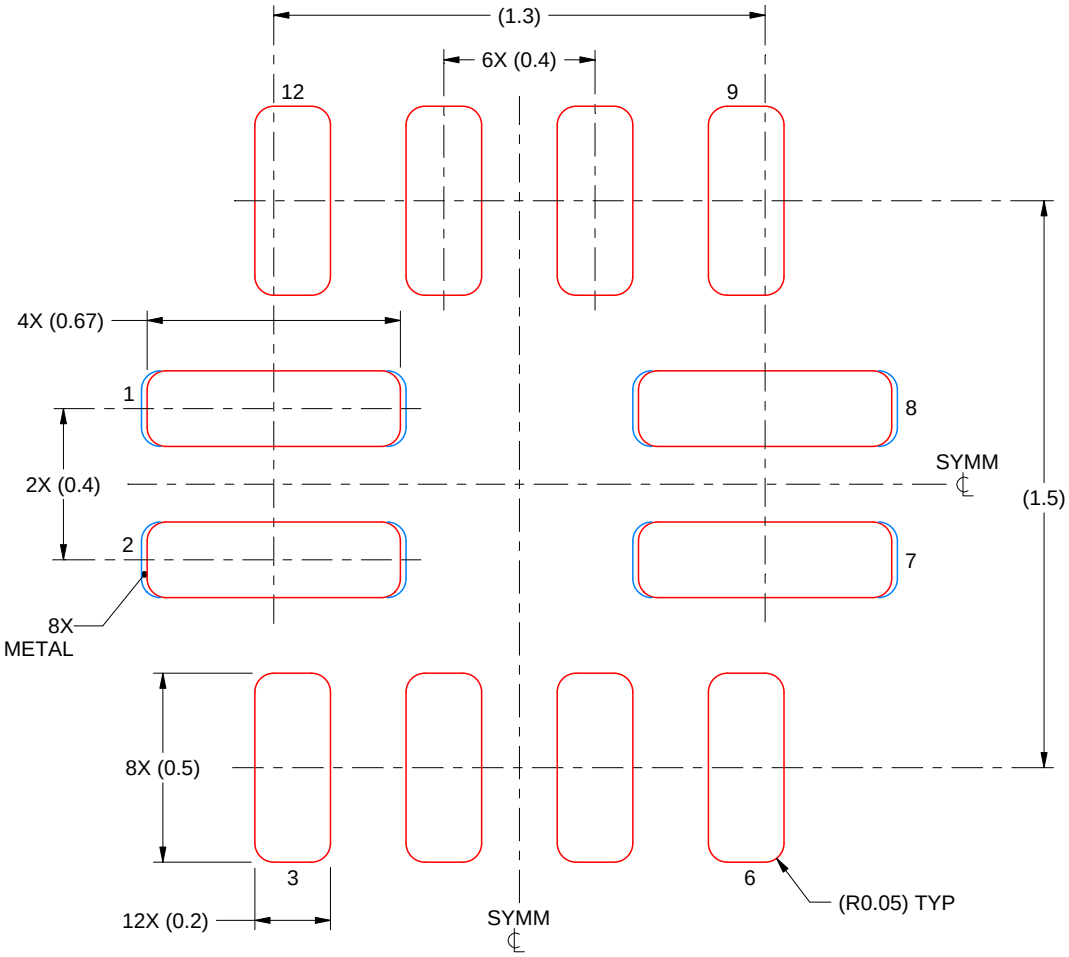
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

4221631/B 07/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月