

USB 端口单刀双掷 (SP2T) 开关支持 USB 和通用异步接收发器 (UART)

查询样品: [TSU6111A](#)

特性

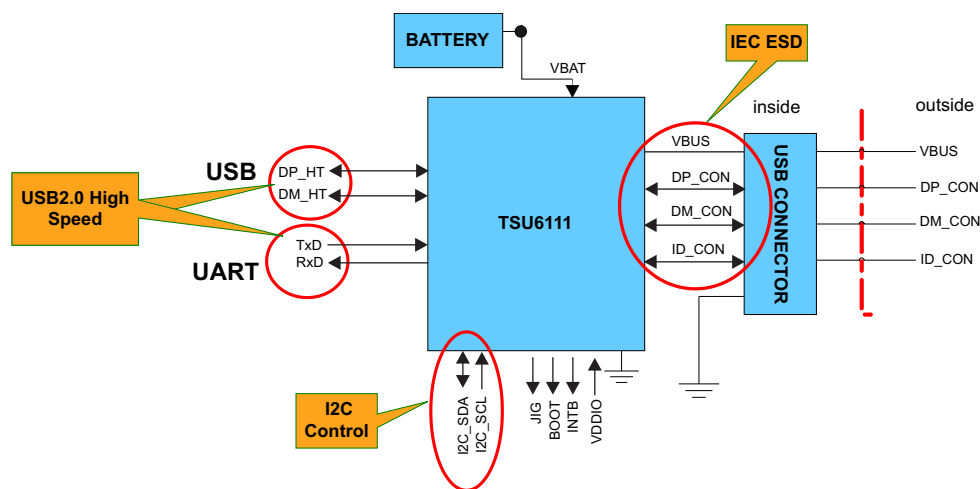
- 开关矩阵
 - **USB**
 - **UART** 支持高速 **USB 2.0**
- 充电设备侦测
 - 与 **USB BCDv1.1** 兼容
 - **VBUS** 检测
 - 数据接触检测
 - 一级和二级检测
- 兼容附件
 - **USB** 充电器 (专用充电端口 (**DCP**), 充电下行端口 (**CDP**))
 - 厂家电缆
- 附加特性
 - 与主机处理器的 **I²C** 接口
 - 由自动侦测或者手动控制的开关
 - 为插/拔生成的中断
 - 支持制造中使用的控制信号 (**JIG**, **BOOT**)

- 最大电压
 - 额定 **28V VBUS**
- 静电放电 (**ESD**) 性能测试符合 **JESD 22** 标准
 - **5000V** 人体模型 (**A114-B**, II 类)
 - **1000-V** 充电器件模型 (**C101**)
- **IEC ESD** 性能
 - 针对 **VBUS/DP_CON/DM_CON/ID_CON** 接地 (**GND**) 的 **±8kV** 接触放电 (**IEC 61000-4-2**)
- **VBUS/DP_CON/DM_CON** 上的冲击保护
 - 无需外部组件的 **USB** 连接器引脚

应用范围

- 手机与智能电话
- 平板电脑
- 数码相机与摄像机
- 全球卫星定位 (**GPS**) 导航系统
- 具有 **USB/UART** 的微型 **USB** 接口

典型应用图



订购信息⁽¹⁾

T _A	封装 ⁽²⁾		可订购部件号	正面标记
-40°C 至 85°C	超薄四方扁平无引线封装 (uQFN) 0.4-mm 引脚中心距 - RSV	卷带封装	TSU6111ARSVR	ZTN

(1) 要获得最新的封装和订购信息, 请见本文档末尾的封装选项附录, 或者浏览 TI 网站 [www.ti.com](#)。

(2) 封装图样、热数据和符号可登录 [www.ti.com/packaging](#) 获取。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

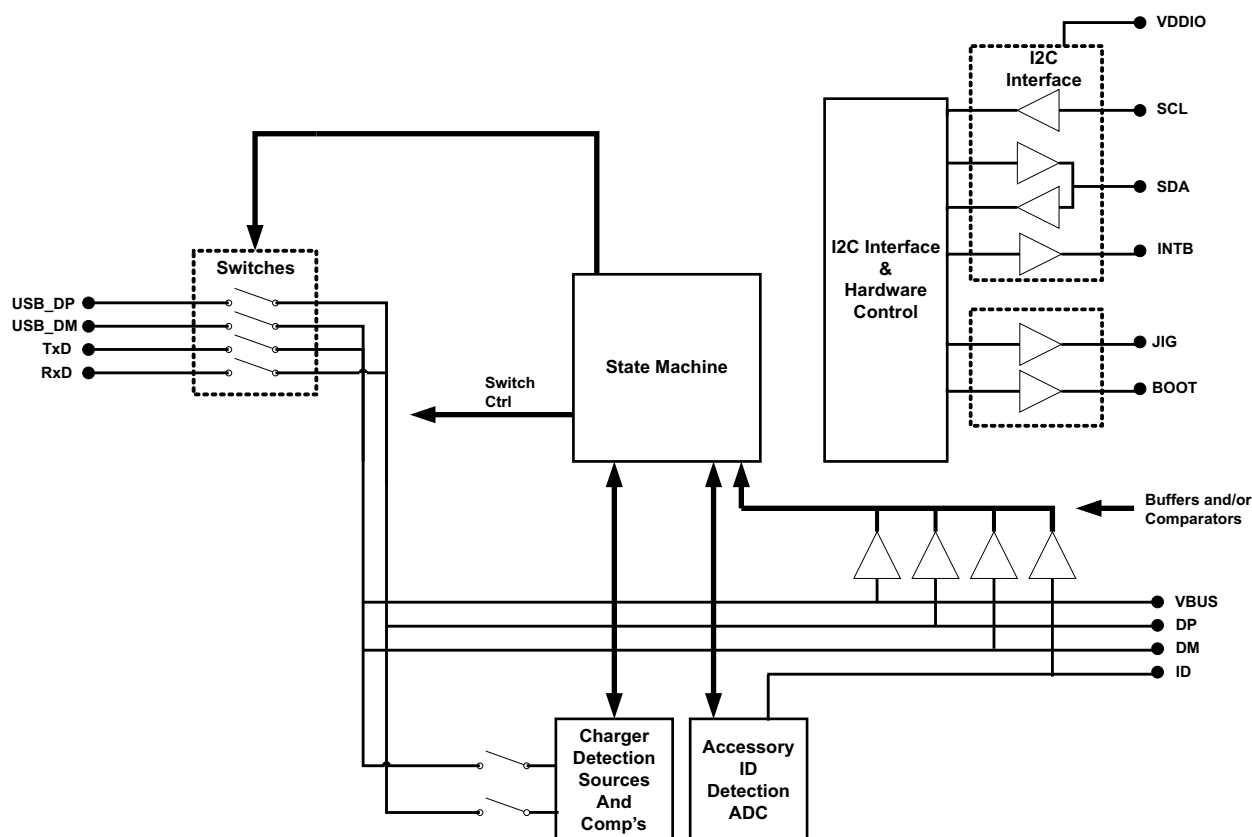
版权 © 2012, Texas Instruments Incorporated
English Data Sheet: [SCDS331](#)

说明

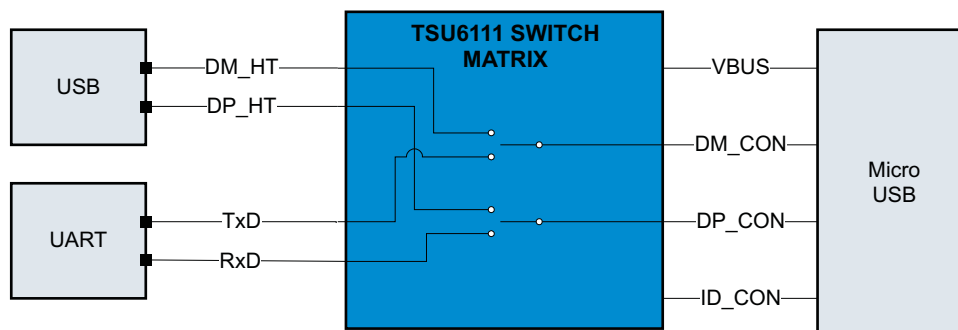
TSU6111A 是一款支持阻抗检测的高性能差分自主 SP2T 开关。此开关支持对多种通过 DP, DM, 和 ID 所连接的附件的检测。此充电器检测满足 USB 充电器规格 v1.1 并且 V_{BUS_IN} 具有一个 28V 的耐压以消除对外部保护的需要。当附加在一个充电器上时, 通过系统的 VBAT 或者 V_{BUS_IN} 为这个器件供电。

SP2T 开关由自动检测逻辑电路或者通过 I²C 的手动配置进行控制。当使用 USB 或者 UART 线缆来测试开发和制造中的器件时, JIG 和 BOOT 引脚被启用。TSU6111A 具有开漏 JIG 输出 (低电平有效)。

BLOCK DIAGRAM

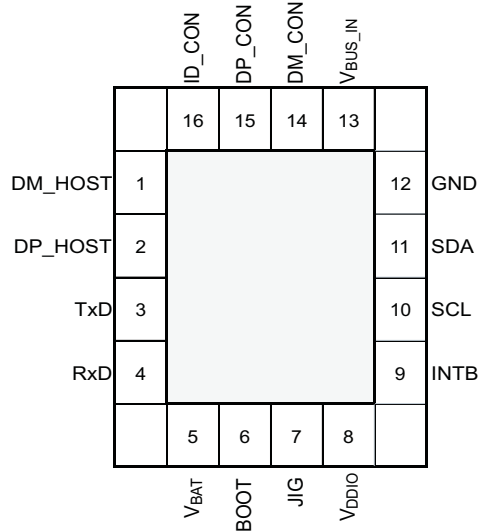


SWITCH MATRIX





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PINOUT DIAGRAM (TOP VIEW)

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DM_HOST	I/O	USB DM connected to host
2	DP_HOST	I/O	USB DP connected to host
3	TxD	I/O	UART Tx
4	RxD	I/O	UART Rx
5	VBAT	I	Connected to battery
6	BOOT	O	BOOT mode out (push-pull). Used for factory test modes.
7	JIG	O	JIG detection JIG detection (Open-drain). Used for factory test modes
8	VDDIO	O	I/O voltage reference
9	INTB	O	Interrupt to host (push-pull)
10	SCL	I	I2C clock
11	SDA	I/O	I2C data
12	GND		Ground
13	VBUS_IN	I	VBUS connected to USB receptacle
14	DM_CON	I/O	USB DM connected to USB receptacle
15	DP_CON	I/O	USB DP connected to USB receptacle
16	ID_CON	I/O	USB ID connected to USB receptacle

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{BUS}	Supply voltage from USB connector		–0.5	28	V
V _{BAT}	Supply voltage from battery		–0.5	6.0	
V _{DDIO}	Logic supply voltage		–0.5	4.6	V
V _{ID_CON}	ID Connector voltage		–0.5	V _{BAT} +0.5	V
V _{USBIO}	Switch I/O voltage range	USB Switch	–0.5	V _{BAT} +0.5	V
V _{UARTIO}	Switch I/O voltage range	UART Switch	–0.5	V _{BAT} +0.5	V
V _{JIG}	JIG voltage		–0.5	V _{BAT} +0.5	V
V _{LOGIC_O}	Voltage applied to logic output (SCL, SDA, INTB, BOOT)		–0.5	4.6	V
I _K	Analog port diode current		–50	50	mA
I _{SW-DC}	ON-state continuous switch current		–60	60	mA
I _{SW}	ON-state peak switch current PEAK		–150	150	mA
I _{IK}	Digital logic input clamp current	V _{DDIO} < 0		–50	mA
I _{LOGIC_O}	Continuous current through logic output (SCL, SDA, INTB, BOOT)		–50	50	mA
I _{GND}	Continuous current through GND			100	mA
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

THERMAL IMPEDANCE RATINGS

				UNIT
θJA	Package thermal impedance	RSV package	184	°C/W

SUMMARY OF TYPICAL CHARACTERISTICS

AMBIENT TEMPERATURE = 25°C	USB/UART PATH
Number of channels	2
ON-state resistance (r_{on})	8 Ω
ON-state resistance match (Δr_{on})	0.5 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.5 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	95 μ s/ 3.5 μ s
Bandwidth (BW)	920 MHz
OFF isolation (O_{ISO})	–26 dB at 250 MHz
Crosstalk (X_{TALK})	–32 dB at 250 MHz
Leakage current ($I_{IO(ON)}$)	50 nA

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{BUS_IN}	VBUS voltage	4.0	6.5	V
V_{BAT}	VBAT voltage	3.0	4.4	V
V_{DDIO}	VDDIO voltage	1.65	3.6	V
ID_CON_Cap	ID_CON capacitance		1	nF
USB_I/O	USB path signal range	0	3.6	V
Temperature	Operating Temperature	–40	85	°C

ELECTRICAL SPECIFICATION

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	MAX	UNIT
DIGITAL SIGNALS – I2C INTERFACE (SCL and SDA)					
V _{DDIO}	Logic and I/O supply voltage		1.65	3.6	V
V _{IH}	High-level input voltage		V _{DDIO} × 0.7	V _{DDIO}	V
V _{IL}	Low-level input voltage		0	V _{DDIO} × 0.3	V
V _{OH}	High-level output voltage	I _{OH} = –3 mA	V _{DDIO} × 0.7		V
V _{OL}	Low-level output voltage	I _{OL} = 3 mA		0.4	V
f _{SCL}	SCL frequency			400	kHz
JIG OUTPUT (TSU6111A – OPEN-DRAIN OUTPUT, ACTIVE LOW)					
V _{OL}	Low-level output voltage	I _{OL} = 10 mA, V _{BAT} = 3.0 V		0.5	V
INTB AND BOOT (PUSH-PULL OUTPUT)					
V _{OH}	High-level output voltage	I _{OH} = –4 mA, V _{DDIO} = 1.65 V	1.16	V _{DDIO}	V
V _{OL}	Low-level output voltage	I _{OL} = 4 mA, V _{DDIO} = 1.65 V	0	0.33	V

ELECTRICAL SPECIFICATIONS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TOTAL SWITCH CURRENT CONSUMPTION						
I _{BAT(Standby)}	V _{BAT} Standby current consumption	V _{BUS} = 0 V, Idle state		25	30	μA
I _{DD(Operating)}	V _{BAT} Operating current consumption	V _{BUS_IN} = 0 V, USB switches ON		45	75	μA
VOLTAGE PROTECTION						
V _{VBUS_UVLO}	V _{BUS} under voltage +	Voltage is rising		2.85		V
	V _{BUS} under voltage–	Voltage is falling		2.55		
V _{VBAT_UVLO}	V _{BUS} under voltage +	Voltage is rising		2.65		V
	V _{BUS} under voltage–	Voltage is falling		2.45		
V _{VDDIO_UVLO}	V _{BUS} under voltage +	Voltage is rising		1.30		V
	V _{BUS} under voltage–	Voltage is falling		1.05		

- (1) V_O is equal to the asserted voltage on DP_CON and DM_CON pins. V_I is equal to the asserted voltage on DP_HT and DM_HT pins. I_O is equal to the current on the DP_CON and DM_CON pins. I_I is equal to the current on the DP_HT and DM_HT pins.

USB AND UART SWITCH ELECTRICAL CHARACTERISTICS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V _{USBIO}	Analog signal range			0		V _{BAT}	V
r _{ON}	ON-state resistance	DM_HT, DP_HT, DM_CON, DP_CON	V _I = 0 V to 3.6 V, I _O = –2 mA, V _{BAT} = 3.0 V		8	15	Ω
Δr _{ON}	ON-state resistance match between channels	DM_HT, DP_HT, DM_CON, DP_CON	V _I = 0.4 V, I _O = –2 mA, V _{BAT} = 3.0 V		0.5	2	Ω
r _{ON(flat)}	ON-state resistance flatness	DM_HT, DP_HT, DM_CON, DP_CON	V _I = 0 V to 3.6 V, I _O = –2 mA, V _{BAT} = 3.0 V		0.5	2	Ω
I _{IO(OFF)}	V _I or V _O OFF leakage current		V _I = 0.3 V, V _O = 2.7 V or V _I = 2.7 V, V _O = 0.3 V, V _{BAT} = 4.4 V, Switch OFF		45	200	nA
I _{IO(ON)}	V _O ON leakage current		V _I = OPEN, V _O = 0.3 V or 2.7 V, V _{BAT} = 4.4 V, Switch ON		50	200	nA
DYNAMIC							
t _{ON}	Turn-ON time	From receipt of I ² C ACK bit	V _I or V _O = V _{BAT} , R _L = 50 Ω, C _L = 35 pF		95		μs
t _{OFF}	Turn-OFF time	From receipt of I ² C ACK bit	V _I or V _O = V _{BAT} , R _L = 50 Ω, C _L = 35 pF		3.5		μs
C _{I(OFF)}	V _I OFF capacitance		DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		4		pF
C _{O(OFF)}	V _O OFF capacitance		DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		7		pF
C _{I(ON)} , C _{O(ON)}	V _I , V _O ON capacitance		DC bias = 0 V or 3.6 V, f = 10 MHz, Switch ON		9		pF
BW	Bandwidth		R _L = 50 Ω, Switch ON		920		MHz
O _{ISO}	OFF Isolation		f = 240 MHz, R _L = 50 Ω, Switch OFF		–26		dB
X _{TALK}	Crosstalk		f = 240 MHz, R _L = 50 Ω		–32		dB

(1) V_O is equal to the asserted voltage on DP_CON and DM_CON pins. V_I is equal to the asserted voltage on DP_HT and DM_HT pins. I_O is equal to the current on the DP_CON and DM_CON pins. I_I is equal to the current on the DP_HT and DM_HT pins.

GENERAL OPERATION

The TSU6111A will automatically detect accessories plugged into the phone via the mini/micro USB 5 pin connector. The type of accessory detected will be stored in I²C registers within the TSU6111A for retrieval by the host. The TSU6111A has a network of switches that are automatically opened and closed based on the accessory detection. See [Table 1](#) for details of which switches are open during each mode of operation. The TSU6111A also offers a manual switching mode that allows the host processor to decide which switches should be opened and closed. The manual switching settings are executed through the I²C interface.

STANDBY MODE

Standby mode is the default mode upon power up and occurs when no accessory has been detected. During this mode, the VBUS and ID lines are continually monitored through comparators to determine when an accessory is inserted. Power consumption is minimal during standby mode.

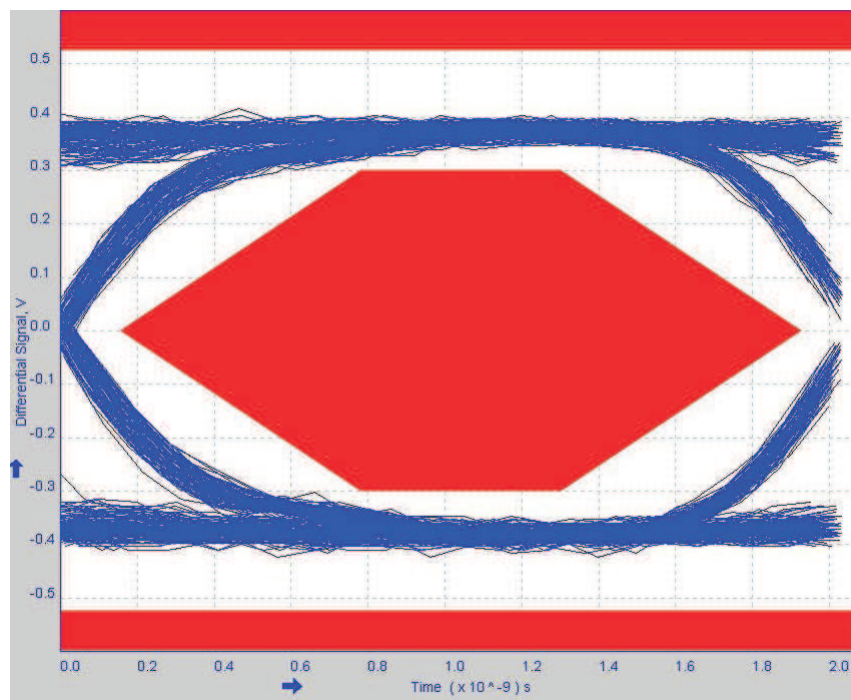
POWER SUPERVISOR

TSU6111A uses VBAT as the primary supply voltage. VBUS is the secondary supply. VDDIO is used for I²C communication.

Table 1. Function Table

TSU6111A					
VBAT	VBUS	VDDIO	DETECTION	I2C	COMMENTS
Yes	No	No	Enabled	Not enabled	VBAT is supply
Yes	Yes	No	Enabled	Not enabled	VBAT is supply
Yes	No	Yes	Enabled	Enabled	VBAT is supply
Yes	Yes	Yes	Enabled	Enabled	VBAT is supply
No	Yes	No	Enabled	Not enabled	VBUS is supply
No	Yes	Yes	Not valid		
No	No	Yes	Not valid		
No	No	No	Power Down Reset		

EYE DIAGRAM USB 2.0 HIGH SPEED



ACCESSORY ID DETECTION

If V_{BUS_IN} is high and the attachment is not a charger, then determine the impedance on the ID pin. If V_{BUS_IN} is low and an accessory is attached, then use an ADC for impedance sensing on the ID pin to identify which accessory is attached.

IMPEDANCE BUCKETS FOR EACH ACCESSORY

In order to implement ID detection, each accessory should contain a ID impedance resistor value (refer to [Table 2](#)) which has a 5% tolerance accuracy.

Table 2. Accessory ID and Switch States

ACCESSORY	DETECTED IMPEDANCE ON ID	RESISTOR TOLERANCE (%)	ADC VALUE	SWITCH STATE		FACTORY CABLE	
				DP/DM		JIG	BOOT
				USB	UART		
OTG	0	—	0	ON	OFF	OFF	OFF
MHL	1K	5%	0	OFF	OFF	OFF	OFF
Audio Device Type 3	28.7K	5%	1110	OFF	OFF	OFF	OFF
Reserved Accessory #1	34K	5%	1111	OFF	OFF	OFF	OFF
Reserved Accessory #2	40.2K	5%	10000	OFF	OFF	OFF	OFF
Reserved Accessory #3	49.9K	5%	10001	OFF	OFF	OFF	OFF
Reserved Accessory #4	64.9K	5%	10010	OFF	OFF	OFF	OFF
Audio Device Type 2	80.27K	5%	10011	OFF	OFF	OFF	OFF
Phone Powered Device	102K	5%	10100	OFF	ON	OFF	OFF
TTY Converter	121K	5%	10101	OFF	OFF	OFF	OFF
UART Cable	150K	5%	10110	OFF	ON	OFF	OFF
Type 1 Charger	200K	5%	10111	OFF	OFF	OFF	OFF
Factory Mode Cable - Boot Off USB	255K	5%	11000	ON	OFF	ON	OFF
Factory Mode Cable - Boot On USB	301K	5%	11001	ON	OFF	ON	ON
Audio/Video Cable	365K	5%	11010	OFF	OFF	OFF	OFF
Type 2 Charger	442K	5%	11011	OFF	OFF	OFF	OFF
Factory Mode Cable - Boot Off UART	523K	5%	11100	OFF	ON	ON	OFF
Factory Mode Cable - Boot On UART	619K	5%	11101	OFF	ON	ON	ON
Stereo Headset with Remote (Audio Device Type 1)	1000.07K	10%	11110	OFF	OFF	OFF	OFF
Mono/Stereo Headset (Audio Device Type 1)	1002K	10%	11110	OFF	OFF	OFF	OFF
No ID	—	—	11111	OFF	OFF	OFF	OFF
USB Standard Downstream Port	—	—	11111	ON	OFF	OFF	OFF
USB Charging Downstream Port	—	—	11111	ON	OFF	OFF	OFF
Dedicated Charging Port	—	—	11111	OFF	OFF	OFF	OFF

Power-On Reset

When power (from 0 V) is applied to V_{BAT} , an internal power-on reset holds the TSU6111A in a reset condition until V_{BAT} has reached V_{POR} . Once V_{BAT} has reached V_{POR} , the reset condition is released, and the TSU6111A registers and I²C state machine initialize to their default states.

After the initial power-up phase, V_{BAT} must be lowered to below 0.2 V and then back up to the operating voltage (V_{DDIO}) for a power-reset cycle.

Software Reset

The TSU6111A has software reset feature.

- Hold low both I²C_SCL and I²C_SDA for more than 30ms to reset digital logic of the TSU6111A.

After resetting the digital logic, INTB will keep low until INT_Mask bit of Control register (0x02) is cleared.

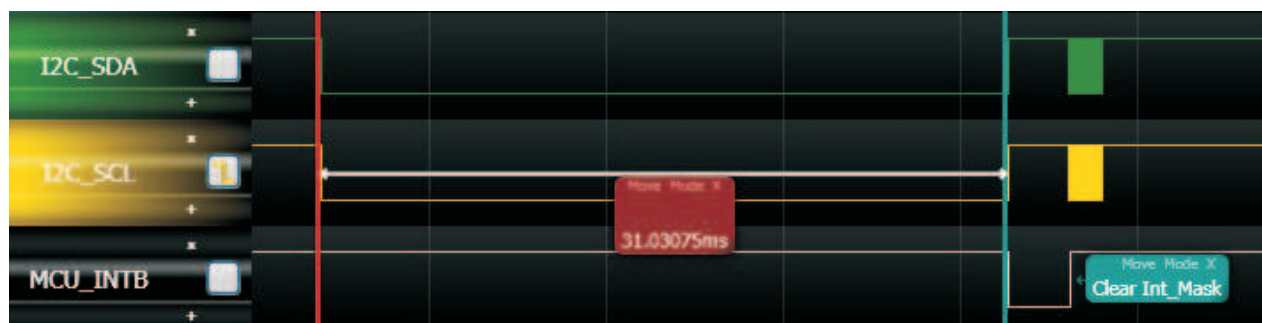


Figure 1. Software Reset

Standard I²C Interface Details

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. The SCL and SDA lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by the master sending a START condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 2). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, the device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

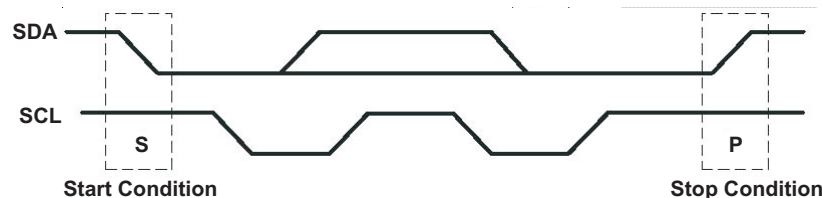


Figure 2. Definition of Start and Stop Conditions

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data is sent only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP, see Figure 3).

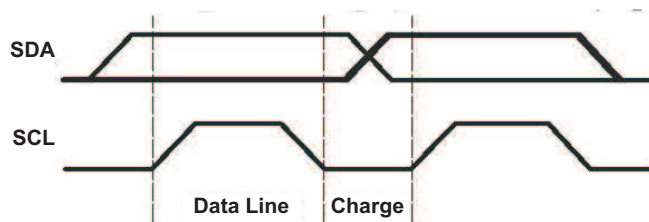


Figure 3. Bit Transfer

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 2).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver address must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 4). Setup and hold times must be taken into account.

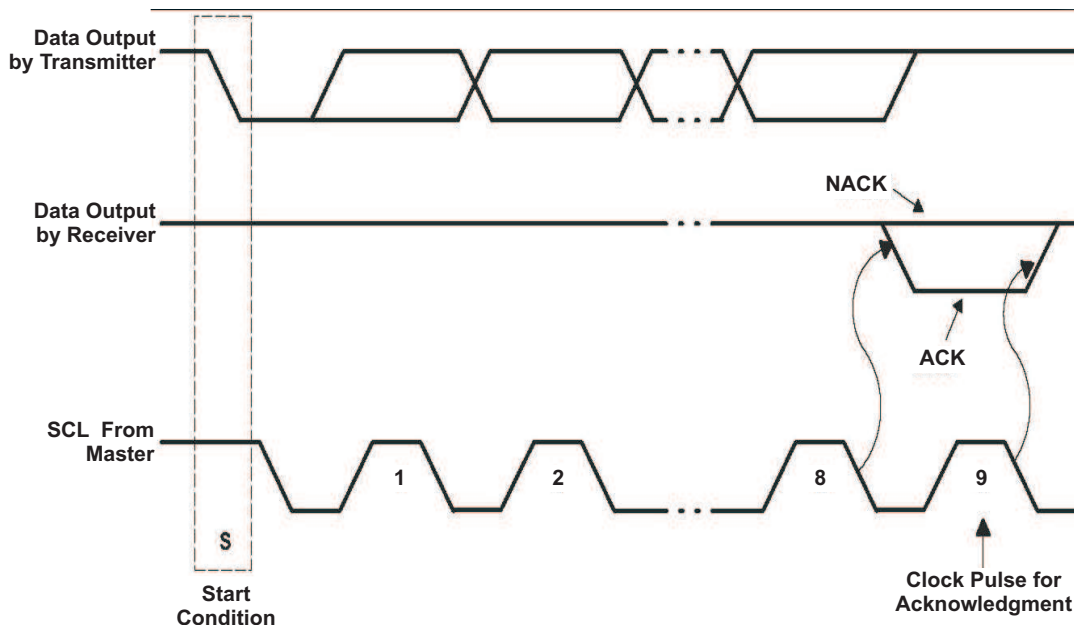


Figure 4. Acknowledgment on I²C Bus

Writes

Data is transmitted to the TSU6111A by sending the device slave address and setting the LSB to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. The next byte is written to the specified register on the rising edge of the ACK clock pulse.

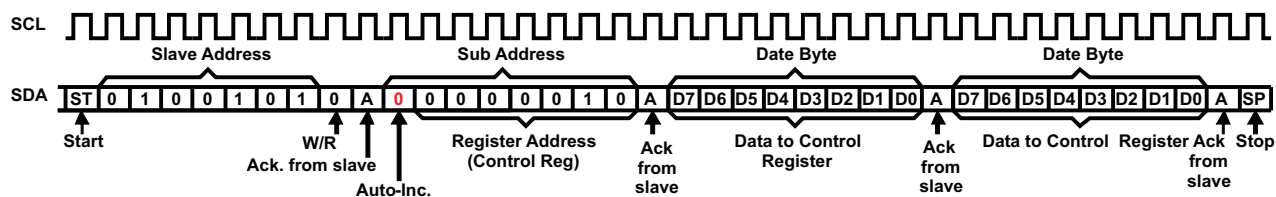


Figure 5. Repeated Data Write to a Single Register

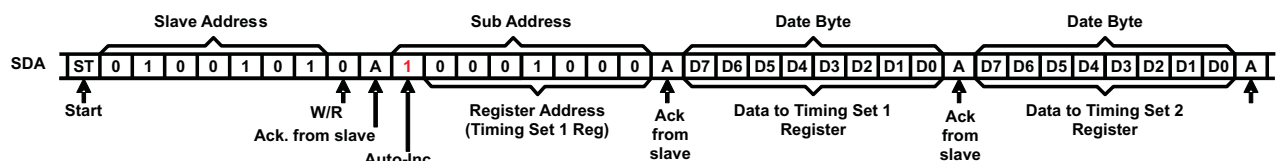


Figure 6. Burst Data Write to Multiple Registers

Reads

The bus master must first send the TSU6111A slave address with the LSB set to logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device slave address is sent again but, this time, the LSB is set to logic 1. Data from the register defined by the command byte then is sent by the TSU6111A. Data is clocked into the SDA output shift register on the rising edge of the ACK clock pulse (See Figure 7).

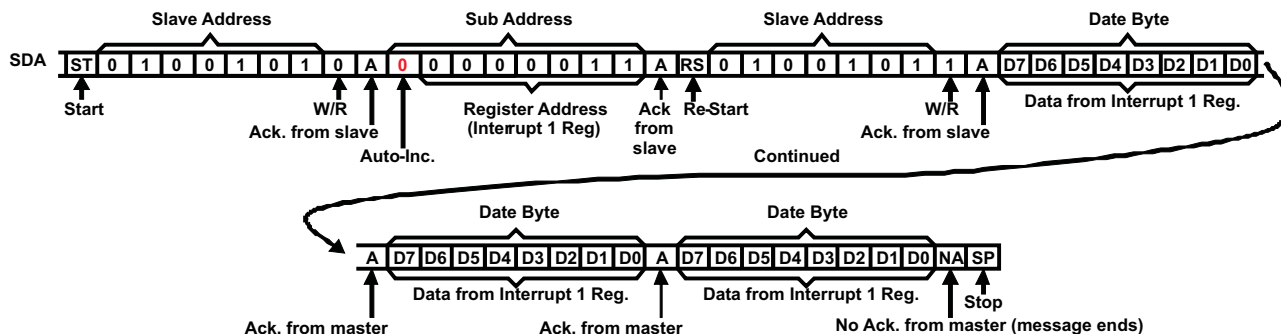


Figure 7. Repeated Data Read from a Single Register – Combined Mode

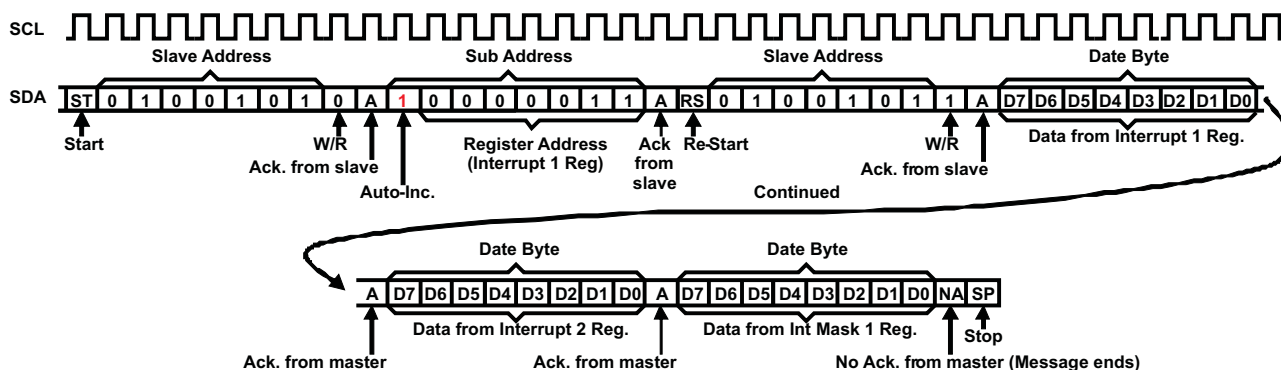


Figure 8. Burst Data Read from Multiple Registers – Combined Mode

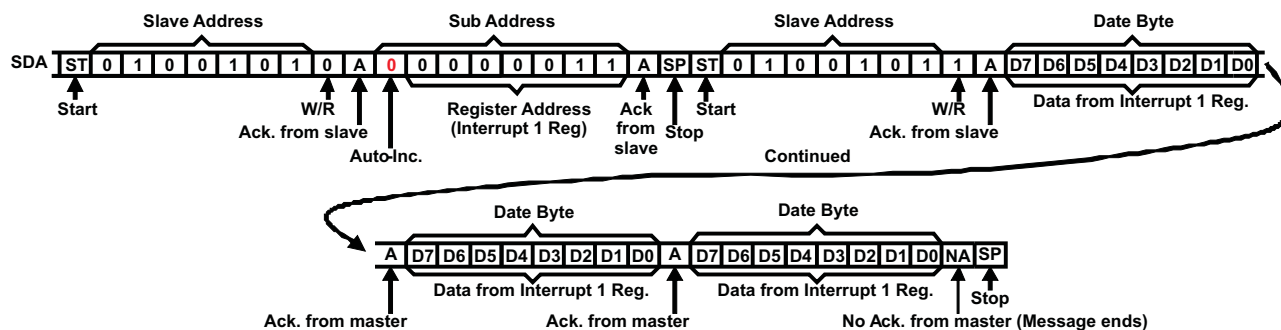


Figure 9. Repeated Data Read from a Single Register – Split Mode

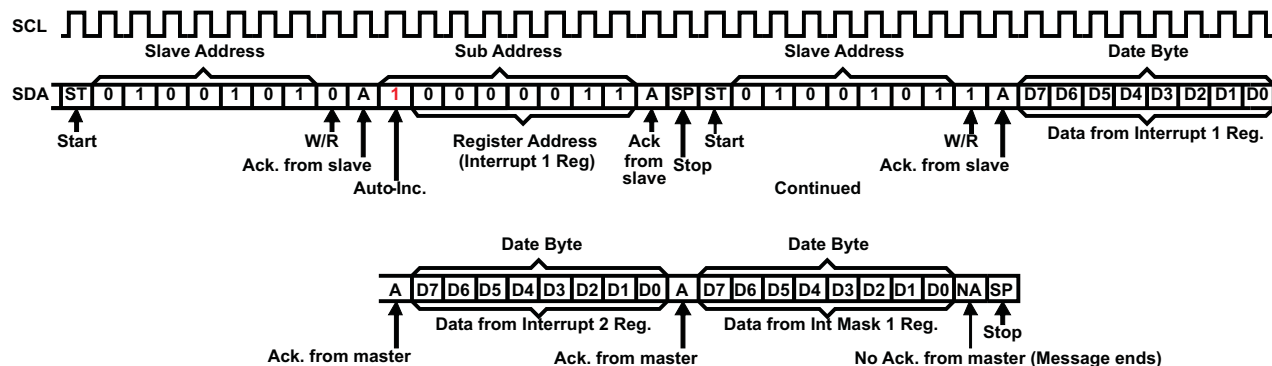


Figure 10. Burst Data Read from Multiple Registers – Split Mode

Notes (Applicable to Figure 5–Figure 10):

- SDA is pulled low on Ack. from slave or Ack. from master.
- Register writes always require sub-address write before first data byte.
- Repeated data that writes to a single register continues indefinitely until a Stop or a Re-Start.
- Repeated data reads from a single register continues indefinitely until No Ack. from master.
- Burst data writes start at the specified register address, then advance to the next register address, even to the read-only registers. For these registers, data write appears to occur; however, no data is changed by the writes. After register 14h is written, writing resumes to register 01h and continues until a Stop or a Re-Start.
- Burst data reads starts at the specified register address, then advances to the next register address. Once register 14h is read, reading resumes from register 01h and continues until No Ack. from master.

I²C Register Map⁽¹⁾⁽²⁾⁽³⁾

ADDR	REGISTER	TYPE	RESET VALUE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	
01h	Device ID	R	00010010	Version ID					Vendor ID			
02h	Control	R/W	xxx11111				Switch Open	Raw Data	Manual S/W	Wait	INT Mask	
03h	Interrupt 1	R	xxxxxx00							Detach	Attach	
04h	Interrupt 2	R	xx0xx000			CONNECT			ADC_Change	Reserved_Attach	Charging_A/V	
05h	Interrupt Mask 1	R/W	xxxxxx00							Detach	Attach	
06h	Interrupt Mask 2	R/W	xx0xx000			CONNECT			ADC_Change	Reserved_Attach	Charging_A/V	
07h	ADC	R	xxx11111				ADC Value					
08h	Timing Set 1	R/W	xxxx0000					Device Wake Up				
09h	Timing Set 2	R/W	0000xxxx	Switching Wait								
0Ah	Device Type 1	R	00000000	USG OTG	DCP	CDP		UART	USG	Audio Type2	Audio Type1	
0Bh	Device Type 2	R	00000000	Audio Type3	Audio/Video	TTY	PPD	JIG_UART_OFF	JIG_UART_ON	JIG_USB_OFF	JIG_USB_ON	
0Ch	Button 1	R	00000000	7	6	5	4	3	2	1	Send_End	
0Dh	Button 2	R	x0000000		Unknown	Error	12	11	10	9	8	
13h	Manual S/W 1	R/W	000000xx	D- Switching			D+ Switching					
14h	Manual S/W 2	R/W	xxxx00xx					BOOT_SW	JIG-ON			
15h	Device Type 3	R	xxxxxx00							VBUS		MHL

- (1) Do not use blank register bits.
 (2) Write “0” to the blank register bits.
 (3) Values read from the blank register bits are not defined and invalid.

Slave Address

NAME	SIZE (BITS)	DESCRIPTION							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Slave address	8	0	1	0	0	1	0	1	R/W

Device ID

Address: 01h

Reset Value: 00010010

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
2-0	Vendor ID	3	A unique number for vendor 010 for Texas Instruments
7-3	Version ID	5	A unique number for chip version 00001b for TSU6111A

Control

Address: 02h

Reset Value: xxx11111

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	INT Mask	1	0: Unmask interrupt 1: Mask interrupt
1	Wait	1	0: Wait until host re-sets this bit(WAIT bit) high 1: Wait until Switching timer is expired
2	Manual S/W	1	0: Manual Switching 1: Automatic Switching
3	RAW Data	1	0: Report the status changes on ID to Host 1: Don't report the status changes on ID
4	Switch Open	1	0: Open all Switches 1: Automatic Switching by accessory status
7-5	Reserved		

Interrupt 1

Address: 03h

Reset Value: xxxxxx00

Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Attach	1	1: Accessory is attached
1	Detach	1	1: Accessory is detached
7-2	Unused	6	Unused

Interrupt 2

Address: 04h

Reset Value:xx0xx000

Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Charging_A/V	1	1: Charger detected when A/V cable is attached
1	Reserved_Attach	1	1: Reserved Device is attached
2	ADC_Change	1	1: ADC value is changed when RAW data is enabled
4-3	Unused	2	
5	Connect	1	1: Switch is connected(closed)
7-6	Unused	2	

Interrupt Mask 1

Address: 05h

Reset Value:xxxxxx00

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Attach	1	0: Unmask Attach Interrupt 1: Mask Attach Interrupt
1	Detach	1	0: Unmask Key press Interrupt 1: Mask Detach Interrupt
7-2	Unused	6	Unused

Interrupt Mask 2

Address: 06h

Reset Value:xx0xx000

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Charging_A/V	1	0: Unmask A/V_Charging Interrupt 1: Mask A/V_Charging Interrupt
1	Reserved_Attach	1	0: Unmask Reserved_Attach Interrupt 1: Mask Reserved_Attach Interrupt
2	ADC_Change	1	0: Unmask ADC_Change Interrupt 1: Mask ADC_Change Interrupt
4-3	Unused	2	
5	Connect	1	0: Unmask Connect Interrupt 1: Mask Connect Interrupt
7-6	Unused	2	

ADC Value

Address: 07h

Reset Value: xxx11111

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
4-0	ADC value	5	ADC value read from ID
7-5	Unused	3	

Timing Set 1

Address: 08h

Reset Value: xxxx0000

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
3-0	Device Wake Up	4	Device wake up duration
7-4	Unused	4	

Timing Set 2

Address: 09h

Reset Value: 0000xxxx

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
3-0	Unused	4	
7-4	Switching wait	4	Waiting duration before switching

Time Table⁽¹⁾

SETTING VALUE	DEVICE WAKE UP	SWITCHING WAIT
0000	50 ms	10 ms
0001	100 ms	30 ms
0010	150 ms	50 ms
0011	200 ms	70 ms
0100	300 ms	90 ms
0101	400 ms	110 ms
0110	500 ms	130 ms
0111	600 ms	150 ms
1000	700 ms	170 ms
1001	800 ms	190 ms
1010	900 ms	210 ms
1011	1000 ms	–
1100	–	–
1101	–	–
1110	–	–
1111	–	–

(1) Maximum variation of these timing is $\pm 20\%$

Device Type 1

Address: 0Ah

Reset Value: 00000000

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Audio type 1	1	Audio device type 1
1	Audio type 2	1	Audio device type 2
2	USB	1	USB host
3	UART	1	UART
4	Unused	1	Unused
5	CDP	1	Charging Downstream Port (USB Host Hub Charger)
6	DCP	1	Dedicated Charging Port
7	USB OTG	1	USB on-the-go device

Device Type 2

Address: 0Bh

Reset Value: 00000000

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	JIG_USB_ON	1	Factory mode cable
1	JIG_USB_OFF	1	Factory mode cable
2	JIG_UART_ON	1	Factory mode cable
3	JIG_UART_OFF	1	Factory mode cable
4	PPD	1	Phone-powered device
5	TTY	1	TTY converter
6	Audio/Video	1	A/V cable
7	Audio type 3	1	Audio device type 3

Button 1

Address: 0Ch

Reset Value: 00000000

Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Send_End	1	Send_End key is pressed
1	1	1	Number 1 key is pressed
2	2	1	Number 2 key is pressed
3	3	1	Number 3 key is pressed
4	4	1	Number 4 key is pressed
5	5	1	Number 5 key is pressed
6	6	1	Number 6 key is pressed
7	7	1	Number 7 key is pressed

Button 2

Address: 0Dh

Reset Value:x0000000

Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	8	1	Number 8 key is pressed
1	9	1	Number 9 key is pressed
2	10	1	Number 10 key is pressed
3	11	1	Number 11 key is pressed
4	12	1	Number 12 key is pressed
5	Error	1	Error key is pressed
6	Unknown	1	Unknown key is pressed
7	Unused		

Manual S/W 1

Address: 13h

Reset Value: 000000xx

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
1-0	Unused	2	
4-2	D+ Switching	3	000: Open all switch 001: D+ is connected to D+ of USB port 010: Open all switch 011: D+ is connected to RxD of UART
7-5	D– Switching	3	000: Open all switch 001: D– is connected to D– of USB port 010: Open all switch 011: D– is connected to TxD of UART

Manual S/W 2

Address: 14h

Reset Value: xxxx00xx

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
1-0	Unused	2	
2	JIG	1	TSU6111A: 0: High Impedance 1: GND
3	BOOT	1	0: Low 1: High
7-4	Unused	4	

Device Type 3

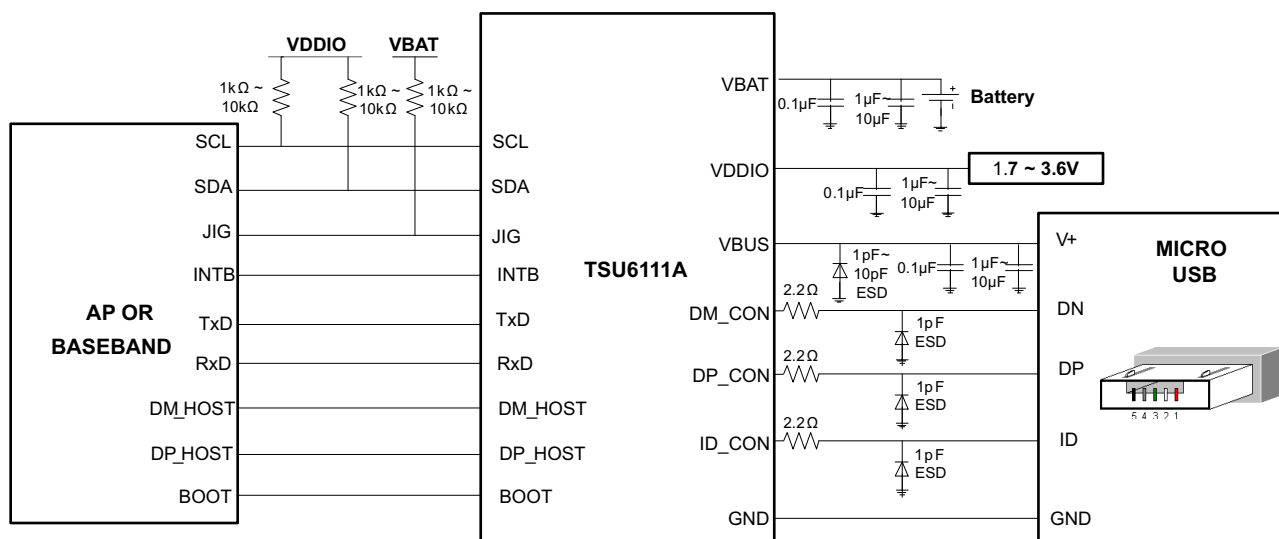
Address: 15h

Reset Value: xxxxxx00

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	MHL	2	MHL device
1	VBUS	1	VBUS valid
7-1	Unused	7	Unused

APPLICATION SCHEMATIC



PIN NAME	PIN NO.	CRITICAL COMPONENT
V _{BUS_IN}	13	1µF~10µF
		ESD Protection Diode
		0.1µF
V _{DDIO}	8	1µF~10µF
		0.1µF
V _{BAT}	5	1µF~10µF
		Battery
		0.1µF
Jig	7	1kΩ
SCL	10	1kΩ
SDA	11	1kΩ
DM_CON	14	2.2Ω
		ESD Protection Diode
DP_CON	15	2.2Ω
		ESD Protection Diode
ID_CON	16	2.2Ω ⁽¹⁾
		ESD Protection Diode

(1) Optional components

SCHEMATIC GUIDELINES

1. V_{BUS_IN} , V_{DDIO} , and V_{BAT} require $1\mu F \sim 10\mu F$ and $0.1\mu F$ decoupling capacitors to reduce noise from circuit elements. The capacitors act as a shunt to block off the noise. The $0.1\mu F$ capacitor smoothes out high frequencies and has a lower series inductance. The $1\mu F \sim 10\mu F$ capacitors smoothes out the lower frequencies and has a much higher series inductance. Placing both capacitors will provide better load regulation across the frequency spectrum.
2. JIG is an open-drain output and therefore requires a $1k\Omega \sim 10k\Omega$ pull-up resistor to V_{BAT} .
3. SCL and SDA require $1k\Omega \sim 10k\Omega$ pull-up resistors to V_{DDIO} to prevent floating inputs.
4. V_{BUS_IN} , DM_CON , and DP_CON are recommended to have an external resistor 2.2Ω to provide extra ballasting to protect the chip and internal circuitry.
 - (a) For ID_CON , if there is less stress on the ID pin then the external 2.2Ω resistor is optional.
5. DM_CON , DP_CON , and ID_CON are recommended to have a $1pF$ external ESD Protection Diode rated for $8kV$ IEC protection to prevent failure in case of an $8kV$ IEC contact discharge.
6. V_{BUS_IN} is recommended to have a $1pF \sim 10pF$ external ESD Protection Diode rated for $8kV$ IEC protection to prevent failure in case of an $8kV$ IEC contact discharge.

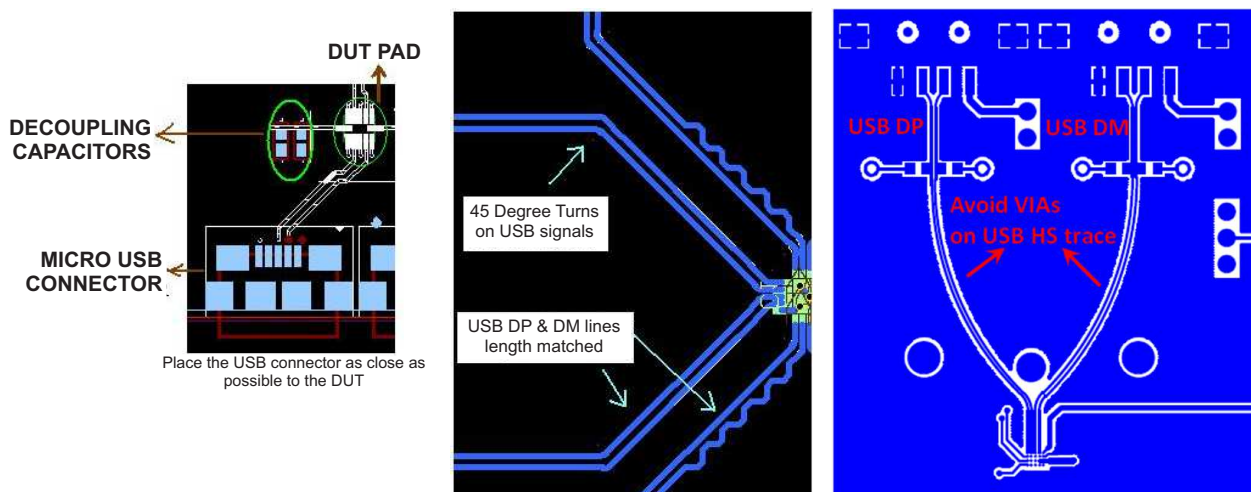
RECOMMENDED OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V_{BUS_IN}	VBUS voltage	4.0	6.5	V
V_{BAT}	VBAT voltage	3.0	4.4	V
V_{DDIO}	VDDIO voltage	1.65	3.6	V
ID_CON_Cap	ID_CON capacitance		1	nF
USB_I/O	USB path signal range	0	3.6	V
Temperature	Operating Temperature	-40	85	°C

PCB ROUTING GUIDELINES

Routing Guidelines for USB Signal Integrity

1. All the USB lines DP_CON, DM_CON, DP_HT, DM_HT, TxD, and RxD
 - Must have 45Ω single ended characteristic impedance
 - Must have 90Ω differential ended impedance
 - To fulfill USB 2.0 requirements
2. TSU6111A location
 - Close to the USB connector as possible
 - Keep the distance between the USB controller and the device less than 1 inch
 - Shortening the length of the trace will reduce effect of stray noise and radiate less EMI
3. Minimize use of VIAs for USB related signals
 - Differential transmission lines should be matched as close as possible
 - For optimum USB2.0 performance, use no VIAs



REVISION HISTORY

Changes from Original (February 2012) to Revision A

Page

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSU6111ARSVR	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTN
TSU6111ARSVR.B	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTN

- (1) Status:** For more details on status, see our [product life cycle](#).
- (2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSU6111ARSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSU6111ARSVR	UQFN	RSV	16	3000	202.0	201.0	28.0

GENERIC PACKAGE VIEW

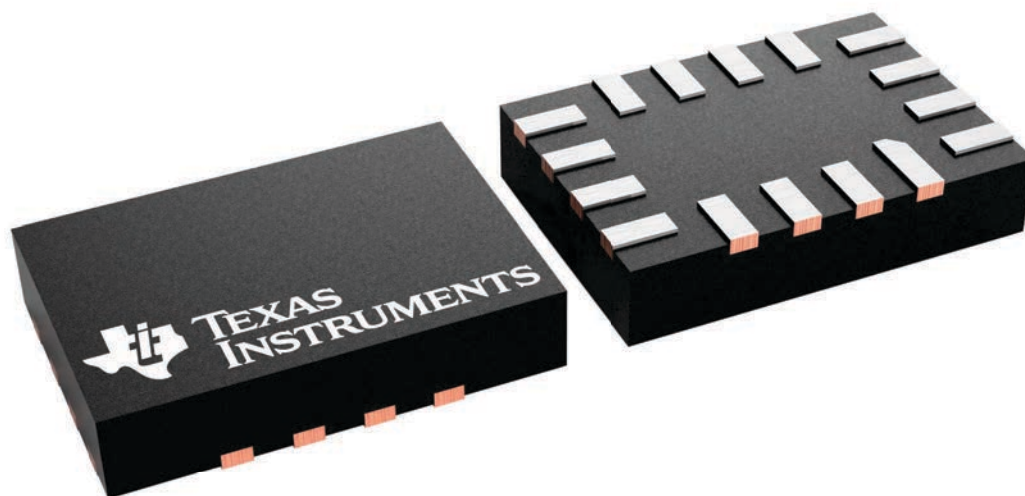
RSV 16

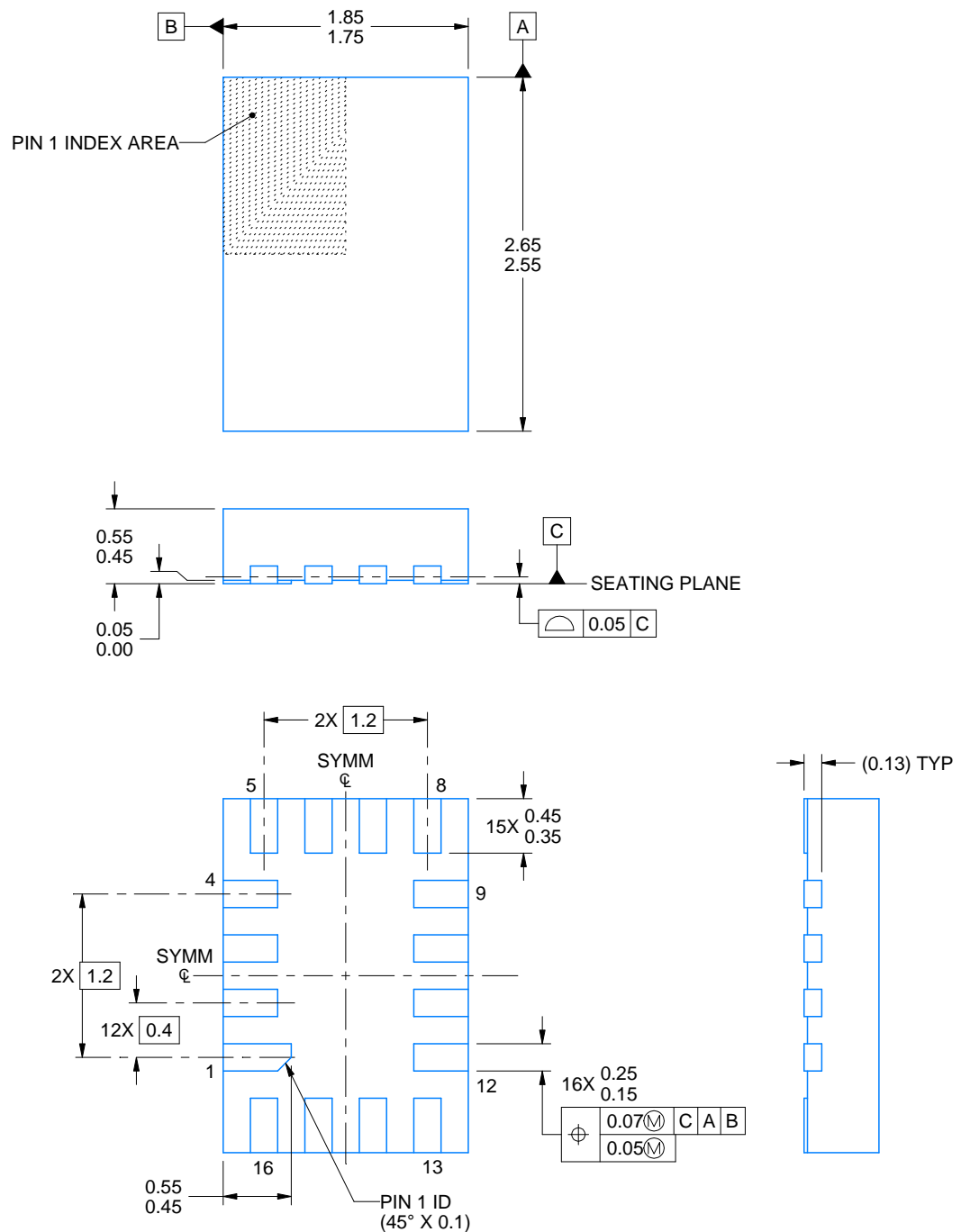
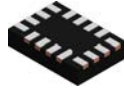
UQFN - 0.55 mm max height

1.8 x 2.6, 0.4 mm pitch

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4220314/C 02/2020

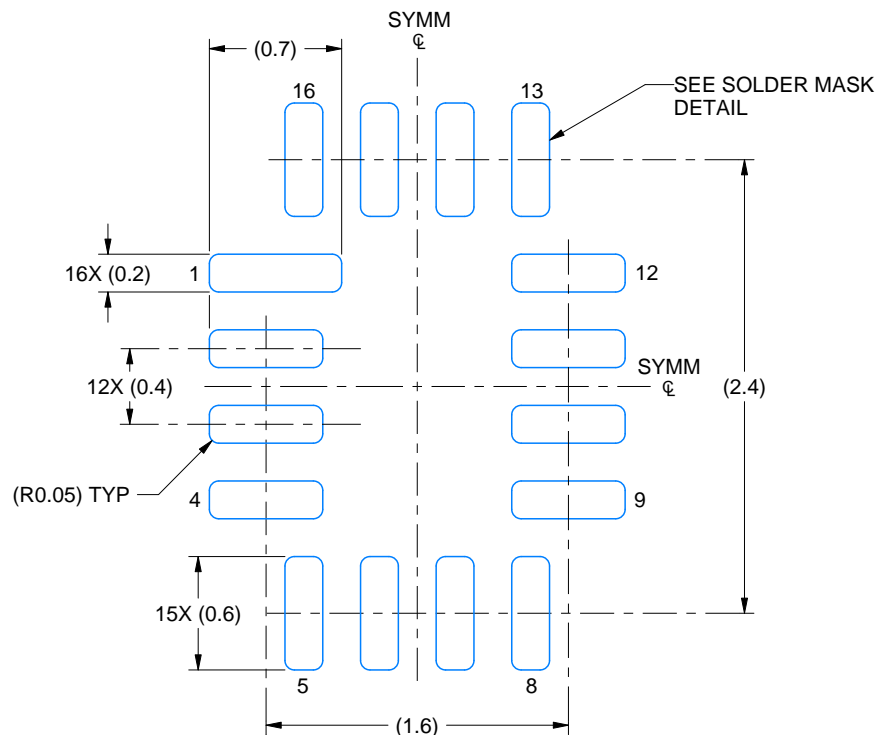
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

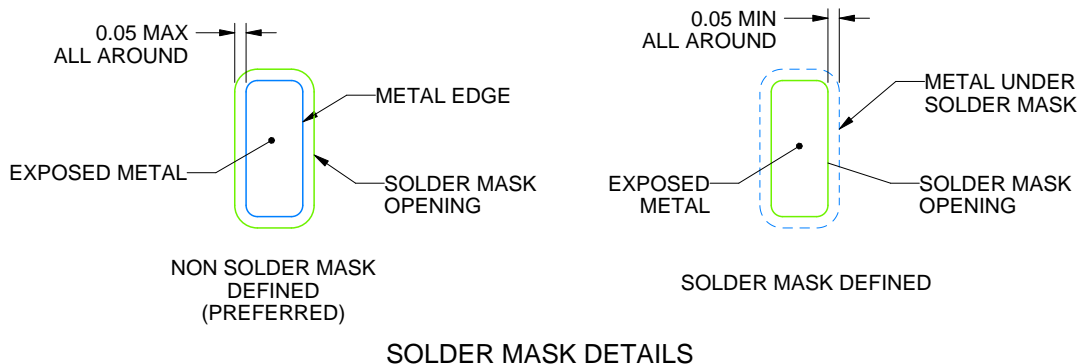
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4220314/C 02/2020

NOTES: (continued)

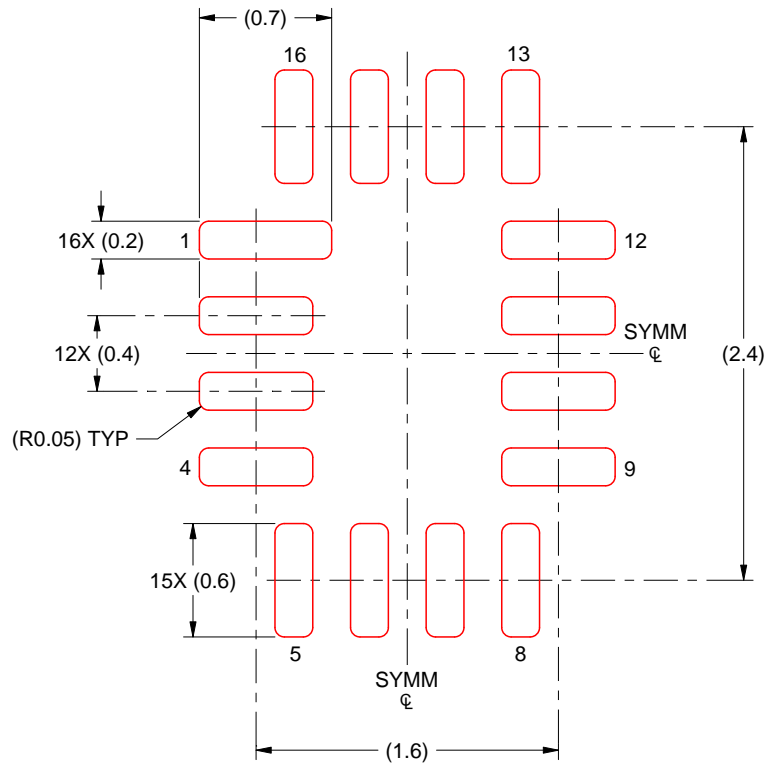
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).

EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司