TS5A3167 0.9Ω 1 通道 1:1 SPST 模拟开关

1 特性

- 断电模式下的隔离，V_{CC} = 0
- 低导通状态电阻 (0.9Ω)
- 控制输入可承受 5.5V 电压
- 低电荷注入
- 低总谐波失真 (THD)
- 1.65V 至 5.5V 单电源运行
- 锁断性能超过 100mA（符合 JESD 78，II 类规范的要求）
- 静电放电 (ESD) 性能测试符合 JESD 22 规范
  - 2000V 人体放电模式（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

2 应用

- 手机
- 掌上电脑 (PDA)
- 便携式仪表
- 音频和视频信号路由
- 低压数据采集系统
- 通信电路
- 调制解调器
- 硬盘
- 计算机外设
- 无线终端和外设
- 麦克风开关 – 笔记本电脑扩展坞

3 说明

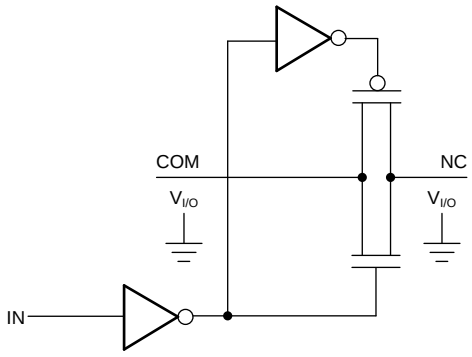
TS5A3167 是一款工作电压范围为 1.65V 至 5.5V 的双向、单通道、单刀双掷 (SPDT) 模拟开关。TS5A3167 器件具有较低的导通状态电阻。该器件具有出色的总谐波失真 (THD) 性能和极低的功耗。这些 特性 再加上低功耗性能，使得这款器件适合于便携式音频 应用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS5A3167	SOT-23	2.90mm x 1.60mm
	SC70	2.00mm x 1.25mm
	DSBGA	1.50mm x 0.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简单原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (March 2017) to Revision C **Page**

- 在*器件信息* 表中将 DSBGA 封装尺寸从 1.50mm x 9.00mm 更改成了 1.50mm x 0.90mm ... 1
- Changed the YZP package pinout view From: Top View To: Bottom View ... 3

Changes from Revision A (October 2012) to Revision B **Page**

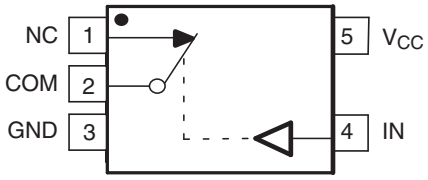
- 添加了*器件信息* 表、*引脚配置和功能*、*ESD 额定值*、*建议运行条件*、*热性能信息*、*详细 说明*、*特性 说明*、*器件功能模式*、*应用和实施*、*电源建议*、*布局*、*器件和文档支持* ... 1
- 删除了*订购信息* 表 ... 1

Changes from Original (February 2005) to Revision A **Page**

- 更新了 *订购信息* 表 ... 1

5 Pin Configuration and Functions

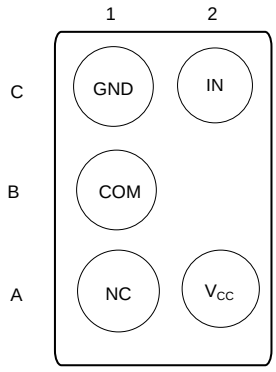
DBV or DCK Package
5- Pin (SOT-23 or SC70)
Top View



Pin Functions

PIN NUMBER	NAME	DESCRIPTION
1	NC	Normally Closed
2	COM	Common
3	GND	Ground
4	IN	Digital control pin, COM connected to NC when logic low
5	V_{CC}	Power Supply

YZP Package
5-Pin (DSBGA)
Bottom View



Pin Functions

PIN NUMBER	NAME	DESCRIPTION
A1	NC	Normally Closed
B1	COM	Common
C1	GND	Ground
A2	V_{CC}	Power Supply
C2	IN	Digital control pin, COM connected to NC when logic low

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(3)		–0.5	6.5	V
V_{NC} V_{COM}	Analog voltage range(3)(4)(5)		–0.5	V_{CC} + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{COM} < 0	–50		mA
I_{NC} I_{COM}	On-state switch current	V_{NC}, V_{COM} = 0 to V_{CC}	–200	200	mA
	On-state peak switch current(6)		–400	400	
V_I	Digital input voltage range(3)(4)		–0.5	6.5	V
I_{IK}	Digital clamp current	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	1.65	5.5	V
V_{NC} V_{COM}	Analog voltage range	0	V_{CC}	V
V_I	Digital input voltage range	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC(1)		TS5A3167			UNIT
		DBV (SOT-23)	DCK (SOT-23)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	230.3	268.0	146.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	111.9	171.8	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.5	64.5	39.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	33.0	40.5	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.0	62.9	39.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 5-V Supply(1)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	$0 \le V_{NC} \le V_{CC}$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.8	1.1	Ω
				Full				1.2	
ON-state resistance	r_{on}	V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.75	0.9	Ω
				Full				1	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NC} \le V_{CC}$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.2		Ω
		V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,		25°C			0.15	0.25	
				Full				0.25	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 4.5 V, or V_{NC} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	0	4	20	nA
				Full		–150		150	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,		25°C	0 V	–10	0.2	10	µA
				Full		–50		50	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 4.5 V, or V_{COM} = 4.5 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	0	4	20	nA
				Full		–150		150	
	$I_{COM(PWROFF)}$	V_{COM} = 5.5 V to 0, V_{NC} = 0 to 5.5 V,		25°C	0 V	–10	0.2	10	µA
				Full		–50		50	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–5	0.4	5	nA
				Full		–50		50	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 4.5 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–5	0.4	5	nA
				Full		–20		20	
Digital Control Inputs (IN)									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.6 Electrical Characteristics for 5-V Supply(1) (continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	VCC	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	1	4.5	7.5	ns
				Full	4.5 V to 5.5 V	1		9	
Turn-off time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	4.5	8	11	ns
				Full	4.5 V to 5.5 V	3.5		13	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0 ,	C_L = 1 nF, See Figure 20	25°C	5 V		6		pC
NC OFF capacitance	$C_{NC(OFF)}$	V_{NC} = V_{CC} or GND,	Switch OFF, See Figure 16	25°C	5 V		19		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND,	Switch OFF, See Figure 16	25°C	5 V		18		pF
NC ON capacitance	$C_{NC(ON)}$	V_{NC} = V_{CC} or GND,	Switch ON, See Figure 16	25°C	5 V		35.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND,	Switch ON, See Figure 16	25°C	5 V		35.5		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 16	25°C	5 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 18	25°C	5 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	5 V		–62		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 21	25°C	5 V		0.005%		
Supply									
Positive supply current	I_{CC}	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	µA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.7 Electrical Characteristics for 3.3-V Supply(1)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		1.3	1.6	Ω
				Full				1.8	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		1.1	1.5	Ω
				Full				1.7	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		0.3		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			0.15	0.25	
				Full				0.25	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–5	0.5	5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–5	0.1	5	µA
				Full		–25		25	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–5	0.5	5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 3.6 V to 0, V_{NC} = 0 to 3.6 V,		25°C	0 V	–5	0.1	5	µA
				Full		–25		25	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.8 Electrical Characteristics for 3.3-V Supply(1) (continued)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	VCC	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	1.5	5	9.5	ns
				Full	3 V to 3.6 V	1.0		10	
Turn-off time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	4.5	8.5	11	ns
				Full	3 V to 3.6 V	3		12.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 20	25°C	3.3 V		6		pC
NC OFF capacitance	$C_{NC(OFF)}$	V_{NC} = V_{CC} or GND,	Switch OFF, See Figure 16	25°C	3.3 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND,	Switch OFF, See Figure 16	25°C	3.3 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	V_{NC} = V_{CC} or GND,	Switch ON, See Figure 16	25°C	3.3 V		36		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND,	Switch ON, See Figure 16	25°C	3.3 V		36		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 16	25°C	3.3 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 18	25°C	3.3 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	3.3 V		–62		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 21	25°C	3.3 V		0.01%		
Supply									
Positive supply current	I_{CC}	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	3.6 V		0.001	0.05	µA
				Full				0.3	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.9 Electrical Characteristics for 2.5-V Supply(1)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.8	2.4	Ω
				Full				2.6	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.2	2.1	Ω
				Full				2.4	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.7		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			0.4	0.6	
				Full				0.6	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–2	0.05	2	µA
				Full		–15		15	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 3.6 V to 0, V_{NC} = 0 to 3.6 V,		25°C	0 V	–2	0.05	2	µA
				Full		–15		15	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN)									
Input logic high	V_{IH}			Full		1.8		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.10 Electrical Characteristics for 2.5-V Supply(1) (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	VCC	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
Turn-off time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	4.5	8	10.5	ns
				Full	2.3 V to 2.7 V	3		15	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 20	25°C	2.5 V		4		pC
NC OFF capacitance	$C_{NC(OFF)}$	V_{NC} = V_{CC} or GND,	Switch OFF, See Figure 16	25°C	2.5 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND,	Switch OFF, See Figure 16	25°C	2.5 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	V_{NC} = V_{CC} or GND,	Switch ON, See Figure 16	25°C	2.5 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND,	Switch ON, See Figure 16	25°C	2.5 V		36.5		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 16	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 18	25°C	2.5 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		–62		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 21	25°C	2.5 V		0.02%		
Supply									
Positive supply current	I_{CC}	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.02	µA
				Full				0.25	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.11 Electrical Characteristics for 1.8-V Supply(1)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		4.2	25	Ω
				Full				30	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		1.6	3.9	Ω
				Full				4.0	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		2.8		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			4.1	22	
				Full				27	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–2		2	µA
				Full		–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NC} = 3.6 V to 0,		25°C	0 V	–2		2	µA
				Full		–10		10	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
Digital Control Inputs (IN)									
Input logic high	V_{IH}			Full		1.5		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.12 Electrical Characteristics for 1.8-V Supply(1) (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	VCC	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
Turn-off time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 20	25°C	1.8 V		2		pC
NC OFF capacitance	$C_{NC(OFF)}$	V_{NC} = V_{CC} or GND,	Switch OFF, See Figure 16	25°C	1.8 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND,	Switch OFF, See Figure 16	25°C	1.8 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	V_{NC} = V_{CC} or GND,	Switch ON, See Figure 16	25°C	1.8 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND,	Switch ON, See Figure 16	25°C	1.8 V		36.5		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 16	25°C	1.8 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 18	25°C	1.8 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	1.8 V		–62		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz See Figure 21	25°C	1.8 V		0.055%		
Supply									
Positive supply current	I_{CC}	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.01	µA
				Full				0.15	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.13 Typical Performance

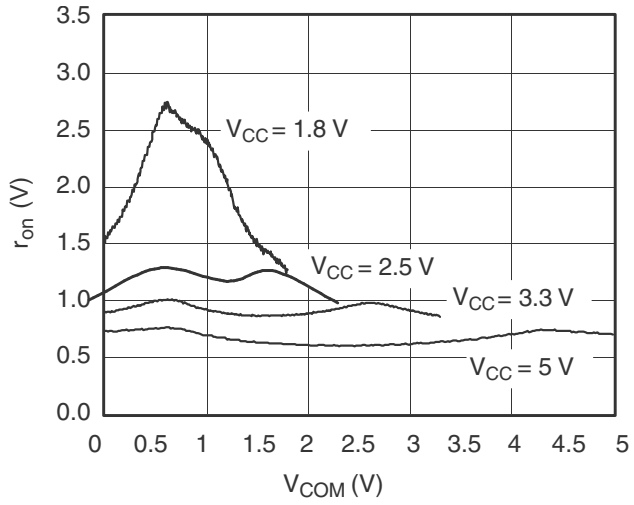


Figure 1. r_{on} vs V_{COM}

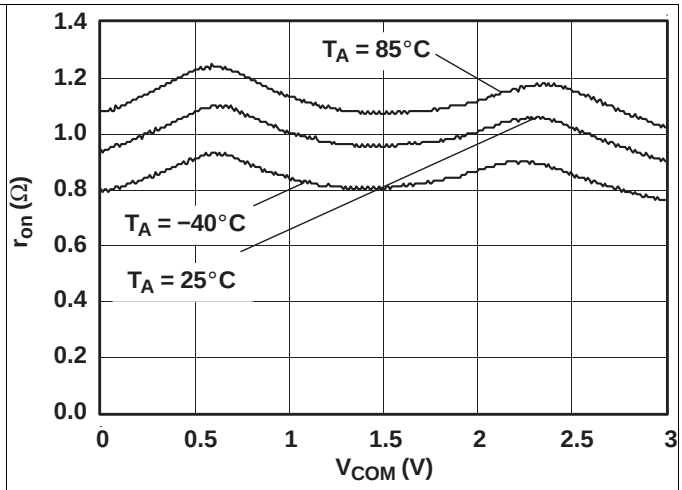


Figure 2. r_{on} vs V_{COM} (V_{CC} = 3 V)

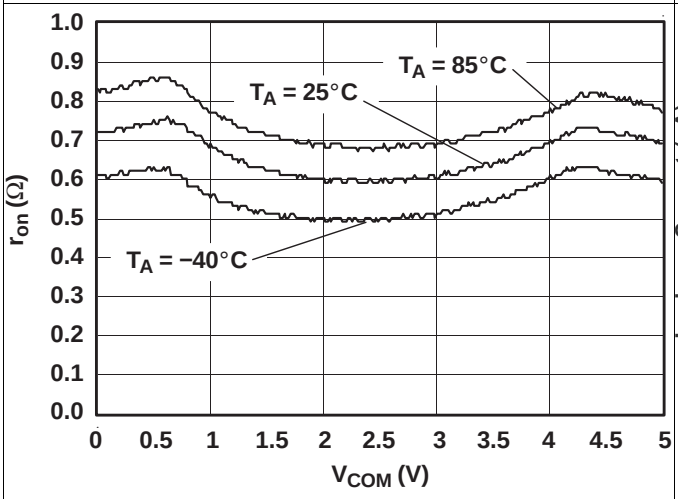


Figure 3. r_{on} vs V_{COM} (V_{CC} = 5 V)

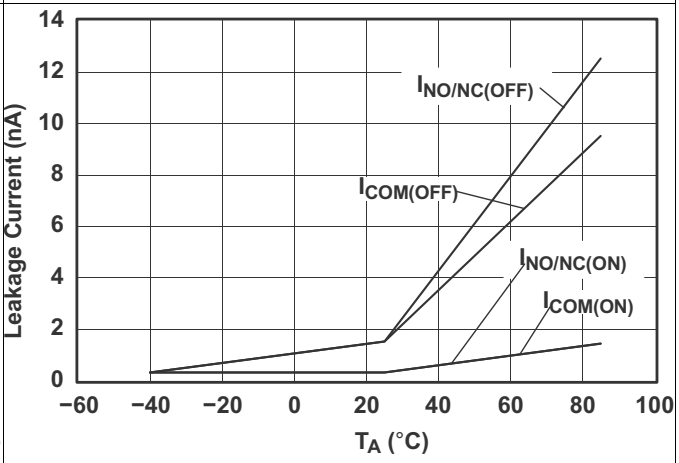


Figure 4. Leakage Current vs Temperature (V_{CC} = 5.5 V)

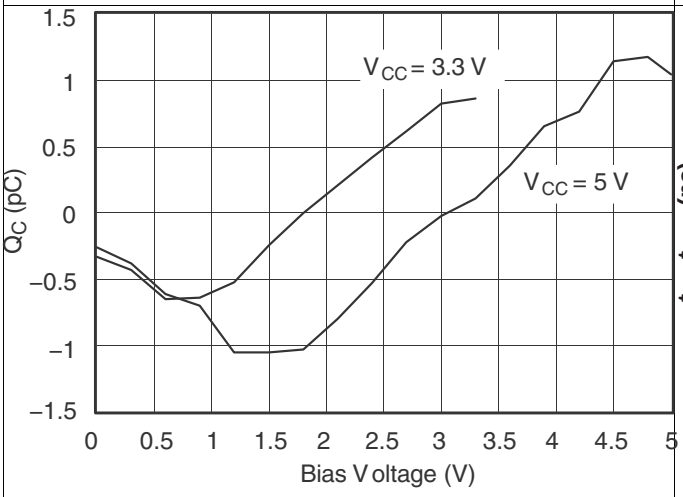


Figure 5. Charge Injection (Q_C) vs V_{COM}

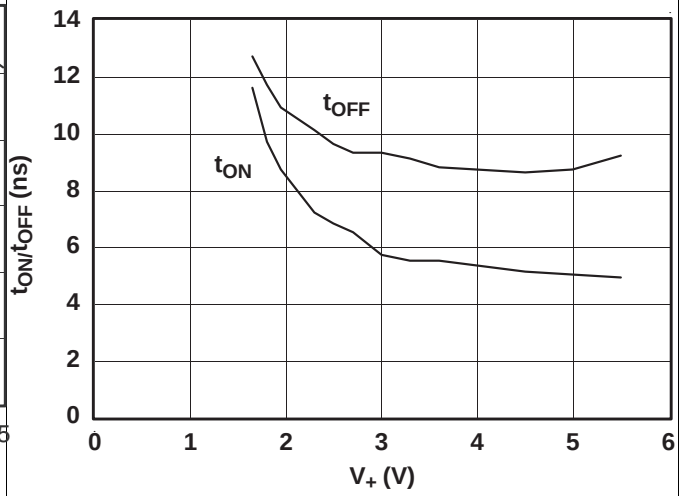


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Performance (continued)

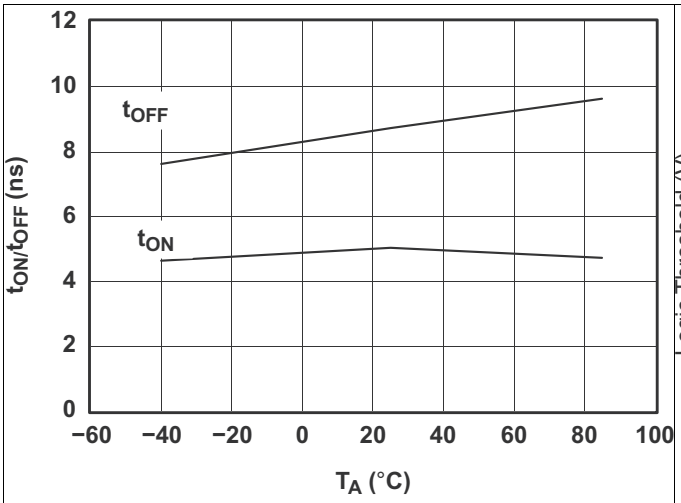


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_{CC} = 5 V)

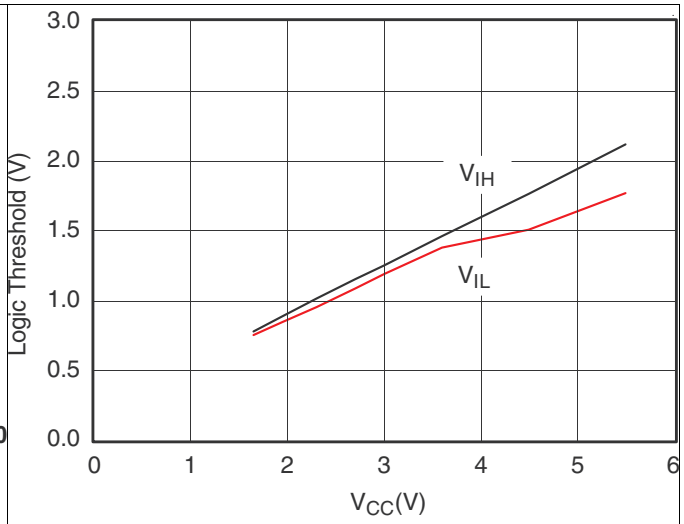


Figure 8. Logic Threshold vs V_{CC}

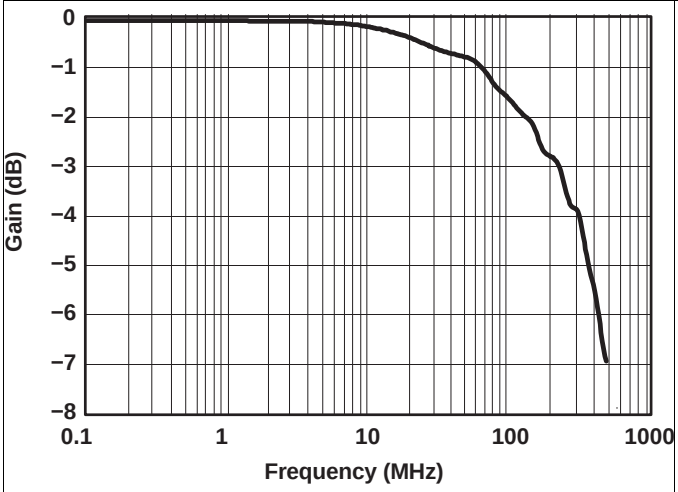


Figure 9. Gain vs Frequency (V_{CC} = 5 V)

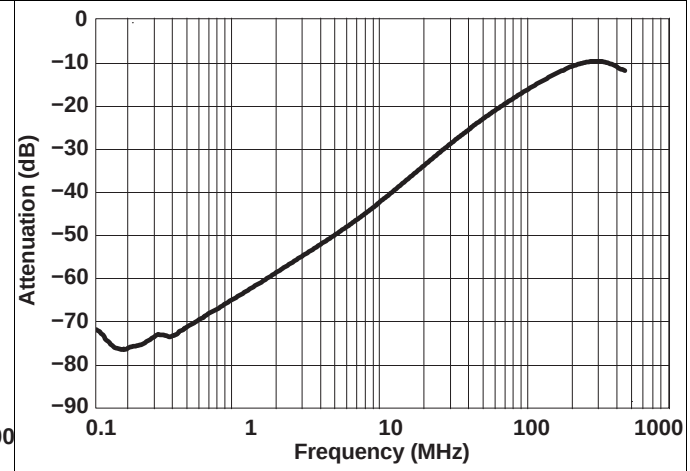


Figure 10. OFF Isolation vs Frequency (V_{CC} = 5 V)

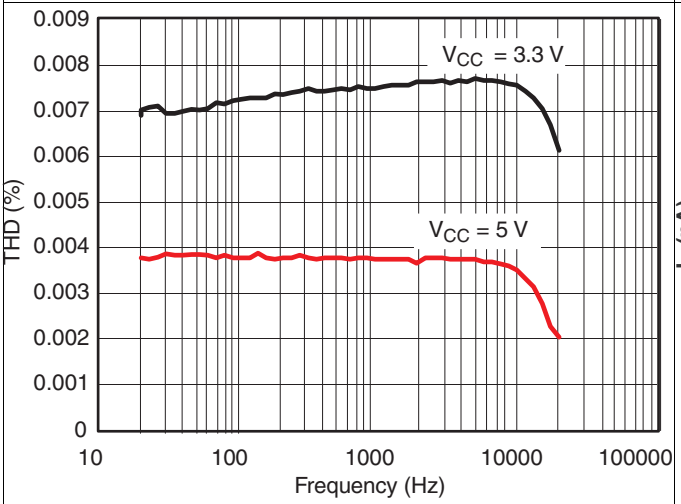


Figure 11. Total Harmonic Distortion vs Frequency (V_{CC} = 5 V)

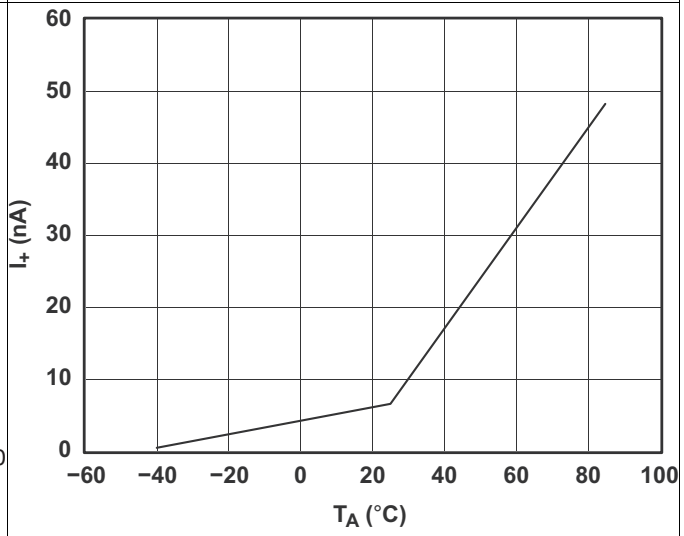


Figure 12. Power-Supply Current vs Temperature (V_{CC} = 5 V)

7 Parameter Measurement Information

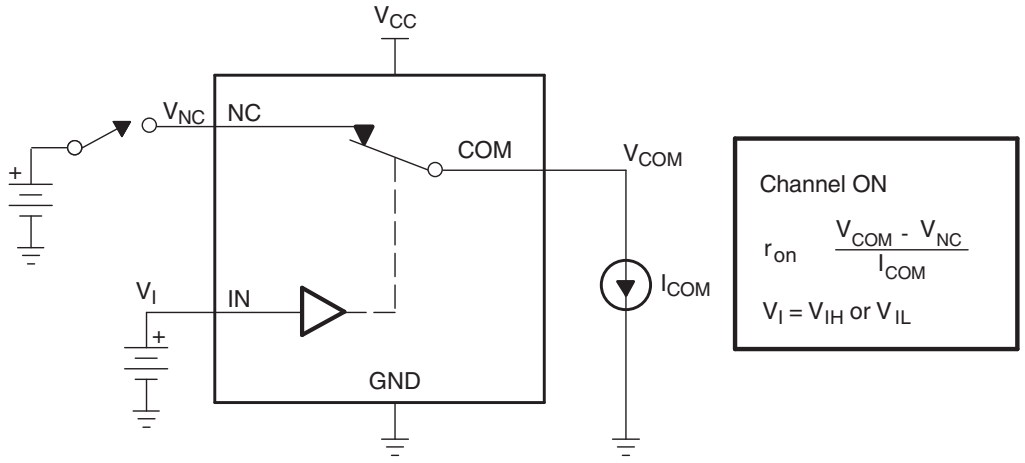


Figure 13. ON-State Resistance (r_{on})

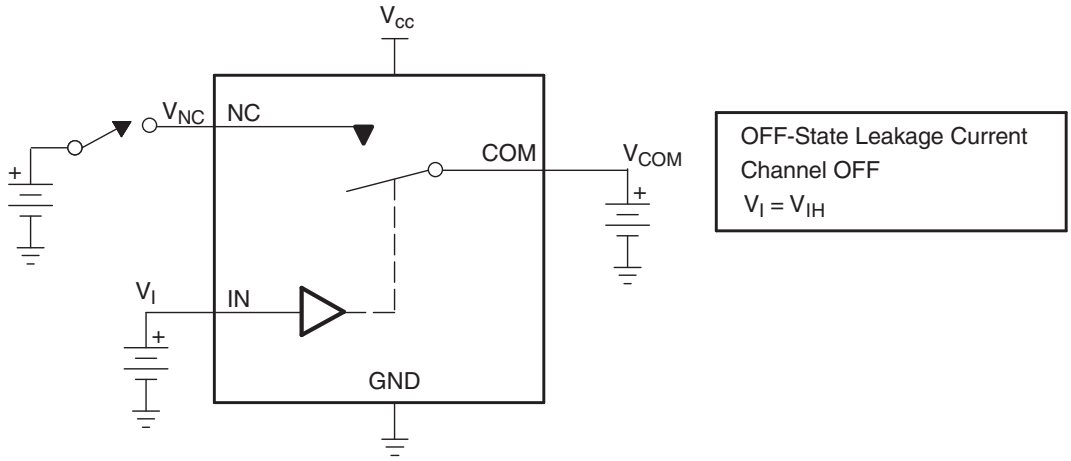


Figure 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWROFF)}$)

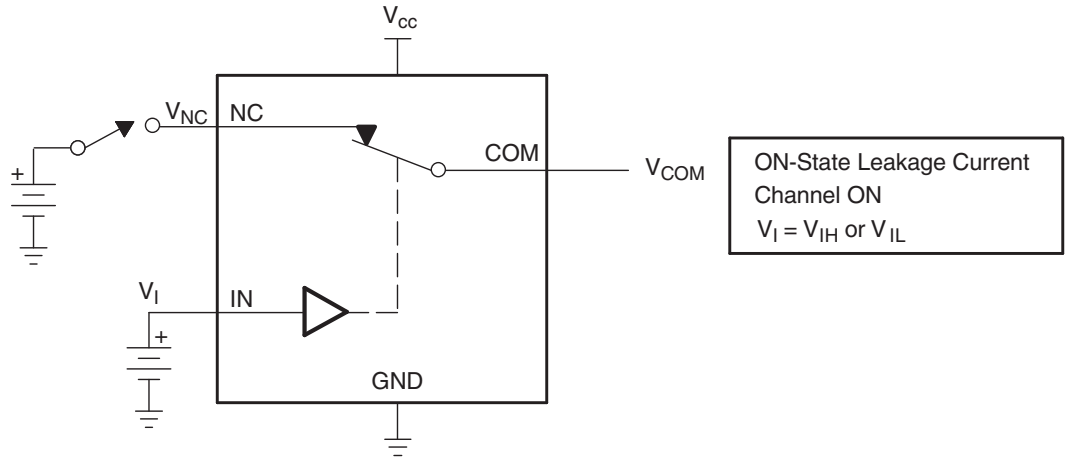


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

Parameter Measurement Information (continued)

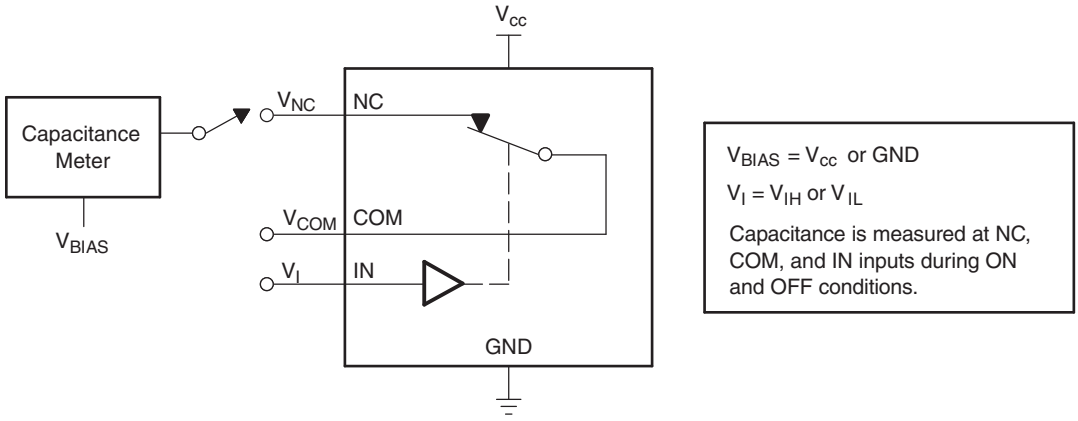
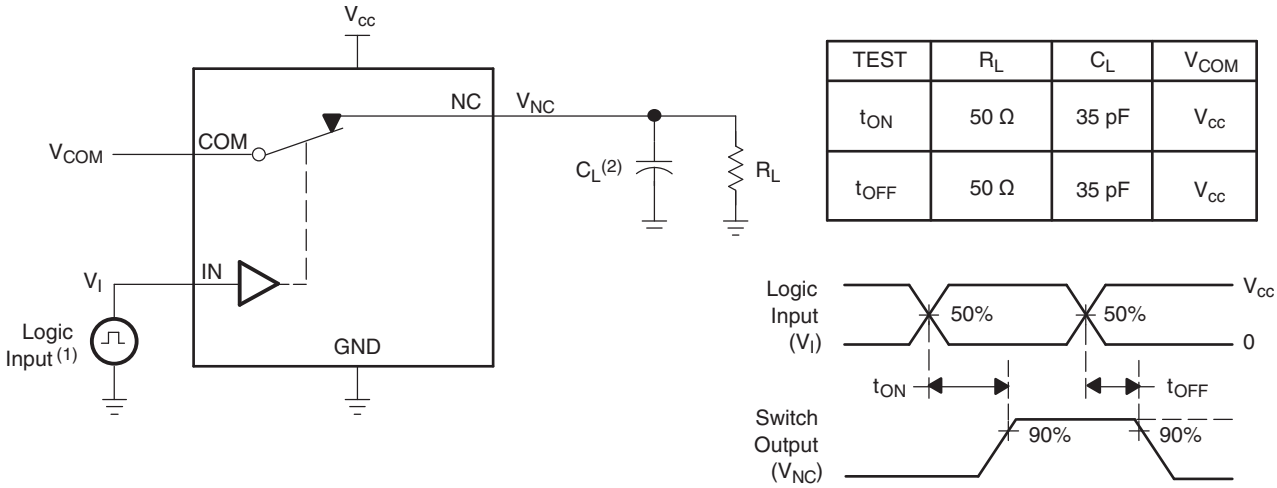


Figure 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{cc}
t_{OFF}	50 Ω	35 pF	V_{cc}

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

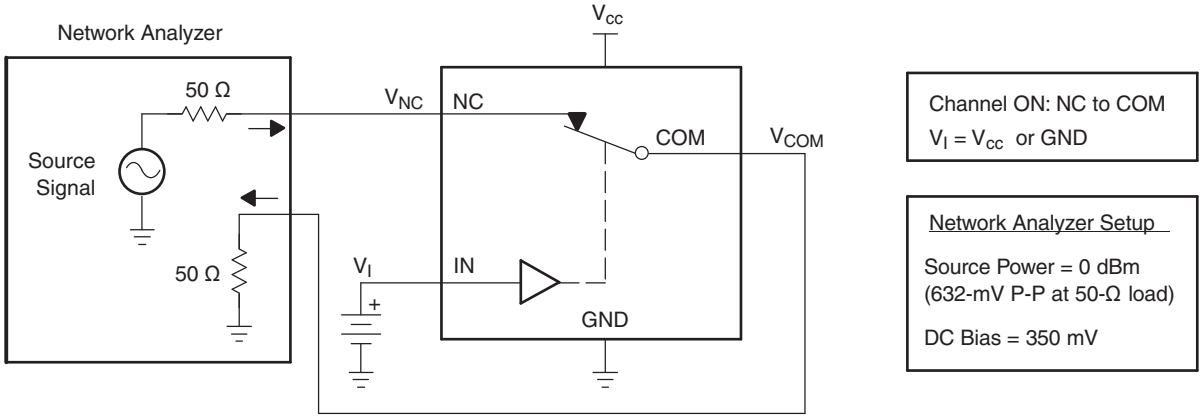


Figure 18. Bandwidth (BW)

Parameter Measurement Information (continued)

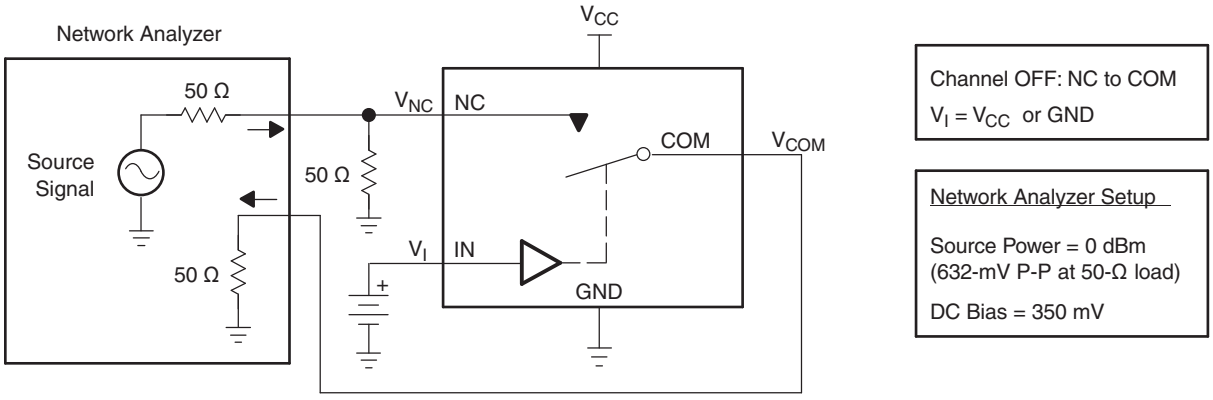
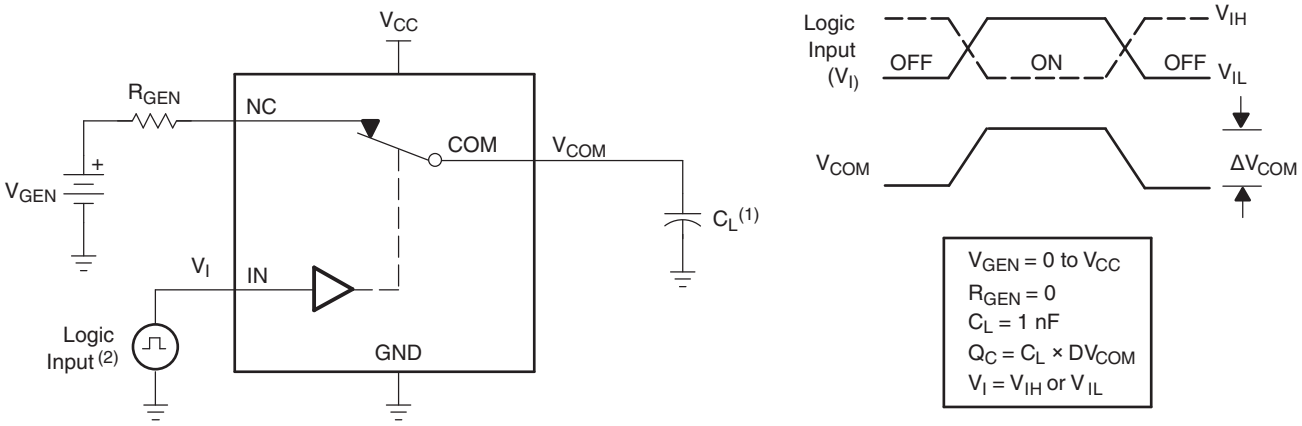


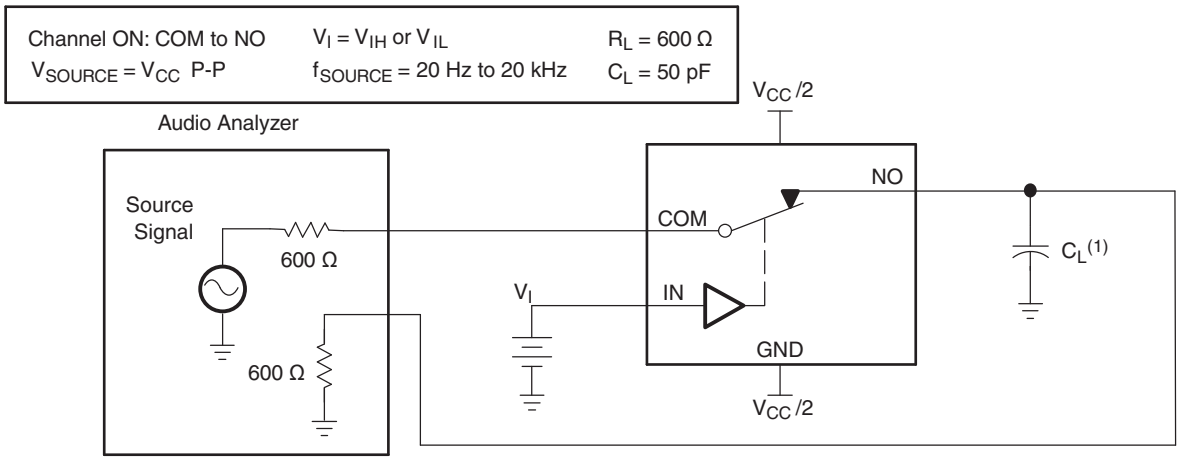
Figure 19. OFF Isolation (O_{ISO})



(1) C_L includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 20. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

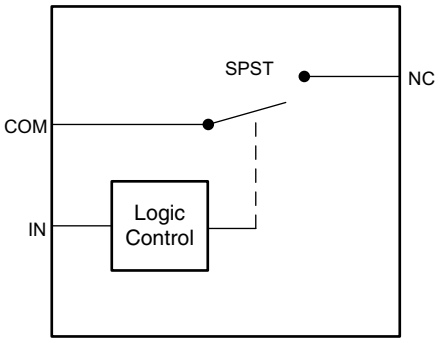
Figure 21. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A3167 is a bidirectional, single-channel, single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3367 suitable for a wide range of applications in various markets including personal electronics, portable instrumentation, and test and measurement equipment. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. The device consumes very low power and provides isolation when VCC = 0.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Isolation in Powered-Off Mode, V_{CC} = 0

When power is not supplied to the V_{CC} pin, V_{CC} = 0 , the signal paths NC and COM are high impedance. This is specificed in the electrical characterisitics table under the COM and NC OFF leakage current when V_{CC} = 0. Because the device is high impedance when it is not powered, you may connect other signals to the signal chain without interference of the TS5A3167.

8.4 Device Functional Modes

Placing a logic low signal on the IN pin of the device will turn on the switch and provide a low impedance path from NC to COM.

Table 1. Function Table

IN	NC TO COM, COM TO NC
L	ON
H	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3167 switch is bidirectional, so the NC and COM pins can be used as either inputs or outputs. This switch is typically used when there is one signal path that needs to be isolated at certian times.

9.2 Typical Application

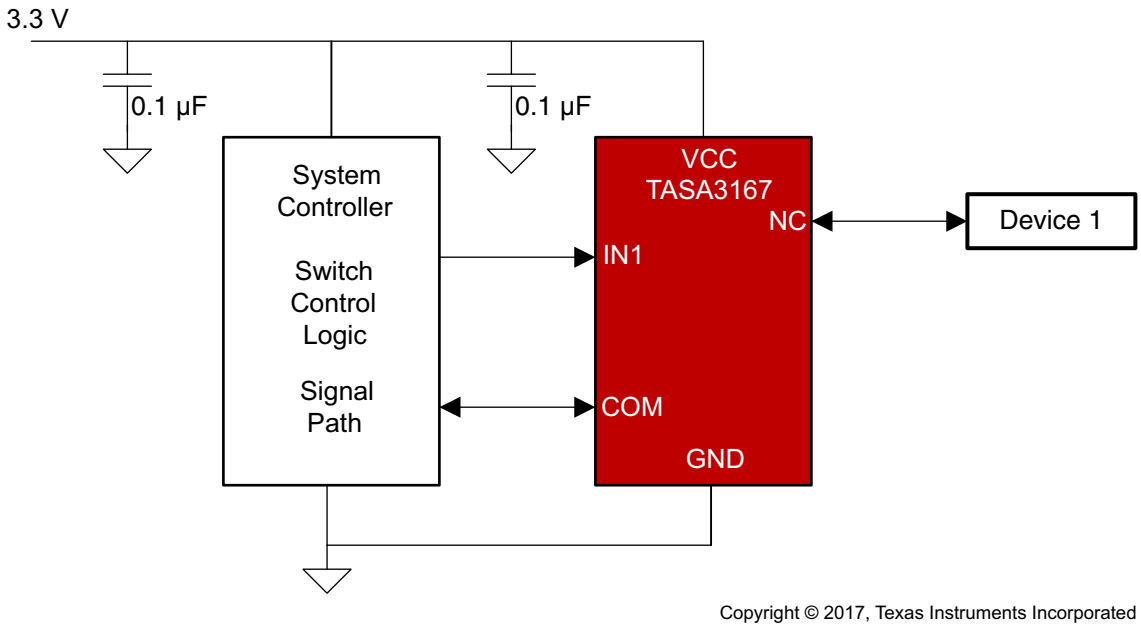


Figure 22. Typical Application

9.2.1 Design Requirements

The TS5A3167 device can be properly operated without any external components.

Unused pin may be left floating or connected to ground.

TI recommends pulling up the digital control pin (IN) to V_{CC} or pulling down to GND to avoid undesired switch positions that could result from the floating pin. A floating digital pin could cause excess current consumption refer to *Implications of Slow or Floating CMOS Inputs*.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3167 input and output signal swing through NC and COM are dependent on the supply voltage V_{CC}. For example, if the desired signal level to pass through the switch is 5 V, V_{CC} must be greater than or equal to 5 V. V_{CC} = 3.3 V would not be valid for passing a 5-V signal since the analog signal voltage cannot exceed the supply.

Typical Application (continued)

9.2.3 Application Curves

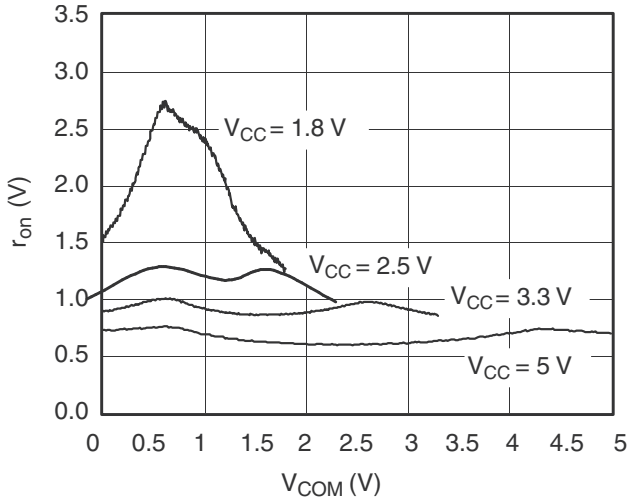


Figure 23. r_{on} vs V_{COM}

10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. It is recommended that V_{CC} is powered on first, followed by NC or COM but not required because of the Isolation in Powered-Off Mode, V_{CC} = 0 feature.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1-μF capacitor, connected from V_{CC} to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example

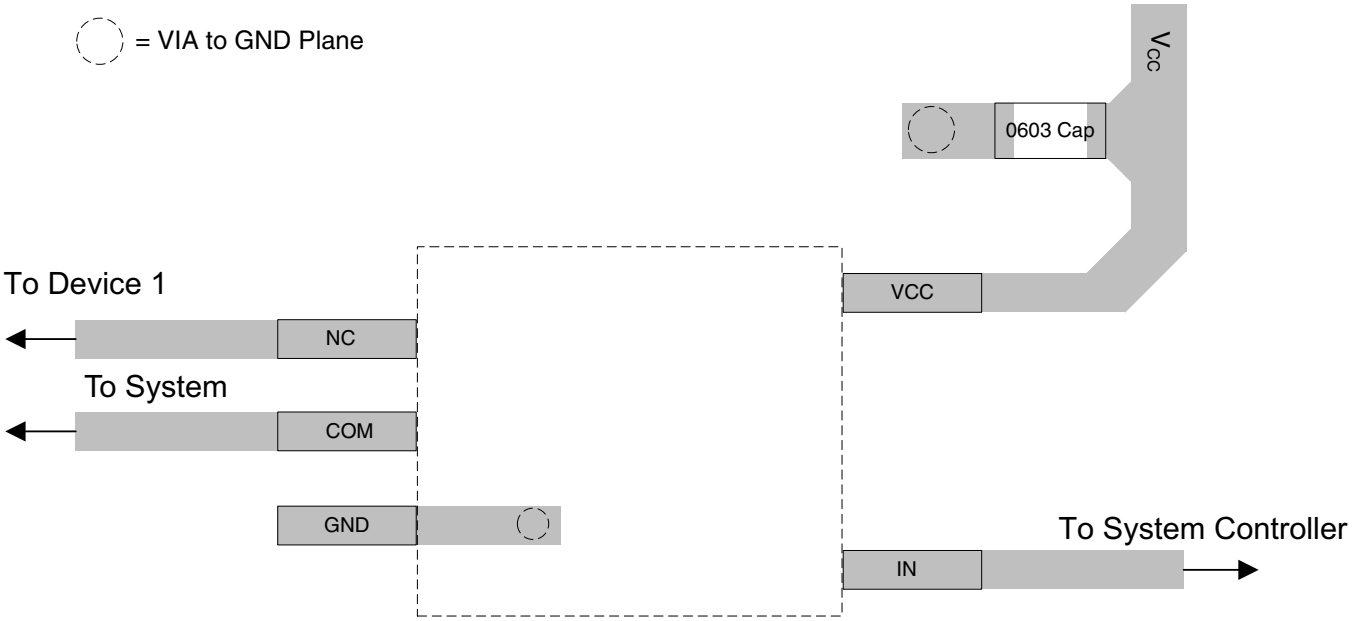


Figure 24. Example Layout

12 器件和文档支持

12.1 文档支持

表 2. 参数 说明

符号	说明
V_{COM}	COM 处的电压。
V_{NC}	NC 处的电压。
r_{on}	通道导通时 COM 和 NC 端口之间的电阻。
r_{peak}	额定电压范围的通态电阻峰值。
$r_{on(flat)}$	额定条件范围下，同一通道内 r_{on} 最大值与最小值之间的差值。
$I_{NC(OFF)}$	相应通道（NC 到 COM）处于关断状态时，在 NC 端口测得的泄漏电流（在最坏输入和输出条件下）。
$I_{NC(PWROFF)}$	在电源关闭状态下，V_{CC} = 0 时，在 NC 端口测得的泄漏电流。
$I_{COM(OFF)}$	在最坏的输入和输出条件下，相应通道（COM 到 NC）处于关断状态时，在 COM 端口测得的泄漏电流。
$I_{COM(PWROFF)}$	在电源关闭状态下，V_{CC} = 0 时，在 COM 端口测得的泄漏电流。
$I_{NC(ON)}$	相应通道（NC 到 COM）处于导通状态且输出 (COM) 处于开路状态时，在 NC 端口测得的泄漏电流。
$I_{COM(ON)}$	相应通道（COM 到 NC）处于导通状态且输出 (NC) 处于开路状态时，在 COM 端口测得的泄漏电流。
V_{IH}	控制输入 (IN) 逻辑高电平的最小输入电压。
V_{IL}	控制输入 (IN) 逻辑低电平的最大输入电压。
V_I	控制输入 (IN) 处的电压。
I_{IH}、I_{IL}	控制输入 (IN) 处测量的泄漏电流。
t_{ON}	开关导通时间。此参数是在特定条件范围下，开关导通时，通过数字控制 (IN) 信号和模拟输出（COM 或 NC）信号之间的传播延迟测得的。
t_{OFF}	开关关断时间。此参数是在特定条件范围下，开关关断时，通过数字控制 (IN) 信号和模拟输出（COM 或 NC）信号之间的传播延迟测得的。
Q_C	电荷注入是测量从控制 (IN) 输入到模拟（NC 或 COM）输出产生的不需要的信号耦合的方法。电荷注入以库仑 (C) 为单位，可通过测量开关控制输入产生的总感应电荷得出该值。电荷注入，$Q_C = C_L \times \Delta V_{COM}$，$C_L$ 是负载电容，ΔV_{COM} 是模拟输出电压的变化。
$C_{NC(OFF)}$	相应通道（NC 到 COM）关闭时 NC 端口的电容。
$C_{COM(OFF)}$	相应通道（COM 到 NC）关闭时 COM 端口的电容。
$C_{NC(ON)}$	相应通道（NC 到 COM）开启时 NC 端口的电容。
$C_{COM(ON)}$	相应通道（COM 到 NC）开启时 COM 端口的电容。
C_I	控制输入 (IN) 电容。
O_{ISO}	开关关断隔离用于衡量关断状态开关阻抗的大小。关断隔离以 dB 为单位，当相应通道（NC 到 COM）处于关断状态时，在额定频率下测量得出。
BW	开关带宽。这是导通通道增益低于直流增益 -3dB 时的频率。
THD	总谐波失真用于描述由模拟开关导致的信号失真。其定义为二次、三次和更高次谐波与基波绝对幅度之比的均方根 (RMS) 值。
I_{CC}	控制 (IN) 引脚处于 V_{CC} 或 GND 状态时的静态电源电流。

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

社区资源 **(**接下页**)**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

E2E is a trademark of Texas Instruments.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A3167DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JATF, JATR) (JATH, JATP)
TS5A3167DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JATF, JATR) (JATH, JATP)
TS5A3167DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JG5, JGF, JGR) (JGH, JGP, JGS)
TS5A3167DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JG5, JGF, JGR) (JGH, JGP, JGS)
TS5A3167DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JG5, JGF, JGR) (JGH, JGP, JGS)
TS5A3167DCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JG5, JGF, JGR) (JGH, JGP, JGS)
TS5A3167YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JGN
TS5A3167YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JGN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

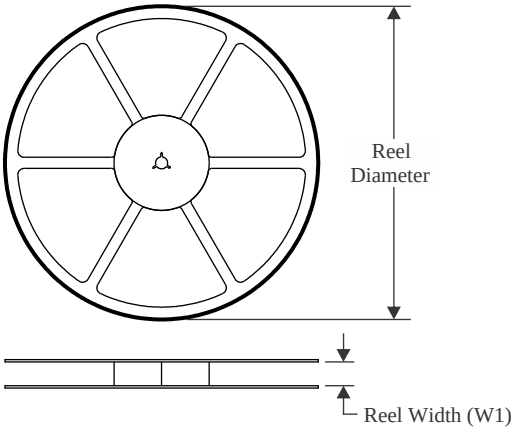
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

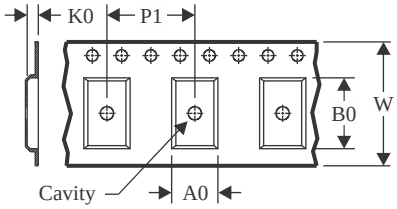
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

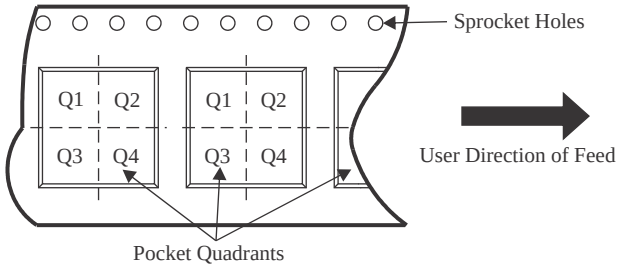


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

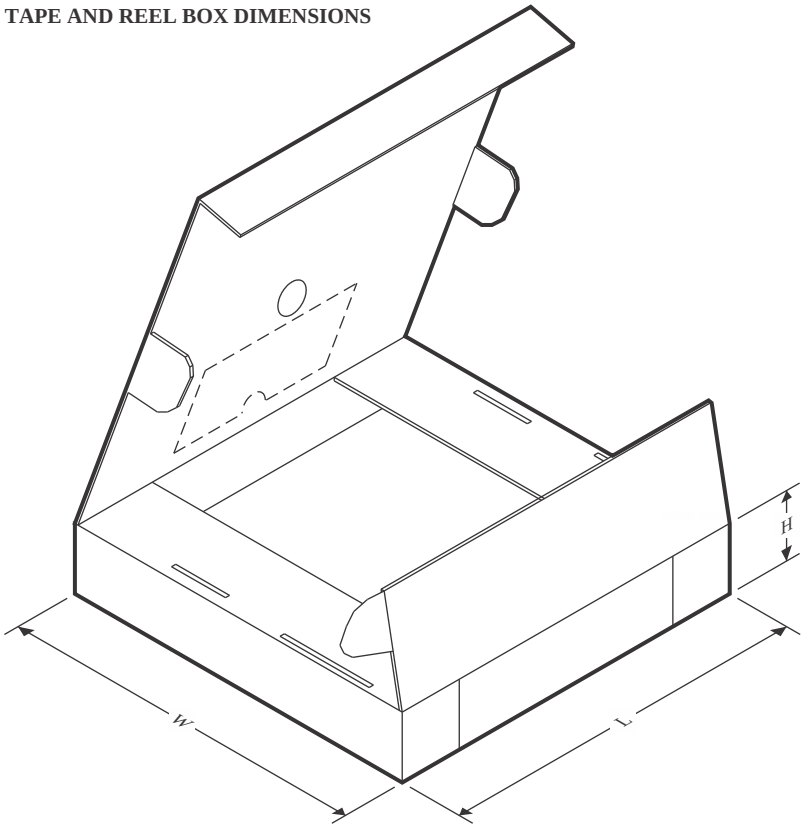
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3167DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3167DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TS5A3167DCKRG4	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TS5A3167YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

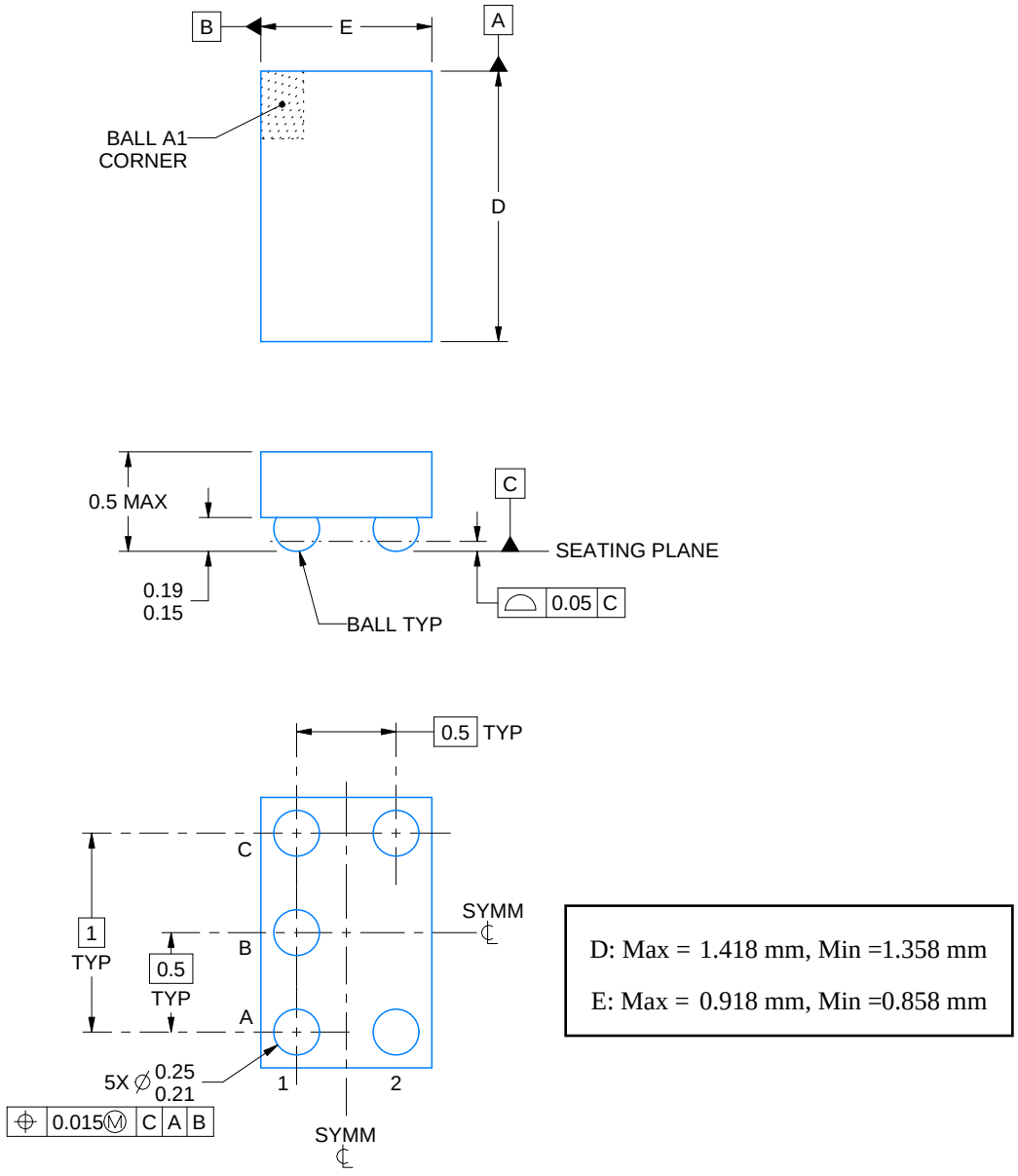
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3167DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A3167DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TS5A3167DCKRG4	SC70	DCK	5	3000	202.0	201.0	28.0
TS5A3167YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



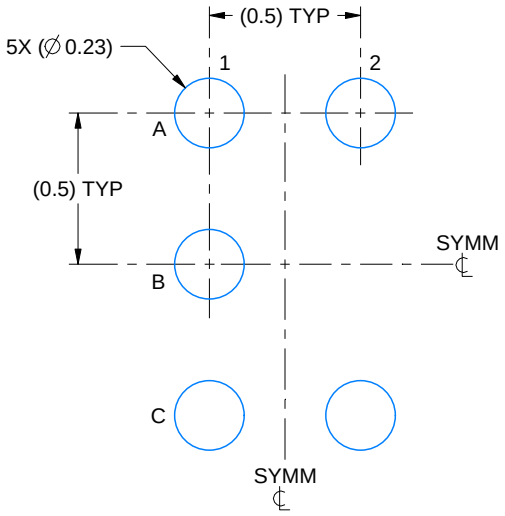
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

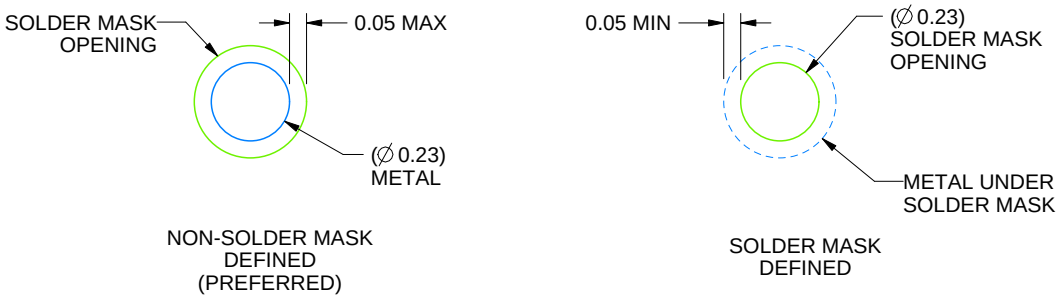
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

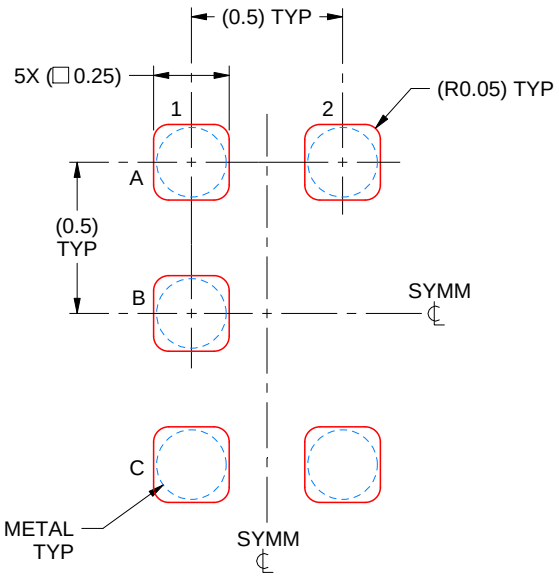


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

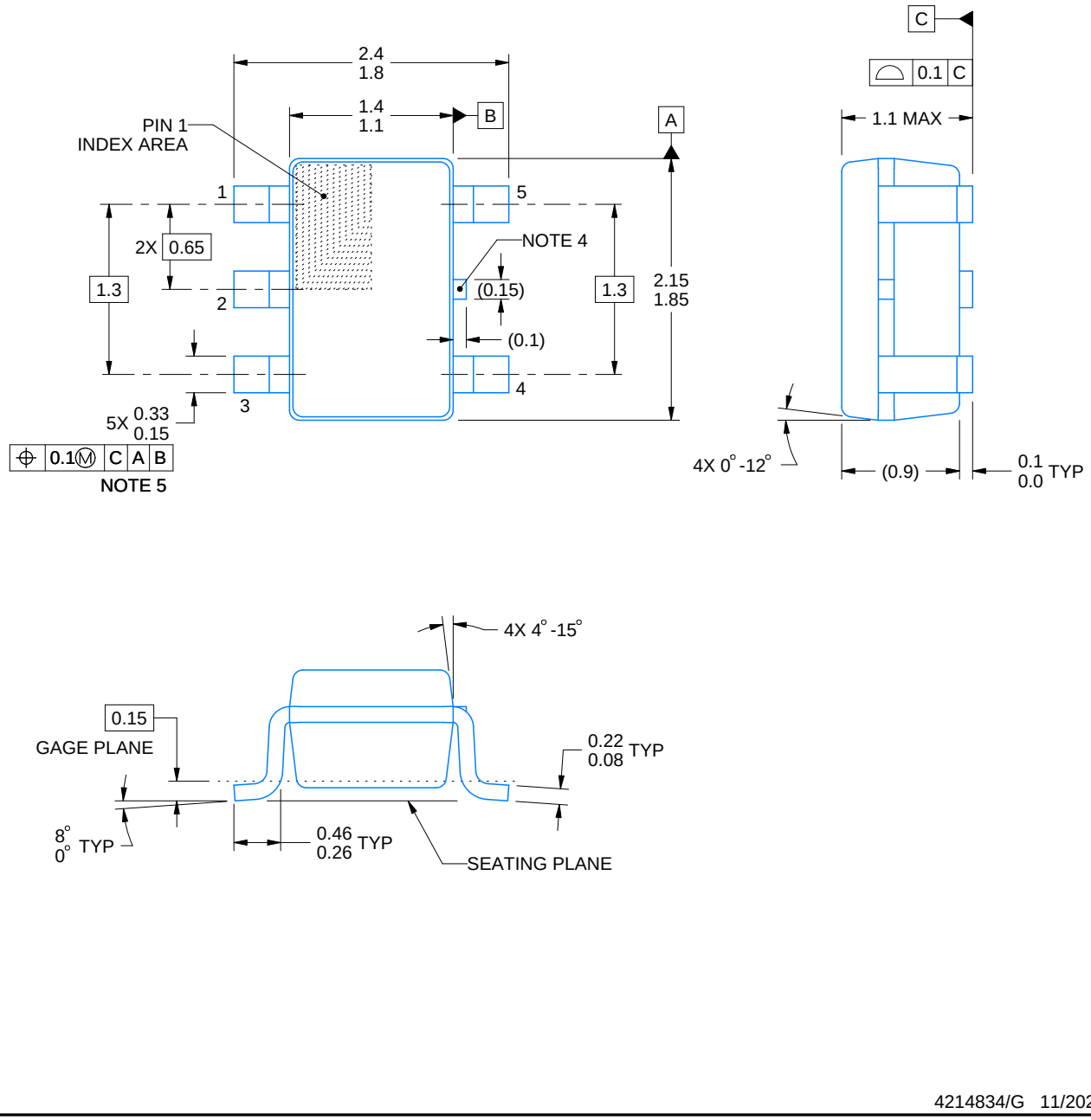
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

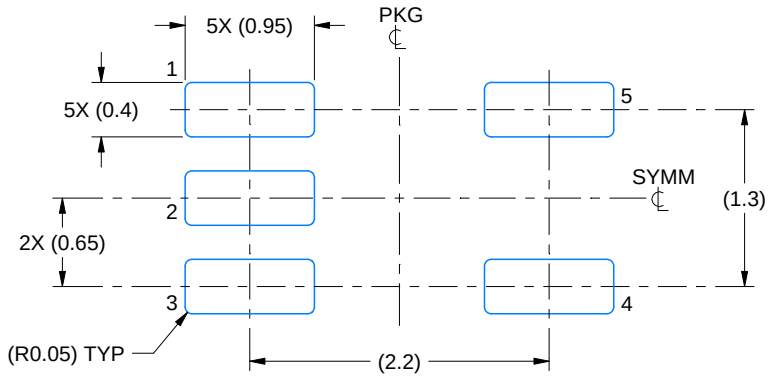
SMALL OUTLINE TRANSISTOR



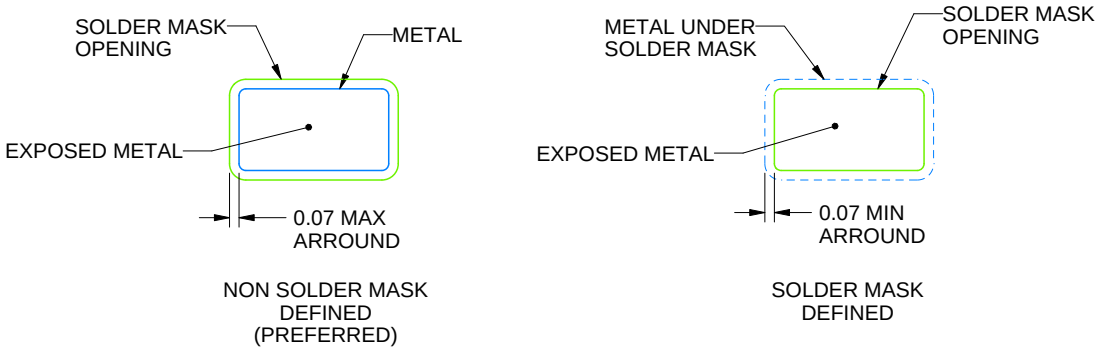
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

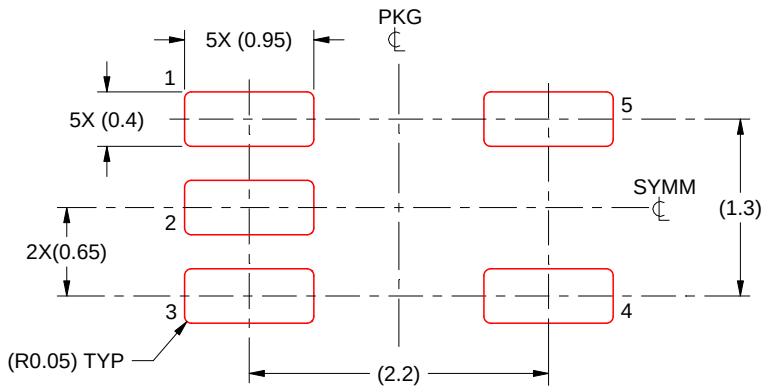


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

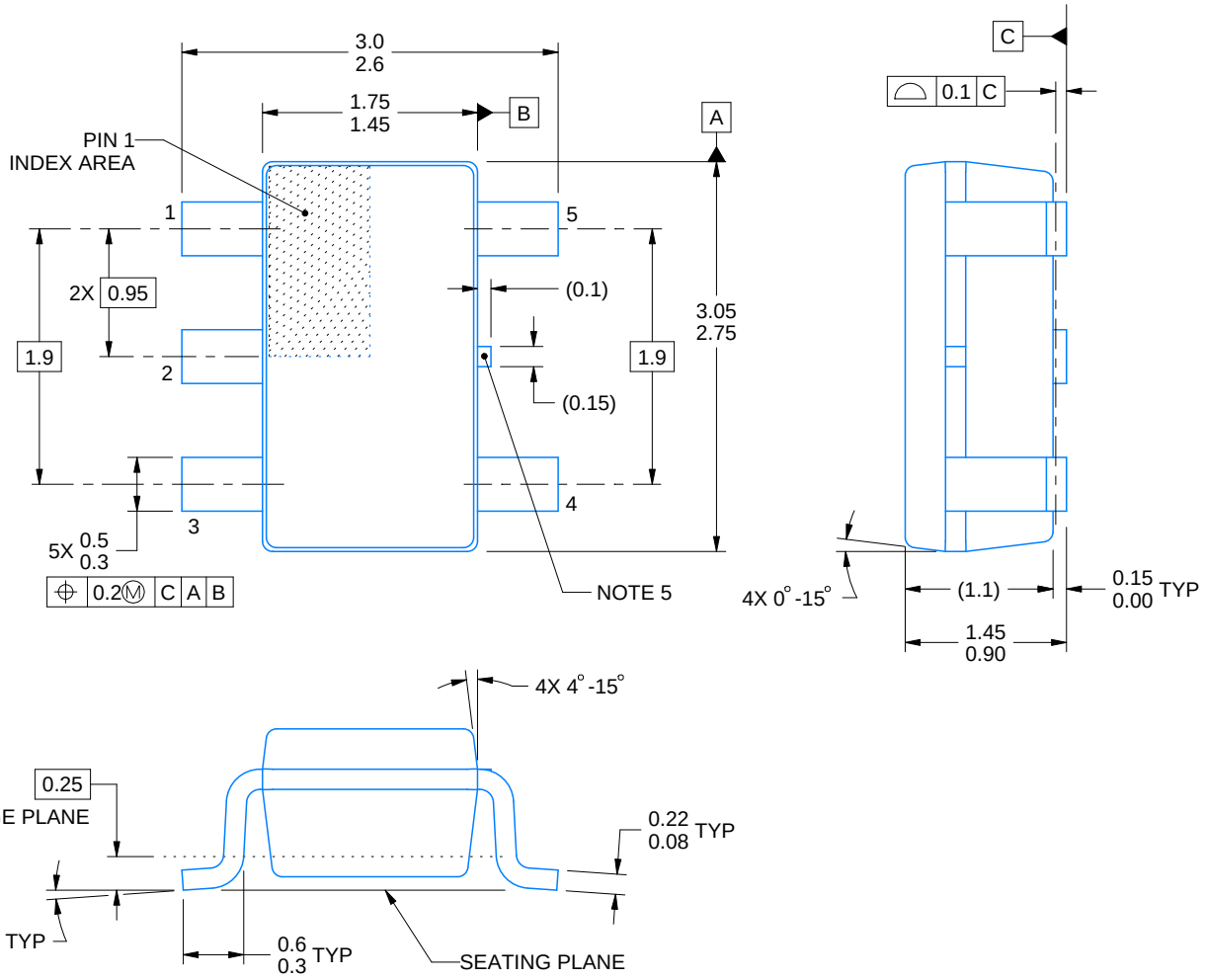
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

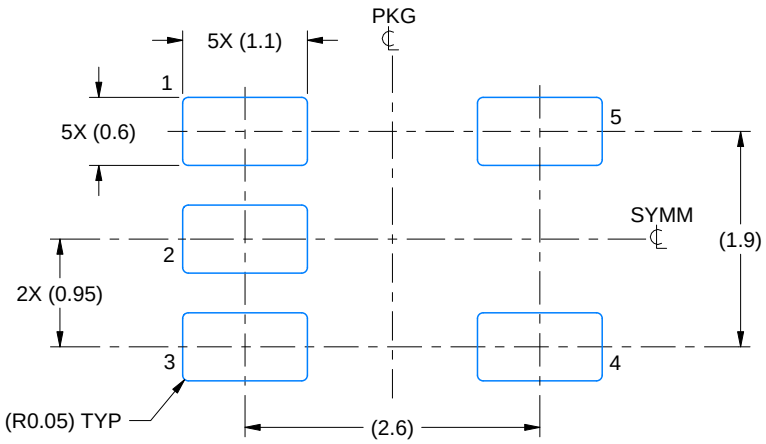
SMALL OUTLINE TRANSISTOR



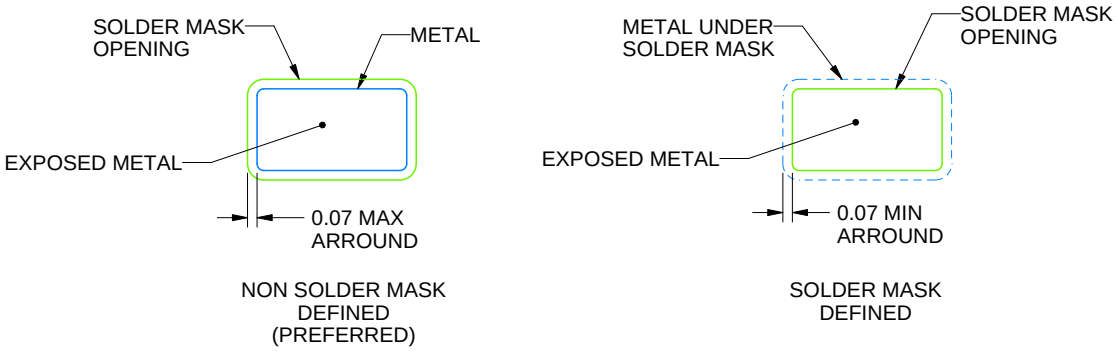
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

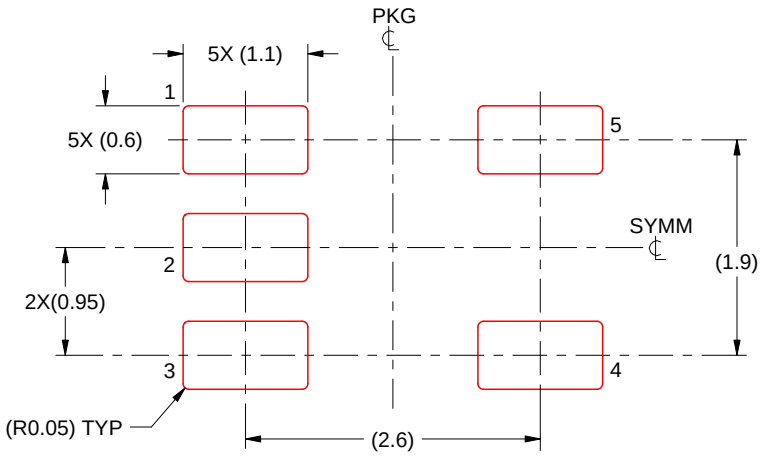


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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