

TS5A3166-Q1 0.9Ω SPST 模拟开关

1 特性

- 符合汽车应用要求
- 断电模式下的隔离, $V_{+} = 0$
- 低导通状态电阻 (0.9Ω)
- 控制输入为 5.5V 耐压
- 低电荷注入
- 低总谐波失真 (THD)
- 1.65V 至 5.5V 单电源运行
- 锁断性能超过 100mA (符合 JESD 78, II 类规范的要求)
- 静电放电 (ESD) 性能测试符合 JESD 22 标准
 - 2000V 人体放电模式 (A114-B, II 类)
 - 1000V 充电器件模型 (C101)

2 应用

- 远程信息处理
- 汽车雷达系统
- 信息娱乐系统
- 车身控制模块
- 引擎控制单元
- 锁相环 (PLL) 应用

3 说明

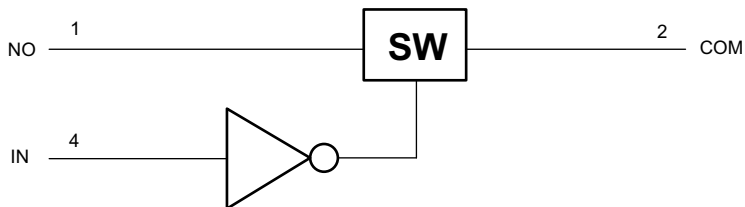
TS5A3166-Q1 是一款单刀单掷 (SPST) 模拟开关, 工作电压范围为 1.65V 至 5.5V。该器件具有较低的导通状态电阻。该器件的总谐波失真 (THD) 性能出色, 并且功耗超低。这些特性使得这款器件适合于便携式音频应用。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TS5A3166-Q	SC70 (5)	2.00mm × 1.25mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

4 简化电路原理图



目录

1 特性 1 2 应用 1 3 说明 1 4 简化电路原理图 1 5 修订历史记录 2 6 Pin Configuration and Functions 3 7 Specifications 3 7.1 Absolute Maximum Ratings 3 7.2 ESD Ratings 3 7.3 Recommended Operating Conditions 4 7.4 Thermal Information 4 7.5 Electrical Characteristics for 5-V Supply 5 7.6 Electrical Characteristics for 3.3-V Supply 7 7.7 Electrical Characteristics for 2.5-V Supply 9 7.8 Electrical Characteristics for 1.8-V Supply 11 7.9 Typical Characteristics 13 8 Parameter Measurement Information 15	9 Detailed Description 18 9.1 Overview 18 9.2 Functional Block Diagram 19 9.3 Feature Description 19 9.4 Device Functional Modes 19 10 Application and Implementation 20 10.1 Application Information 20 10.2 Typical Application 21 11 Power Supply Recommendations 22 12 Layout 22 12.1 Layout Guidelines 22 12.2 Layout Example 22 13 器件和文档支持 23 13.1 商标 23 13.2 静电放电警告 23 13.3 Glossary 23 14 机械、封装和可订购信息 23
---	--

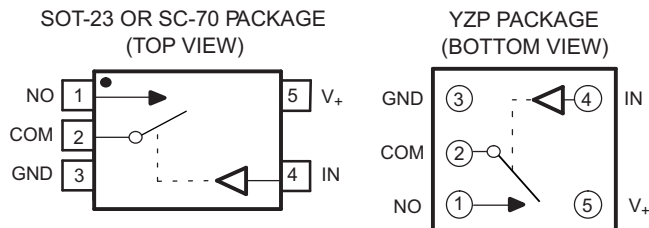
5 修订历史记录

Changes from Original (July 2014) to Revision A

Page

<ul style="list-style-type: none"> • 最初发布的完整版文档。 1 	1
---	---

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
NO	1	IO	Normally closed
COM	2	IO	Common
GND	3	GND	Digital ground
IN	4	Input	Digital control pin to connect COM to NO
V ₊	5	Power	Power Supply

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT		
V ₊	Supply voltage range ⁽³⁾	-0.5	6.5	V		
V _{NO} V _{COM}	Analog voltage range ⁽³⁾⁽⁴⁾⁽⁵⁾	-0.5	V ₊ + 0.5	V		
I _K	Analog port diode current	V _{NO} , V _{COM} < 0		-50	mA	
I _{NO} I _{COM}	On-state switch current	V _{NO} , V _{COM} = 0 to V ₊		-200	200	mA
	On-state peak switch current ⁽⁶⁾			-400	400	mA
V _I	Digital input voltage range ⁽³⁾⁽⁴⁾	-0.5	6.5	V		
I _{IK}	Digital clamp current	V _I < 0		-50	mA	
I ₊	Continuous current through V ₊			100	mA	
I _{GND}	Continuous current through GND			-100	mA	
T _{stg}	Storage temperature range	-65	150	°C		

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5.5	V
V_+	Supply voltage	0	5.5	V
V_I	Control Input Voltage	0	5.5	V
T_A	Operating free-air temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS5A3166-Q1	UNIT
		DCK	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	283.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	60.8	
Ψ_{JT}	Junction-to-top characterization parameter	1.7	
Ψ_{JB}	Junction-to-board characterization parameter	60.0	

 (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics for 5-V Supply⁽¹⁾

 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	85°C			125°C			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
Analog Switch												
Analog signal range	V_{COM}, V_{NO}				0		V_+	0		V_+	V	
Peak ON resistance	r_{peak}	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -100 \text{ mA}$,	Switch ON, See Figure 13	25°C	4.5 V	0.8	1.1	0.8	1.1	Ω		
			Full				1.2		1.44			
ON-state resistance	r_{on}	$V_{NO} = 2.5 \text{ V}$, $I_{COM} = -100 \text{ mA}$,	Switch ON, See Figure 13	25°C	4.5 V	0.7	0.9	0.7	0.9	Ω		
			Full				1		1.2			
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -100 \text{ mA}$, $V_{NO} = 1 \text{ V}, 1.5 \text{ V}, 2.5 \text{ V}$, $I_{COM} = -100 \text{ mA}$,	Switch ON, See Figure 13	25°C	4.5 V	0.15		0.15		Ω		
			25°C			0.09	0.15	0.09	0.15			
			Full			0.15		0.18				
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1 \text{ V}$, $V_{COM} = 4.5 \text{ V}$, or $V_{NO} = 4.5 \text{ V}$, $V_{COM} = 1 \text{ V}$,	Switch OFF, See Figure 14	25°C	5.5 V	-20	4	20	-80	4	80	nA
				Full			-100		100	-400		400
	$I_{NO(PWROFF)}$	$V_{NO} = 0 \text{ to } 5.5 \text{ V}$, $V_{COM} = 5.5 \text{ V to } 0$,		25°C	0 V	-5	0.4	5	-5	0.4	5	μA
				Full			-15		15	-30		30
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1 \text{ V}$, $V_{NO} = 4.5 \text{ V}$, or $V_{COM} = 4.5 \text{ V}$, $V_{NO} = 1 \text{ V}$,	Switch OFF, See Figure 14	25°C	5.5 V	-20	4	20	-80	4	80	nA
				Full			-100		100	-400		400
	$I_{COM(PWROFF)}$	$V_{COM} = 5.5 \text{ V to } 0$, $V_{NO} = 0 \text{ to } 5.5 \text{ V}$,		25°C	0 V	-5	0.4	5	-5	0.4	5	μA
				Full			-15		15	-30		30
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1 \text{ V}$, $V_{COM} = \text{Open}$, or $V_{NO} = 4.5 \text{ V}$, $V_{COM} = \text{Open}$,	Switch ON, See Figure 15	25°C	5.5 V	-2	0.3	2	-80	0.3	80	nA
				Full			-20		20	-400		
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1 \text{ V}$, $V_{NO} = \text{Open}$, or $V_{COM} = 4.5 \text{ V}$, $V_{NO} = \text{Open}$,	Switch ON, See Figure 15	25°C	5.5 V	-2	0.3	2	-80	0.3	80	nA
				Full			-20		20	-400		
Digital Control Inputs (IN)												
Input logic high	V_{IH}			Full		2.4		5.5	2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	0		0.8	V
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5 \text{ V or } 0$		25°C	5.5 V	-2	0.3	2				nA
				Full			-20		20	-400		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 5-V Supply⁽¹⁾ (continued)
 $V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	85°C			125°C			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
Dynamic												
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 17	25°C	5 V	2.5	4.5	7	2.5	4.5	7	ns
				Full	4.5 V to 5.5 V	1.5		7.5	1.5		7.5	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 17	25°C	5 V	6	9	11.5	6	9	11.5	ns
				Full	4.5 V to 5.5 V	4		12.5	4		12.5	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1\text{ nF}$, See Figure 20	25°C	5 V		1			1	pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V		19			19	pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V		18			18	pF	
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		35.5			35.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		35.5			35.5	pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	5 V		2			2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	5 V		200			200	MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$,	Switch OFF, See Figure 19	25°C	5 V		-64			-64	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 20\text{ Hz to }20\text{ kHz}$, See Figure 21	25°C	5 V		0.005			0.005	%	
Supply												
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V	0.01	0.1		0.01	0.1	μA	
				Full			0.5		0.8			

7.6 Electrical Characteristics for 3.3-V Supply⁽¹⁾

 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	85°C			125°C			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
Analog Switch												
Analog signal range	V_{COM}, V_{NO}				0		V_+	0		V_+	V	
Peak ON resistance	r_{peak}	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -100\text{ mA}$,	Switch ON, See Figure 13	25°C	3 V	1.1	1.5	1.1	1.5	Ω		
			Full			1.7	2.07					
ON-state resistance	r_{on}	$V_{NO} = 2\text{ V}$, $I_{COM} = -100\text{ mA}$,	Switch ON, See Figure 13	25°C	3 V	1	1.4	1	1.4	Ω		
			Full			1.5	1.8					
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -100\text{ mA}$,	Switch ON, See Figure 13	25°C	3 V	0.3		0.3		Ω		
		$V_{NO} = 2\text{ V}, 0.8\text{ V}$, $I_{COM} = -100\text{ mA}$,		25°C		0.09	0.15	0.09	0.15			
				Full		0.15		0.18				
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1\text{ V}$, $V_{COM} = 3\text{ V}$, or $V_{NO} = 3\text{ V}$, $V_{COM} = 1\text{ V}$,	Switch OFF, See Figure 14	25°C	3.6 V	-2	0.5	2	-2	0.5	2	nA
				Full		-20	20	-360	360			
	$I_{NO(PWROFF)}$	$V_{NO} = 0\text{ to }3.6\text{ V}$, $V_{COM} = 3.6\text{ V to }0$,		25°C	0 V	-1	0.1	1	-1	0.1	1	μA
				Full		-5	5	-27	27			
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}$, $V_{NO} = 3\text{ V}$, or $V_{COM} = 3\text{ V}$, $V_{NO} = 1\text{ V}$,	Switch OFF, See Figure 14	25°C	3.6 V	-2	0.5	2	-72	0.5	72	nA
				Full		-20	20	-360	360			
	$I_{COM(PWROFF)}$	$V_{COM} = 3.6\text{ V to }0$, $V_{NO} = 0\text{ to }3.6\text{ V}$,		25°C	0 V	-1	0.1	1	-2	0.1	2	μA
				Full		-5	5	-27	27			
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}$, $V_{COM} = \text{Open}$, or $V_{NO} = 3\text{ V}$, $V_{COM} = \text{Open}$,	Switch ON, See Figure 15	25°C	3.6 V	-2	0.2	2	-72	72	nA	
			Full	-20		20	-360	360				
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$, $V_{NO} = \text{Open}$, or $V_{COM} = 3\text{ V}$, $V_{NO} = \text{Open}$,	Switch ON, See Figure 15	25°C	3.6 V	-2	0.2	2	-72	72	nA	
			Full	-20		20	-360	360				
Digital Control Inputs (IN)												
Input logic high	V_{IH}			Full		2	5.5	2	5.5	V		
Input logic low	V_{IL}			Full		0	0.8	0	0.8	V		
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5\text{ V or }0$		25°C	3.6 V	-2	0.3	2			nA	
				Full		-20	20	-360	360			

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 3.3-V Supply⁽¹⁾ (continued)
 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	85°C			125°C			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
Dynamic												
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 17	25°C	3.3 V	2	5	10	2	5	10	ns
				Full	3 V to 3.6 V	1.5		11	1.5		11	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 17	25°C	3.3 V	6.5	9	12	6.5	9	12	ns
				Full	3 V to 3.6 V	4		13	4		13	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1\text{ nF}$, See Figure 21	25°C	3.3 V		1			1	pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		19			19	pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		18			18	pF	
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36			36	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36			36	pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	3.3 V		2			2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	3.3 V		200			200	MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$,	Switch OFF, See Figure 19	25°C	3.3 V		-64			-64	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 20\text{ Hz to }20\text{ kHz}$, See Figure 21	25°C	3.3 V		0.01			0.01	%	
Supply												
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V	0.01	0.1		0.01	0.1	μA	
				Full			0.25		0.7			

7.7 Electrical Characteristics for 2.5-V Supply⁽¹⁾

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	85°C			125°C			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
Analog Switch												
Analog signal range	V_{COM}, V_{NO}			2.3 V	0		V_+	0		V_+	V	
Peak ON resistance	r_{peak}	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -100 \text{ mA}$,	Switch ON, See Figure 13	25°C Full	2.3 V	1.8	2.4	1.8	2.4	3.1	Ω	
ON-state resistance	r_{on}	$V_{NO} = 2 \text{ V}$, $I_{COM} = -100 \text{ mA}$,	Switch ON, See Figure 13	25°C Full	2.3 V	1.2	2.1	1.2	2.1	2.88	Ω	
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -100 \text{ mA}$, $V_{NO} = 2 \text{ V}, 0.8 \text{ V}$, $I_{COM} = -100 \text{ mA}$,	Switch ON, See Figure 13	25°C	2.3 V	0.7		0.7		Ω		
				25°C		0.4		0.4				
				Full		0.6		0.72				
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1 \text{ V}$, $V_{COM} = 3 \text{ V}$, or $V_{NO} = 3 \text{ V}$, $V_{COM} = 1 \text{ V}$,	Switch OFF, See Figure 14	25°C	2.7 V	-5	0.3	5	-64	0.3	64	nA
				Full		-50		50	-320		320	
	$I_{NO(PWROFF)}$	$V_{NO} = 0 \text{ to } 3.6 \text{ V}$, $V_{COM} = 3.6 \text{ V to } 0$,	25°C	0 V	-2	0.05	2	-2	0.05	2	μA	
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1 \text{ V}$, $V_{NO} = 3 \text{ V}$, or $V_{COM} = 3 \text{ V}$, $V_{NO} = 1 \text{ V}$,	Switch OFF, See Figure 14	25°C	2.7 V	-5	0.3	5	-64	0.3	64	nA
				Full		-50		50	-320		320	
	$I_{COM(PWROFF)}$	$V_{COM} = 3.6 \text{ V to } 0$, $V_{NO} = 0 \text{ to } 3.6 \text{ V}$,	25°C	0 V	-2	0.05	2	-2	0.05	2	μA	
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1 \text{ V}$, $V_{COM} = \text{Open}$, or $V_{NO} = 3 \text{ V}$, $V_{COM} = \text{Open}$,	Switch ON, See Figure 15	25°C	2.7 V	-2	0.3	2	-64	0.3	64	nA
				Full		-20		20	-320		320	
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1 \text{ V}$, $V_{NO} = \text{Open}$, or $V_{COM} = 3 \text{ V}$, $V_{NO} = \text{Open}$,	Switch ON, See Figure 15	25°C	2.7 V	-2	0.3	2	-64	0.3	64	nA
				Full		-20		20	-320		320	
Digital Control Inputs (IN1, IN2)												
Input logic high	V_{IH}			Full		1.8	5.5	1.8	5.5	V		
Input logic low	V_{IL}			Full		0	0.6	0	0.6	V		
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5 \text{ V or } 0$		25°C	2.7 V	-2	0.3	2			nA	
				Full		-20		20	-320			320

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply⁽¹⁾ (continued)
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	85°C			125°C			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
Dynamic												
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50 \Omega$,	$C_L = 35 \text{ pF}$, See Figure 17	25°C	2.5 V	2	6	10	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	1		12	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50 \Omega$,	$C_L = 35 \text{ pF}$, See Figure 17	25°C	2.5 V	4.5	8	10.5	4.5	8	10.5	ns
				Full	2.3 V to 2.7 V	3		15	3		15	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1 \text{ nF}$, See Figure 21	25°C	2.5 V		4		4		pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		19.5		19.5		pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		18.5		18.5		pF	
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	2.5 V		36.5		36.5		pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	2.5 V		36.5		36.5		pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	2.5 V		2		2		pF	
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON,	See Figure 18	25°C	2.5 V		150		150		MHz	
OFF isolation	O_{ISO}	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	Switch OFF, See Figure 19	25°C	2.5 V		-62		-62		dB	
Total harmonic distortion	THD	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$,	$f = 20 \text{ Hz to } 20 \text{ kHz}$, See Figure 21	25°C	2.5 V		0.02		0.02		%	
Supply												
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V	0.001	0.02		0.001	0.02	μA	
				Full			0.25		0.6			

7.8 Electrical Characteristics for 1.8-V Supply⁽¹⁾

 $V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	85°C			125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Analog Switch											
Analog signal range	V_{COM}, V_{NO}				0		V_+	0		V_+	V
Peak ON resistance	r_{peak}	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -100\text{ mA}$,	Switch ON, See Figure 13	25°C	1.65 V	4.2	25	4.2	25		Ω
			Full			30	36				
ON-state resistance	r_{on}	$V_{NO} = 2\text{ V}$, $I_{COM} = -100\text{ mA}$,	Switch ON, See Figure 13	25°C	1.65 V	1.6	3.9	1.6	3.9		Ω
			Full			4.0	4.8				
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -100\text{ mA}$,	Switch ON, See Figure 13	25°C	1.65 V	2.8		2.8			Ω
		$V_{NO} = 2\text{ V}, 0.8\text{ V}$, $I_{COM} = -100\text{ mA}$,		25°C		4.1	22	4.1	22		
				Full		27		32.4			
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1\text{ V}$, $V_{COM} = 3\text{ V}$, or $V_{NO} = 3\text{ V}$, $V_{COM} = 1\text{ V}$,	Switch OFF, See Figure 14	25°C	1.95 V	-5	5	-58	58		nA
				Full		-50	50	-320	320		
	$I_{NO(PWROFF)}$	$V_{NO} = 0\text{ to }3.6\text{ V}$, $V_{COM} = 3.6\text{ V to }0$,		25°C	0 V	-2	2	-2	2		μA
				Full		-10	10	-22	22		
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}$, $V_{NO} = 3\text{ V}$, or $V_{COM} = 3\text{ V}$, $V_{NO} = 1\text{ V}$,	Switch OFF, See Figure 14	25°C	1.95 V	-5	5	-58	58		nA
				Full		-50	50	-320	320		
	$I_{COM(PWROFF)}$	$V_{COM} = 0\text{ to }3.6\text{ V}$, $V_{NO} = 3.6\text{ V to }0$,		25°C	0 V	-2	2	-2	2		μA
				Full		-10	10	-22	22		
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}$, $V_{COM} = \text{Open}$, or $V_{NO} = 3\text{ V}$, $V_{COM} = \text{Open}$,	Switch ON, See Figure 15	25°C	1.95 V	-2	2	-58	58		nA
			Full	-20		20	-320	320			
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$, $V_{NO} = \text{Open}$, or $V_{COM} = 3\text{ V}$, $V_{NO} = \text{Open}$,	Switch ON, See Figure 15	25°C	1.95 V	-2	2	-58	58		nA
			Full	-20		20	-320	320			
Digital Control Inputs (IN1, IN2)											
Input logic high	V_{IH}			Full		1.5	5.5	1.5	5.5		V
Input logic low	V_{IL}			Full		0	0.6	0	0.6		V
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5\text{ V or }0$		25°C	1.95 V	-2	0.3	2			nA
				Full		-20	20	-320	320		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 1.8-V Supply⁽¹⁾ (continued)
 $V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	85°C			125°C			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
Dynamic												
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 17	25°C	1.8 V	3	9	18	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	1		20	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 17	25°C	1.8 V	5	10	15.5	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	4		18.5	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1\text{ nF}$, See Figure 21	25°C	1.8 V		2		2		pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		19.5		19.5		pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		18.5		18.5		pF	
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5		36.5		pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5		36.5		pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	1.8 V		2		2		pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	1.8 V		150		150		MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$,	Switch OFF, See Figure 19	25°C	1.8 V		-62		-62		dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 20\text{ Hz to }20\text{ kHz}$ See Figure 21	25°C	1.8 V		0.055		0.055		%	
Supply												
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V	0.001	0.01		0.001	0.01	μA	
				Full			0.15		0.6			

7.9 Typical Characteristics

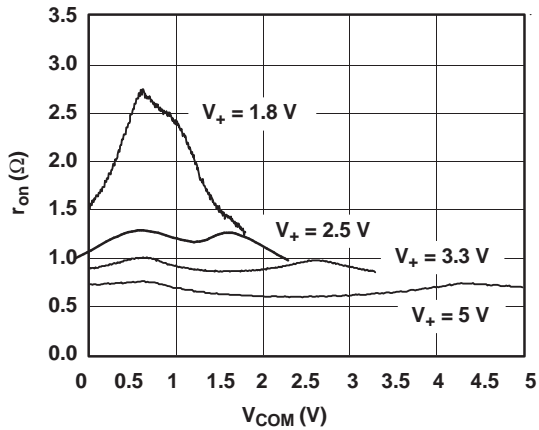


Figure 1. r_{on} vs V_{COM}

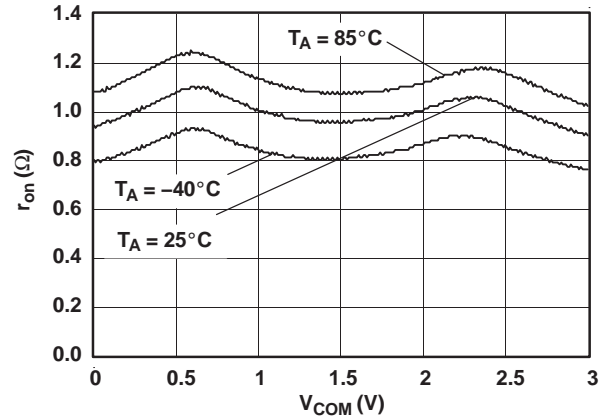


Figure 2. r_{on} vs V_{COM} ($V_+ = 3$ V)

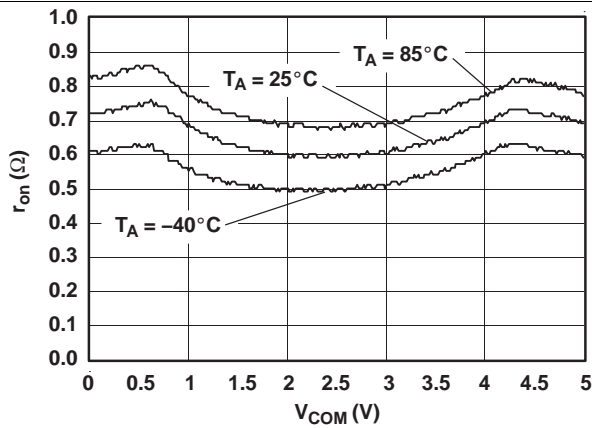


Figure 3. r_{on} vs V_{COM} ($V_+ = 5$ V)

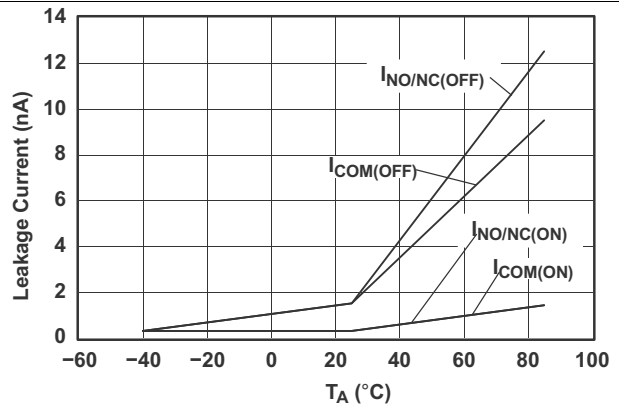


Figure 4. Leakage Current vs Temperature ($V_+ = 5.5$ V)

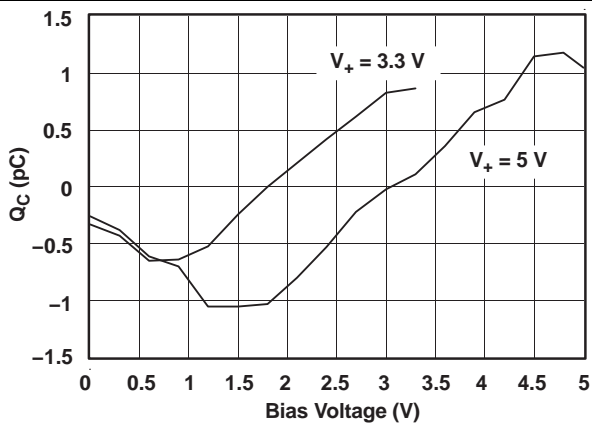


Figure 5. Charge Injection (Q_C) vs V_{COM}

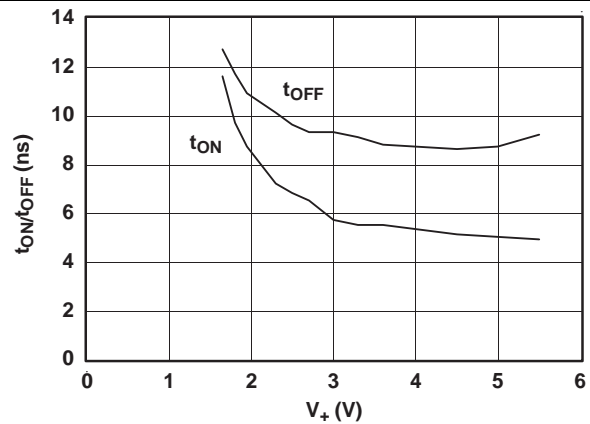


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

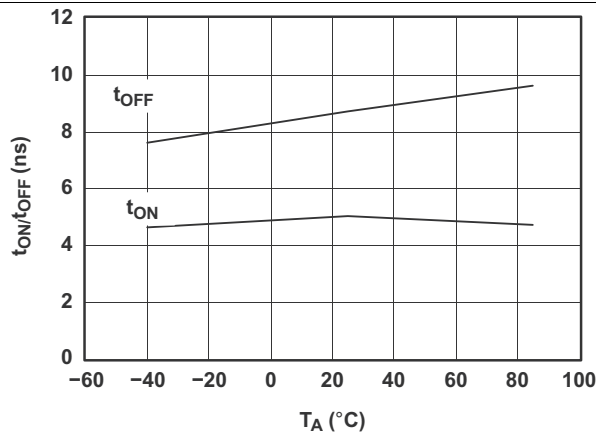


Figure 7. t_{ON} and t_{OFF} vs Temperature (V₊ = 5 V)

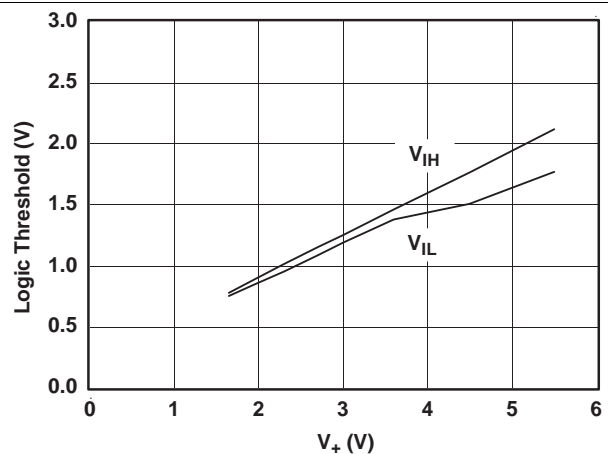


Figure 8. Logic Threshold vs V₊

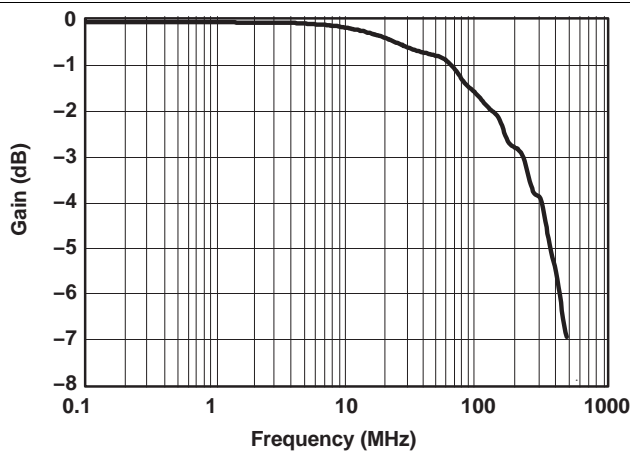


Figure 9. Gain vs Frequency (V₊ = 5 V)

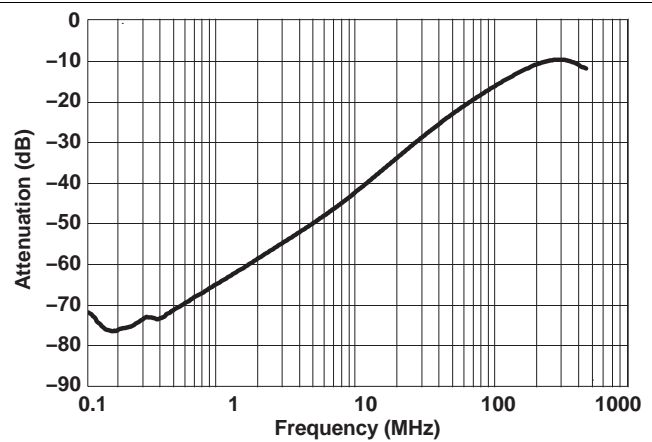


Figure 10. OFF Isolation vs Frequency (V₊ = 5 V)

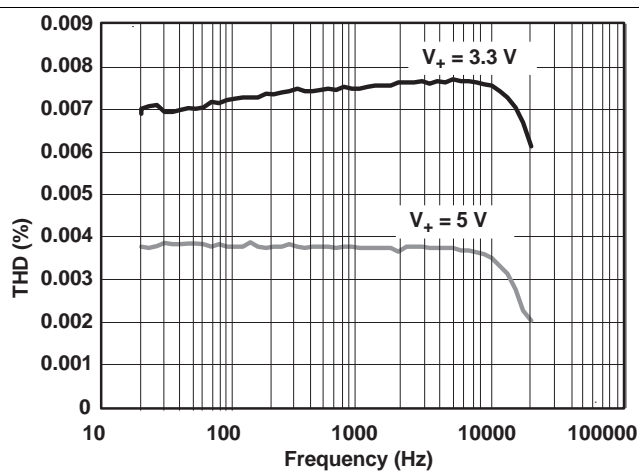


Figure 11. Total Harmonic Distortion vs Frequency (V₊ = 5 V)

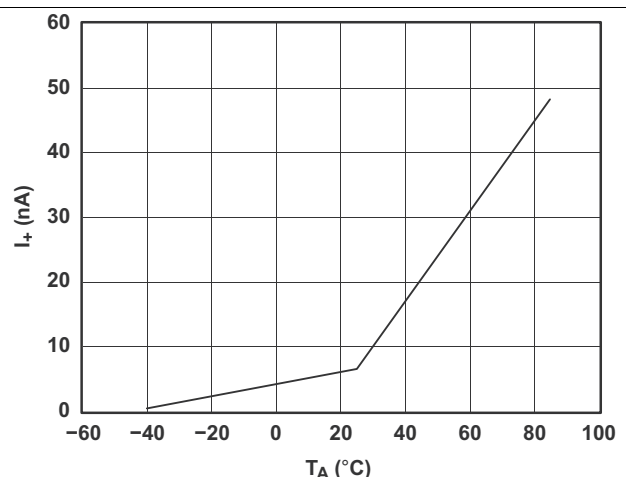


Figure 12. Power-Supply Current vs Temperature (V₊ = 5 V)

8 Parameter Measurement Information

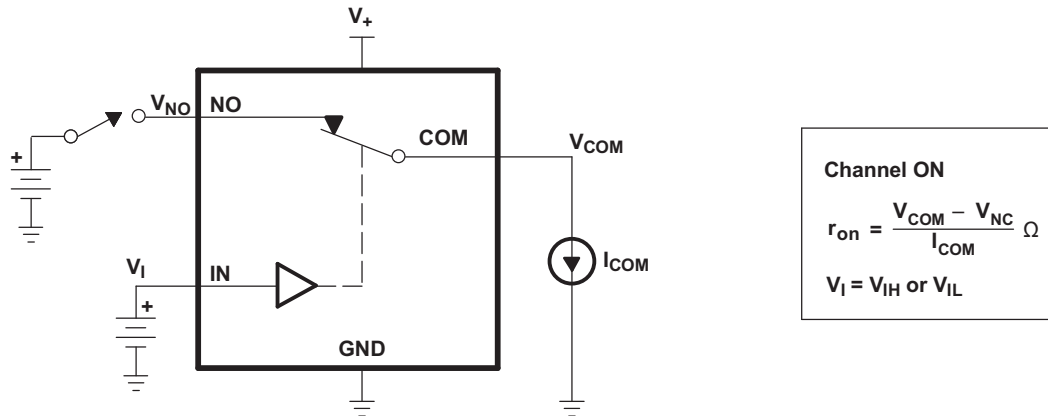


Figure 13. ON-State Resistance (r_{on})

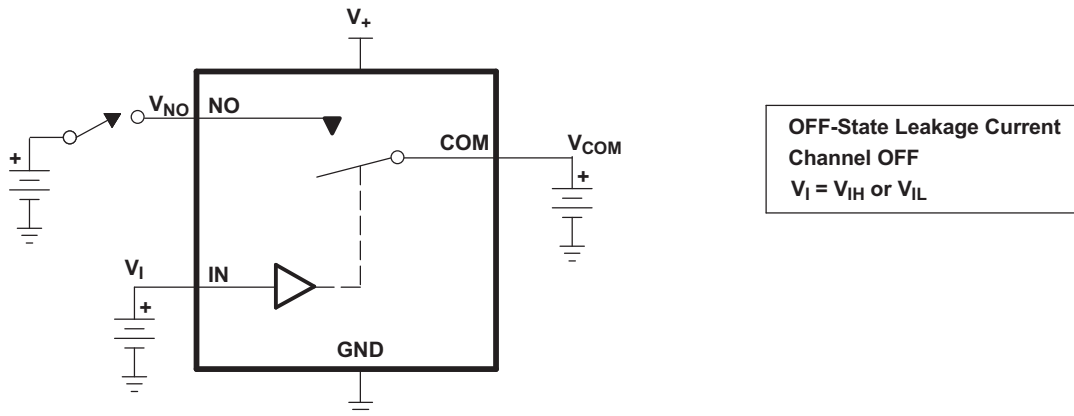


Figure 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$, $I_{COM(PWROFF)}$, $I_{NO(PWRFF)}$)

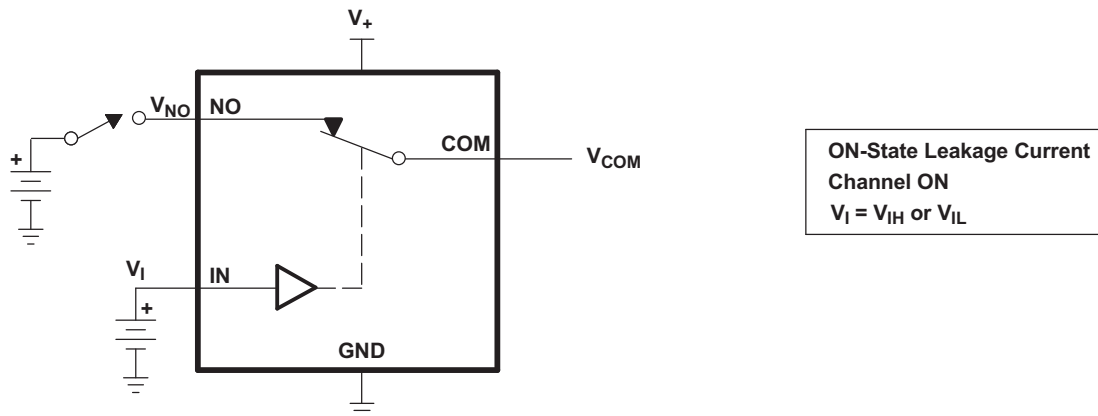


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

Parameter Measurement Information (continued)

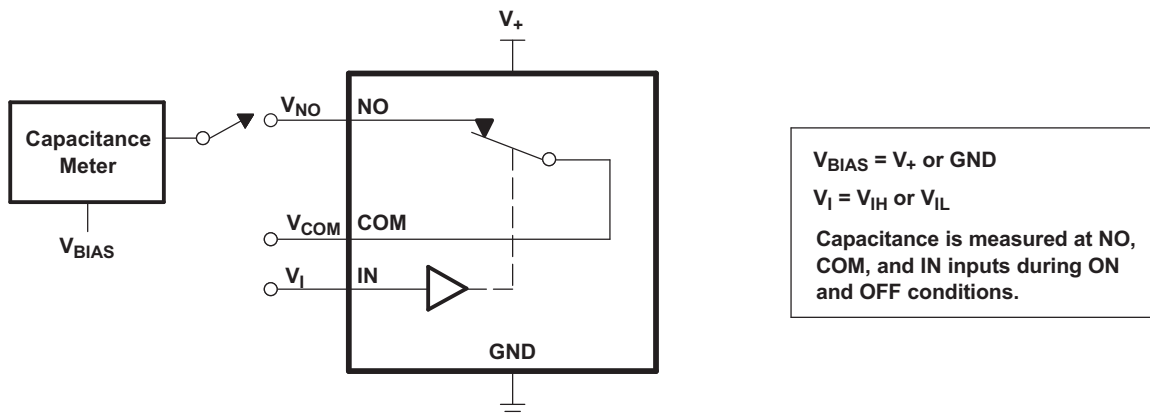
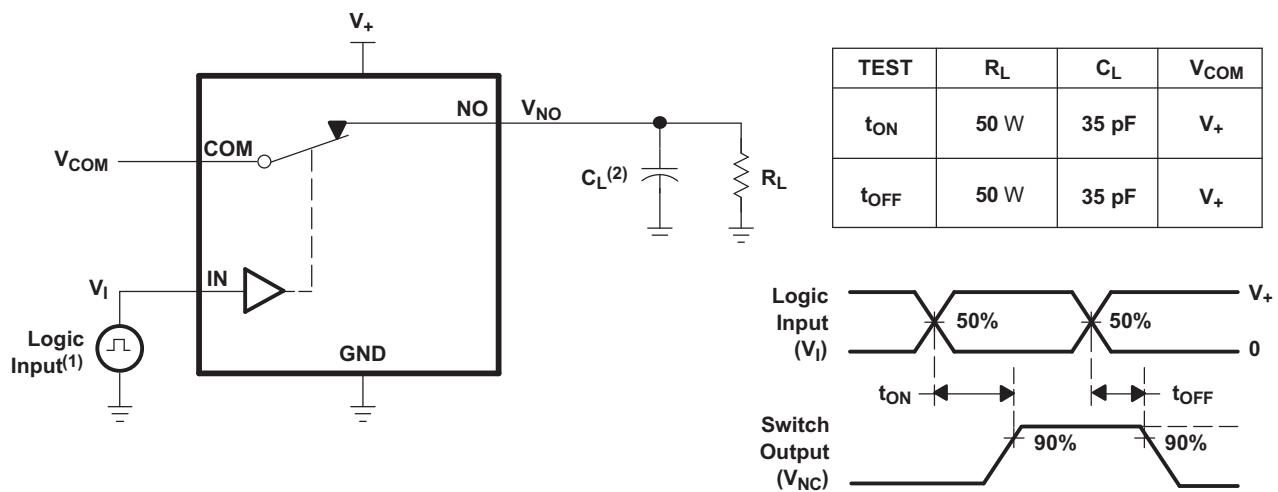


Figure 16. Capacitance (C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



- (1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- (2) C_L includes probe and jig capacitance.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

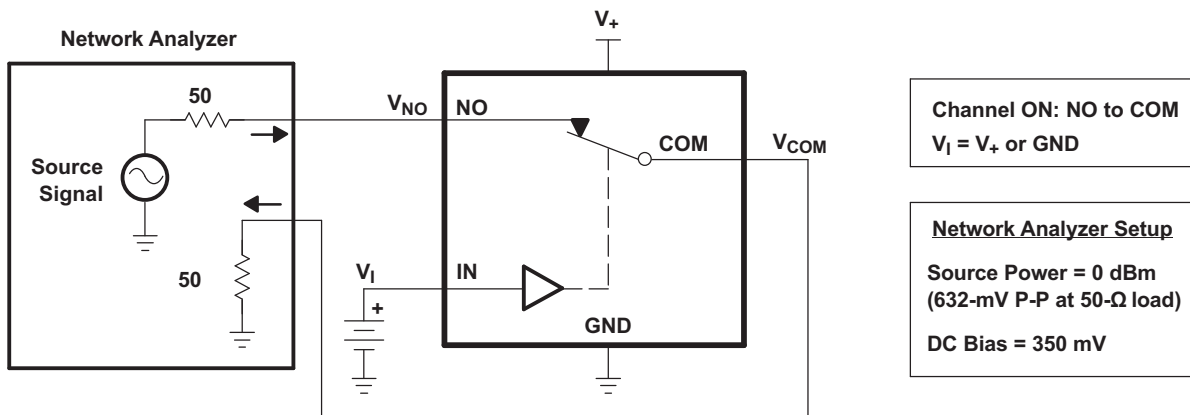


Figure 18. Bandwidth (BW)

Parameter Measurement Information (continued)

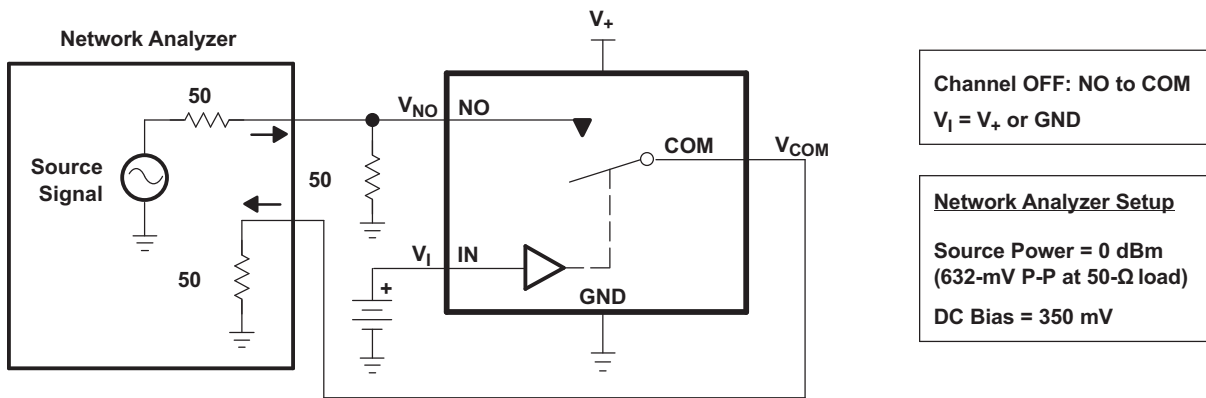
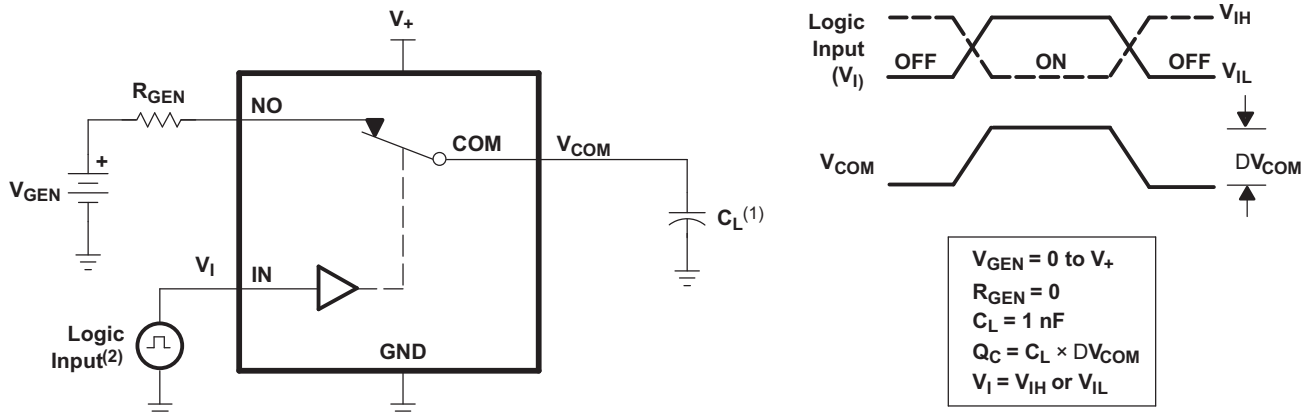
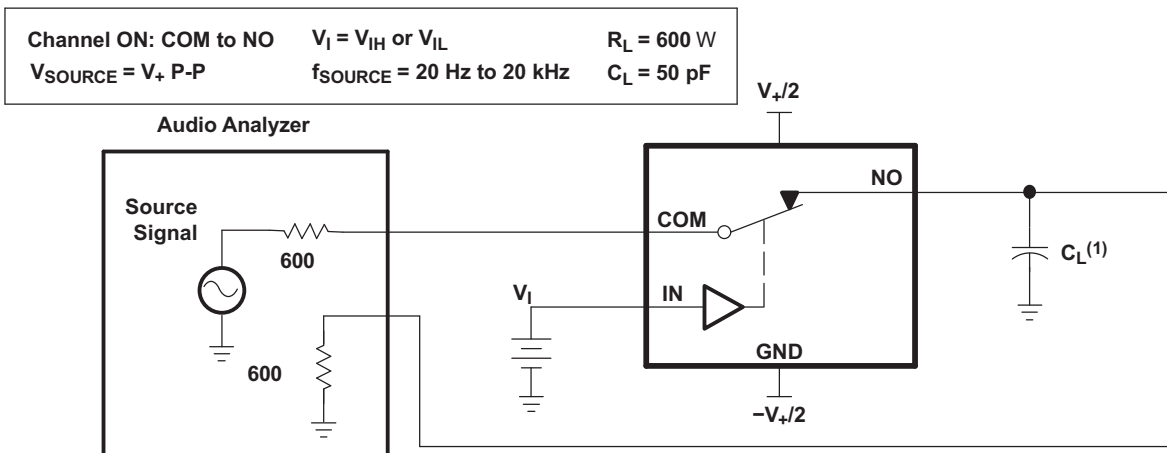


Figure 19. OFF Isolation (O_{ISO})



- (1) C_L includes probe and jig capacitance.
- (2) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.

Figure 20. Charge Injection (Q_C)



- (1) C_L includes probe and jig capacitance.

Figure 21. Total Harmonic Distortion (THD)

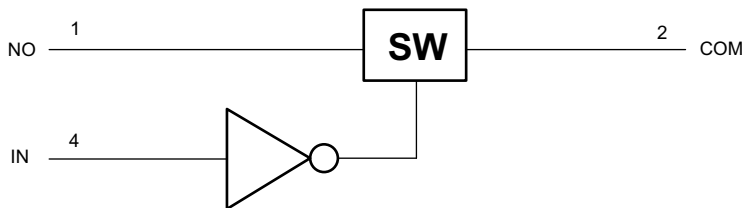
9 Detailed Description

9.1 Overview

Table 1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NO ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
$r_{on(Flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state under worst-case input and output conditions
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance, and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

9.2 Functional Block Diagram



9.3 Feature Description

Table 2. Summary Of Characteristics⁽¹⁾

Configuration	Single Pole Single Throw (SPST)
Number of channels	1
ON-state resistance (r_{on})	0.9 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.15 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	7.5 ns/12.5 ns
Charge injection (Q_C)	1 pC
Bandwidth (BW)	200 MHz
OFF isolation (O_{ISO})	-64 dB at 1 MHz
Total harmonic distortion (THD)	0.005%
Leakage current ($I_{COM(OFF)}$)	± 4 nA
Power-supply current (I_+)	0.5 μ A
Package option	5-pin DSBGA, SOT-23, or SC-70

(1) $V_+ = 5$ V, $T_A = 25^\circ\text{C}$

9.4 Device Functional Modes

Table 3. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

SPST analog switch is a basic component that could be used in any electrical system design. The following are some basic applications that utilize the TS5A3166, more detailed applications may be found in the [Typical Application](#) section.

1. Gain-control circuit for amplifier
 - (a) Additional details are available in the [Typical Application](#) section.
2. Improve lock time of a PLL by changing the time constant
 - (a) Example Diagram:

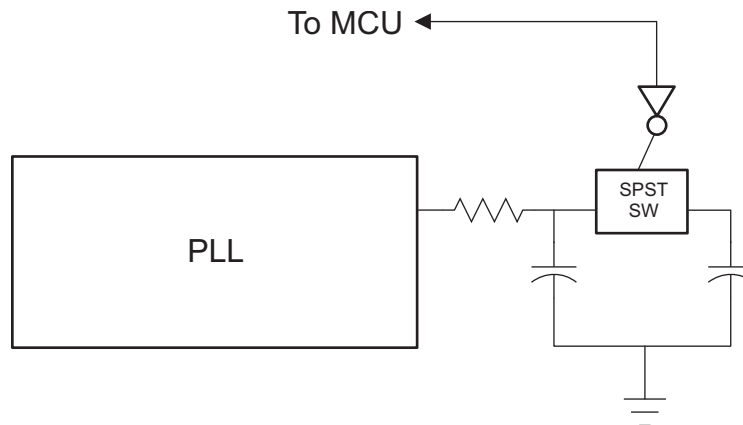


Figure 22. Improved Lock Time Circuit Simplified Block Diagram

1. Improve power consumption for PLL
 - (a) Example Diagram:

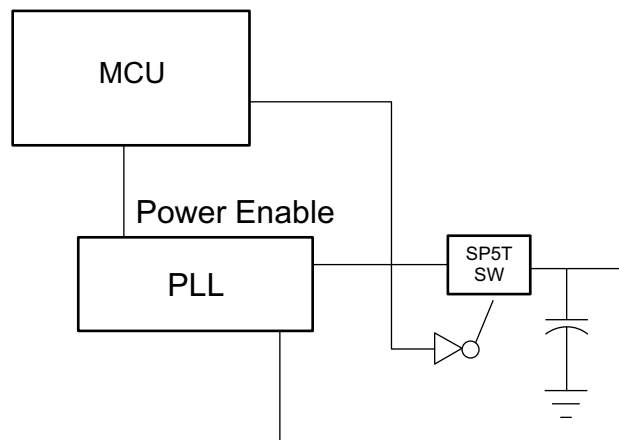


Figure 23. PLL Improved Power Consumption Simplified Block Diagram

10.2 Typical Application

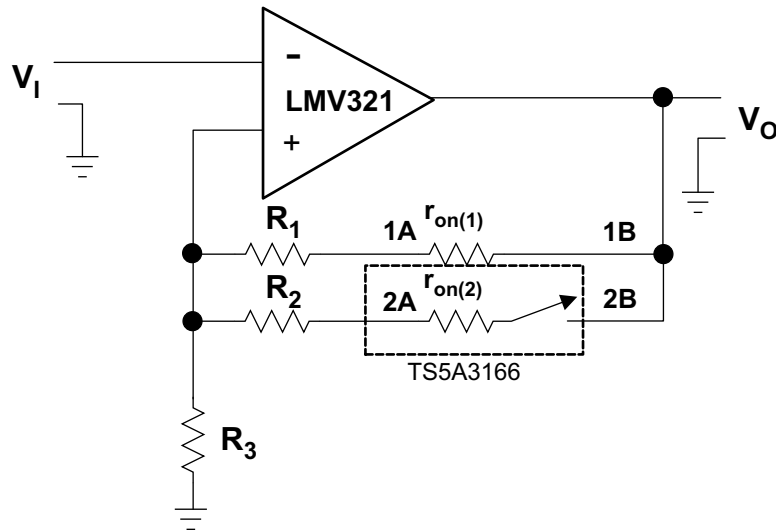


Figure 24. Gain-Control Circuit for OP Amplifier

10.2.1 Design Requirements

Place a switch in series with the input of the op amp. Since the op amp input impedance is very large, a switch on $r_{on(1)}$ is irrelevant.

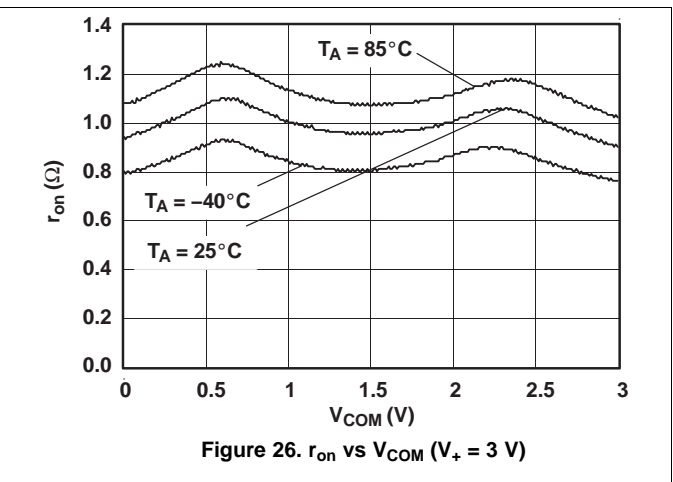
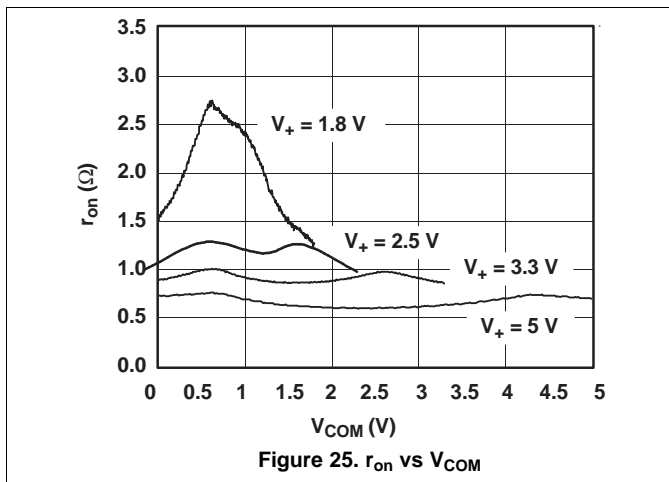
10.2.2 Detailed Design Procedure

By choosing values of R_1 and R_2 , such that $R_x \gg r_{on(x)}$, r_{on} of TS5A3166 can be ignored. The gain of op amp can be calculated as follow:

$$V_o / V_i = 1 + R_{||} / R_3 \tag{1}$$

$$R_{||} = (R_1 + r_{on(1)}) || (R_2 + r_{on(2)}) \tag{2}$$

10.2.3 Application Curves



Typical Application (continued)

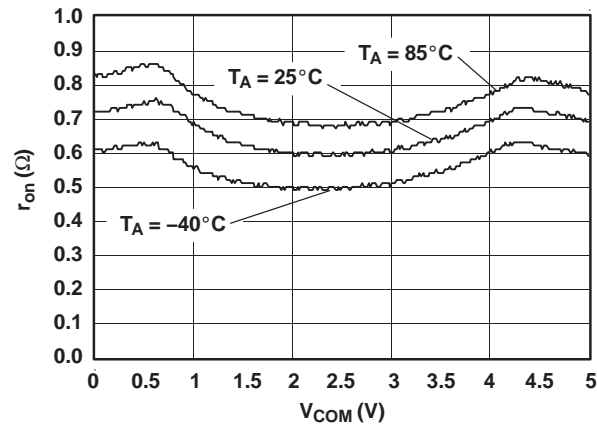


Figure 27. r_{on} vs V_{COM} ($V_+ = 5V$)

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF bypass capacitor is recommended. If there are multiple V_{CC} terminals then a 0.01 μF or 0.022 μF capacitor is recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results

12 Layout

12.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

12.2 Layout Example

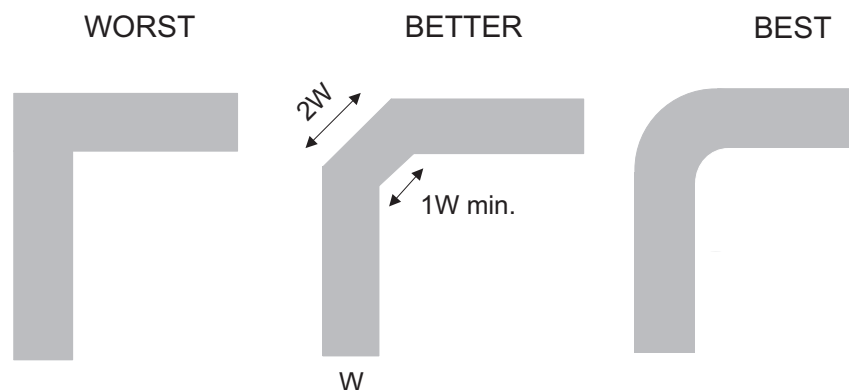


Figure 28. Trace Example

13 器件和文档支持

13.1 商标

All trademarks are the property of their respective owners.

13.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A3166QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU
TS5A3166QDCKRQ1.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

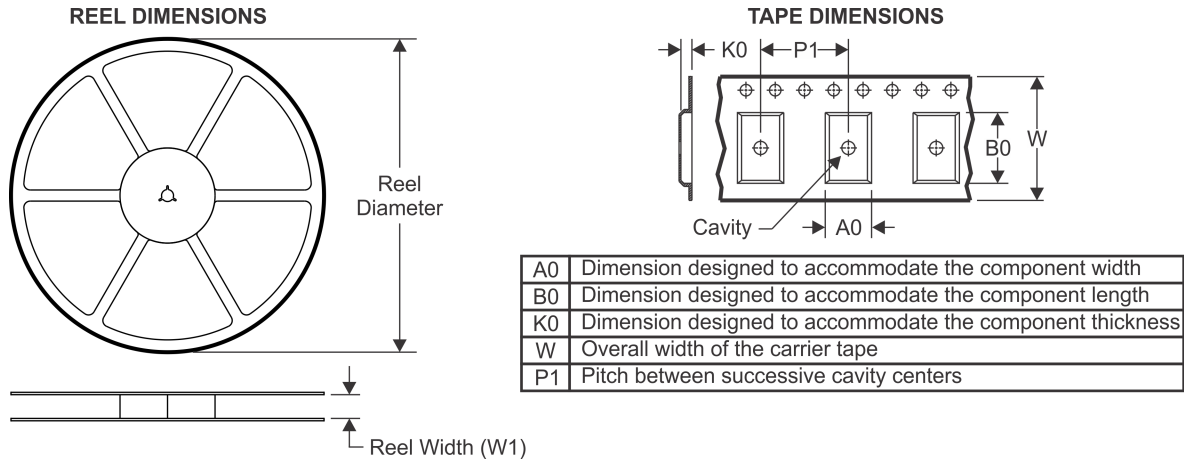
OTHER QUALIFIED VERSIONS OF TS5A3166-Q1 :

- Catalog : [TS5A3166](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3166QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

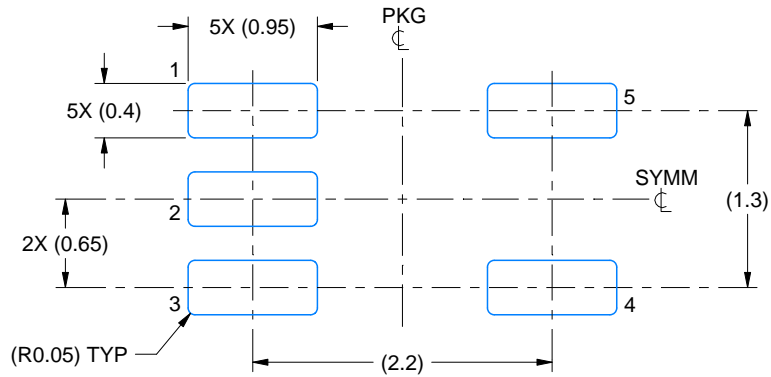
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3166QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0

EXAMPLE BOARD LAYOUT

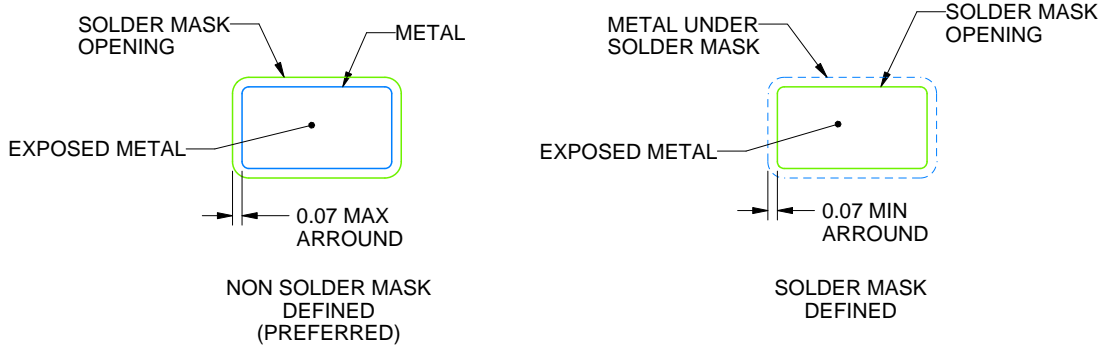
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

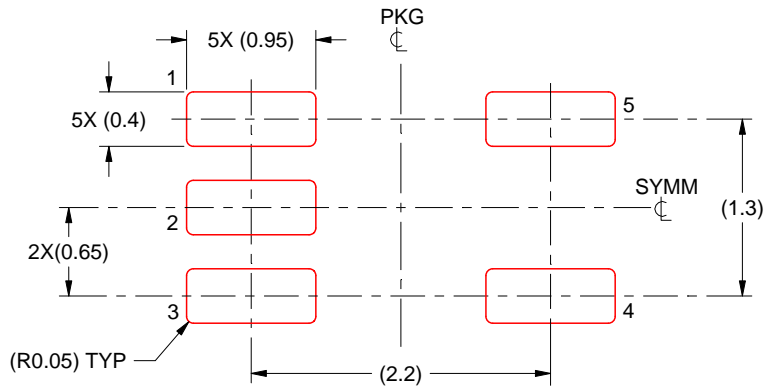
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司