TS5A23157 双通道 10Ω SPDT 模拟开关

1 特性

- 低导通状态电阻（125℃ 条件下为 15Ω）
- 125℃ 运行
- 控制输入可承受 5V 电压
- 指定的先断后合开关
- 低电荷注入
- 出色的导通状态电阻匹配
- 低总谐波失真
- 1.8V 至 5.5V 单电源运行
- 锁断性能超过 100mA（符合 JESD 78，II 类规范的要求）
- 静电放电 (ESD) 性能测试符合 JESD 22 规范
  - 2000V 人体放电模式（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

2 应用

- 采样和保持电路
- 电池供电类设备
- 音频和视频信号路由
- 通信电路

3 说明

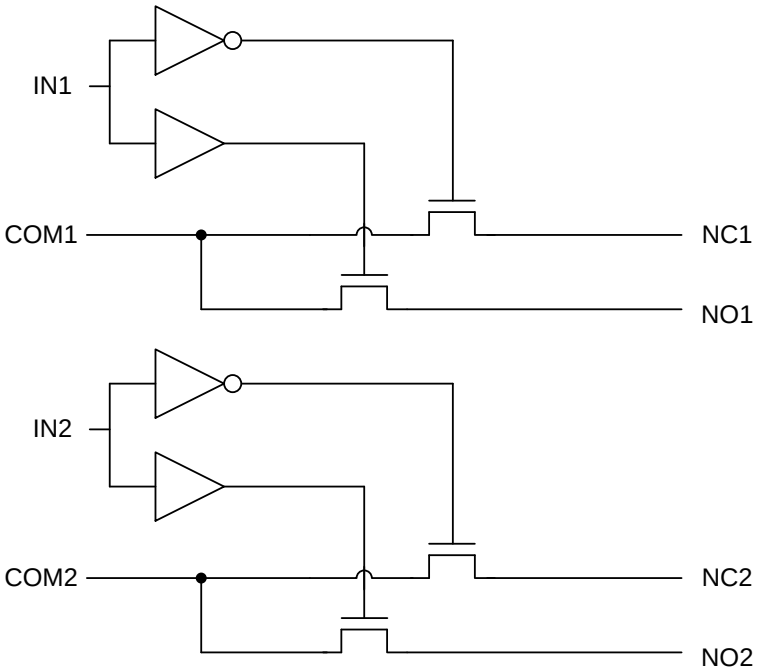
TS5A23157 器件是一款双通道单极双投 (SPDT) 模拟开关，其设计工作电压为 1.65V 至 5.5V。该器件可以同时处理数字和模拟信号。高达 5.5V（峰值）的信号可在任一方向传输。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS5A23157DGS	VSSOP (10)	3.00mm × 3.00mm
TS5A23157RSE	UQFN (10)	2.00mm × 1.50mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

方框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (June 2015) to Revision F **Page**

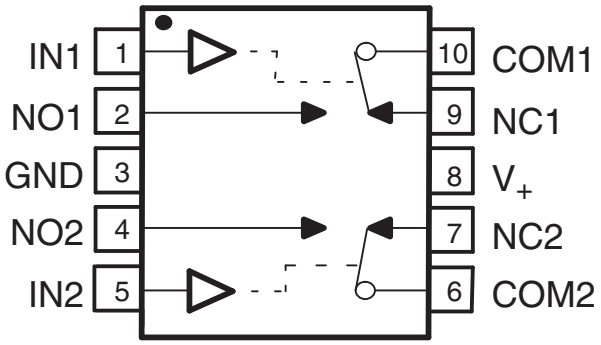
- 将*特性* 从“低导通状态电阻 (10Ω)”更改为“低导通状态电阻（125℃ 条件下为 15Ω）” ... 1
- 添加了*特性*：125℃ 运行条件 ... 1
- Added Junction Temperature To the *Absolute Maximum Ratings* table ... 4
- Changed the Operating temperature MAX value From: 85°C To: 125°C in the *Recommended Operating Conditions* table ... 4
- Changed the *Thermal Information* table ... 4
- Changed r_{on} in the *Electrical Characteristics for 5-V Supply* table ... 5
- Changed V_{IH} in the *Electrical Characteristics for 5-V Supply* table ... 5
- Changed t_{ON} and t_{OFF} in the *Electrical Characteristics for 5-V Supply* table ... 5
- Changed r_{on} in the *Electrical Characteristics for 3.3-V Supply* table ... 7
- Changed t_{ON} and t_{OFF} in the *Electrical Characteristics for 3.3-V Supply* table ... 7
- Changed r_{on} in the *Electrical Characteristics for 2.5-V Supply* table ... 8
- Changed t_{ON} and t_{OFF} in the *Electrical Characteristics for 2.5-V Supply* table ... 8
- Changed r_{on} in the *Electrical Characteristics for 1.8-V Supply* table ... 9
- Changed t_{ON} and t_{OFF} in the *Electrical Characteristics for 1.8-V Supply* table ... 9

Changes from Revision D (October 2013) to Revision E **Page**

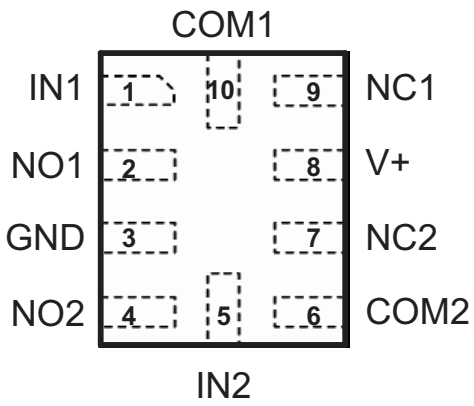
- 已添加 *引脚配置和功能* 部分、*ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实现* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



RSE Package
10-Pin UQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN1	I	Select pin for switch 1
2	NO1	I/O	Normally open I/O for switch 1
3	GND	—	Ground
4	NO2	I/O	Normally open I/O for switch 2
5	IN2	I	Select pin for switch 2
6	COM2	I/O	Common I/O for switch 2
7	NC2	I/O	Normally closed I/O for switch 2
8	V+	—	Power supply pin
9	NC1	I/O	Normally closed I/O for switch 1
10	COM1	I/O	Common I/O for switch 1

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_+	Supply voltage(2)		–0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage(2)(3)(4)		–0.5	V_+ + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NC}, V_{NO}, V_{COM} > V_+		±50	mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+		±50	mA
V_{IN}	Digital input voltage(2)(3)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_{IN} < 0		–50	mA
	Continuous current through V_+ or GND			±100	mA
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage	0	V_+	V
V+	Supply voltage	1.65	5.5	V
V_I	Control input voltage	0	5.5	V
T_A	Operating temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TS5A23157		UNIT
		DGS (VSSOP)	RSE (UQFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.5	215.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	99.1	140.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	132.4	137.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.1	13.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	130.5	137.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –30 mA,	Switch ON, see Figure 9	Full	4.5 V			10	Ω
				-40 to 125°C				15	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 3.15 V, I_{COM} = –30 mA,	Switch ON, see Figure 9	25°C	4.5 V		0.15		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –30 mA,	Switch ON, see Figure 9	25°C	4.5 V		4		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	5.5 V	–1	0.05	1	μA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	5.5 V	–0.1		0.1	μA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	5.5 V	–0.1		0.1	μA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)(2)									
V_{IH}	Input logic high			Full		V_+ × 0.7			V
				-40 to 125°C	4.75 V to 5.25 V	3.1			
V_{IL}	Input logic low			Full				V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	5.5 V	–1	0.05	1	μA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turnon time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	4.5 V to 5.5 V	1.7		5.7	ns
				-40 to 125°C	4.75 V to 5.25 V	1.2		8.7	ns
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	4.5 V to 5.5 V	0.8		3.8	ns
				-40 to 125°C	4.75 V to 5.25 V	0.5		6.8	ns
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	4.5 V to 5.5 V	0.5			ns
Q_C	Charge injection	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	See Figure 17	25°C	5 V		7		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch OFF, see Figure 11	25°C	5 V		5.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch ON, see Figure 11	25°C	5 V		17.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch ON, see Figure 11	25°C	5 V		17.5		pF
C_{IN}	Digital input capacitance	V_{IN} = V_+ or GND,	See Figure 11	25°C	5 V		2.8		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 14	25°C	4.5 V		220		MHz

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	4.5 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	4.5 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	4.5 V		0.01%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	5.5 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	5.5 V			500	µA

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –24 mA,	Switch ON, see Figure 9	Full	3 V			18	Ω
				-40 to 125°C				23	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.1 V, I_{COM} = –24 mA,	Switch ON, see Figure 9	25°C	3 V		0.2		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –24 mA,	Switch ON, see Figure 11	25°C	3 V		9		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)(2)									
V_{IH}	Input logic high			Full		V_+ × 0.7			V
V_{IL}	Input logic low			Full				V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turn-on time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	3 V to 3.6 V	2.5		7.6	ns
				-40 to 125°C		2.0		10.6	ns
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	3 V to 3.6 V	1.5		5.3	ns
				-40 to 125°C		1.0		8.3	ns
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	3 V to 3.6 V	0.5			ns
Q_C	Charge injection	R_L = 50 Ω, C_L = 0.1 nF,	see Figure 17	25°C	3.3 V		3		pC
BW	Bandwidth	R_L = 50 Ω, Switch ON,	see Figure 14	25°C	3 V		220		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	3 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	3 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	3 V		0.015%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	3.6 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	3.6 V			500	µA

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 9	Full	2.3 V			45	Ω
				-40 to 125°C				50	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.6 V, I_{COM} = –8 mA,	Switch ON, see Figure 9	25°C	2.3 V		0.5		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 9	25°C	2.3 V		27		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	2.7 V	–1	0.05	1	µA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)(2)									
V_{IH}	Input logic high			Full		V_+ × 0.7			V
V_{IL}	Input logic low			Full				V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	2.7 V	–1	0.05	1	µA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turnon time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	2.3 V to 2.7 V	3.5		14	ns
				-40 to 125°C		2.5		17	
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	2.3 V to 2.7 V	2		7.5	ns
				-40 to 125°C		1.5		10.5	ns
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	2.3 V to 2.7 V	0.5			ns
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 14	25°C	2.3 V		220		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	2.3 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	2.3 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	2.3 V		0.025%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	2.7 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	2.7 V			500	µA

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.8 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –4 mA,	Switch ON, see Figure 9	Full	1.65 V			140	Ω
				-40 to 125°C				180	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.15 V, I_{COM} = –4 mA,	Switch ON, see Figure 9	25°C	1.65 V		1		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –4 mA,	Switch ON, see Figure 9	25°C	1.65 V		110		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, see Figure 10	25°C	1.95 V	–1	0.05	1	µA
				Full		–1		1	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, see Figure 10	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, see Figure 10	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
DIGITAL INPUTS (IN12, IN2)(2)									
V_{IH}	Input logic high			Full		V_+ × 0.75			V
V_{IL}	Input logic low			Full				V_+ × 0.25	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		25°C	1.95 V	–1	0.05	1	µA
				Full		–1		1	
DYNAMIC									
t_{ON}	Turnon time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	1.65 V to 1.95 V	7		24	ns
				-40 to 125°C		5.5		27	ns
t_{OFF}	Turnoff time	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, see Figure 12	Full	1.65 V to 1.95 V	3		13	ns
				-40 to 125°C		2		16	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 13	Full	1.65 V to 1.95 V	0.5			ns
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 14	25°C	1.8 V		220		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 15	25°C	1.8 V		–60		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 16	25°C	1.8 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 18	25°C	1.8 V		0.015%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	1.95 V			1	µA
				Full				10	
ΔI_+	Change in supply current	V_{IN} = V_+ – 0.6 V		Full	1.95 V			500	µA

(1) T_A = 25°C.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.9 Typical Characteristics

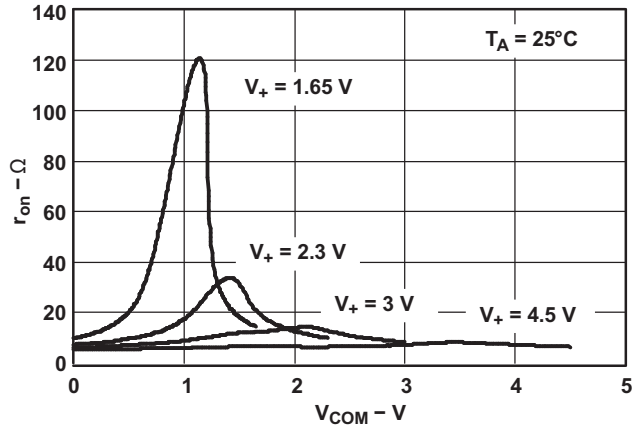


Figure 1. r_{on} vs V_{COM}

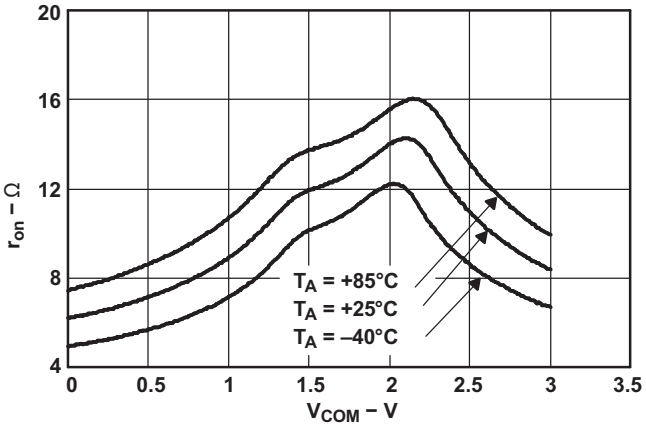


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

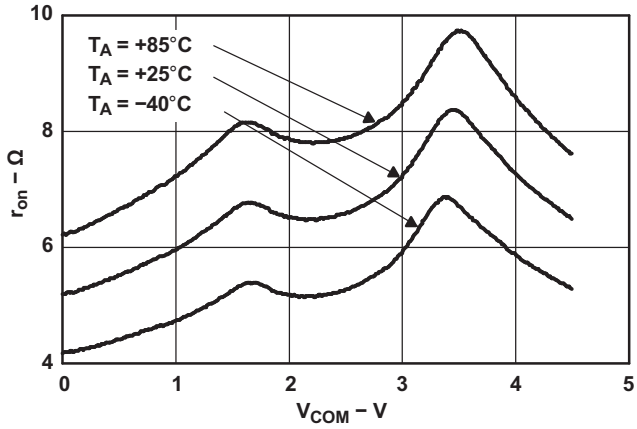


Figure 3. r_{on} vs V_{COM} (V_+ = 5 V)

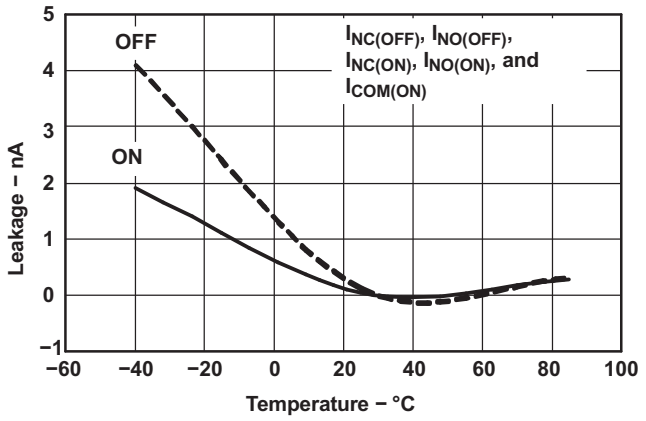


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

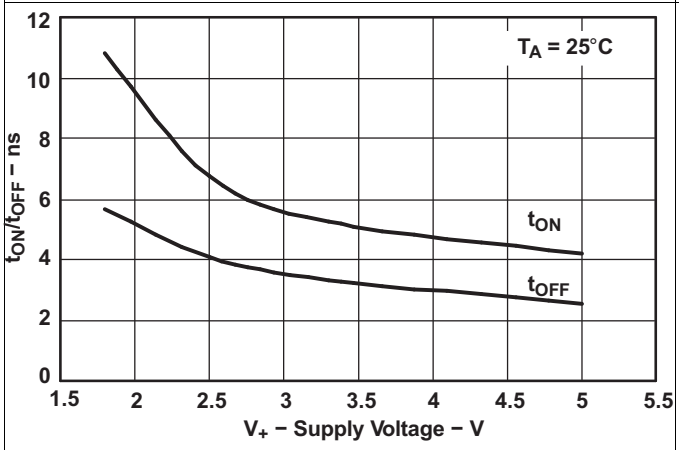


Figure 5. t_{ON} and t_{OFF} vs V_+

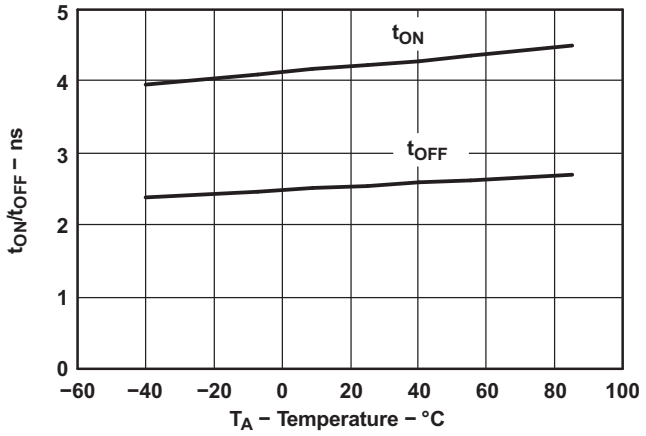


Figure 6. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

Typical Characteristics (continued)

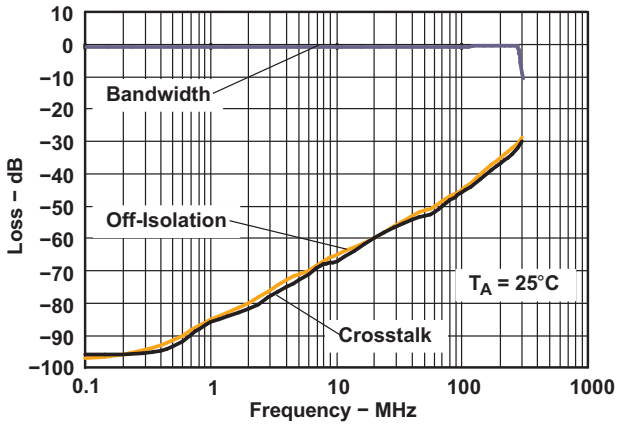


Figure 7. Frequency Response (V_+ = 3 V)

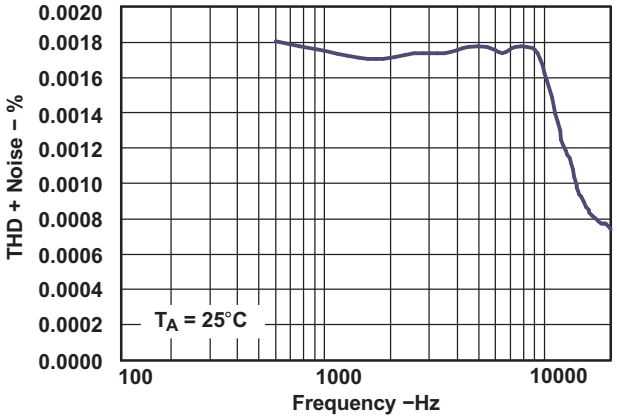


Figure 8. Total Harmonic Distortion (THD) vs Frequency (V_+ = 3 V)

7 Parameter Measurement Information

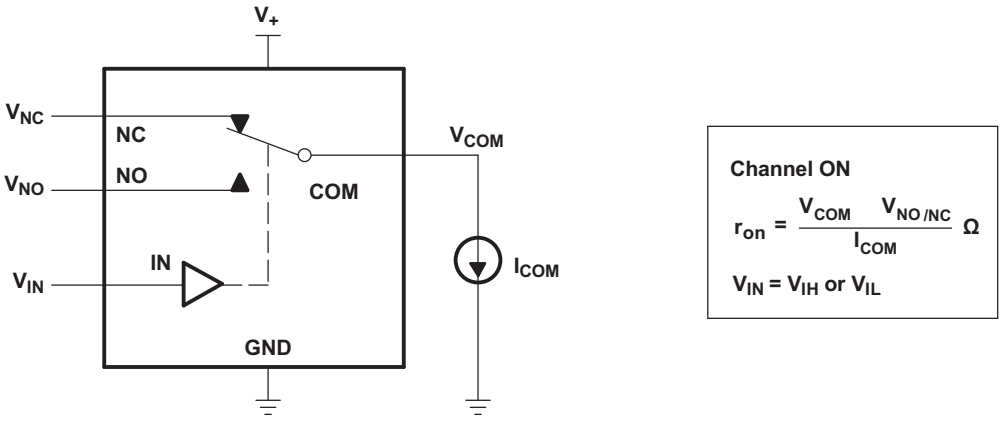


Figure 9. ON-State Resistance (r_{on})

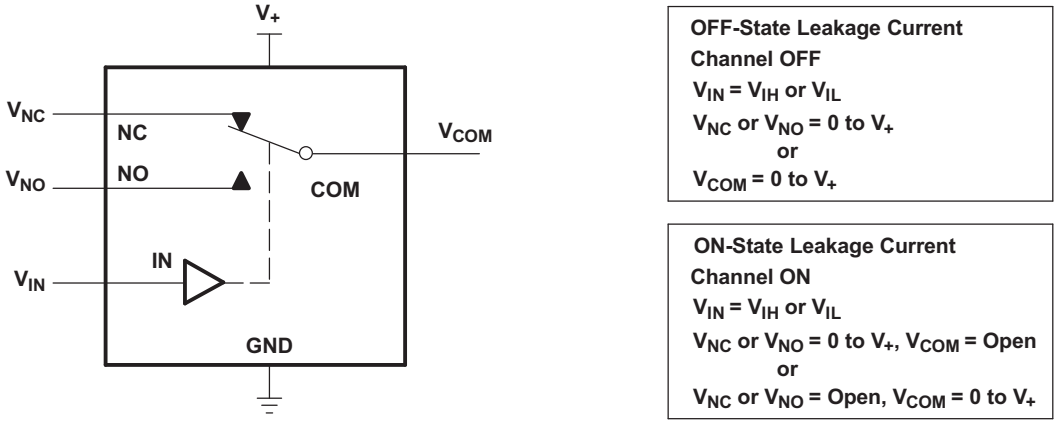


Figure 10. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

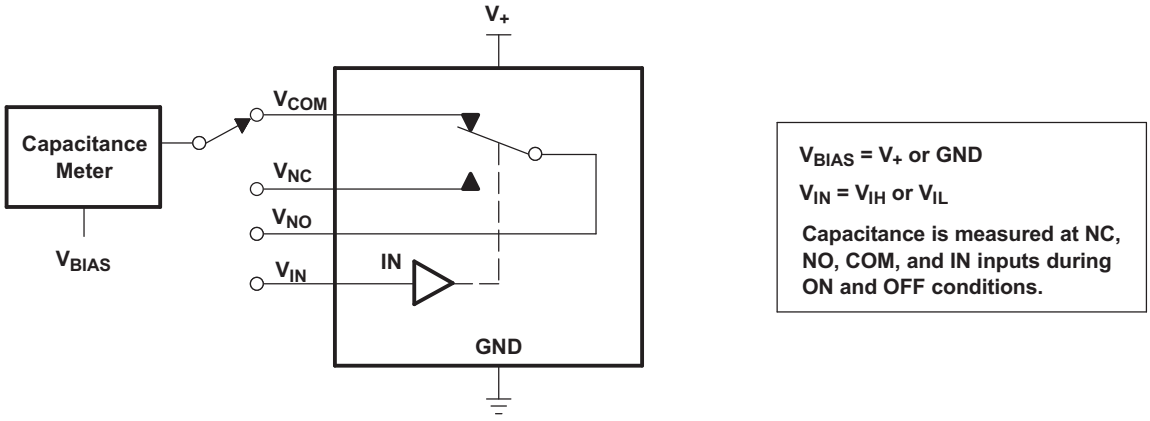
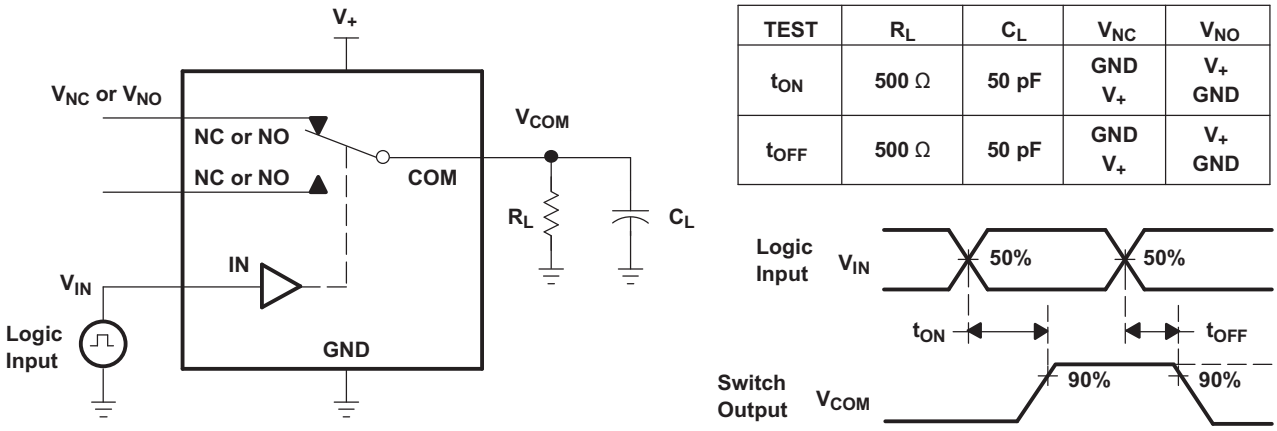


Figure 11. Capacitance (C_{IN}, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

Parameter Measurement Information (continued)



TEST	R_L	C_L	V_{NC}	V_{NO}
t_{ON}	500 Ω	50 pF	GND V_+	V_+ GND
t_{OFF}	500 Ω	50 pF	GND V_+	V_+ GND

Figure 12. Turnon (t_{ON}) and Turnoff (t_{OFF}) Time

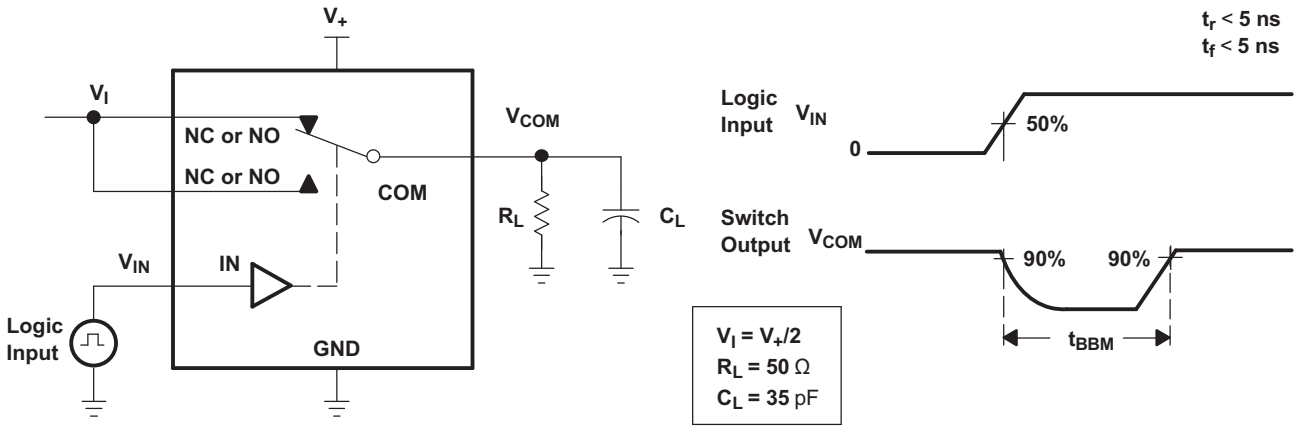


Figure 13. Break-Before-Make (t_{BBM}) Time

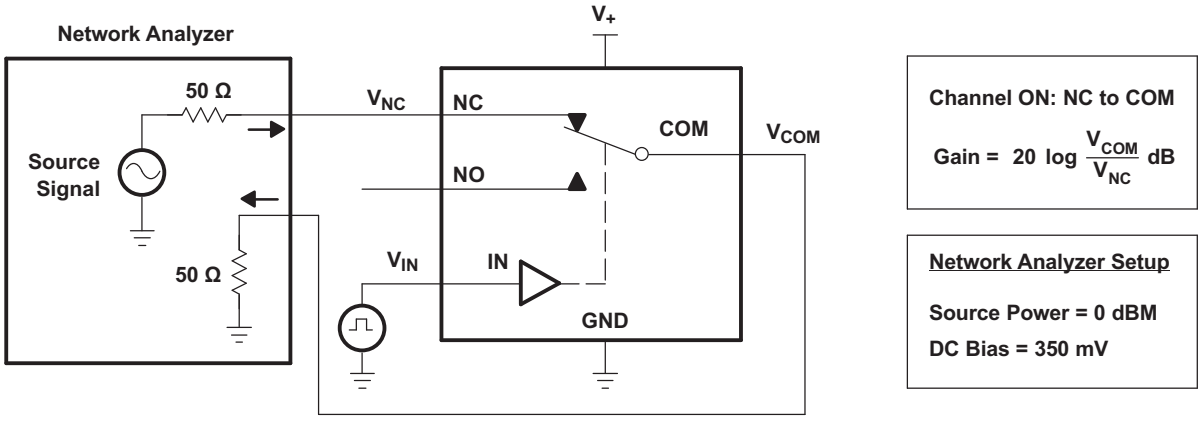


Figure 14. Frequency Response (BW)

Parameter Measurement Information (continued)

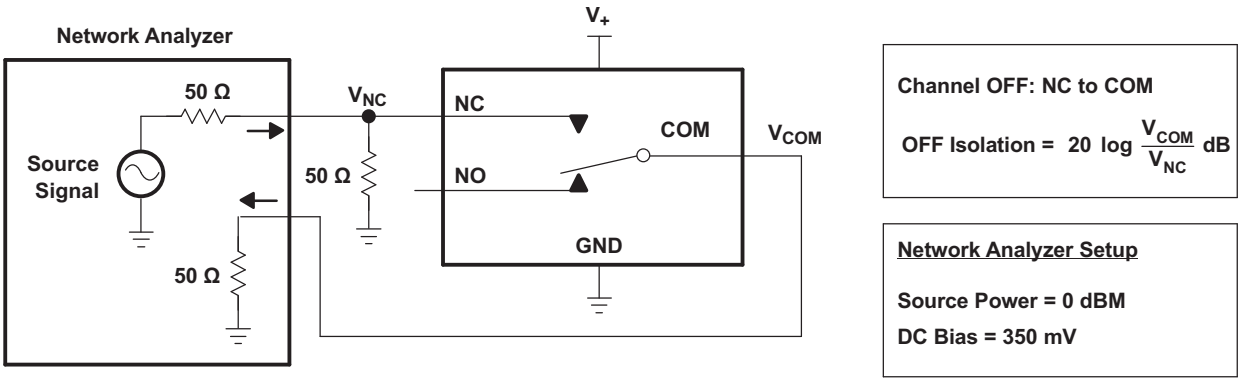


Figure 15. OFF Isolation (O_{ISO})

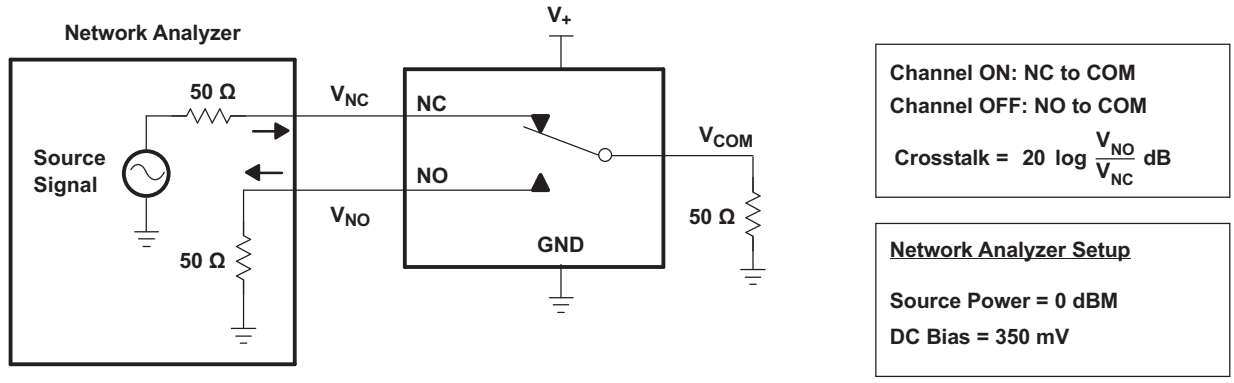


Figure 16. Crosstalk (X_{TALK})

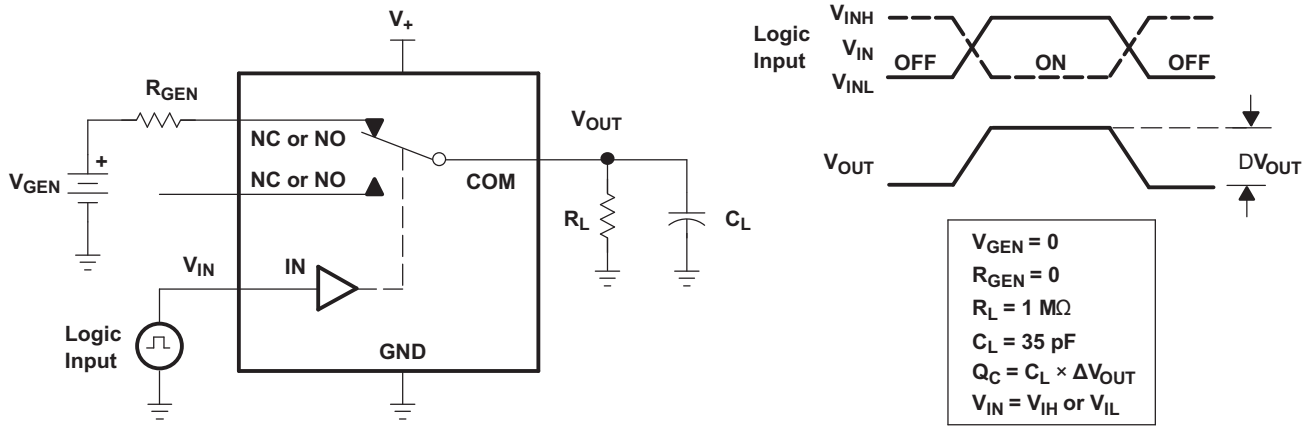


Figure 17. Charge Injection (Q_C)

Parameter Measurement Information (continued)

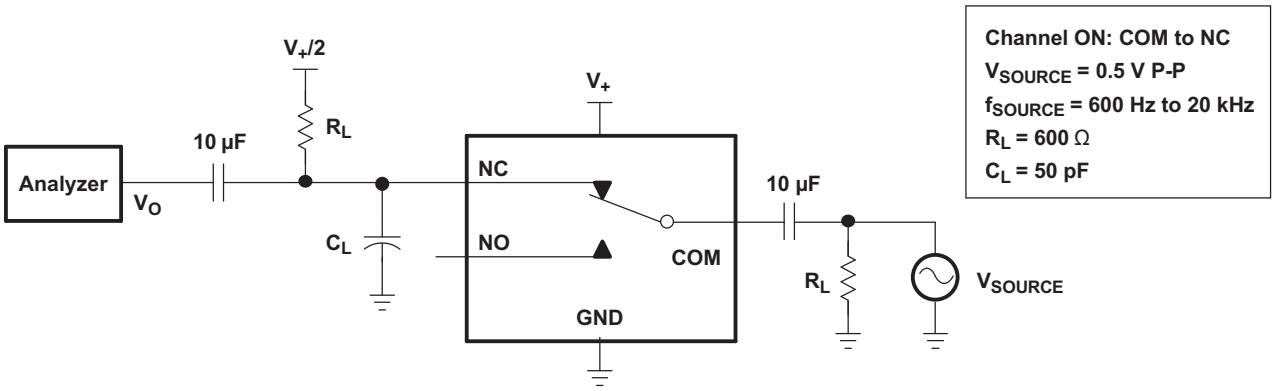


Figure 18. Total Harmonic Distortion (THD)

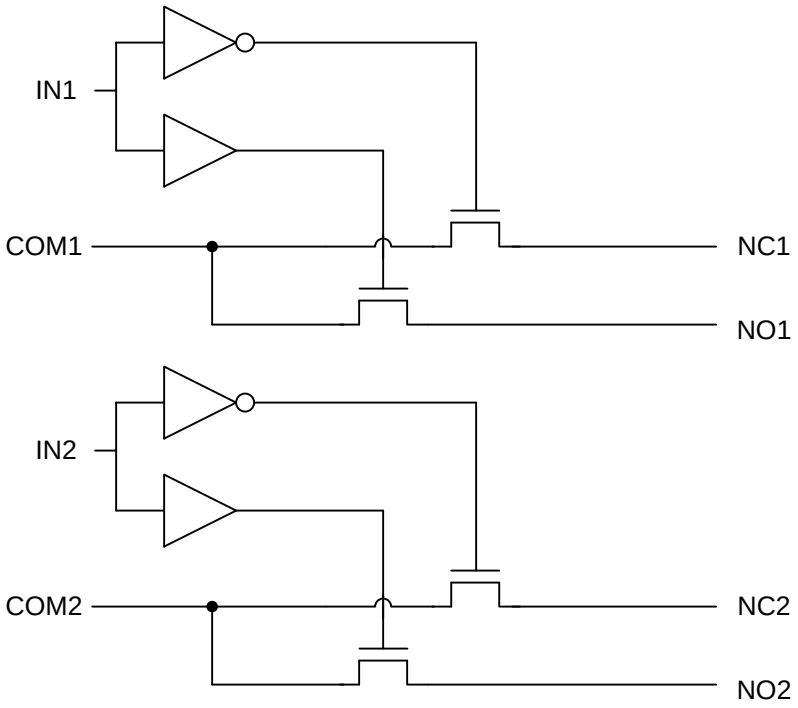
8 Detailed Description

8.1 Overview

The TS5A23157 is a dual single-pole-double-throw (SPDT) solid-state analog switch. The TS5A23157, like all analog switches, is bidirectional. When powered on, each COM pin is connected to its respective NC pin when the IN pin is low. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A23157 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A23157 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion. The control inputs are 5-V tolerant, allowing control signals to be present without V_{CC}.

8.4 Device Functional Modes

Table 1 lists the functional modes for TS5A23157.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3157 can be used in a variety of customer systems. The TS5A3157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

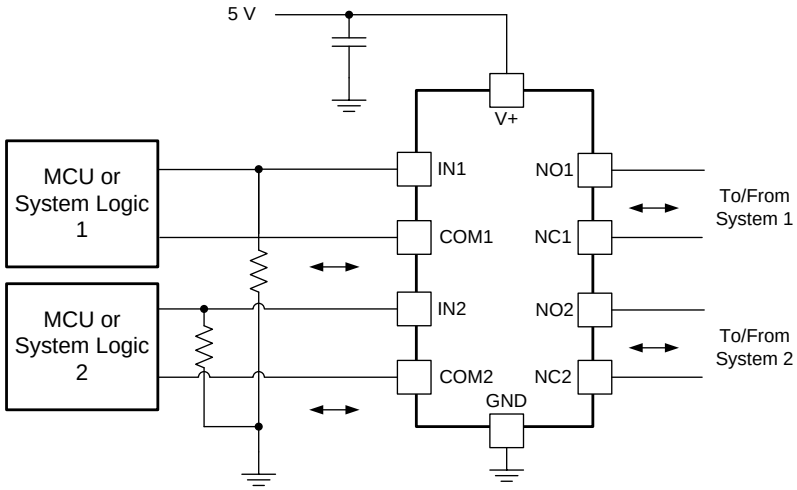


Figure 19. System Schematic for TS5A23157

9.2.1 Design Requirements

In this particular application, V_+ was 5 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (continued)

9.2.3 Application Curve

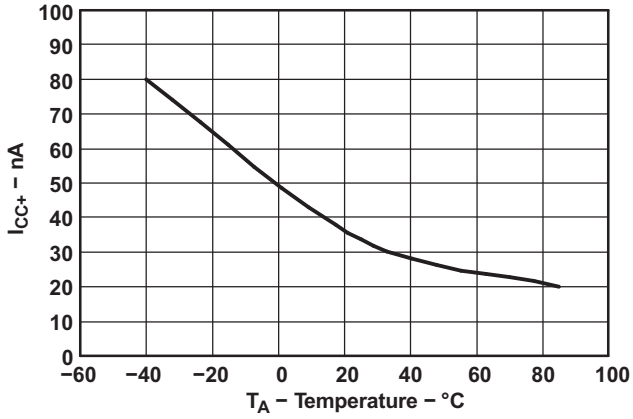


Figure 20. Power-Supply Current vs Temperature (V_+ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

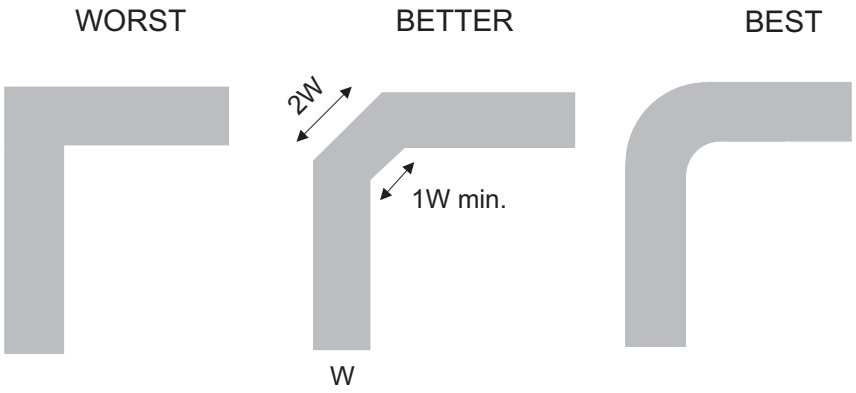


Figure 21. Trace Example

12 器件和文档支持

12.1 器件支持

12.1.1 器件命名规则

表 2. 参数 说明

符号	说明
V_{COM}	COM 处的电压
V_{NC}	NC 处的电压
V_{NO}	NO 处的电压
r_{on}	通道导通时 COM 和 NC 端口之间或 COM 和 NO 端口之间的电阻
Δr_{on}	通道间 r_{on} 的差值
$r_{on(flat)}$	额定条件范围下，同一通道内 r_{on} 最大值与最小值之间的差值
$I_{NC(OFF)}$	相应通道（NC 到 COM）处于关断状态时，在 NC 端口测得的泄漏电流在最坏输入和输出条件下
$I_{NO(OFF)}$	在最不理想的输入和输出条件下，相应通道（NO 到 COM）处于关断状态时，在 NO 端口测得的泄漏电流
$I_{NC(ON)}$	相应通道（NC 到 COM）处于导通状态且输出 (COM) 处于开路状态时在 NC 端口测量的泄漏电流
$I_{NO(ON)}$	相应通道（NO 到 COM）处于导通状态且输出 (COM) 处于开路状态时在 NO 端口测量的泄漏电流
$I_{COM(ON)}$	相应通道（NO 到 COM 或 NC 到 COM）处于导通状态且输出（NC 或 NO）处于开路状态时在 COM 端口测量的泄漏电流
V_{IH}	控制输入 (IN) 逻辑高电平的最小输入电压
V_{IL}	控制输入 (IN) 逻辑低电平的最小输入电压
V_{IN}	IN 处的电压
I_{IH}、I_{IL}	在 IN 处测量的泄漏电流
t_{ON}	开关导通时间。此参数是在额定条件范围下，开关导通时，通过数字控制 (IN) 信号和模拟输出 (COM/NC/NO) 信号之间的传播延迟测量得出。
t_{OFF}	开关关断时间。此参数是在额定条件范围下，开关关断时，通过数字控制 (IN) 信号和模拟输出 (COM/NC/NO) 信号之间的传播延迟测量得出。
t_{BBM}	先断后合时间。此参数是在额定条件范围下，控制信号改变状态时，通过两个相邻模拟通道（NC 和 NO）的输出之间的传播延迟测量得出。
Q_C	电荷注入是测量从控制 (IN) 输入到模拟（NC、NO、或 COM）输入产生的不需要的信号耦合的方法。电荷注入以库仑 (C) 为单位，可通过测量开关控制输入产生的总感应电荷得出该值。电荷注入，$Q_C = C_L \times \Delta V_O$，$C_L$ 是负载电容，ΔV_O 是模拟输出电压的变化。
$C_{NC(OFF)}$	相应通道（NC 到 COM）关断时 NC 端口的电容
$C_{NO(OFF)}$	相应通道（NC 到 COM）关断时 NO 端口的电容
$C_{NC(ON)}$	相应通道（NC 到 COM）导通时 NC 端口的电容
$C_{NO(ON)}$	相应通道（NC 到 COM）导通时 NO 端口的电容
$C_{COM(ON)}$	相应通道（COM 到 NC 或 COM 到 NO）导通时 COM 端口的电容
C_{IN}	IN 的电容
O_{ISO}	开关关断隔离用于衡量关断状态开关阻抗的大小。关断隔离以 dB 为单位，当相应通道（NC 到 COM 或 NO 到 COM）处于关断状态时，在额定频率下测量得出。关断隔离，$O_{ISO} = 20 \text{ LOG } (V_{NC}/V_{COM})$ dB，V_{COM} 是输入，V_{NC} 是输出。
X_{TALK}	串扰是测量从导通通道到关断通道（NC 到 NO 或 NO 到 NC）产生的不必要信号耦合的方法。串扰在额定频率下测量得出且以 dB 为单位。串扰，$X_{TALK} = 20 \text{ log } (V_{NC1}/V_{NO1})$，$V_{NO1}$ 是输入，V_{NC1} 是输出。
BW	开关带宽。这是导通通道增益低于直流增益 -3dB 时的频率。增益的计算方程式是 $20 \text{ log } (V_{NC}/V_{COM})$ dB，V_{NC} 是输出，V_{COM} 是输入。
I_+	静态电源电流，以及 V_+ 或 GND 的控制 (IN) 引脚
ΔI_+	这是在额定电压下的每个控制 (IN) 输入 I_+ 增量，而不是在 V_+ 或 GND 的控制输入增量。

表 3. 特性总结

配置	2:1 多路复用器/多路解复用器 (2 × SPDT)
通道数量	2
导通状态电阻 (r_{on})	10Ω

表 **3.** 特性总结 **(**接下页**)**

配置	**2:1** 多路复用器/多路解复用器 **(2 × SPDT)**
通道间的导通状态电阻匹配 (Δr_{on})	0.15Ω
导通状态电阻稳定性 ($r_{on(flat)}$)	4Ω
导通/关断时间 (t_{ON}/t_{OFF})	5.7ns/3.8ns
先断后合时间 (t_{BBM})	0.5ns
电荷注入 (Q_C)	7pC
带宽 (BW)	220MHz
关断 (O_{SIO})	10MHz 时为 –65dB
串扰 9XTALK）	10MHz 时为 –66dB
总谐波失真 (THD)	0.01%
泄漏电流 ($I_{COM(OFF)}/I_{NC(OFF)}$)	±1μA
封装选项	10 引脚 DGS 和 RSE

12.2 文档支持

12.2.1 相关文档

如需相关文档，请参阅：

- 《*CMOS 输入缓慢变化或悬空的影响*》，SCBA004

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A23157DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(3BR, JBR)
TS5A23157DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(3BR, JBR)
TS5A23157DGSRG4	Active	Production	VSSOP (DGS) | 10	2500 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR
TS5A23157DGSRG4.B	Active	Production	VSSOP (DGS) | 10	2500 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR
TS5A23157RSER	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO
TS5A23157RSER.B	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO
TS5A23157RSERG4.B	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TS5A23157 :

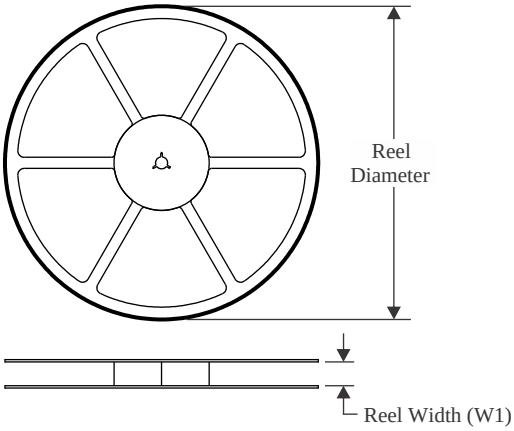
- Automotive : TS5A23157-Q1

NOTE: Qualified Version Definitions:

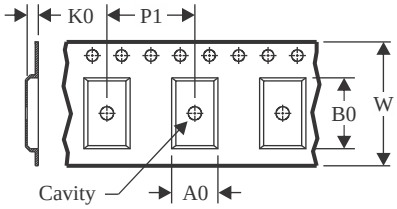
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

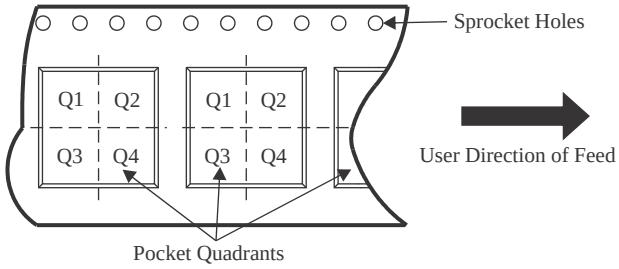


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

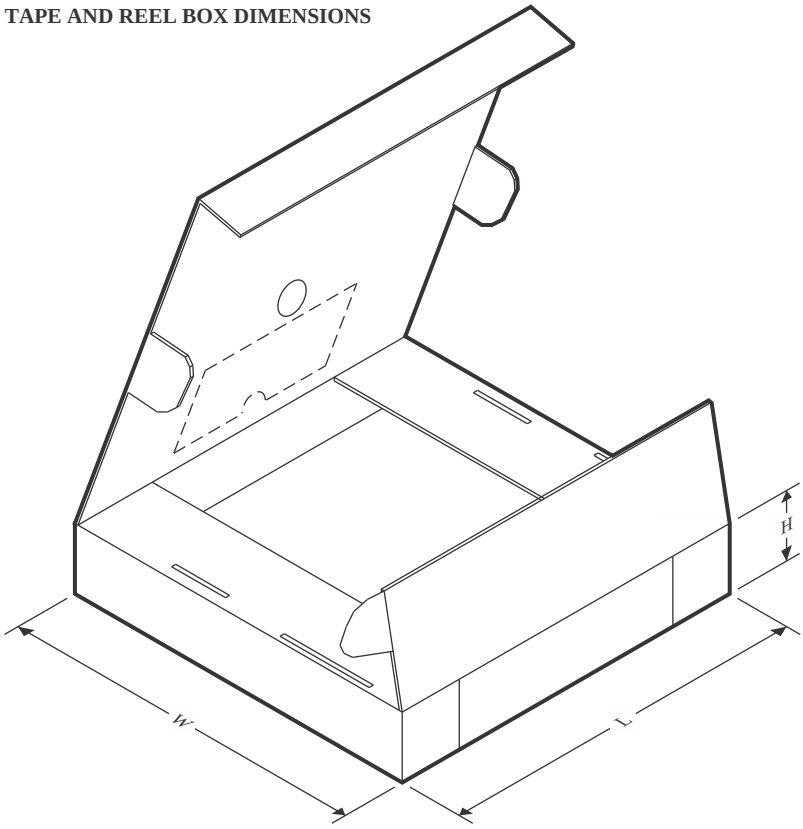
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TS5A23157RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

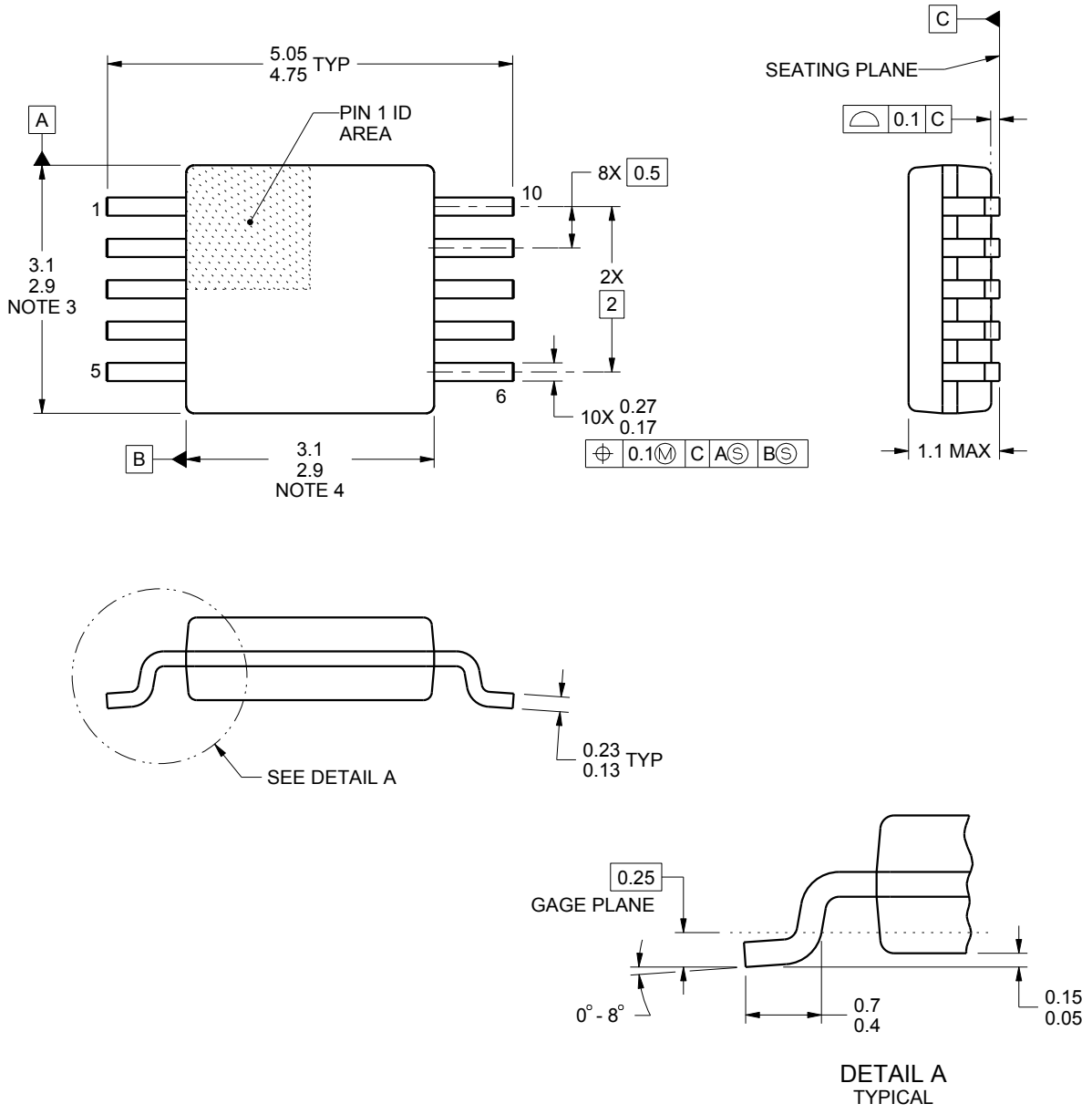
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23157DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TS5A23157RSER	UQFN	RSE	10	3000	189.0	185.0	36.0

PACKAGE OUTLINE

DGS0010A

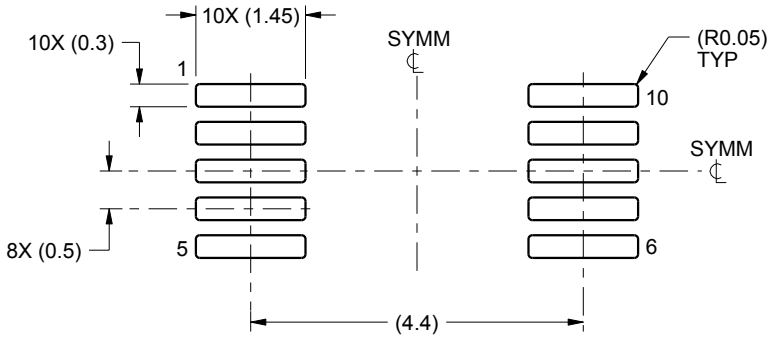
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

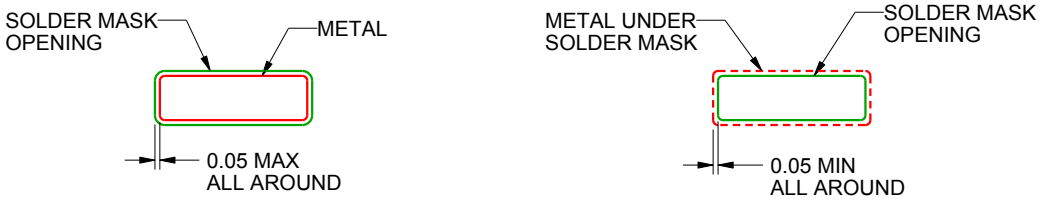


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

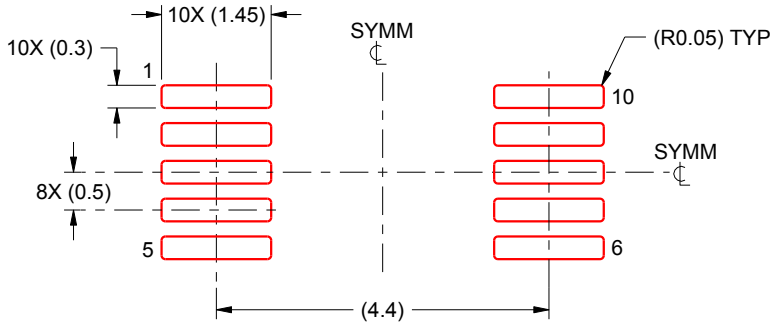


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

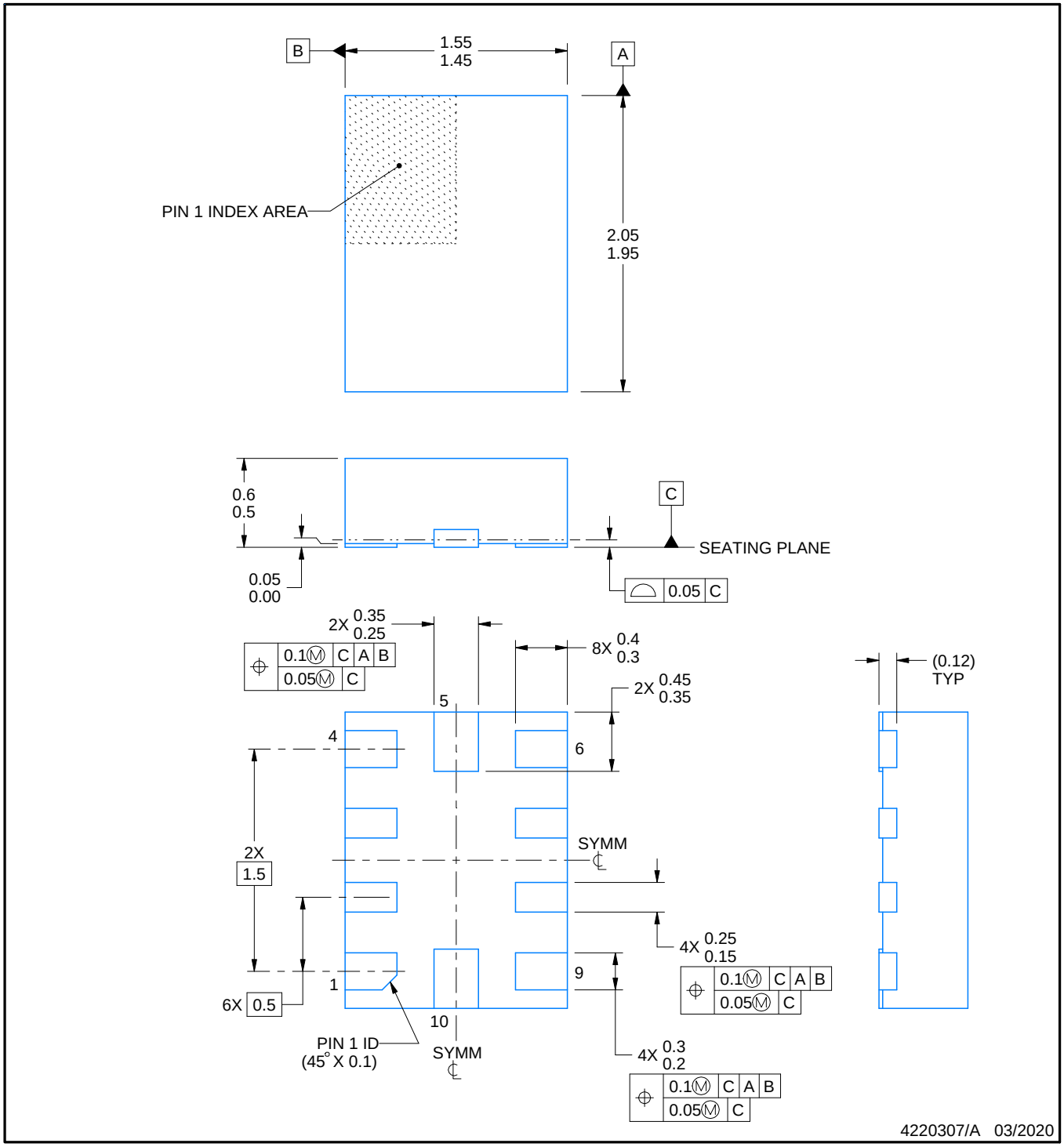
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RSE0010A

PACKAGE OUTLINE

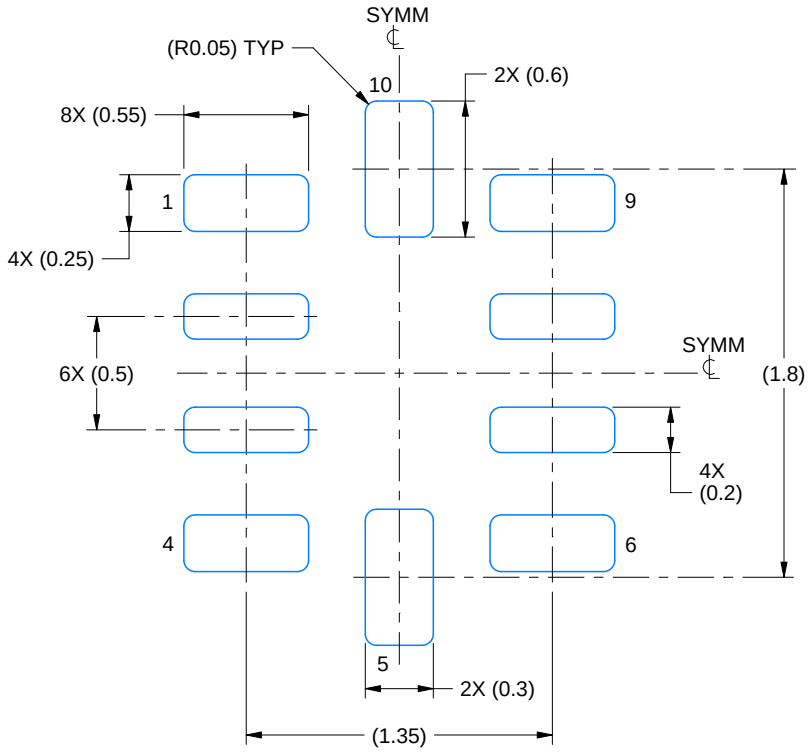
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

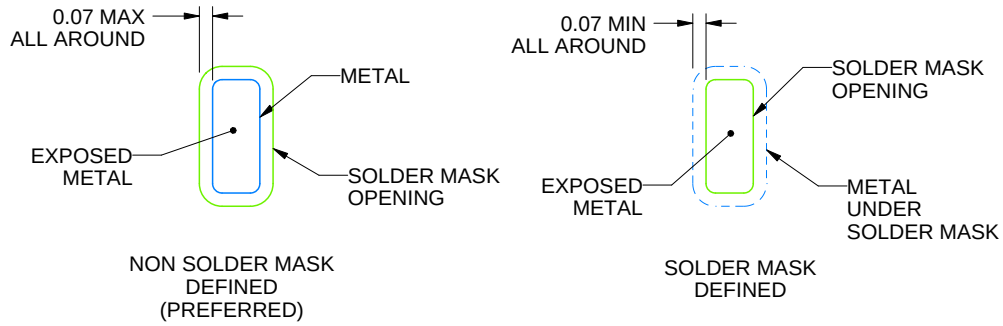


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

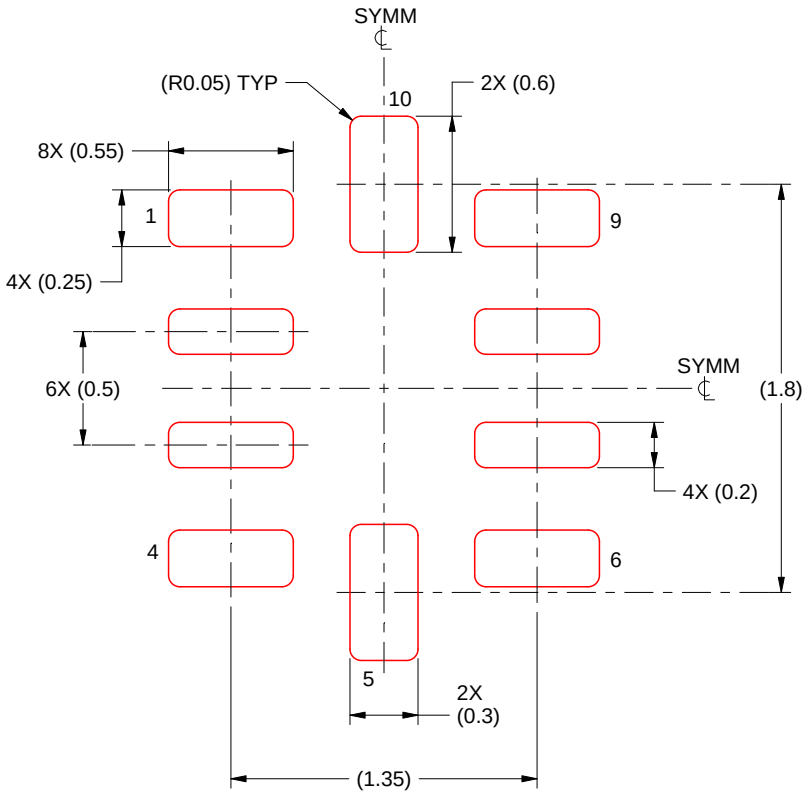


SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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