

TS3A24159 0.3Ω 双通道 SPDT 双向模拟开关 双通道 2:1 多路复用器和多路信号分离器

1 特性

- 指定的先断后合开关
- 低导通电阻 (最大值为 0.3Ω)
- 低电荷注入
- 出色的导通状态电阻匹配
- 低总谐波失真 (THD)
- 1.65V 至 3.6V 单电源运行
- 控制输入兼容 1.8V 逻辑
- 闩锁性能超过 100 mA, 符合 JESD 78 II 类规范
- ESD 性能经测试符合 JESD 22 规范
 - 2000V 人体放电模型 (A114-B, II 类)
 - 1000V 带电器件模型 (C101)

2 应用

- [手机](#)
- 个人数字助理 (PDA)
- [便携式仪器](#)
- [音频和视频信号路由](#)
- [低压数据采集系统](#)
- [通信电路](#)
- [调制解调器](#)
- [硬盘](#)
- [计算机外设](#)
- [无线终端和外设](#)

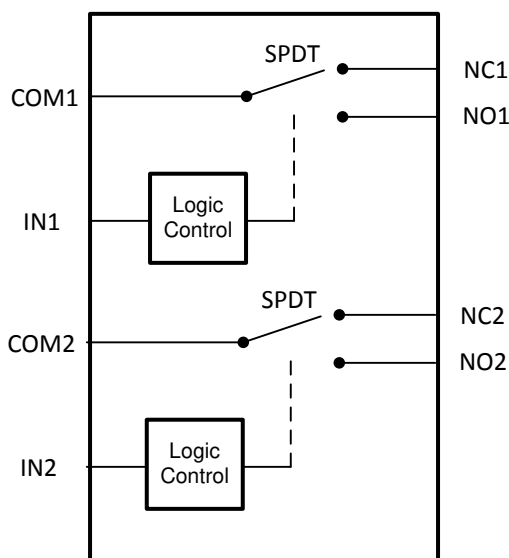
3 说明

TS3A24159 器件是一款 2 通道单极双投 (SPDT) 双向模拟开关, 设计的工作电压为 1.65V 至 3.6V。该器件提供低通态电阻和出色的通态电阻匹配以及先断后合功能, 能够防止信号从一个通道传输至另一通道时失真。该器件具有出色的总谐波失真 (THD) 性能、低通态电阻和极低的功耗。该器件所具备的一些特性使其适用于各种市场和不同的应用。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TS3A24159	VSSOP (10)	3.00mm × 3.00mm
	VSON (10)	3.00mm × 3.00mm
	DSBGA (10)	1.86mm × 1.35mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



功能方框图



Table of Contents

1 特性	1	8.2 Functional Block Diagram	18
2 应用	1	8.3 Feature Description	18
3 说明	1	8.4 Device Functional Modes	18
4 Revision History	2	9 Application and Implementation	19
5 Pin Configuration and Functions	3	9.1 Application Information.....	19
6 Specifications	5	9.2 Typical Application.....	19
6.1 Absolute Maximum Ratings.....	5	10 Power Supply Recommendations	20
6.2 ESD Ratings.....	5	11 Layout	21
6.3 Recommended Operating Conditions.....	5	11.1 Layout Guidelines.....	21
6.4 Thermal Information.....	6	11.2 Layout Example.....	21
6.5 Electrical Characteristics for 3-V Supply.....	6	12 Device and Documentation Support	22
6.6 Electrical Characteristics for 2.5-V Supply.....	7	12.1 Documentation Support.....	22
6.7 Electrical Characteristics for 1.8-V Supply.....	9	12.2 接收文档更新通知.....	22
6.8 Switching Characteristics for a 3-V Supply.....	10	12.3 支持资源.....	22
6.9 Switching Characteristics for a 2.5-V Supply.....	10	12.4 Trademarks.....	22
6.10 Switching Characteristics for a 1.8-V Supply.....	11	12.5 Electrostatic Discharge Caution.....	22
6.11 Typical Characteristics.....	12	12.6 术语表.....	22
7 Parameter Measurement Information	14	13 Mechanical, Packaging, and Orderable Information	22
8 Detailed Description	18		
8.1 Overview.....	18		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (February 2022) to Revision H (August 2022)	Page
• Changed the maximum V_{CC} from: 3.6 V to: 4 V	5
Changes from Revision F (September 2019) to Revision G (February 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Updated the part number in the <i>Detailed Design Procedure</i>	20
Changes from Revision E (March 2019) to Revision F (September 2019)	Page
• Changed the YZP package image view From: Top-Through View To: Bottom View.....	3
Changes from Revision D (July 2015) to Revision E (March 2019)	Page
• Changed the YZP package image and deleted the <i>YZP Package, Terminal Assignments</i> table.....	3
• Changed Turnon time V_{CC} (Full) value From: 2.3 V to 2.7 V To: 2.7 V to 3.6 V in <i>Switching Characteristics for a 3-V Supply</i>	10
• Changed Turnon time V_{CC} (Full) value From: 2.3 V to 2.7 V To: 2.7 V to 3.6 V in <i>Switching Characteristics for a 2.5-V Supply</i>	10
Changes from Revision C (February 2008) to Revision D (March 2015)	Page
• 添加了 引脚配置和功能 部分、ESD 等级表、特性说明 部分、器件功能模式、应用和实施 部分、电源相关建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分.....	1
• 通篇将 V+ 改为 V_{CC} 以符合 JEDEC 标准.....	1

5 Pin Configuration and Functions

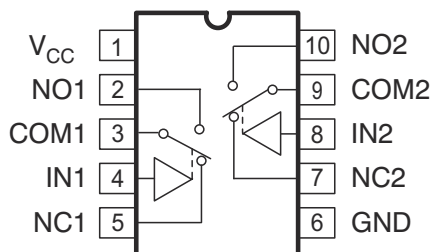


图 5-1. DGS Package, 10-Pin VSSOP (Top View)

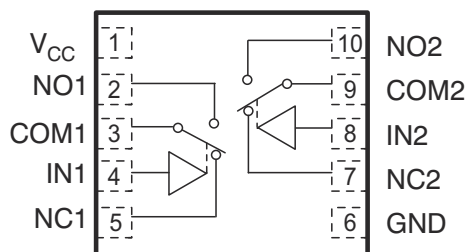


图 5-2. DRC Package, 10-Pin VSON (Top View)

表 5-1. Pin Functions - VSSOP and VSON

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	V _{CC}	—	Power supply
2	NO1	I/O	Normally open signal path
3	COM1	I/O	Common signal path
4	IN1	I	Digital control to connect COM to NO or NC
5	NC1	I/O	Normally closed signal path
6	GND	—	Ground
7	NC2	I/O	Normally closed signal path
8	IN2	I	Digital control to connect COM to NO or NC
9	COM2	I/O	Common signal path
10	NO2	I/O	Normally open signal path

(1) I = input, O = output

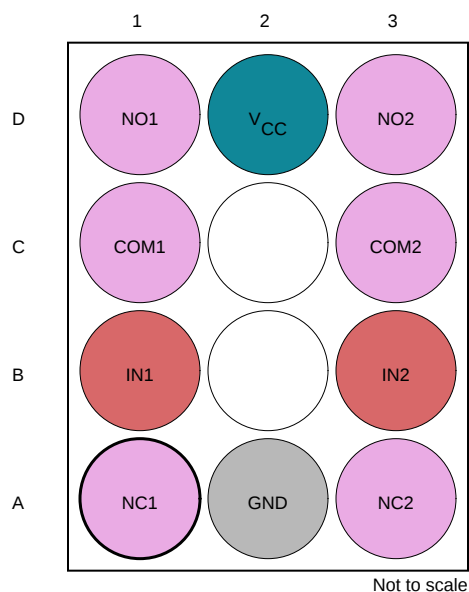


图 5-3. YZP Package, 10-Pin DSBGA (Bottom View)

Legend	
Input or Output	Input
Ground	Power

表 5-2. Pin Functions - DSBGA

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
A1	NC1	I/O	Normally closed signal path
A2	GND	—	Ground
A3	NC2	I/O	Normally closed signal path
B1	IN1	I	Digital control to connect COM to NO or NC
B3	IN2	I	Digital control to connect COM to NO or NC
C1	COM1	I/O	Common signal path
C3	COM2	I/O	Common signal path
D1	NO1	I/O	Normally open signal path
D2	V _{CC}	—	Power supply
D3	NO2	I/O	Normally open signal path

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽³⁾		- 0.5	4	V
V_{NC} V_{NO} V_{COM}	Signal voltage ⁽³⁾ ⁽⁴⁾		- 0.5	$V_{CC} + 0.5$	V
$I_{I/O}$	Analog port diode current	$V_{NC}, V_{NO}, V_{COM} < 0$	- 50	50	mA
I_{NC} I_{NO} I_{COM}	ON-state switch current ON-state peak switch current ⁽⁵⁾	$V_{NC}, V_{NO}, V_{COM} = 0 \text{ to } V_{CC}$	- 300 - 500	300 500	mA
V_{IN}	Digital input voltage		- 0.5	3.6	V
I_{IK}	Digital input clamp current ⁽³⁾	$V_I < 0$	- 50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		- 100		mA
T_{stg}	Storage temperature		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) This value is limited to 5.5 V maximum.
- (5) Pulse at 1-ms duration <10% duty cycle.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 ⁽²⁾	1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	1.65	3.6	V
V_{NC} V_{NO} V_{COM}	Signal Voltage	0	V_{CC}	V
V_{IN}	Digital Input Voltage	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS3A24159			UNIT
		DGS (VSSOP)	DRC (VSON)	YZP (DSBGA)	
		10 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154	49.4	90.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.9	71.2	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.6	23.8	8.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	2.2	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.2	23.8	8.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics for 3-V Supply

$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITIONS		T _A	V _{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V _{COM} , V _{NO} , V _{NC}					0		V _{CC}	V
Peak ON resistance	r _{peak}	0 ≤ (V _{NO} or V _{NC}) ≤ V _{CC} , I _{COM} = - 100 mA,	Switch ON, See 图 7-1	25°C Full	2.7 V	0.2	0.3	0.35	Ω
ON-state resistance	r _{on}	V _{NO} or V _{NC} = 2 V, I _{COM} = - 100 mA,	Switch ON, See 图 7-1	25°C Full	2.7 V	0.26	0.3	0.34	Ω
ON-state resistance match between channels	Δ r _{on}	V _{NO} or V _{NC} = 2 V, 0.8 V, I _{COM} = - 100 mA,	Switch ON, See 图 7-1	25°C Full	2.7 V	0.01	0.05	0.05	Ω
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NO} or V _{NC}) ≤ V _{CC} , I _{COM} = - 100 mA,	Switch ON, See 图 7-1	25°C	2.7 V	0.13			Ω
		V _{NO} or V _{NC} = 2 V, 0.8 V, I _{COM} = - 100 mA,	Switch ON, See 图 7-1	25°C		0.01	0.04	Ω	
			Full			0.05			
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 1 V, V _{COM} = 3 V, or V _{NC} or V _{NO} = 3 V, V _{COM} = 1 V,	Switch OFF, See 图 7-2	25°C Full	3.6 V	- 10		10	nA
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 1 V, V _{COM} = Open, or V _{NC} or V _{NO} = 3 V, V _{COM} = Open,	Switch ON, See 图 7-3	25°C Full	3.6 V	- 10		10	nA
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 1 V, or V _{NC} or V _{NO} = Open, V _{COM} = 3 V,	Switch ON, See 图 7-3	25°C Full	3.6 V	- 10		10	nA
DIGITAL CONTROL INPUTS (IN1, IN2) ⁽²⁾									
Input logic high	V _{IH}			Full		1.4			V
Input logic low	V _{IL}			Full			0.5		V
Input leakage current	I _{IH} , I _{IL}	V _I = 3.6 V or 0		25°C Full	3.6 V	- 40	5	40	nA
						- 50		50	

6.5 Electrical Characteristics for 3-V Supply (continued)

$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC							
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1 \text{ nF}$, See 图 7-10	25°C	3 V	9		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_{CC}$ or GND, Switch OFF,	See 图 7-4	25°C	3 V	90	pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_{CC}$ or GND, Switch ON,	See 图 7-4	25°C	3 V	224	pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND, Switch ON,	See 图 7-4	25°C	3 V	250	pF
Digital input capacitance	C_I	$V_{IN} = V_{CC}$ or GND,	See 图 7-4	25°C	3 V	2	pF
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON,	See 图 7-7	25°C	3 V	23	MHz
OFF isolation	O_{ISO}	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	See 图 7-8	25°C	3 V	- 72	dB
Crosstalk	X_{TALK}	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	See 图 7-9	25°C	3 V	- 96	dB
Total harmonic distortion	THD	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$,	$f = 20 \text{ Hz to } 20 \text{ kHz}$, See 图 7-11	25°C	3 V	0.003%	
SUPPLY							
Positive supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	25°C	3.6 V	15	100	nA
			Full		1		μA

- (1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
 (2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

6.6 Electrical Characteristics for 2.5-V Supply

$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS		T _A	V _{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH								
Analog signal range	V _{COM} , V _{NO} , V _{NC}				0		V _{CC}	V
Peak ON resistance	r _{peak}	0 ≤ (V _{NO} or V _{NC}) ≤ V _{CC} , I _{COM} = − 8 mA,	Switch ON, See 图 7-1	25°C Full	2.3 V	0.35 0.45		Ω
ON-state resistance	r _{on}	V _{NO} or V _{NC} = 1.8 V, I _{COM} = − 8 mA,	Switch ON, See 图 7-1	25°C Full		2.3 V	0.4	
ON-state resistance match between channels	Δ r _{on}	V _{NO} or V _{NC} = 1.8 V, 0.8 V, I _{COM} = − 8 mA,	Switch ON, See 图 7-1	25°C Full	2.3 V		0.01 0.05 0.05 0.05	
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NO} or V _{NC}) ≤ V _{CC} , I _{COM} = − 8 mA,	Switch ON, See 图 7-1	25°C		2.3 V	0.05	
		V _{NO} or V _{NC} = 0.8 V, 1.8 V, I _{COM} = − 8 mA,	Switch ON, See 图 7-1	25°C	0.03 0.08			
				Full	0.1			
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 0.5 V, V _{COM} = 2.2 V, or V _{NC} or V _{NO} = 2.2 V, V _{COM} = 0.5 V,	Switch OFF, See 图 7-2	25°C Full	2.7 V	− 10 10 − 50 50		nA

6.6 Electrical Characteristics for 2.5-V Supply (continued)

$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITIONS		T _A	V _{CC}	MIN TYP MAX			UNIT
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 0.5 V, V _{COM} = Open, or V _{NC} or V _{NO} = 2.2 V, V _{COM} = Open, Switch ON, See 图 7-3		25°C	2.7 V	- 10 10			nA
				Full		- 100 100			
ANALOG SWITCH (continued)									
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 0.5 V, or V _{NC} or V _{NO} = Open, V _{COM} = 2.2 V, Switch ON, See 图 7-3		25°C	2.7 V	- 10 10			nA
				Full		- 100 100			
DIGITAL CONTROL INPUTS (IN1, IN2) ⁽²⁾									
Input logic high	V _{IH}			Full		1.25			V
Input logic low	V _{IL}			Full		0.5			V
Input leakage current	I _{IH} , I _{IL}	V _I = 2.7 V or 0		25°C	2.7 V	- 40 5 40			nA
				Full		- 50 50			
DYNAMIC									
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0, C _L = 1 nF, See 图 7-10		25°C	2.5 V	8			pC
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V _{CC} or GND, Switch OFF, See 图 7-4		25°C	2.5 V	90			pF
NC, NO ON capacitance	C _{NC(ON)} , C _{NO(ON)}	V _{NC} or V _{NO} = V _{CC} or GND, Switch ON, See 图 7-4		25°C	2.5 V	250			pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V _{CC} or GND, Switch ON, See 图 7-4		25°C	2.5 V	250			pF
Digital input capacitance	C _I	V _I = V _{CC} or GND, See 图 7-4		25°C	2.5 V	2			pF
Bandwidth	BW	R _L = 50 Ω, Switch ON, See 图 7-7		25°C	2.5 V	23			MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz, See 图 7-8		25°C	2.5 V	- 72			dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz, See 图 7-9		25°C	2.5 V	- 96			dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF, f = 20 Hz to 20 kHz, See 图 7-11		25°C	2.5 V	0.003%			
SUPPLY									
Positive supply current	I _{CC}	V _I = V _{CC} or GND		25°C	2.7 V	10 100			nA
				Full		700			

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

6.7 Electrical Characteristics for 1.8-V Supply

$V_{CC} = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
Analog signal range	V_{COM}, V_{NO}, V_{NC}			0		V_{CC}	V
Peak ON resistance	r_{peak}	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_{CC}$, $I_{COM} = -2\text{ mA}$, Switch ON, See 图 7-1	25°C Full	1.65 V	0.4	0.7 0.8	Ω
ON-state resistance	r_{on}	$V_{NO} \text{ or } V_{NC} = 1.5\text{ V}$, $I_{COM} = -2\text{ mA}$, Switch ON, See 图 7-1	25°C Full	1.65 V	0.3	0.45 0.5	Ω
ANALOG SWITCH (continued)							
ON-state resistance match between channels	Δr_{on}	$V_{NO} \text{ or } V_{NC} = 0.6\text{ V}, 1.5\text{ V}$, $I_{COM} = -2\text{ mA}$, Switch ON, See 图 7-1	25°C Full	1.65 V	0.02	0.04 0.05	Ω
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_{CC}$, $I_{COM} = -2\text{ mA}$, Switch ON, See 图 7-1	25°C	1.65 V	0.13	0.08 0.15	Ω
		$V_{NO} \text{ or } V_{NC} = 0.6\text{ V}, 1.5\text{ V}$, $I_{COM} = -8\text{ mA}$, Switch ON, See 图 7-1	25°C Full		0.2		
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0.3\text{ V}, V_{COM} = 1.65\text{ V}$, or $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}, V_{COM} = 0.3\text{ V}$, Switch OFF, See 图 7-2	25°C Full	1.95	- 10	10 50	nA
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0.3\text{ V}, V_{COM} = \text{Open}$, or $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}, V_{COM} = \text{Open}$, Switch ON, See 图 7-3	25°C Full	1.95 V	- 10	10 100	nA
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}, V_{COM} = 0.3\text{ V}$, or $V_{NC} \text{ or } V_{NO} = \text{Open}, V_{COM} = 1.65\text{ V}$, Switch ON, See 图 7-3	25°C Full	1.95 V	- 10	10 100	nA
DIGITAL CONTROL INPUTS (IN1, IN2) ⁽²⁾							
Input logic high	V_{IH}		Full		1		V
Input logic low	V_{IL}		Full			0.4	V
Input leakage current	I_{IH}, I_{IL}	$V_I = 1.95\text{ V or }0$	25°C Full	1.95 V	- 40	5 40 50	nA
DYNAMIC							
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1\text{ nF}$, See 图 7-10	25°C	1.8 V		5	pC
NC, NO OFF capacitance	$C_{NC(OFF)}, C_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = V_{CC} \text{ or GND}$, Switch OFF, See 图 7-4	25°C	1.8 V		90	pF
NC, NO ON capacitance	$C_{NC(ON)}, C_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = V_{CC} \text{ or GND}$, Switch ON, See 图 7-4	25°C	1.8 V		250	pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC} \text{ or GND}$, Switch ON, See 图 7-4	25°C	1.8 V		250	pF
Digital input capacitance	C_{IN}	$V_I = V_{CC} \text{ or GND}$, See 图 7-4	25°C	1.8 V		2	pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON, See 图 7-7	25°C	1.8 V		23	MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$, See 图 7-8	25°C	1.8 V		- 73	dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$, See 图 7-9	25°C	1.8 V		- 97	dB

6.7 Electrical Characteristics for 1.8-V Supply (continued)

$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS		T _A	V _{CC}	MIN	TYP	MAX	UNIT
Total harmonic distortion THD	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz, See 图 7-11	25°C	1.8 V	0.005%			
SUPPLY								
Positive supply current I _{CC}	V _I = V _{CC} or GND	25°C	1.95 V	100	50	nA		
		Full		700				

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

6.8 Switching Characteristics for a 3-V Supply

$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic							
Turnon time t_{ON}	$V_{COM} = V_{CC}$, $R_L = 50 \, \Omega$, $C_L = 35 \text{ pF}$, See 图 7-5	25°C	3.0 V	20		35	ns
		Full	2.7 V to 3.6 V			40	
Turnoff time t_{OFF}	$V_{COM} = V_{CC}$, $R_L = 50 \, \Omega$, $C_L = 35 \text{ pF}$, See 图 7-5	25°C	3.0 V	12		25	ns
		Full	2.7 V to 3.6 V			30	
Break-before-make time t_{BBM}	$V_{NC} = V_{NO} = V_{CC}$, $R_L = 50 \, \Omega$, $C_L = 35 \text{ pF}$, See 图 7-6	25°C	3.0 V	1	10	25	ns
		Full	2.7 V to 3.6 V	0.5		30	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.9 Switching Characteristics for a 2.5-V Supply

$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic							
Turnon time t_{ON}	$V_{COM} = V_{CC}$, $R_L = 50 \, \Omega$, $C_L = 35 \text{ pF}$, See 图 7-5	25°C	2.5 V	23		45	ns
		Full	2.3 V to 2.7 V			50	
Turnoff time t_{OFF}	$V_{COM} = V_{CC}$, $R_L = 50 \, \Omega$, $C_L = 35 \text{ pF}$, See 图 7-5	25°C	2.5 V	17		27	ns
		Full	2.3 V to 2.7 V			30	
Break-before-make time t_{BBM}	$V_{NC} = V_{NO} = V_{CC}$, $R_L = 50 \, \Omega$, $C_L = 35 \text{ pF}$, See 图 7-6	25°C	2.5 V	2	14	30	ns
		Full	2.3 V to 2.7 V	1		35	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.10 Switching Characteristics for a 1.8-V Supply

$V_{CC} = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic							
Turnon time t_{ON}	$V_{COM} = V_{CC}$, $R_L = 50\ \Omega$ $C_L = 35\text{ pF}$, See 图 7-5	25°C	1.8 V		53	75	ns
		Full	1.65 V to 1.96 V			80	
Turnoff time t_{OFF}	$V_{COM} = V_{CC}$, $R_L = 50\ \Omega$ $C_L = 35\text{ pF}$, See 图 7-5	25°C	1.8 V		24	35	ns
		Full	1.65 V to 1.96 V			40	
Break-before- make time t_{BBM}	$V_{NC} = V_{NO} = V_{CC}$, $R_L = 50\ \Omega$ $C_L = 35\text{ pF}$, See 图 7-6	25°C	1.8 V	2	30	40	ns
		Full	1.65 V to 1.96 V	1		50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.11 Typical Characteristics

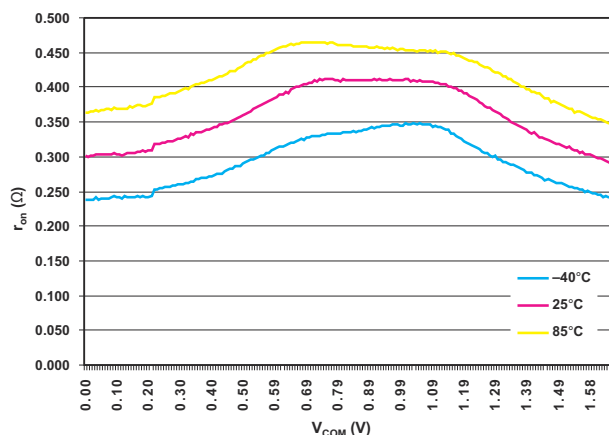
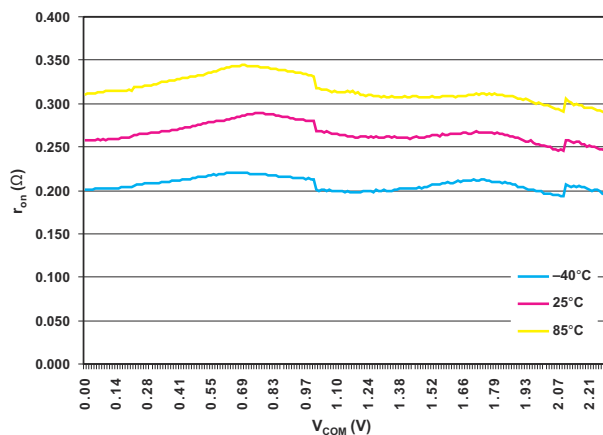
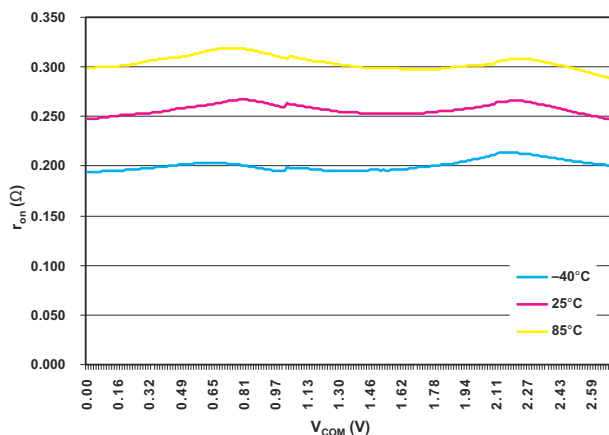
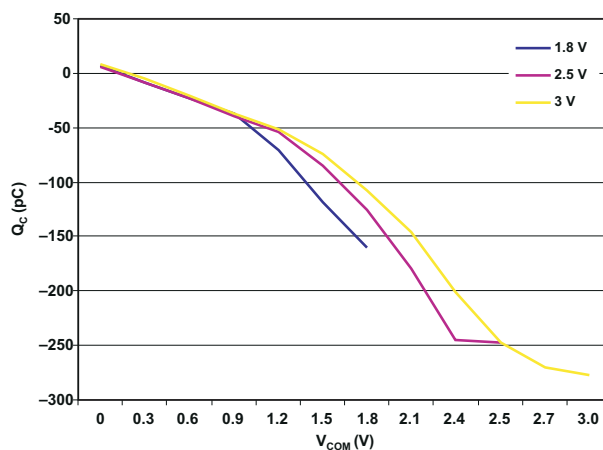
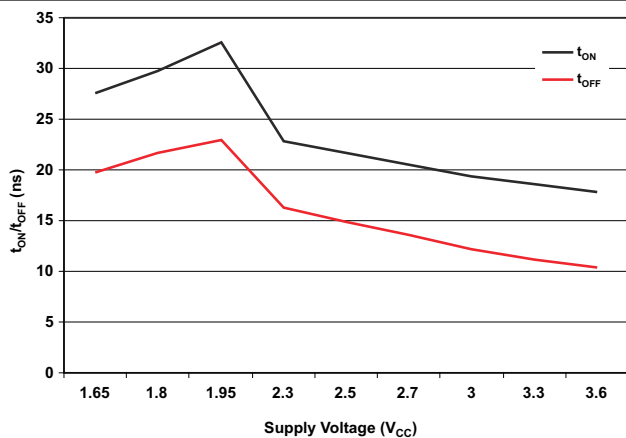
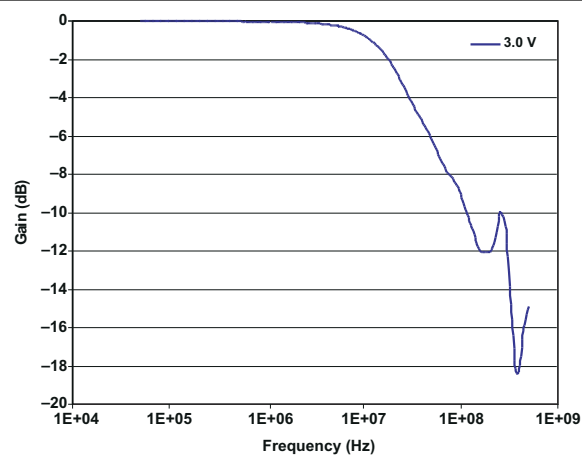
图 6-1. r_{on} vs V_{COM} ($V_{CC} = 1.65$ V)图 6-2. r_{on} vs V_{COM} ($V_{CC} = 2.3$ V)图 6-3. r_{on} vs V_{COM} ($V_{CC} = 2.7$ V)图 6-4. Charge Injection (Q_C) vs V_{COM} ($T_A = 25^\circ\text{C}$)图 6-5. t_{ON} and t_{OFF} vs Supply Voltage ($T_A = 25^\circ\text{C}$)

图 6-6. Bandwidth

6.11 Typical Characteristics (continued)

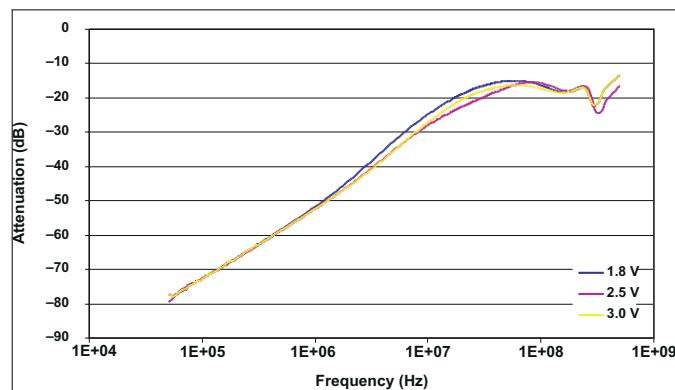


图 6-7. OFF Isolation

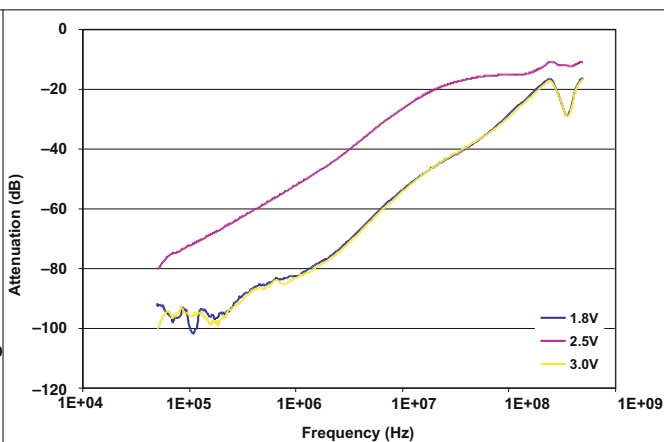


图 6-8. Crosstalk

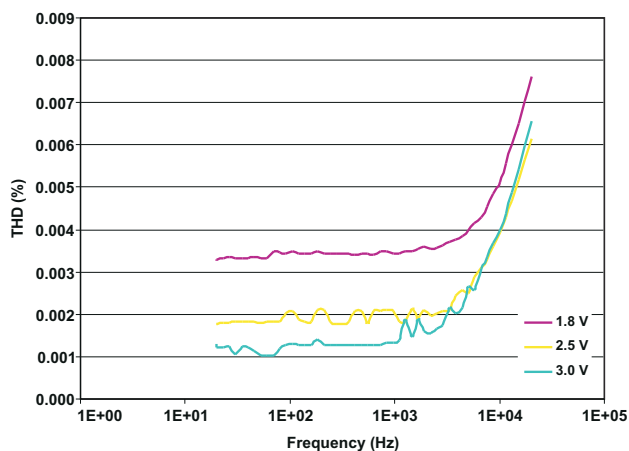


图 6-9. Total Harmonic Distortion vs Frequency

7 Parameter Measurement Information

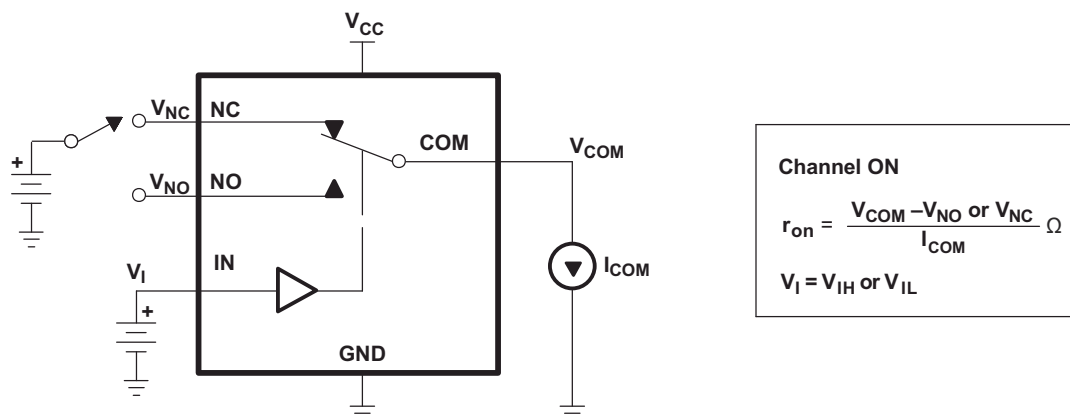


图 7-1. ON-State Resistance

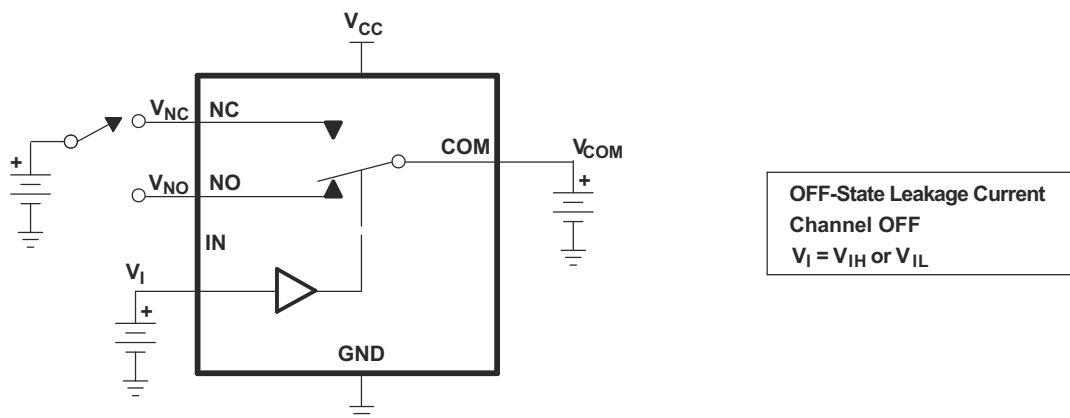


图 7-2. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

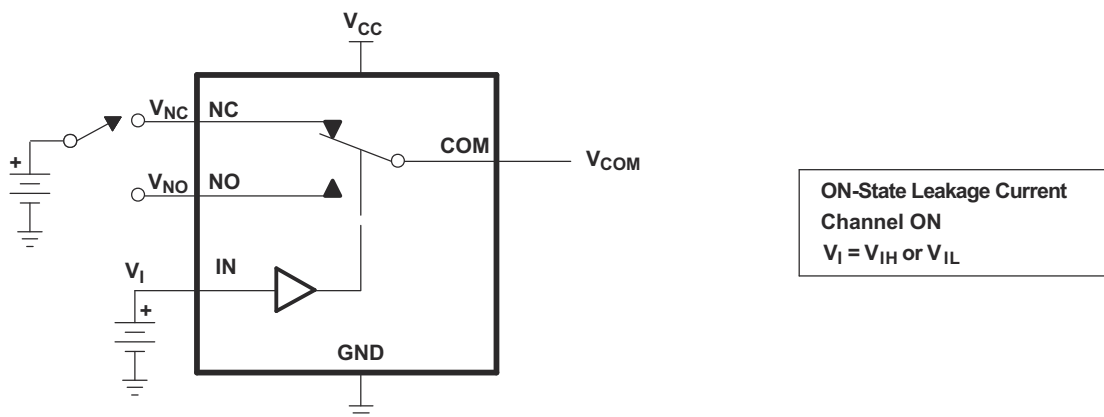


图 7-3. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

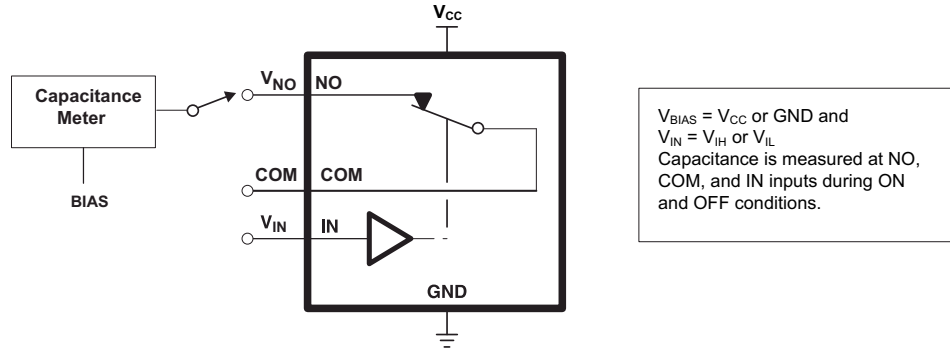
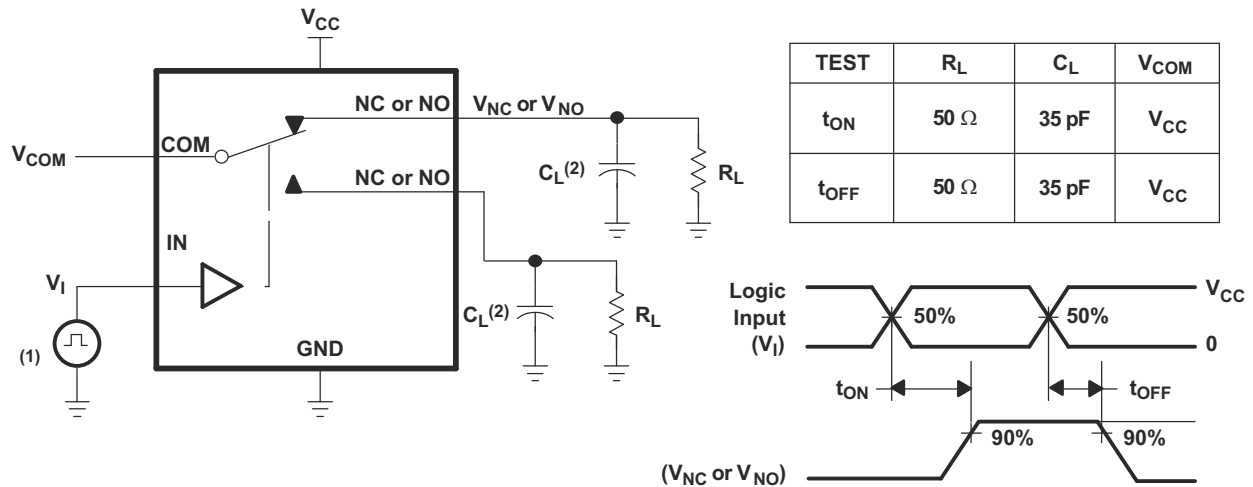
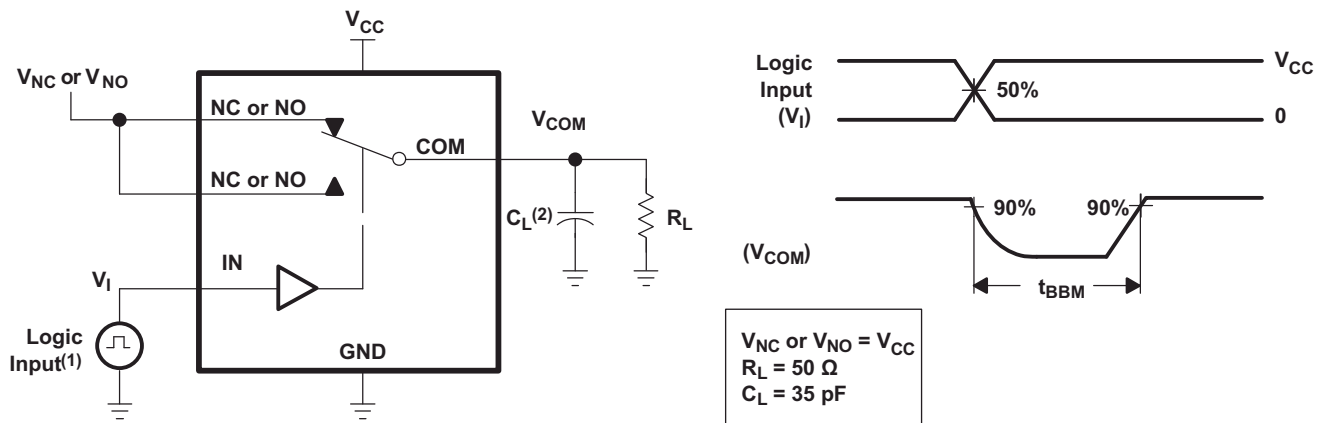


图 7-4. Capacitance C_I , $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$



- A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
 B. C_L includes probe and jig capacitance.

图 7-5. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



- A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
 B. C_L includes probe and jig capacitance.

图 7-6. Break-Before-Make Time (t_{BBM})

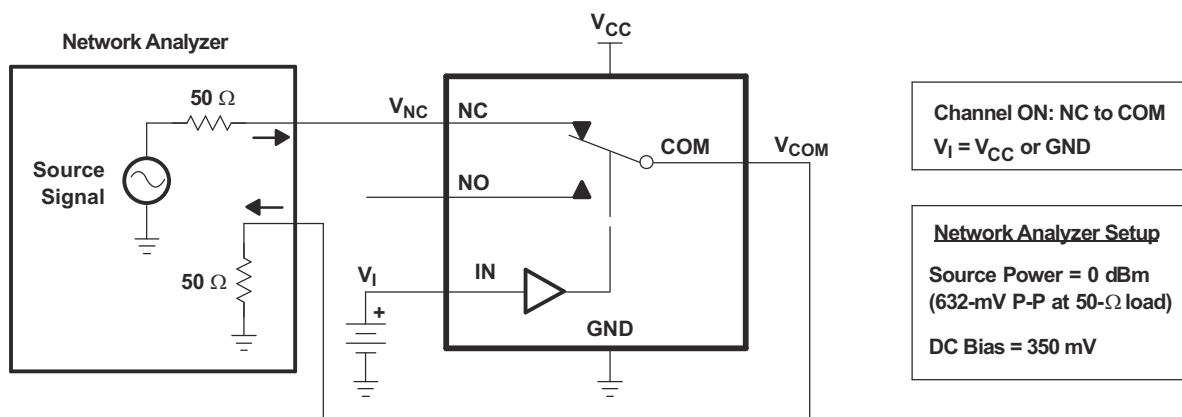
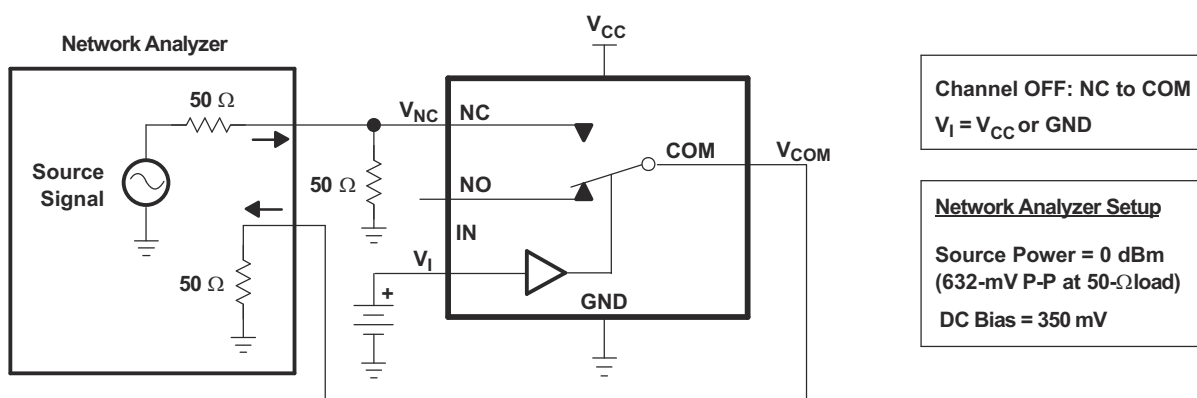
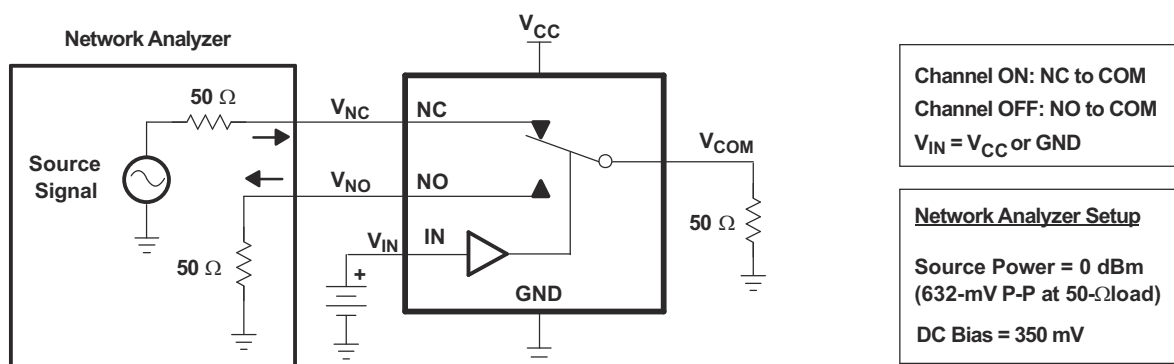
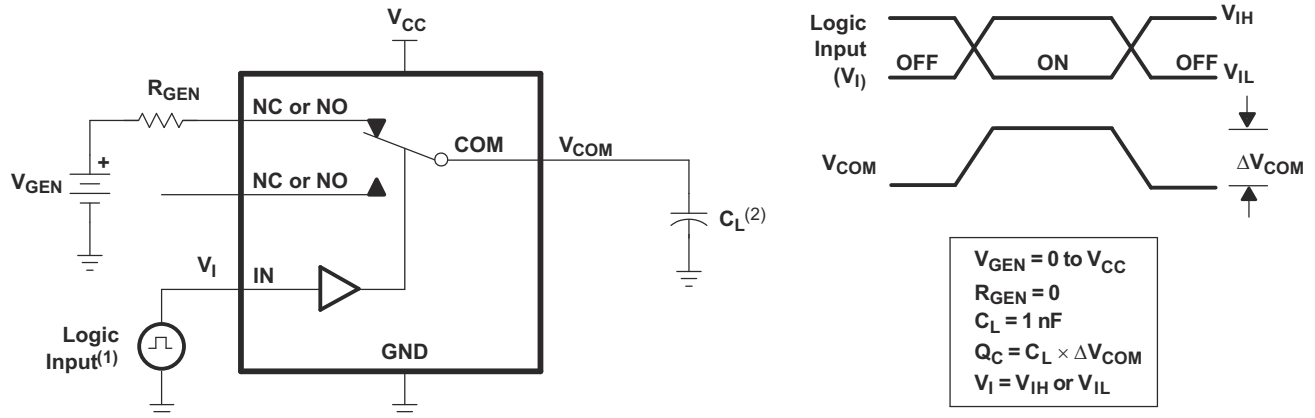


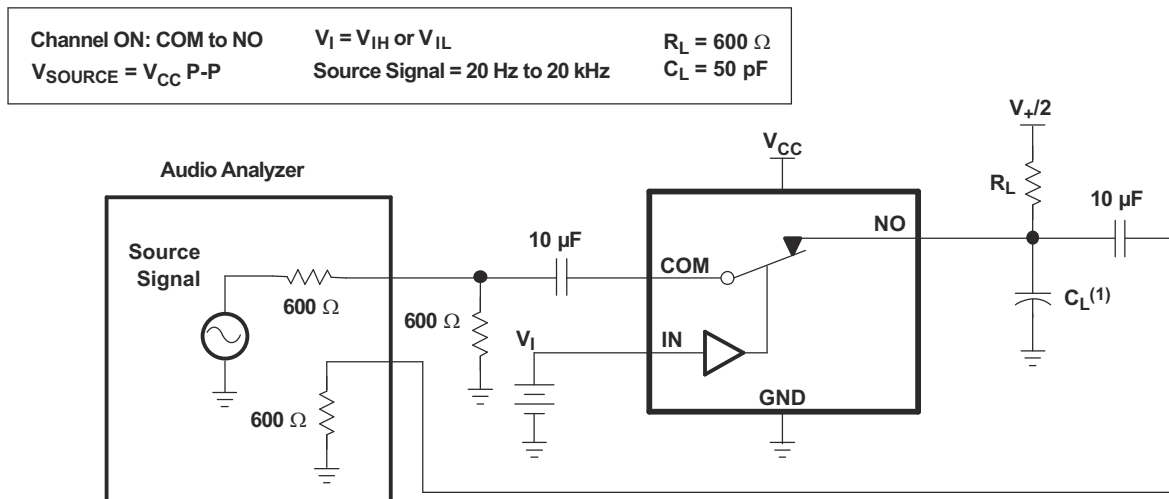
图 7-7. Bandwidth (BW)

图 7-8. OFF Isolation (O_{ISO})图 7-9. Crosstalk (X_{TALK})



- A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
 B. C_L includes probe and jig capacitance.

图 7-10. Charge Injection (Q_C)



- A. C_L includes probe and jig capacitance.

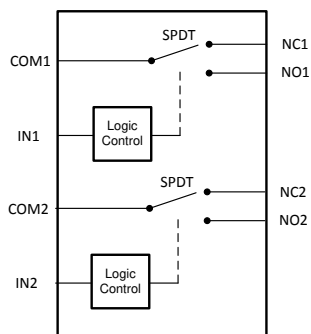
图 7-11. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS3A24159 is a 2-channel single-pole double-throw (SPDT) bidirectional analog switch that is designed to operate from 1.65 V to 3.6 V. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance, low ON-state resistance, and consumes very low power. These are some of the features that make this device suitable for a variety of markets and many different applications.

8.2 Functional Block Diagram



8.3 Feature Description

The TS3A24159 device is bidirectional with two single-pole, double-throw switches. Each of the two switches are controlled independently by two digital signals.

8.4 Device Functional Modes

表 8-1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

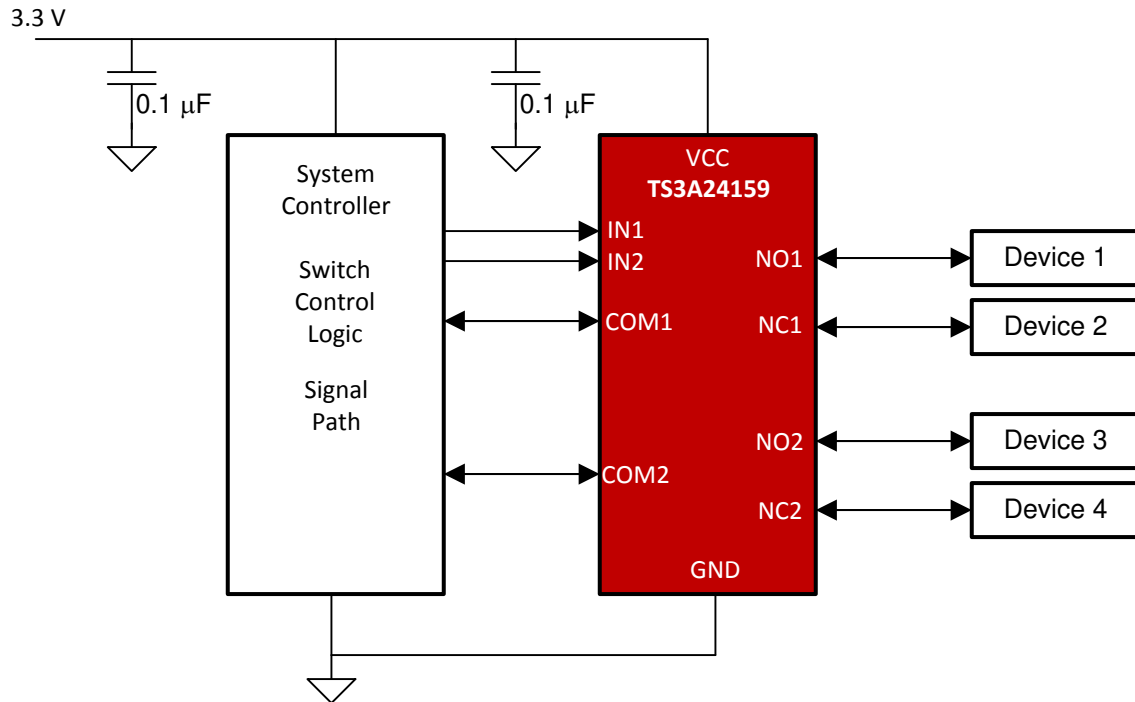
备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The switch of the TS3A24159 device is bidirectional. Hence, NO, NC, and COM pins can be used as both inputs or outputs.

9.2 Typical Application



9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the specified ranges to ensure proper performance.

表 9-1. Design Parameters

		MIN	MAX	UNIT
V _{CC}	Supply Voltage	1.65	3.6	V
V _{NC} V _{NO} V _{COM}	Signal Voltage	0	V _{CC}	V
V _{IN}	Digital Input Voltage	0	V _{CC}	V

9.2.2 Detailed Design Procedure

The TS3A24159 device can be properly operated without any external components. However, it is recommended to connect the unused pins to ground through a 50- Ω resistor to prevent signal reflections back into the device. It is also recommended that the digital control pins (IN1 and IN2) be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS3A24159 input/output signal swing through NO and COM are dependant of the supply voltage V_{CC} .

9.2.3 Application Curve

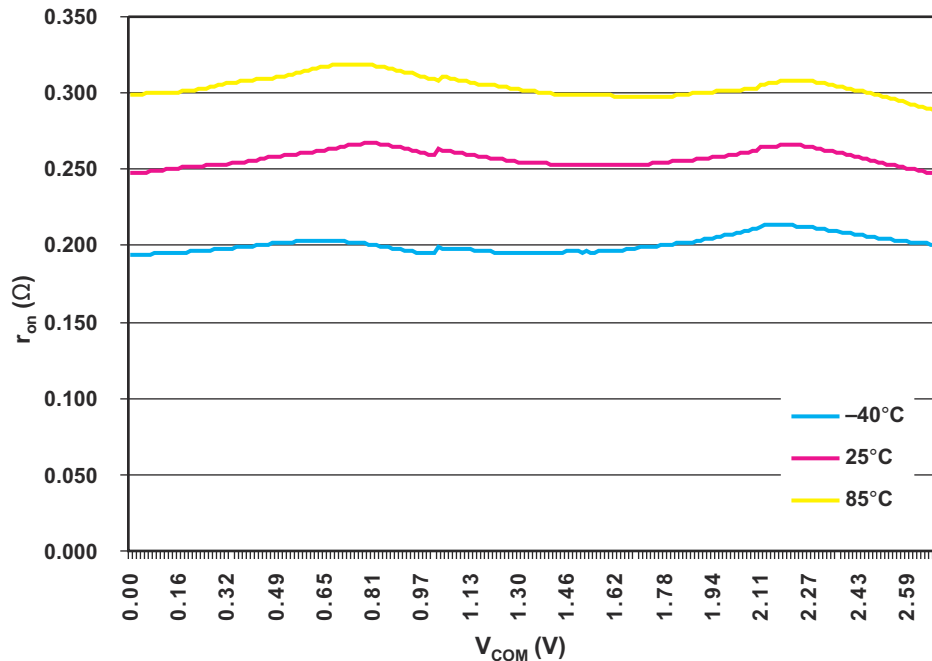


图 9-1. r_{ON} vs V_{COM}

10 Power Supply Recommendations

- Proper power-supply sequencing is recommended for all CMOS devices.
- Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device.
- Always sequence V_{CC} on first, followed by NO or COM.
- Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components.
- A 0.1- μ F capacitor, connected from V_{CC} to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended. Bypass capacitors must be used on power supplies. Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example

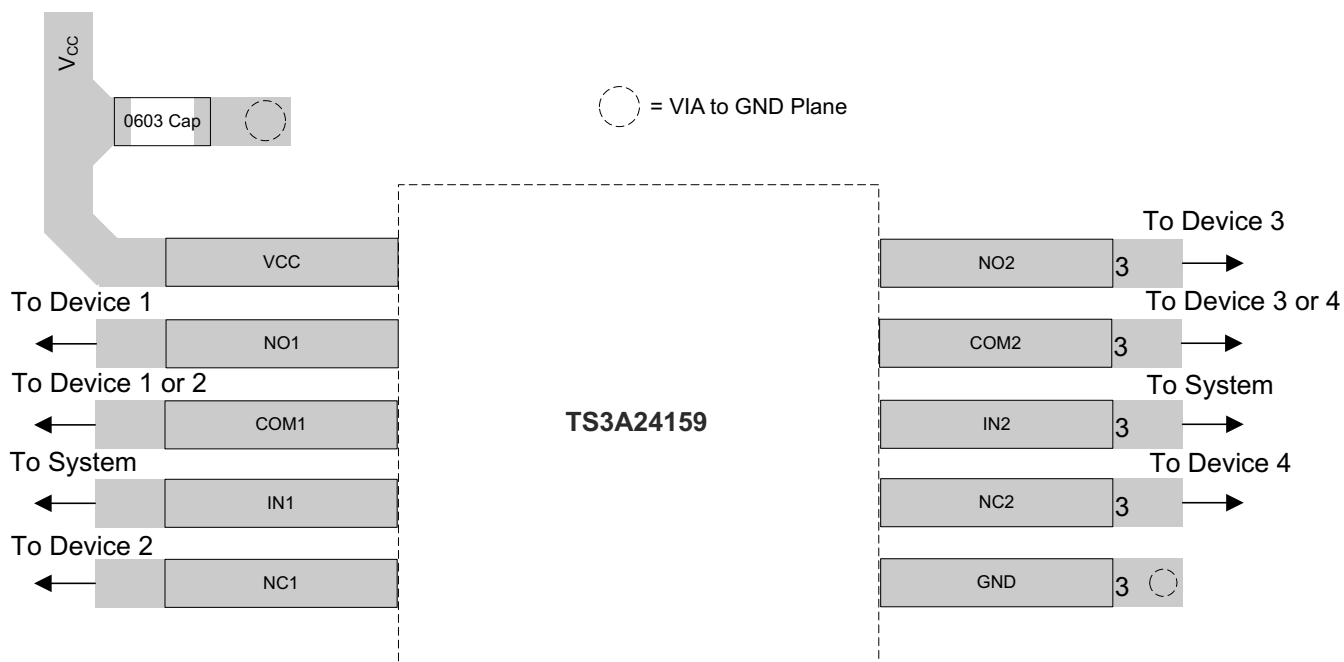


图 11-1. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3A24159DGSR	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L8Q, L8R)
TS3A24159DGSR.B	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L8Q, L8R)
TS3A24159DRCR	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWS
TS3A24159DRCR.B	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWS
TS3A24159YZPR	Active	Production	DSBGA (YZP) 10	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	L87
TS3A24159YZPR.B	Active	Production	DSBGA (YZP) 10	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	L87

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

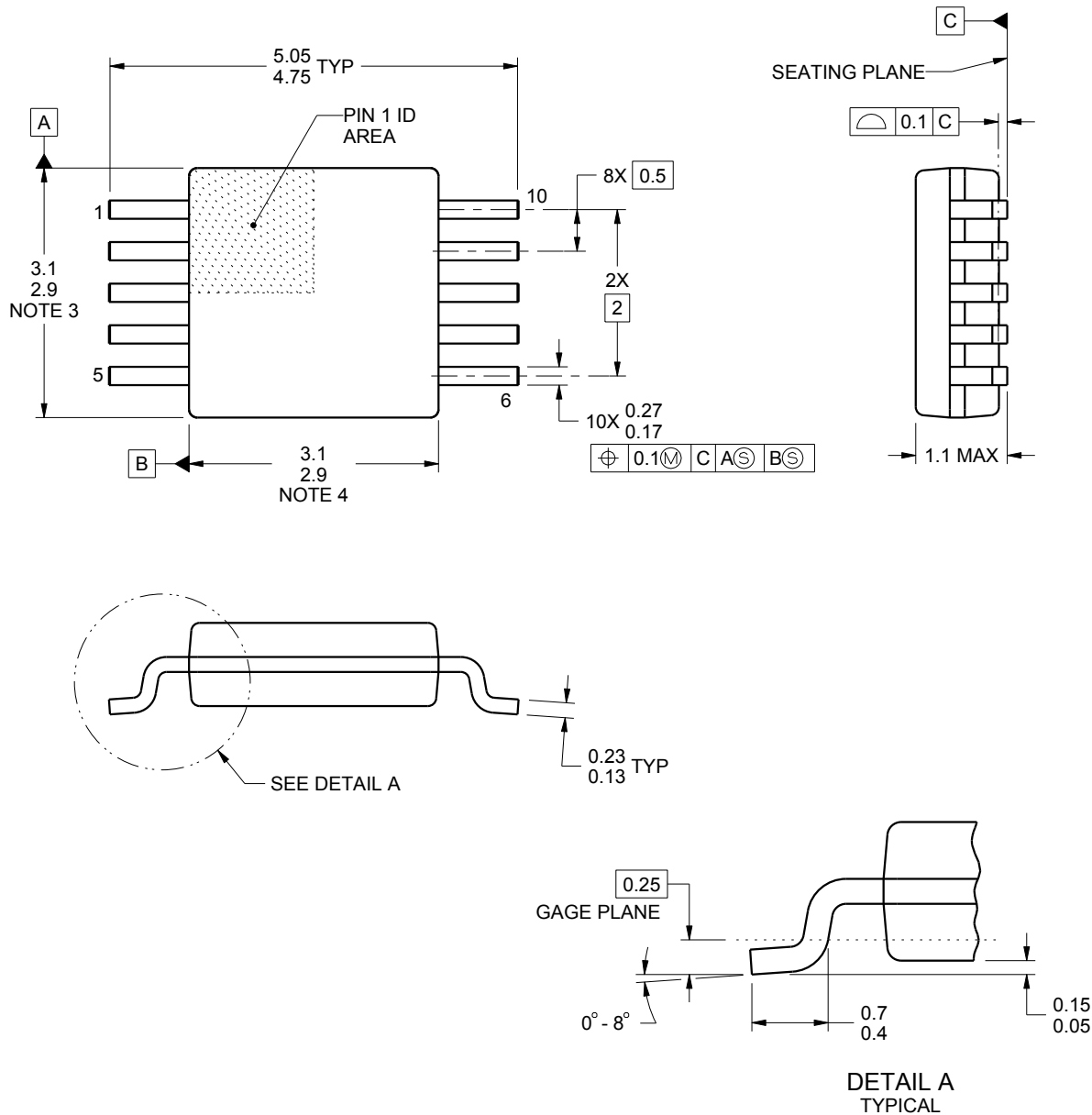
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A24159DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS3A24159DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3A24159YZPR	DSBGA	YZP	10	3000	178.0	9.2	1.49	1.99	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A24159DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS3A24159DRCR	VSON	DRC	10	3000	353.0	353.0	32.0
TS3A24159YZPR	DSBGA	YZP	10	3000	220.0	220.0	35.0



4221984/A 05/2015

NOTES:

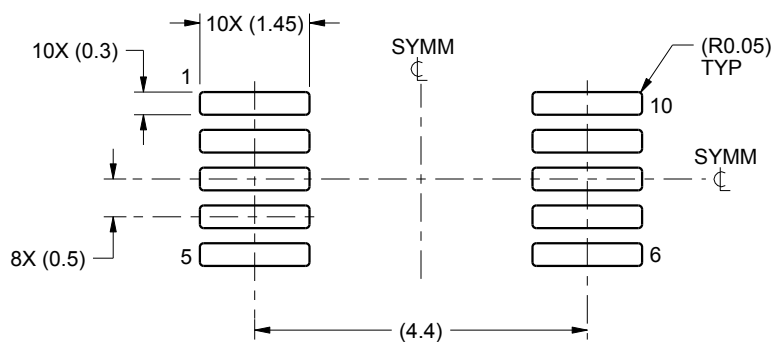
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

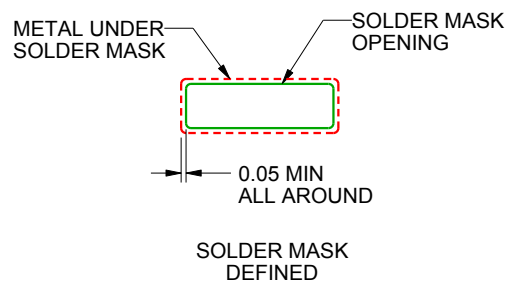
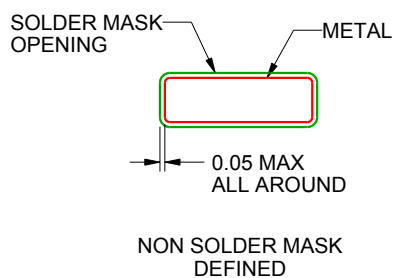
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

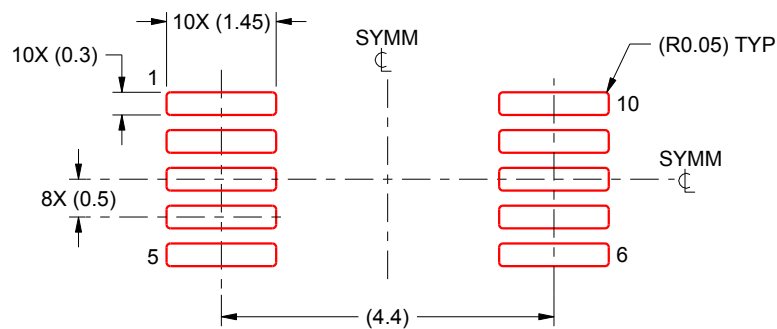
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

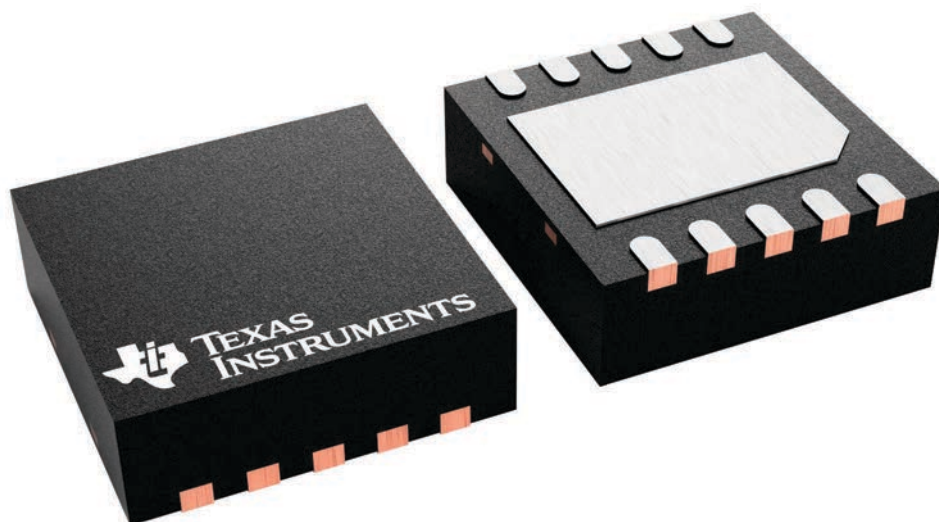
DRC 10

VSON - 1 mm max height

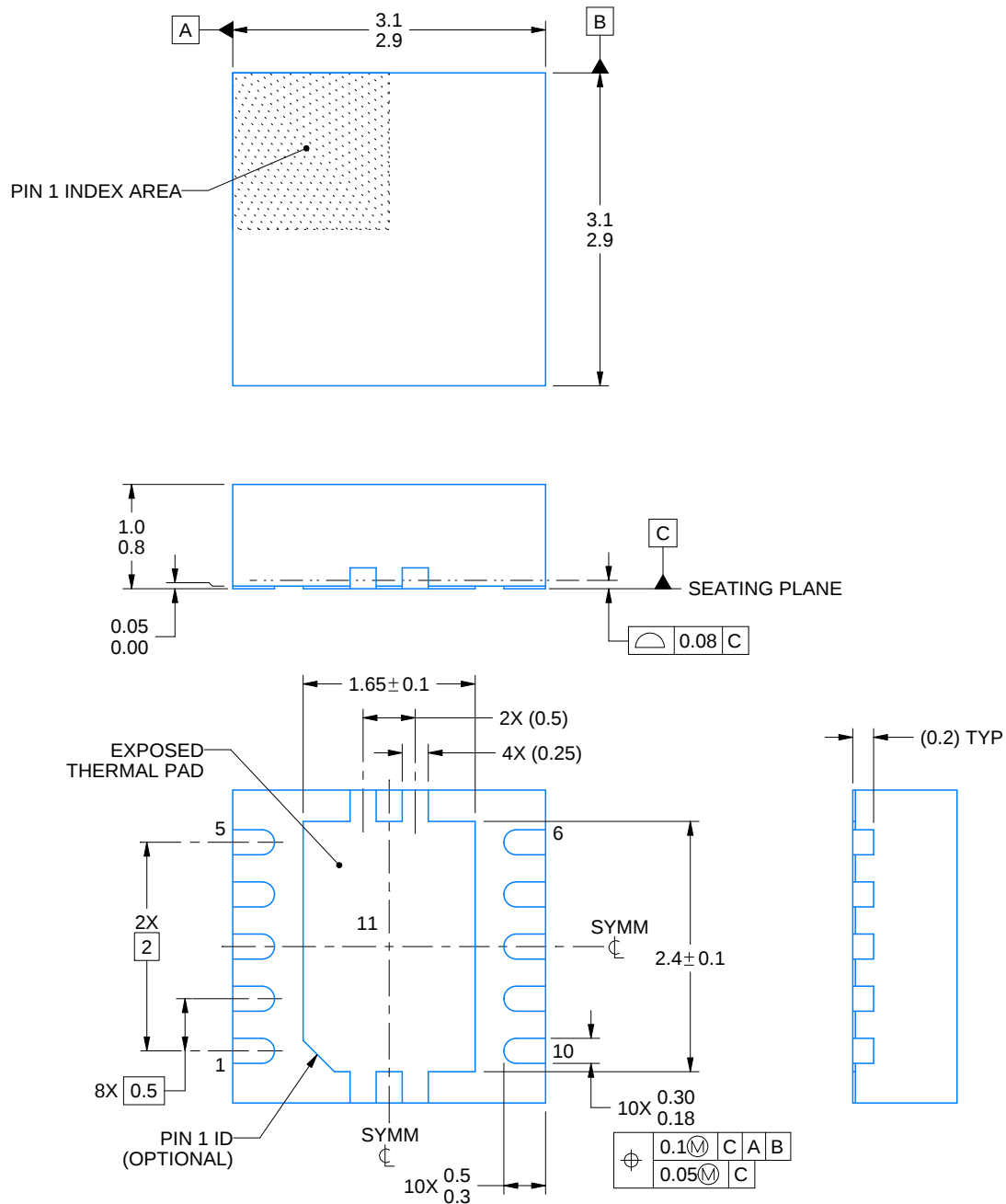
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226193/A



4218878/B 07/2018

NOTES:

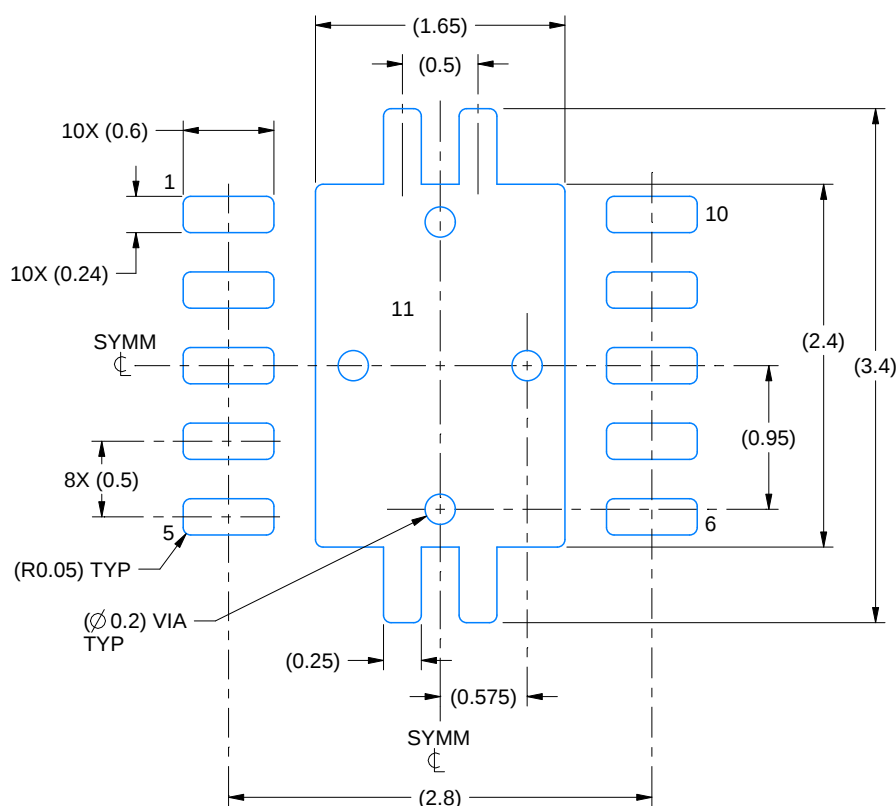
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

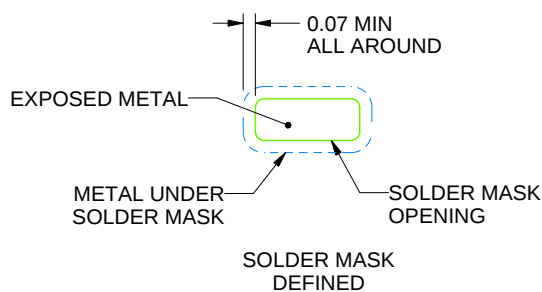
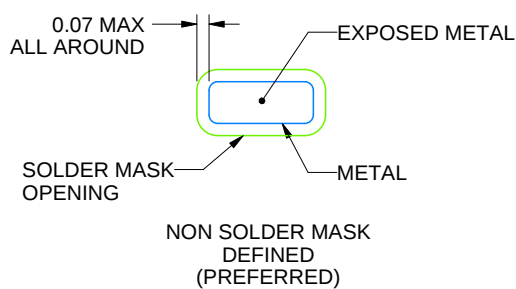
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

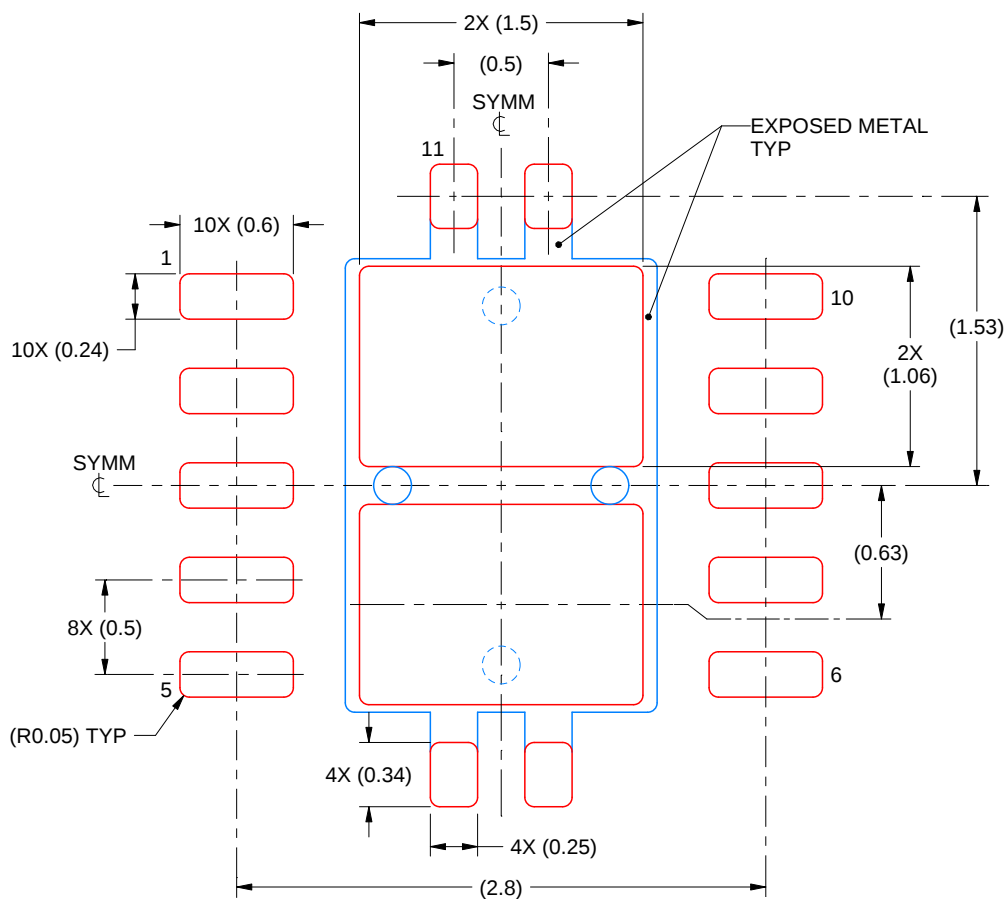
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

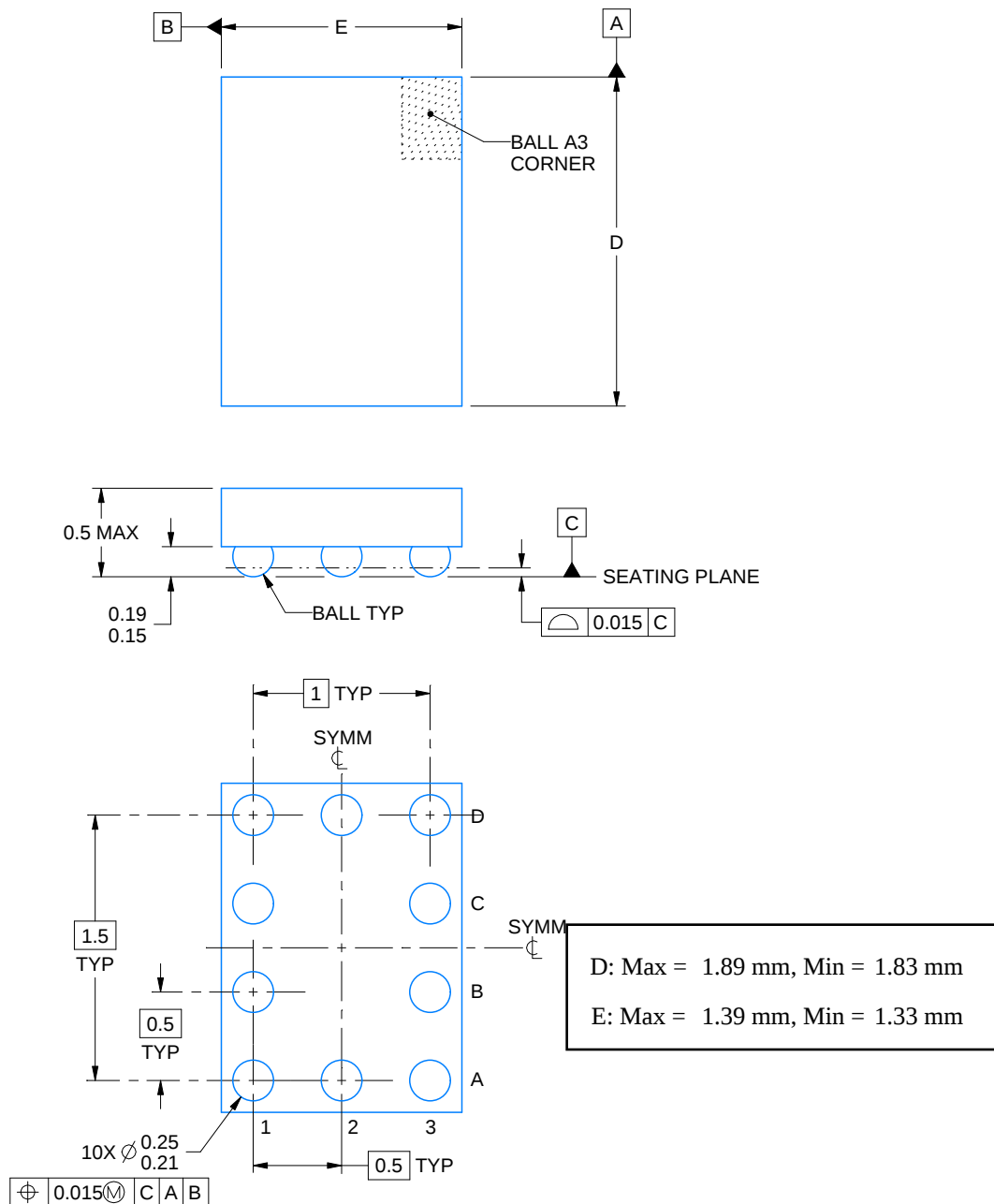
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0010

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219350/B 11/2017

NOTES:

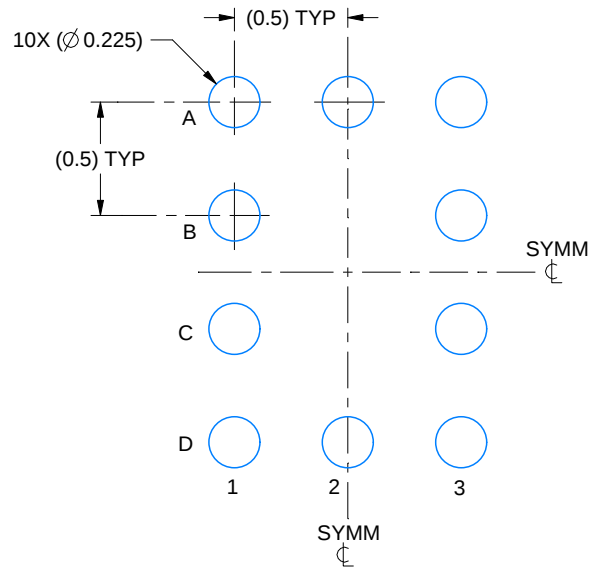
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

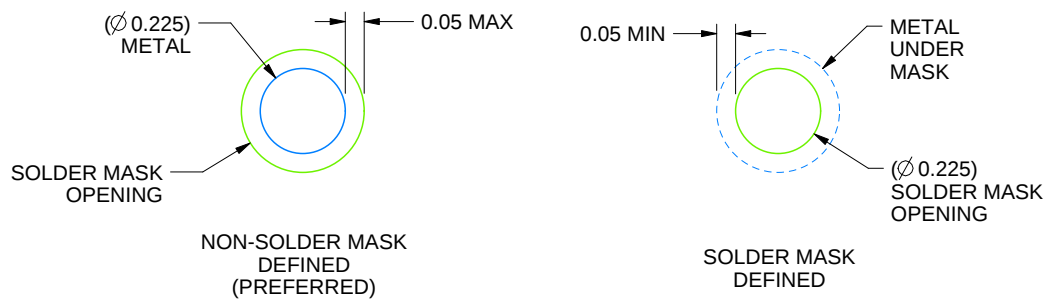
YZP0010

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4219350/B 11/2017

NOTES: (continued)

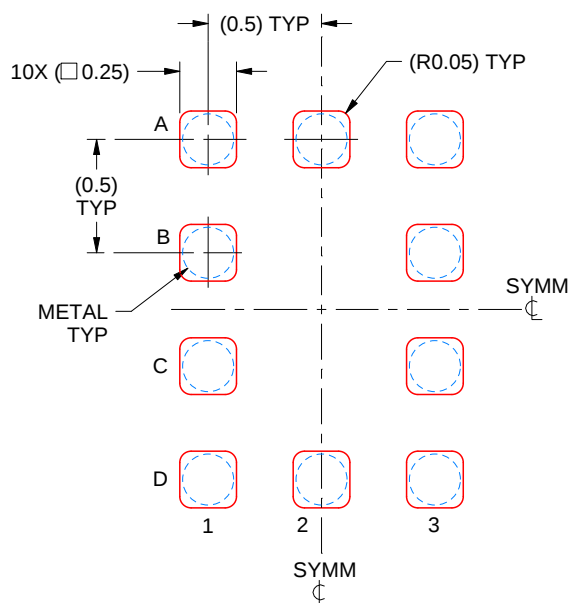
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0010

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219350/B 11/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司