

## TS12A12511 具有负信号处理功能的 5Ω 单通道 SPDT 模拟开关

### 1 特性

- $\pm 2.7\text{V}$  至  $\pm 6\text{V}$  双电源
- 2.7V 至 12V 单电源
- $5\Omega$  (典型值) 导通状态电阻
- $1.6\Omega$  (典型值) 导通状态电阻平坦度
- 3.3V、5V 兼容数字控制输入
- 轨到轨模拟信号处理
- 快速  $t_{\text{ON}}$ 、 $t_{\text{OFF}}$  时间
- 支持数字和模拟信号应用
- 微型 8 引线 SOT-23、8 引线 MSOP 和 QFN-8 封装
- 闩锁性能超过 100 mA，符合 JESD 78 II 类规范
- ESD 性能经测试符合 JESD 22 规范
  - $\pm 2000\text{V}$  人体放电模型 (A114-B, II 类)
  - $\pm 1000\text{V}$  组件充电模式 (C101)

### 2 应用

- 自动测试设备
- 电源布线
- 通信系统
- 数据采集系统
- 采样保持系统
- 继电器更换
- 电网基础设施

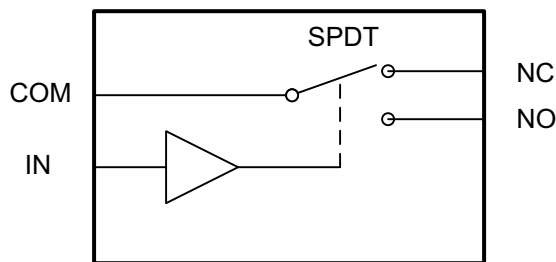
### 3 说明

TS12A12511 是一款双向单通道单极双投 (SPDT) 模拟开关，可传递摆幅为 0V 至 12V 或 -6V 至 6V 的信号。此开关开启时，在两个方向上都表现得很好。该器件还具备  $5\Omega$  (典型值) 的低导通状态电阻，与通道间电阻的差额小于  $1\Omega$ 。其最大电流消耗小于  $1\mu\text{A}$ ，-3dB 带宽大于 93MHz。TS12A12511 具有先断后合开关操作，可防止切换通道时发生瞬时短路。此器件可采用 8 引线 VSSOP、8 引线 SOT-23 和 8 引脚 WSON 封装。

#### 封装信息<sup>(1)</sup>

| 器件型号       | 封装              | 封装尺寸 (标称值)      |
|------------|-----------------|-----------------|
| TS12A12511 | DCN (SOT-23, 8) | 2.90mm × 1.63mm |
|            | DGK (VSSOP, 8)  | 3.00mm × 3.00mm |
|            | DRJ (WSON, 8)   | 4.00mm × 4.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图



## Table of Contents

|                                                             |           |                                                                  |           |
|-------------------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 特性</b> .....                                           | <b>1</b>  | <b>8.2 Functional Block Diagram</b> .....                        | <b>14</b> |
| <b>2 应用</b> .....                                           | <b>1</b>  | <b>8.3 Feature Description</b> .....                             | <b>14</b> |
| <b>3 说明</b> .....                                           | <b>1</b>  | <b>8.4 Device Functional Modes</b> .....                         | <b>14</b> |
| <b>4 Revision History</b> .....                             | <b>2</b>  | <b>9 Application and Implementation</b> .....                    | <b>15</b> |
| <b>5 Pin Configuration and Functions</b> .....              | <b>3</b>  | 9.1 Application Information.....                                 | 15        |
| <b>6 Specifications</b> .....                               | <b>4</b>  | 9.2 Typical Application.....                                     | 15        |
| 6.1 Absolute Maximum Ratings.....                           | 4         | <b>10 Power Supply Recommendations</b> .....                     | <b>17</b> |
| 6.2 ESD Ratings.....                                        | 4         | <b>11 Layout</b> .....                                           | <b>17</b> |
| 6.3 Recommended Operating Conditions.....                   | 4         | 11.1 Layout Guidelines.....                                      | 17        |
| 6.4 Thermal Information.....                                | 4         | 11.2 Layout Example.....                                         | 17        |
| 6.5 Electrical Characteristics: $\pm 5$ -V Dual Supply..... | 5         | <b>12 Device and Documentation Support</b> .....                 | <b>18</b> |
| 6.6 Electrical Characteristics: 12-V Single Supply.....     | 6         | 12.1 接收文档更新通知.....                                               | 18        |
| 6.7 Electrical Characteristics: 5-V Single Supply.....      | 7         | 12.2 支持资源.....                                                   | 18        |
| 6.8 Typical Characteristics.....                            | 8         | 12.3 Trademarks.....                                             | 18        |
| <b>7 Parameter Measurement Information</b> .....            | <b>10</b> | 12.4 Electrostatic Discharge Caution.....                        | 18        |
| 7.1 Test Circuits.....                                      | 10        | 12.5 术语表.....                                                    | 18        |
| <b>8 Detailed Description</b> .....                         | <b>14</b> | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | <b>18</b> |
| 8.1 Overview.....                                           | 14        |                                                                  |           |

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

|                                                                                                                                     |             |
|-------------------------------------------------------------------------------------------------------------------------------------|-------------|
| <b>Changes from Revision D (January 2019) to Revision E (September 2022)</b> .....                                                  | <b>Page</b> |
| • 更新了整个文档中的表格、图和交叉参考的编号格式.....                                                                                                      | 1           |
| • 更新了应用部分.....                                                                                                                      | 1           |
| • Updated the <i>Leakage Current vs I/O Voltage (Switch ON)</i> and <i>Leakage Current vs I/O Voltage (Switch OFF)</i> figures..... | 8           |
| <b>Changes from Revision C (January 2015) to Revision D (January 2019)</b> .....                                                    | <b>Page</b> |
| • Added Junction temperature to the <i>Absolute Maximum Ratings</i> table.....                                                      | 4           |
| <b>Changes from Revision B (April 2011) to Revision C (January 2015)</b> .....                                                      | <b>Page</b> |
| • 添加了引脚配置和功能部分、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....                                            | 1           |
| <b>Changes from Revision A (May 2010) to Revision B (April 2011)</b> .....                                                          | <b>Page</b> |
| • Deleted preview status from DGK and DCN packages.....                                                                             | 3           |

## 5 Pin Configuration and Functions

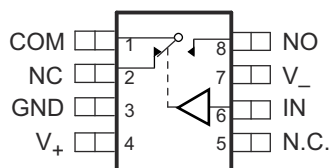


图 5-1. DGK Package, 8-Pin VSSOP (Top View)

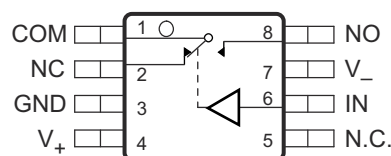
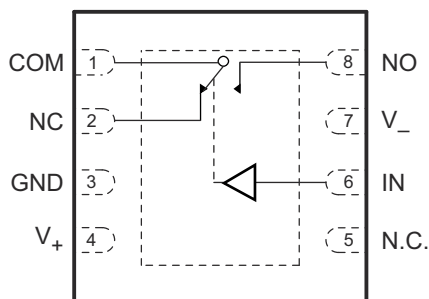


图 5-2. DCN Package, 8-Pin SOT-23 (Top View)



N.C. – Not internally connected NC – Normally closed NO – Normally open

The Exposed Thermal Pad must be electrically connected to  $V_-$  or left floating.

图 5-3. DRJ Package, 8-Pin WSON (Top View)

表 5-1. Pin Functions

| PIN         |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                               |
|-------------|-----|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| NAME        | NO. |                     |                                                                                                                                           |
| COM         | 1   | I/O                 | Common. Can be an input or output.                                                                                                        |
| GND         | 3   | —                   | Ground (0 V) reference                                                                                                                    |
| IN          | 6   | I                   | Logic control input                                                                                                                       |
| NC          | 2   | I/O                 | Normally closed. Can be an input or output.                                                                                               |
| N.C.        | 5   | —                   | No connect. Not internally connected.                                                                                                     |
| NO          | 8   | I/O                 | Normally open. Can be an input or output.                                                                                                 |
| $V_{CC}$    | 4   | I                   | Most positive power supply                                                                                                                |
| $-V_{CC}$   | 7   | I                   | Most negative power supply. This pin is only used in dual-supply applications and should be tied to ground in single-supply applications. |
| Thermal pad |     | —                   | The Exposed Thermal Pad must be electrically connected to $V_-$ or left floating.                                                         |

(1) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$  (unless otherwise noted).<sup>(1)</sup>

|                       |                       |                | MIN             | MAX            | UNIT             |
|-----------------------|-----------------------|----------------|-----------------|----------------|------------------|
| $V_{CC}$ to $-V_{CC}$ |                       |                | 0               | 13             | V                |
| $V_{CC}$ to GND       |                       |                | -0.3            | 13             | V                |
| $-V_{CC}$ to GND      |                       |                | -6.5            | 0.3            | V                |
| $V_{I/O}$             | Analog inputs         | NC, NO, or COM | $-V_{CC} - 0.5$ | $V_{CC} + 0.5$ | V                |
| $I_{IN}$              | Digital inputs        |                |                 | $\pm 30$       | mA               |
| $I_{I/O}$             | Peak current          | NC, NO, or COM |                 | $\pm 100$      | mA               |
|                       | Continuous current    | NC, NO, or COM |                 | $\pm 50$       | mA               |
| $T_A$                 | Operating temperature |                | -40             | 85             | $^\circ\text{C}$ |
| $T_J$                 | Junction temperature  |                |                 | 150            | $^\circ\text{C}$ |
| $T_{stg}$             | Storage temperature   |                | -65             | 150            | $^\circ\text{C}$ |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [§ 6.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|             |                         |                                                                                | VALUE      | UNIT |
|-------------|-------------------------|--------------------------------------------------------------------------------|------------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | $\pm 2000$ | V    |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | $\pm 1000$ |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|           | MIN       | MAX      | UNIT |
|-----------|-----------|----------|------|
| $V_{CC}$  | 0         | 12       | V    |
| $-V_{CC}$ | -6        | 0        | V    |
| $V_{I/O}$ | $-V_{CC}$ | $V_{CC}$ | V    |
| $V_{IN}$  | 0         | $V_{CC}$ | V    |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TS12A12511 |       |      | UNIT |
|-------------------------------|----------------------------------------------|------------|-------|------|------|
|                               |                                              | DCN        | DGK   | DRJ  |      |
|                               |                                              |            |       |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 218.4      | 184.5 | 47.8 | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 89.9       | 71.0  | 48.6 |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 144.4      | 104.5 | 24.2 |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 7.8        | 11.3  | 1.2  |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 141.7      | 103.3 | 24.4 |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A        | N/A   | 9.0  |      |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics: $\pm 5$ -V Dual Supply

$V_{CC} = 5\text{ V} \pm 10\%$ ,  $-V_{CC} = -5\text{ V} \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                                              |                                                  | TEST CONDITIONS                                                                                                               | T <sub>A</sub> = 25°C |      |     | T <sub>A</sub> = - 40°C to 85°C |                 |     | UNIT |
|------------------------------------------------------------------------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|-----------------------|------|-----|---------------------------------|-----------------|-----|------|
|                                                                        |                                                  |                                                                                                                               | MIN                   | TYP  | MAX | MIN                             | TYP             | MAX |      |
| ANALOG SWITCH                                                          |                                                  |                                                                                                                               |                       |      |     |                                 |                 |     |      |
| Analog signal range                                                    |                                                  |                                                                                                                               |                       |      |     | -V <sub>CC</sub>                | V <sub>CC</sub> | V   |      |
| R <sub>ON</sub>                                                        | ON-state resistance                              | V <sub>NC</sub> = -4.5 V to +4.5 V<br>or V <sub>NO</sub> = - 4.5 V to 4.5 V, I <sub>COM</sub> = - 10 mA;<br>see 图 7-1         | 5                     |      |     | 5                               | 8               | Ω   |      |
| Δ R <sub>ON</sub>                                                      | ON-state resistance<br>match between<br>channels | V <sub>NC</sub> = -4.5 V to +4.5 V<br>or V <sub>NO</sub> = -4.5 V to +4.5 V,<br>I <sub>COM</sub> = - 10 mA                    | 1                     |      |     | 1.2                             | 1.6             | Ω   |      |
| R <sub>ON(flat)</sub>                                                  | ON-state resistance<br>flatness                  | V <sub>NC</sub> = -3.3 V to +3.3 V<br>or V <sub>NO</sub> = -3.3 V to +3.3 V,<br>I <sub>COM</sub> = - 10 mA                    | 1.6                   |      |     | 2.2                             | 2.2             | Ω   |      |
| LEAKAGE CURRENTS                                                       |                                                  |                                                                                                                               |                       |      |     |                                 |                 |     |      |
| I <sub>NC(OFF)</sub> ,<br>I <sub>NO(OFF)</sub>                         | OFF leakage current                              | V <sub>NC</sub> = -4.5 V to +4.5 V<br>or V <sub>NO</sub> = -4.5 V to +4.5 V<br>V <sub>COM</sub> = -4.5 V to +4.5 V; see 图 7-2 | - 1                   | ±0.5 | 1   | - 50                            | 50              | nA  |      |
| I <sub>NC(ON)</sub> ,<br>I <sub>NO(ON)</sub>                           | ON leakage current                               | V <sub>NC</sub> = -4.5 V to +4.5 V<br>or V <sub>NO</sub> = -4.5 V to +4.5 V<br>V <sub>COM</sub> = open; see 图 7-3             | - 1                   | ±0.5 | 1   | - 50                            | 50              | nA  |      |
| DIGITAL INPUTS                                                         |                                                  |                                                                                                                               |                       |      |     |                                 |                 |     |      |
| V <sub>INH</sub>                                                       | High-level input<br>voltage                      |                                                                                                                               |                       |      |     | 2.4                             | V <sub>CC</sub> | V   |      |
| V <sub>INL</sub>                                                       | Low-level input voltage                          |                                                                                                                               |                       |      |     | 0                               | 0.8             | V   |      |
| I <sub>INL</sub> , I <sub>INH</sub>                                    | Input current                                    | V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>                                                                        | 0.005                 |      |     | - 1                             | 1               | μ A |      |
| C <sub>IN</sub>                                                        | Control input<br>capacitance                     |                                                                                                                               | 2.5                   |      |     |                                 |                 | pF  |      |
| DYNAMIC <sup>(1)</sup>                                                 |                                                  |                                                                                                                               |                       |      |     |                                 |                 |     |      |
| t <sub>ON</sub>                                                        | Turn-ON time                                     | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,<br>V <sub>COM</sub> = 3.3 V; see 图 7-5                                        | 80                    |      |     | 95                              | 115             | ns  |      |
| t <sub>OFF</sub>                                                       | Turn-OFF time                                    | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,<br>V <sub>COM</sub> = 3.3 V                                                   | 41                    |      |     | 50                              | 56              | ns  |      |
| t <sub>BBM</sub>                                                       | Break-before-make<br>time delay                  | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,<br>V <sub>NC</sub> = V <sub>NO</sub> = 3.3 V; see 图 7-6                       | 36                    |      |     | 18                              |                 | ns  |      |
| Q <sub>C</sub>                                                         | Charge injection                                 | V <sub>NC</sub> = V <sub>NO</sub> = 0 V, R <sub>GEN</sub> = 0 Ω, C <sub>L</sub> = 1 nF;<br>see 图 7-7                          | 26                    |      |     |                                 |                 | pC  |      |
| O <sub>ISO</sub>                                                       | OFF isolation                                    | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz;<br>see 图 7-8                                                         | - 70                  |      |     |                                 |                 | dB  |      |
| X <sub>TALK</sub>                                                      | Channel-to-channel<br>crosstalk                  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz,<br>see 图 7-9                                                         | - 70                  |      |     |                                 |                 | dB  |      |
| BW                                                                     | Bandwidth - 3 dB                                 | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF; see 图 7-10                                                                      | 93                    |      |     |                                 |                 | MHz |      |
| THD                                                                    | Total harmonic<br>distortion                     | R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 15pF, V <sub>NO</sub> = 1V <sub>RMS</sub> ,<br>f = 20 kHz; see 图 7-11                | 0.004%                |      |     |                                 |                 |     |      |
| C <sub>NC(OFF)</sub> ,<br>C <sub>NO(OFF)</sub>                         | NC, NO<br>OFF capacitance                        | f = 1 MHz; see 图 7-4                                                                                                          | 14                    |      |     |                                 |                 | pF  |      |
| C <sub>COM(ON)</sub> ,<br>C <sub>NC(ON)</sub> ,<br>C <sub>NO(ON)</sub> | COM, NC, NO<br>ON capacitance                    | f = 1 MHz; see 图 7-4                                                                                                          | 60                    |      |     |                                 |                 | pF  |      |
| SUPPLY                                                                 |                                                  |                                                                                                                               |                       |      |     |                                 |                 |     |      |
| I <sub>CC</sub>                                                        | Positive supply current                          |                                                                                                                               | 0.03                  |      |     |                                 | 1               | μ A |      |

(1) Specified by design, not subject to production test.

## 6.6 Electrical Characteristics: 12-V Single Supply

$V_{CC} = 12\text{ V} \pm 10\%$ ,  $-V_{CC} = 0\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                                              |                                            | TEST CONDITIONS                                                                                                      | T <sub>A</sub> = 25°C |      |     | T <sub>A</sub> = - 40°C to 85°C |                 |     | UNIT |
|------------------------------------------------------------------------|--------------------------------------------|----------------------------------------------------------------------------------------------------------------------|-----------------------|------|-----|---------------------------------|-----------------|-----|------|
|                                                                        |                                            |                                                                                                                      | MIN                   | TYP  | MAX | MIN                             | TYP             | MAX |      |
| ANALOG SWITCH                                                          |                                            |                                                                                                                      |                       |      |     |                                 |                 |     |      |
| Analog signal range                                                    |                                            |                                                                                                                      |                       |      |     | 0                               | V <sub>CC</sub> | V   |      |
| R <sub>on</sub>                                                        | ON-state resistance                        | V <sub>NC</sub> =0 V to 10.8 V or V <sub>NO</sub> = 0 V to 10.8 V,<br>I <sub>COM</sub> = - 10 mA, see 图 7-1          | 5                     |      |     | 5                               | 8               | Ω   |      |
| Δ R <sub>on</sub>                                                      | ON-state resistance match between channels | V <sub>NC</sub> = 0 V to 10.8 V or V <sub>NO</sub> = 0 V to 10.8 V,<br>I <sub>COM</sub> = - 10 mA                    | 1.6      2.4          |      |     | 2.6                             |                 | Ω   |      |
| R <sub>on(flat)</sub>                                                  | ON-state resistance flatness               | V <sub>NC</sub> = 3.3 V to 7V or V <sub>NO</sub> = 3.3 V to 7 V,<br>I <sub>COM</sub> = - 10 mA                       | 1.7                   |      |     | 1.8                             | 3.2             | Ω   |      |
| LEAKAGE CURRENTS                                                       |                                            |                                                                                                                      |                       |      |     |                                 |                 |     |      |
| I <sub>NC(OFF)</sub> ,<br>I <sub>NO(OFF)</sub>                         | OFF leakage current                        | V <sub>NC</sub> = 0 V to 10.8 V or V <sub>NO</sub> = 0 V to 10.8 V,<br>V <sub>COM</sub> = 0 V to 10.8 V; see 图 7-2   | - 10                  | ±0.5 | 10  | - 50                            | 50              | nA  |      |
| I <sub>NC(ON)</sub> ,<br>I <sub>NO(ON)</sub>                           | ON leakage current                         | V <sub>NC</sub> = 0 V to 10.8V or V <sub>NO</sub> = 0 V to 10.8 V,<br>V <sub>COM</sub> = open; see 图 7-3             | - 10                  | ±0.5 | 10  | - 50                            | 50              | nA  |      |
| DIGITAL INPUTS                                                         |                                            |                                                                                                                      |                       |      |     |                                 |                 |     |      |
| V <sub>INH</sub>                                                       | High-level input voltage                   |                                                                                                                      |                       |      |     | 5                               | V <sub>CC</sub> | V   |      |
| V <sub>INL</sub>                                                       | Low-level input voltage                    |                                                                                                                      |                       |      |     | 0                               | 0.8             | V   |      |
| I <sub>INL</sub> , I <sub>INH</sub>                                    | Input current                              | V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>                                                               | ±0.005                |      |     | - 0.1                           | 0.1             | μ A |      |
| C <sub>IN</sub>                                                        | Digital input capacitance                  |                                                                                                                      | 2.7                   |      |     |                                 |                 | pF  |      |
| DYNAMIC <sup>(1)</sup>                                                 |                                            |                                                                                                                      |                       |      |     |                                 |                 |     |      |
| t <sub>ON</sub>                                                        | Turn-ON time                               | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,<br>V <sub>COM</sub> = 3.3 V; see 图 7-5                               | 56      85            |      |     | 110                             |                 | ns  |      |
| t <sub>OFF</sub>                                                       | Turn-OFF time                              | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,<br>V <sub>COM</sub> = 3.3 V; see 图 7-5                               | 25      30            |      |     | 31                              |                 | ns  |      |
| t <sub>BBM</sub>                                                       | Break-before-make time delay               | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,<br>V <sub>NC</sub> = V <sub>NO</sub> = 3.3 V; see 图 7-6              | 30                    |      |     | 19                              |                 | ns  |      |
| Q <sub>C</sub>                                                         | Charge injection                           | R <sub>GEN</sub> = V <sub>NC</sub> = V <sub>NO</sub> = 0 V, R <sub>GEN</sub> = 0 Ω, C <sub>L</sub> = 1 nF; see 图 7-7 | 491                   |      |     |                                 |                 | pC  |      |
| O <sub>ISO</sub>                                                       | OFF isolation                              | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see 图 7-8                                                   | - 70                  |      |     |                                 |                 | dB  |      |
| X <sub>TALK</sub>                                                      | Channel-to-channel crosstalk               | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see 图 7-9                                                   | - 70                  |      |     |                                 |                 | dB  |      |
| BW                                                                     | Bandwidth - 3 dB                           | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, see 图 7-10                                                             | 200                   |      |     |                                 |                 | MHz |      |
| THD                                                                    | Total harmonic distortion                  | R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 15pF, V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 20 kHz; see 图 7-11         | 0.04%                 |      |     |                                 |                 |     |      |
| C <sub>NC(OFF)</sub> ,<br>C <sub>NO(OFF)</sub>                         | NC, NO OFF capacitance                     | f = 1 MHz, see 图 7-4                                                                                                 | 14                    |      |     |                                 |                 | pF  |      |
| C <sub>COM(ON)</sub> ,<br>C <sub>NC(ON)</sub> ,<br>C <sub>NO(ON)</sub> | COM, NC, NO ON capacitance                 | f = 1 MHz, see 图 7-4                                                                                                 | 55                    |      |     |                                 |                 | pF  |      |
| SUPPLY                                                                 |                                            |                                                                                                                      |                       |      |     |                                 |                 |     |      |
| I <sub>CC</sub>                                                        | Positive supply current                    |                                                                                                                      | 0.07                  |      |     | 1                               |                 | μ A |      |

(1) Specified by design, not subject to production test.

## 6.7 Electrical Characteristics: 5-V Single Supply

$V_{CC} = 5\text{ V} \pm 10\%$ ,  $-V_{CC} = 0\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                                              |                                            | TEST CONDITIONS                                                                                                         | T <sub>A</sub> = 25°C |      |     | T <sub>A</sub> = - 40°C to 85°C |                 |     | UNIT |
|------------------------------------------------------------------------|--------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|-----------------------|------|-----|---------------------------------|-----------------|-----|------|
|                                                                        |                                            |                                                                                                                         | MIN                   | TYP  | MAX | MIN                             | TYP             | MAX |      |
| ANALOG SWITCH                                                          |                                            |                                                                                                                         |                       |      |     |                                 |                 |     |      |
|                                                                        | Analog signal range                        |                                                                                                                         |                       |      |     | 0                               | V <sub>CC</sub> | V   |      |
| R <sub>on</sub>                                                        | ON-state resistance                        | V <sub>NC</sub> =0 V to 4.5 V or V <sub>NO</sub> = 0 V to 4.5 V,<br>I <sub>COM</sub> = - 10 mA;<br>see 图 7-1            |                       | 8    | 10  |                                 | 12.5            | Ω   |      |
| Δ R <sub>on</sub>                                                      | ON-state resistance match between channels | V <sub>NC</sub> =0 V to 4.5 V or V <sub>NO</sub> = 0 V to 4.5 V,<br>I <sub>COM</sub> = - 10 mA                          |                       | 1    | 1.1 |                                 | 1.5             | Ω   |      |
| R <sub>on(flat)</sub>                                                  | ON-state resistance flatness               | V <sub>NC</sub> =0 V to 4.5 V or V <sub>NO</sub> = 0 V to 4.5 V,<br>I <sub>COM</sub> = - 10 mA                          |                       | 1.3  |     |                                 | 1.3 2           | Ω   |      |
| LEAKAGE CURRENTS                                                       |                                            |                                                                                                                         |                       |      |     |                                 |                 |     |      |
| I <sub>NC(OFF)</sub> ,<br>I <sub>NO(OFF)</sub>                         | OFF leakage current                        | V <sub>NC</sub> =0 V to 4.5 V or V <sub>NO</sub> = 0 V to 4.5 V,<br>V <sub>COM</sub> = 0 V to 4.5 V; see 图 7-2          | - 1                   | ±0.5 | 1   | - 50                            | 50              | nA  |      |
| I <sub>NC(ON)</sub> ,<br>I <sub>NO(ON)</sub>                           | ON leakage current                         | V <sub>NC</sub> = 0 V to 4.5V or V <sub>NO</sub> = 0 V to 4.5 V,<br>V <sub>COM</sub> = open; see 图 7-3                  | - 1                   | ±0.5 | 1   | - 50                            | 50              | nA  |      |
| DIGITAL INPUTS                                                         |                                            |                                                                                                                         |                       |      |     |                                 |                 |     |      |
| V <sub>INH</sub>                                                       | High-level input voltage                   |                                                                                                                         |                       |      |     | 2.4                             | V <sub>CC</sub> | V   |      |
| V <sub>INL</sub>                                                       | Low-level input voltage                    |                                                                                                                         |                       |      |     | 0                               | 0.8             | V   |      |
| I <sub>INL</sub> , I <sub>INH</sub>                                    | Input current                              | V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>                                                                  | 0.01                  |      |     | - 0.1                           | 0.1             | μ A |      |
| C <sub>IN</sub>                                                        | Digital input capacitance                  |                                                                                                                         | 2.8                   |      |     |                                 |                 | pF  |      |
| DYNAMIC <sup>(1)</sup>                                                 |                                            |                                                                                                                         |                       |      |     |                                 |                 |     |      |
| t <sub>ON</sub>                                                        | Turn-ON time                               | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,<br>V <sub>COM</sub> = 3.3 V; see 图 7-5                                  |                       | 119  | 145 |                                 | 178             | ns  |      |
| t <sub>OFF</sub>                                                       | Turn-OFF time                              | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,<br>V <sub>COM</sub> = 3.3 V; see 图 7-5                                  |                       | 38   | 47  |                                 | 95.2            | ns  |      |
| t <sub>BBM</sub>                                                       | Break-before-make time delay               | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,<br>V <sub>NC</sub> = V <sub>NO</sub> = 3.3 V; see 图 7-6                 |                       | 79   |     | 44                              |                 | ns  |      |
| Q <sub>C</sub>                                                         | Charge injection                           | V <sub>GEN</sub> = V <sub>NC</sub> = V <sub>NO</sub> = 0 V, R <sub>GEN</sub> = 0 Ω, C <sub>L</sub> = 1 nF;<br>see 图 7-7 | 65                    |      |     |                                 |                 | pC  |      |
| O <sub>ISO</sub>                                                       | OFF isolation                              | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz,<br>see 图 7-8                                                   | - 70                  |      |     |                                 |                 | dB  |      |
| X <sub>TALK</sub>                                                      | Channel-to-channel crosstalk               | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz,<br>see 图 7-9                                                   | - 70                  |      |     |                                 |                 | dB  |      |
| BW                                                                     | Bandwidth - 3 dB                           | R <sub>L</sub> = 50 Ω, see 图 7-10                                                                                       | 152                   |      |     |                                 |                 | MHz |      |
| THD                                                                    | Total harmonic distortion                  | R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 15 pF, V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 20 kHz; see 图 7-11           | 0.04%                 |      |     |                                 |                 |     |      |
| C <sub>NC(OFF)</sub> ,<br>C <sub>NO(OFF)</sub>                         | NC, NO OFF capacitance                     | f = 1 MHz, see 图 7-4                                                                                                    | 15                    |      |     |                                 |                 | pF  |      |
| C <sub>COM(ON)</sub> ,<br>C <sub>NC(ON)</sub> ,<br>I <sub>NO(ON)</sub> | COM, NC, NO ON capacitance                 | f = 1 MHz, see 图 7-4                                                                                                    | 55                    |      |     |                                 |                 | pF  |      |
| POWER REQUIREMENTS                                                     |                                            |                                                                                                                         |                       |      |     |                                 |                 |     |      |
| I <sub>CC</sub>                                                        | Positive supply current                    | V <sub>IN</sub> = 0 V or V <sub>CC</sub>                                                                                | 0.02                  |      |     | 1                               |                 | μ A |      |

(1) Specified by design, not subject to production test.

## 6.8 Typical Characteristics

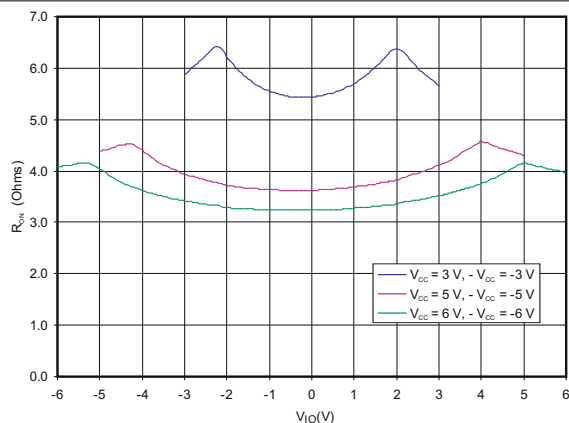
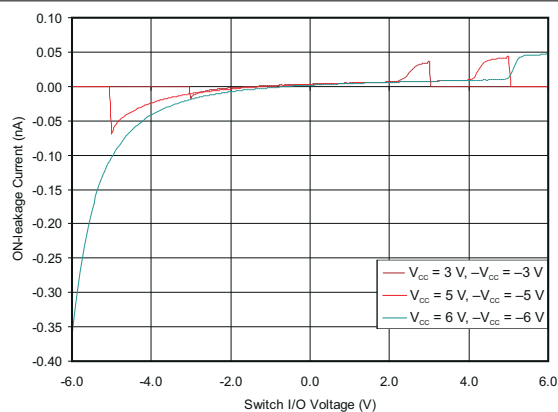
图 6-1.  $R_{ON}$  vs  $V_{IO}$ 

图 6-2. Leakage Current vs I/O Voltage (Switch ON)

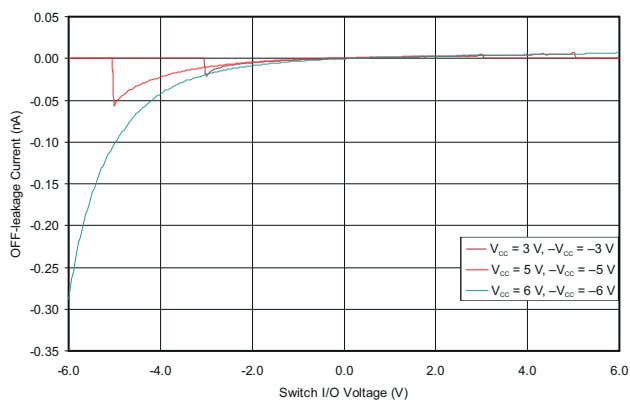


图 6-3. Leakage Current vs I/O Voltage (Switch OFF)

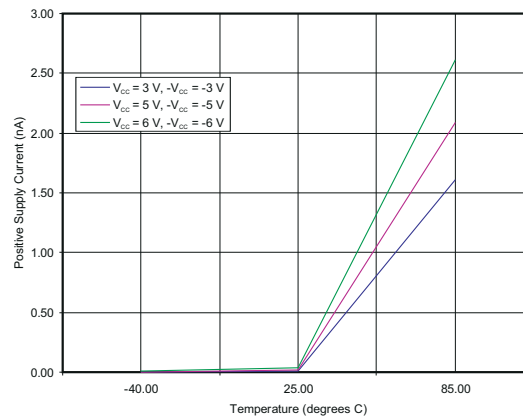


图 6-4. Positive Supply Current vs Temperature

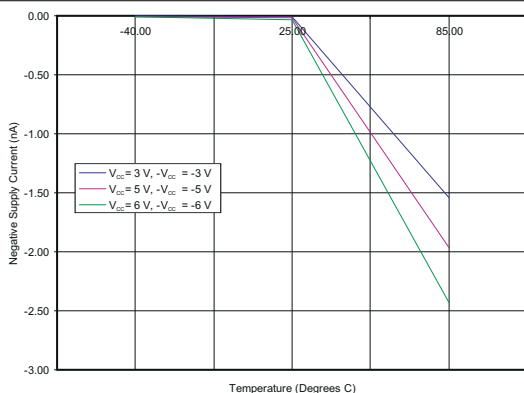


图 6-5. Negative Supply Current vs Temperature

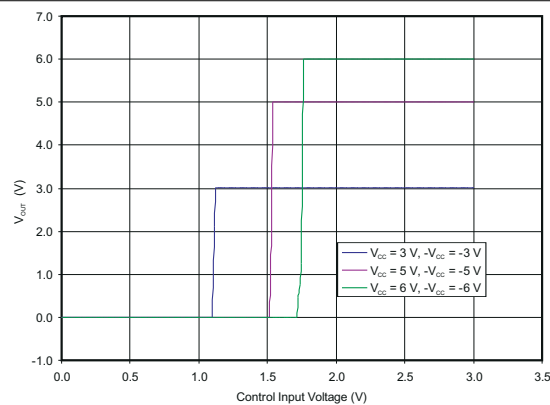


图 6-6. Control Input (IN) Threshold Voltage



## 6.8 Typical Characteristics (continued)

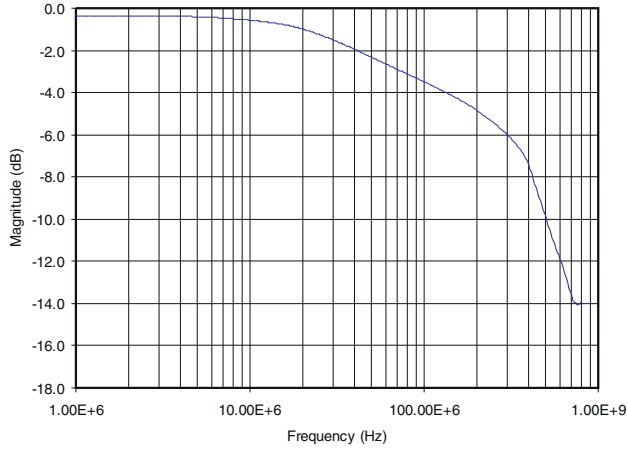


图 6-7. Bandwidth Dual Supply (±5 V)

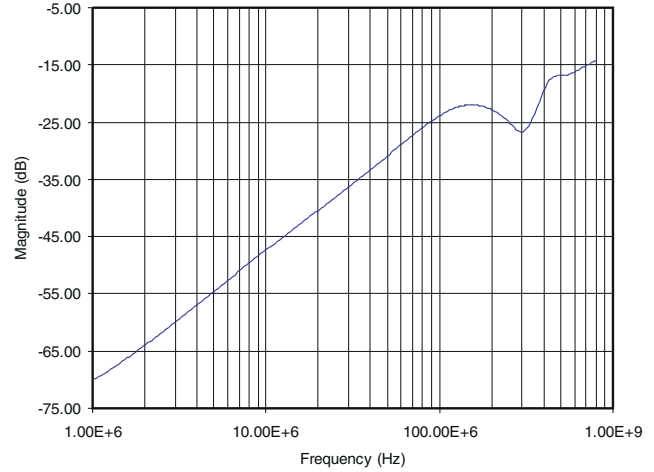


图 6-8. Off Isolation vs Frequency Dual Supply (±5 V)

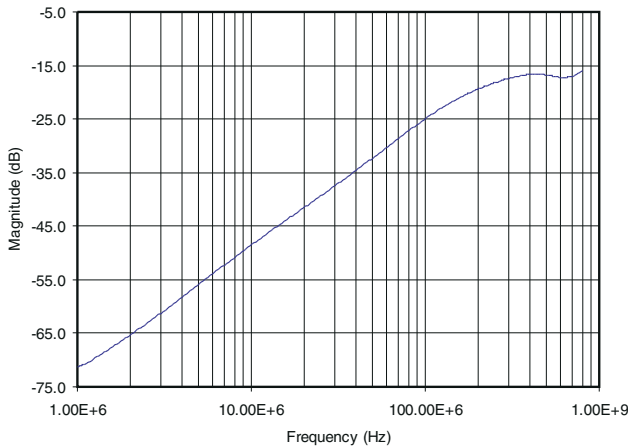


图 6-9. Crosstalk vs Frequency Dual Supply (±5 V)

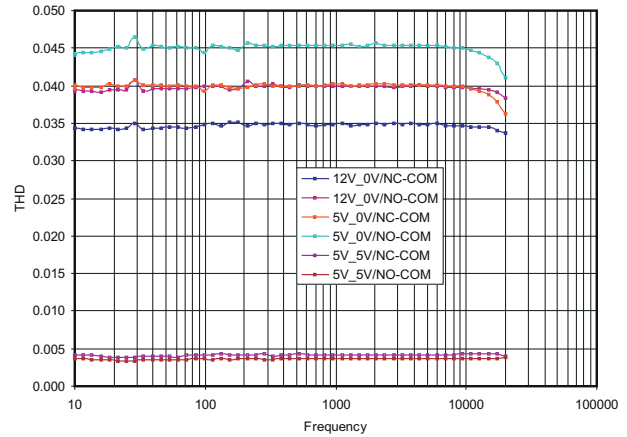


图 6-10. THD+N (%) vs Frequency

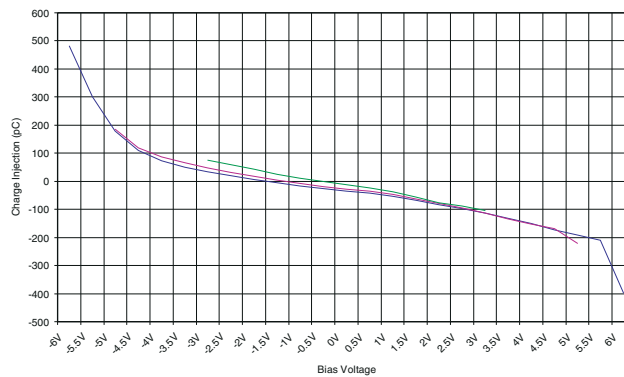
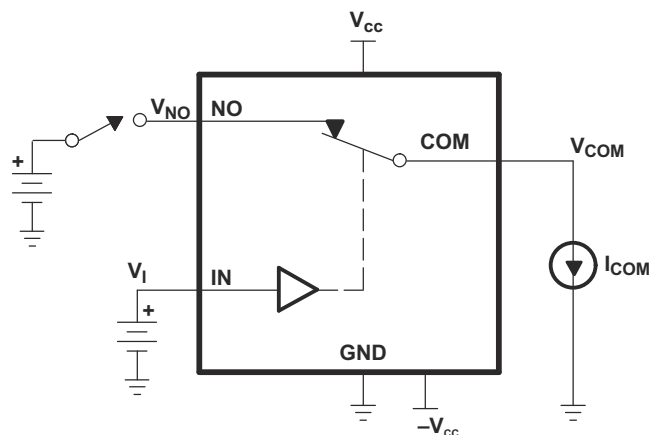


图 6-11. Charge Injection vs Bias Voltage

## 7 Parameter Measurement Information

### 7.1 Test Circuits

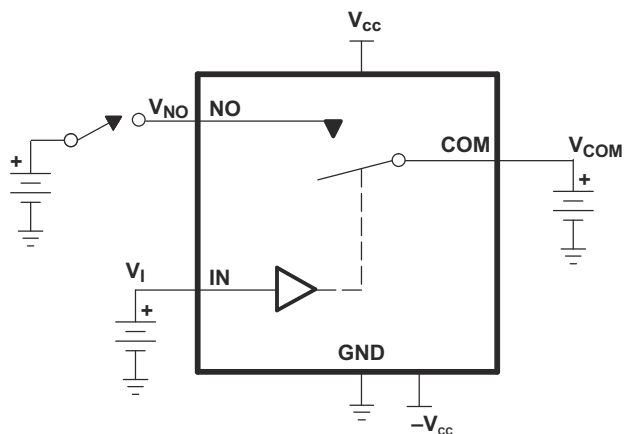


Channel ON

$$R_{on} = \frac{V_{COM} - V_{NO}}{I_{COM}}$$

$V_I = V_{IH} \text{ or } V_{IL}$

图 7-1. ON-State Resistance

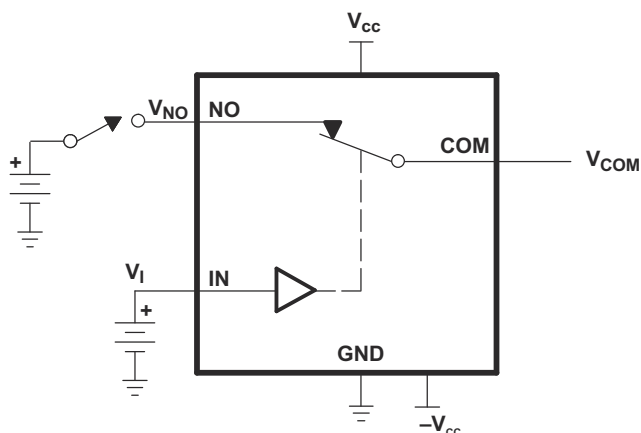


OFF-State Leakage Current

Channel OFF

$V_I = V_{IH} \text{ or } V_{IL}$

图 7-2. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NC(OFF)}$ )



ON-State Leakage Current

Channel ON

$V_I = V_{IH} \text{ or } V_{IL}$

图 7-3. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ )

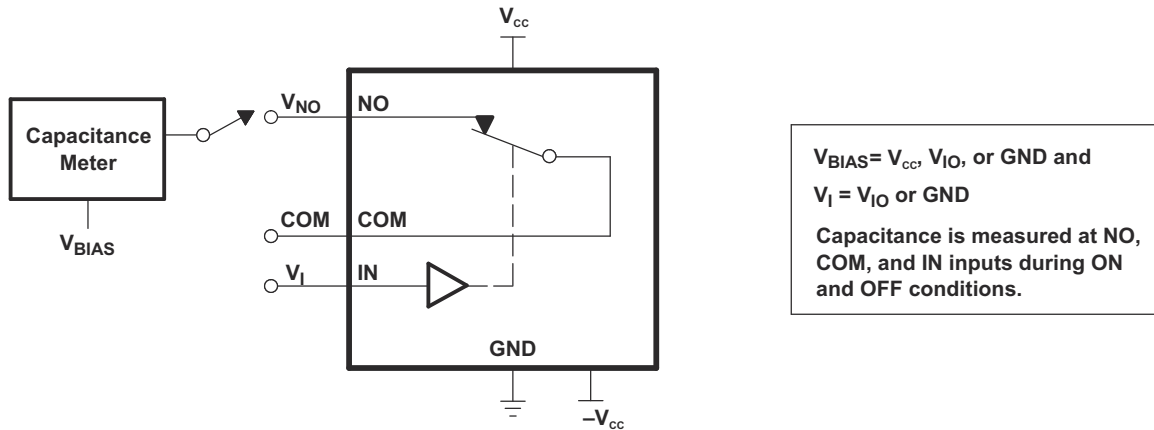
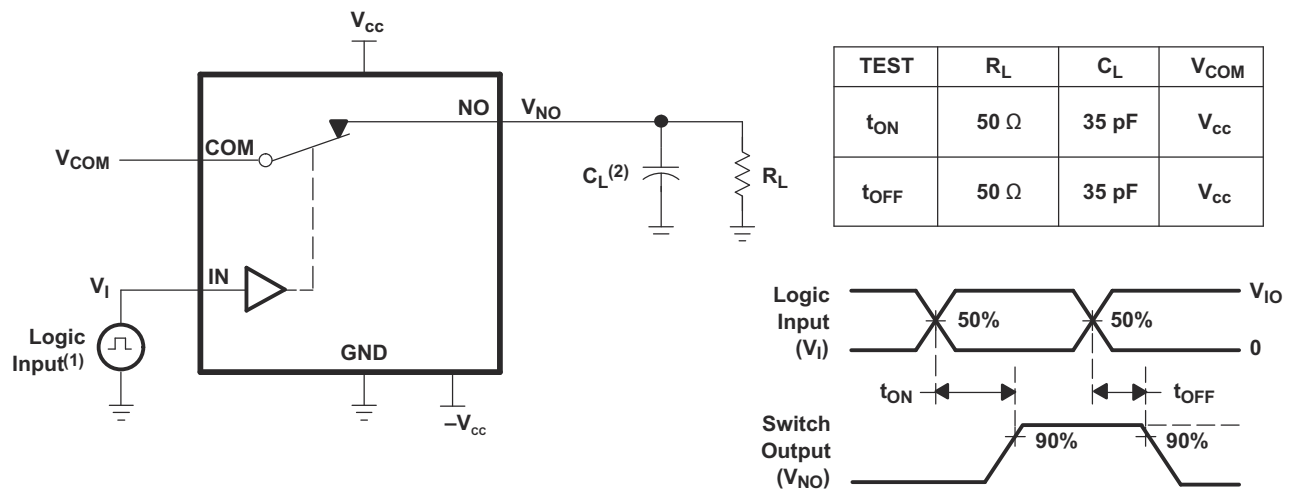
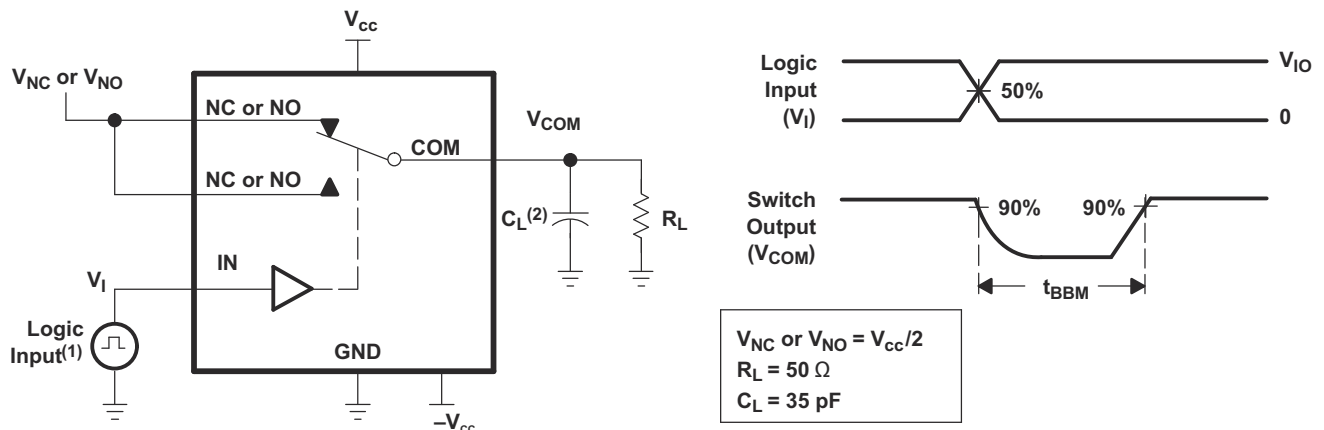


图 7-4. Capacitance ( $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NC(ON)}$ )



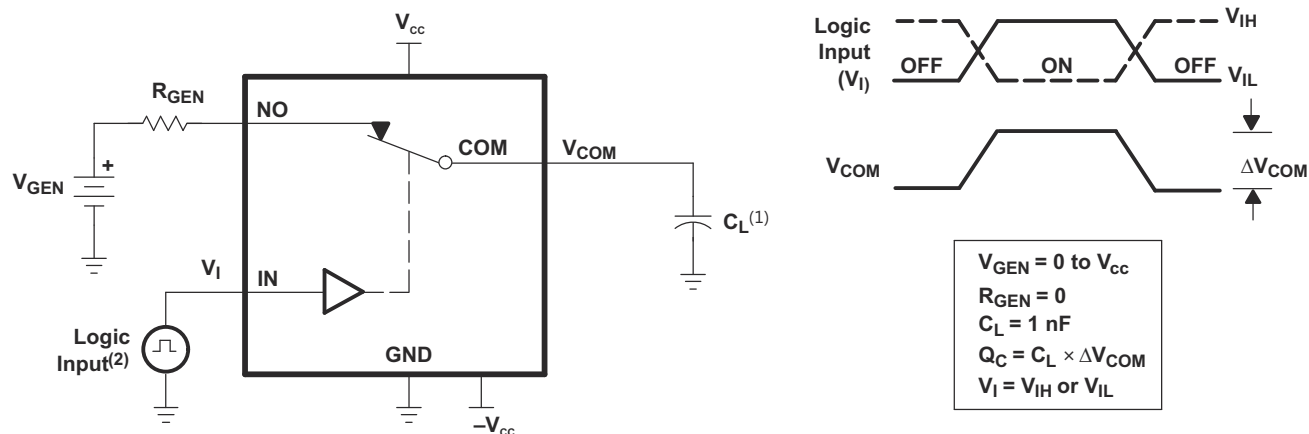
- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.  
(2)  $C_L$  includes probe and jig capacitance.

图 7-5. Turn-ON ( $t_{ON}$ ) and Turn-OFF Time ( $t_{OFF}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.  
(2)  $C_L$  includes probe and jig capacitance.

图 7-6. Break-Before-Make Time Delay ( $t_{BBM}$ )



(1)  $C_L$  includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .

图 7-7. Charge Injection ( $Q_C$ )

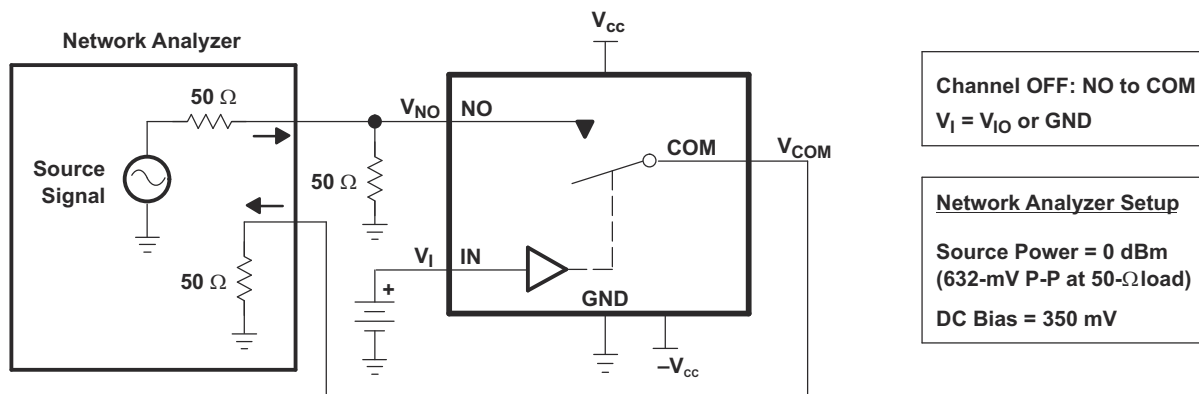


图 7-8. OFF Isolation ( $O_{ISO}$ )

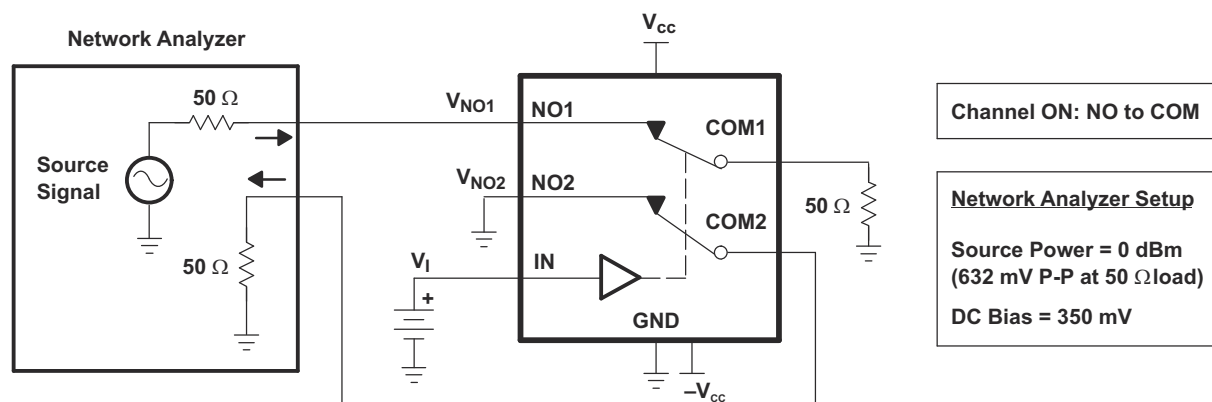


图 7-9. Channel-to-Channel Crosstalk ( $X_{TALK}$ )

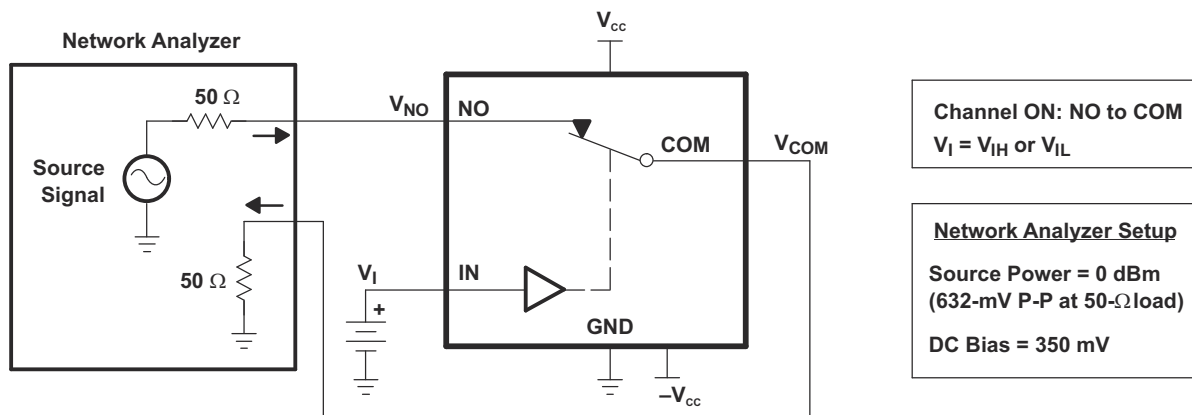
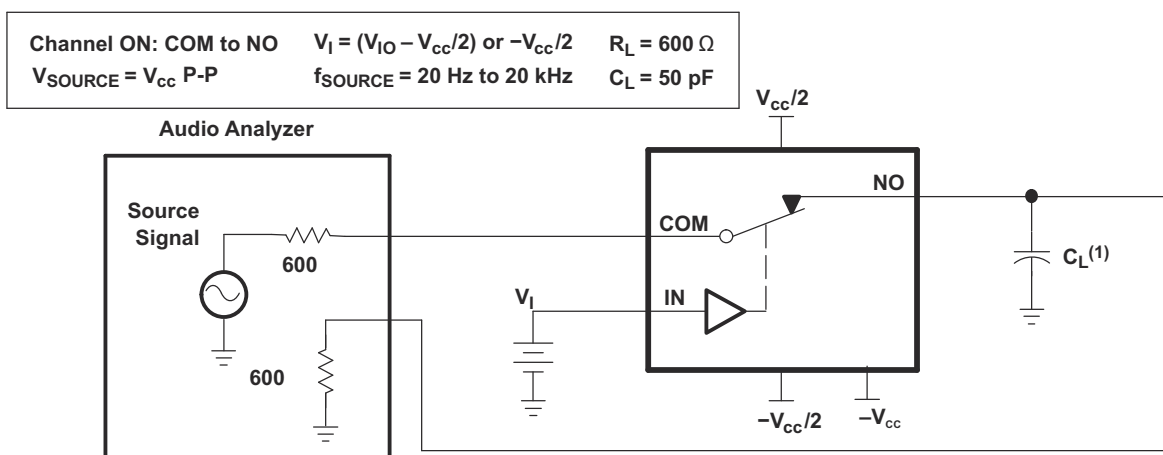


图 7-10. Bandwidth (BW)



<sup>(1)</sup>  $C_L$  includes probe and jig capacitance.

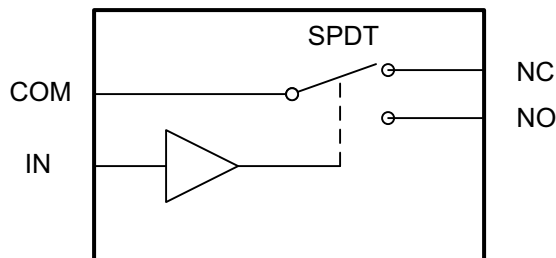
图 7-11. Total Harmonic Distortion

## 8 Detailed Description

### 8.1 Overview

The TS12A12511 is a bidirectional, single channel, single-pole double-throw (SPDT) analog switch that can pass signals with swings of 0 to 12 V or  $-6$  V to 6 V. This switch conducts equally well in both directions when it is on. It also offers a low ON-state resistance of  $5\ \Omega$  (typical), which is matched to within  $1\ \Omega$  between channels. The maximum current consumption is  $< 1\ \mu\text{A}$  and  $-3$  dB bandwidth is  $> 93$  MHz. The TS12A12511 exhibits break-before-make switching action, preventing momentary shorting when switching channels. This device is available in an 8-lead MSOP, 8-lead SOT-23, and 8-pin QFN package.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The TS12A12511 can pass signals with swings of 0 to 12 V or  $-6$  V to 6. The device is great for applications where the AC signals do not have a common mode voltage since both the positive and negative swing of the signal can be passed through the device with little distortion.

### 8.4 Device Functional Modes

表 8-1. Truth Table

| IN | NC TO COM, COM TO NC | NO TO COM, COM TO NO |
|----|----------------------|----------------------|
| L  | On                   | Off                  |
| H  | Off                  | On                   |

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

Analog signals that range over the entire supply voltage ( $V_{CC}$  to GND) or ( $V_{CC}$  to  $-V_{CC}$ ) can be passed with very little change in ON-state resistance. The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

### 9.2 Typical Application

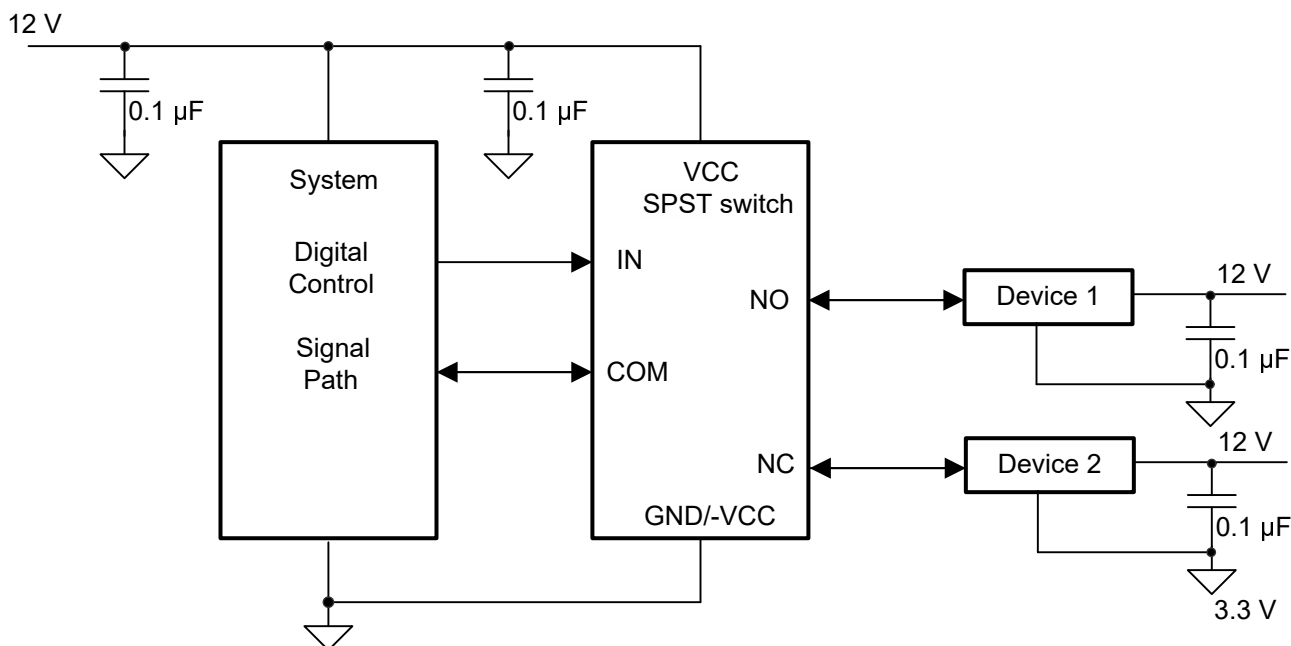


图 9-1. Typical Application Schematic

#### 9.2.1 Design Requirements

Pull the digitally controlled input select pin IN to VCC or GND to avoid unwanted switch states that could result if the logic control pin is left floating.

#### 9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch since the TS12A12511 input or output signal swing of the device is dependant of the supply voltage  $V_{CC}$  and  $-V_{CC}$ .

### 9.2.3 Application Curve

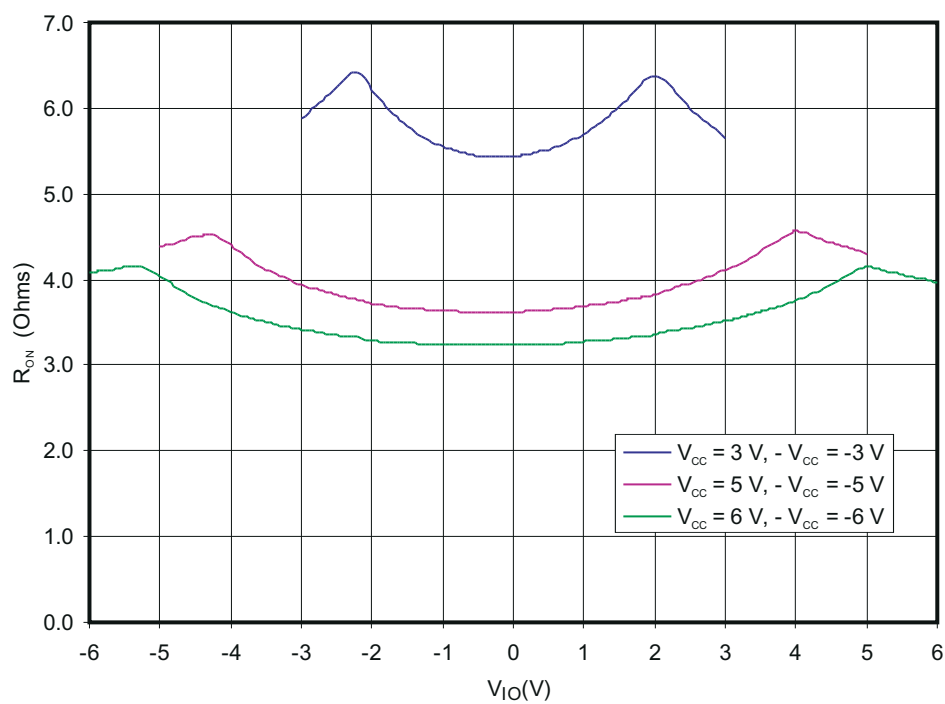


图 9-2.  $R_{ON}$  vs  $V_{IO}$



## 10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC and -VCC on first, followed by NO, NC, or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1- $\mu$ F capacitor, connected from VCC to GND, is adequate for most applications.

## 11 Layout

### 11.1 Layout Guidelines

It is recommended to place a bypass capacitor as close to the supply pins, VCC and -VCC, as possible to help smooth out lower frequency noise and provide better load regulation across the frequency spectrum. Minimize trace lengths and vias on the signal paths to preserve signal integrity.

### 11.2 Layout Example

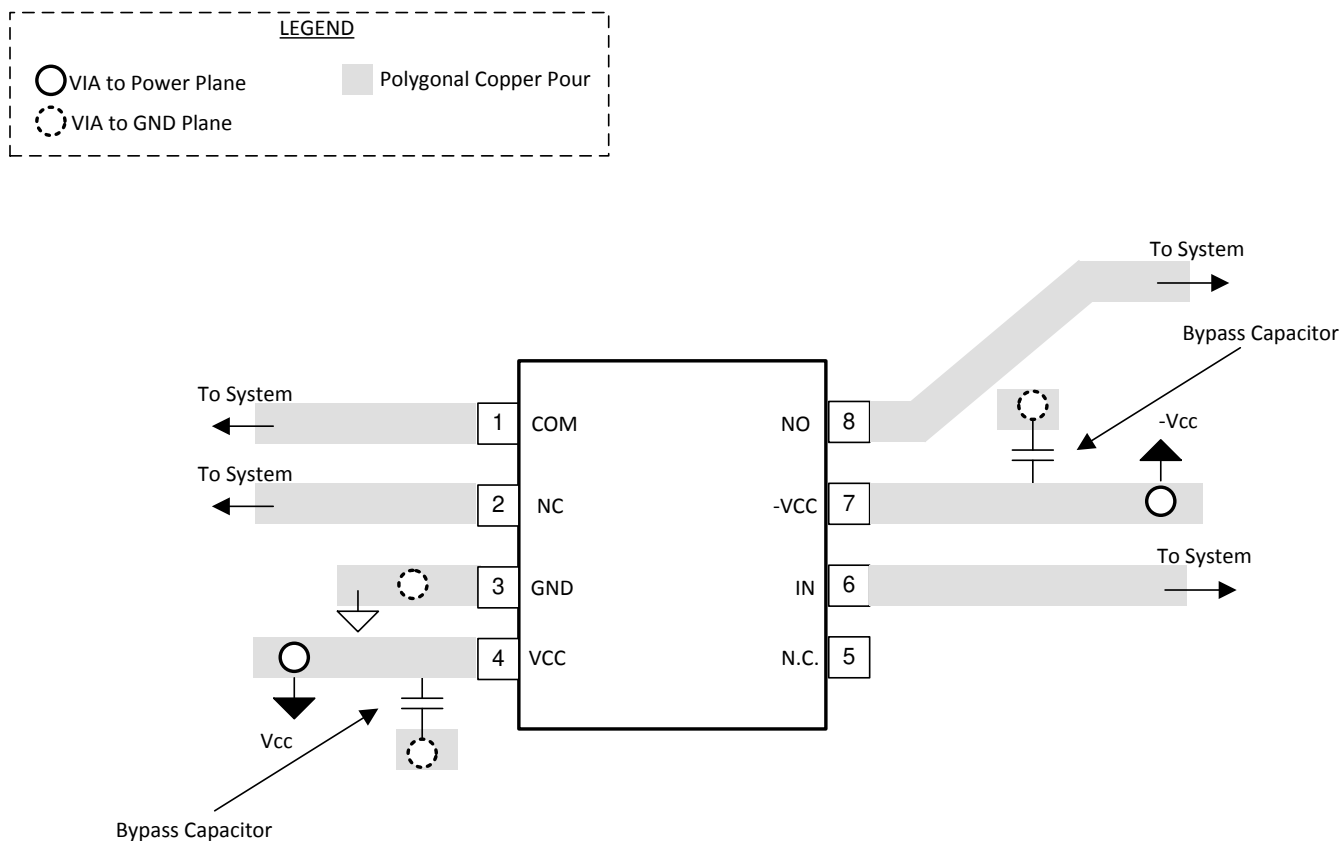


图 11-1. Layout Schematic

## 12 Device and Documentation Support

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 支持资源

**TI E2E™ 支持论坛** 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TS12A12511DCNR</a> | Active        | Production           | SOT-23 (DCN)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | NFHS<br>NFHA        |
| TS12A12511DCNR.A               | Active        | Production           | SOT-23 (DCN)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | NFHS<br>NFHA        |
| TS12A12511DCNR.B               | Active        | Production           | SOT-23 (DCN)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | NFHS<br>NFHA        |
| <a href="#">TS12A12511DGKR</a> | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 2US<br>2UA          |
| TS12A12511DGKR.A               | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 2US<br>2UA          |
| TS12A12511DGKR.B               | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 2US<br>2UA          |
| <a href="#">TS12A12511DRJR</a> | Active        | Production           | SON (DRJ)   8    | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | ZVE                 |
| TS12A12511DRJR.A               | Active        | Production           | SON (DRJ)   8    | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | ZVE                 |
| TS12A12511DRJR.B               | Active        | Production           | SON (DRJ)   8    | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | ZVE                 |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

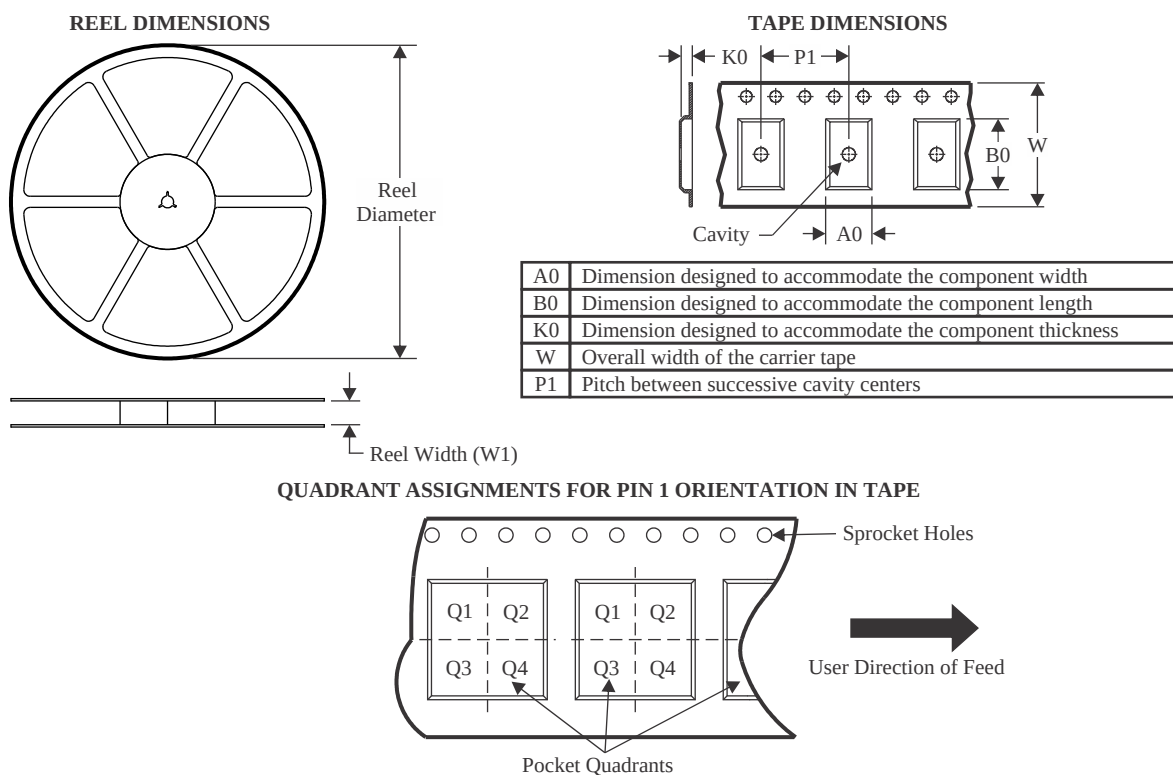
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

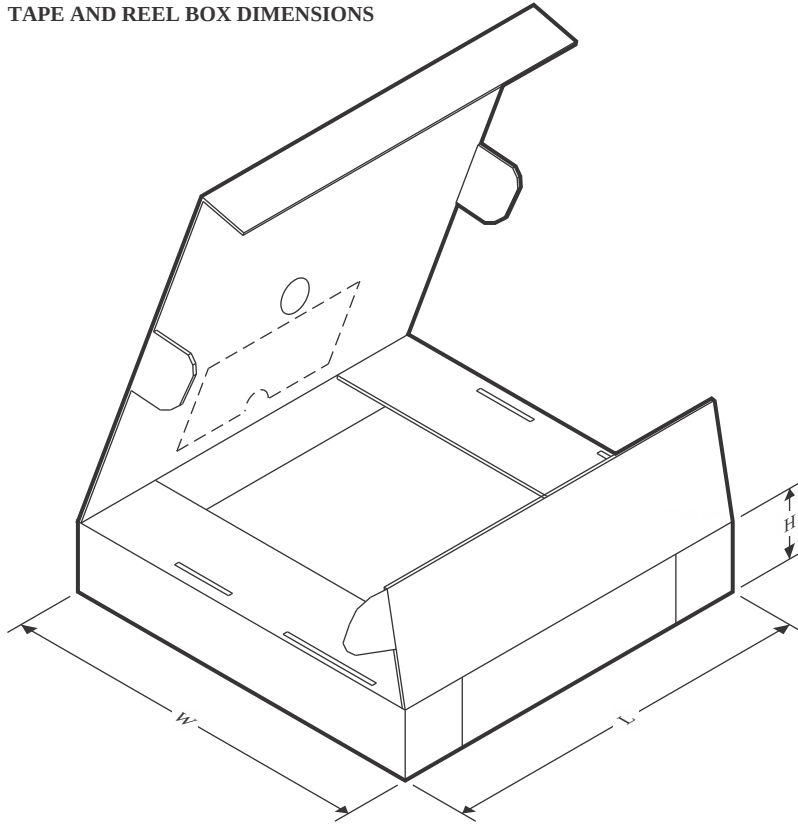
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

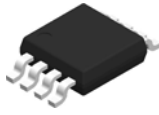
| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TS12A12511DCNR | SOT-23       | DCN             | 8    | 3000 | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| TS12A12511DGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TS12A12511DRJR | SON          | DRJ             | 8    | 1000 | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

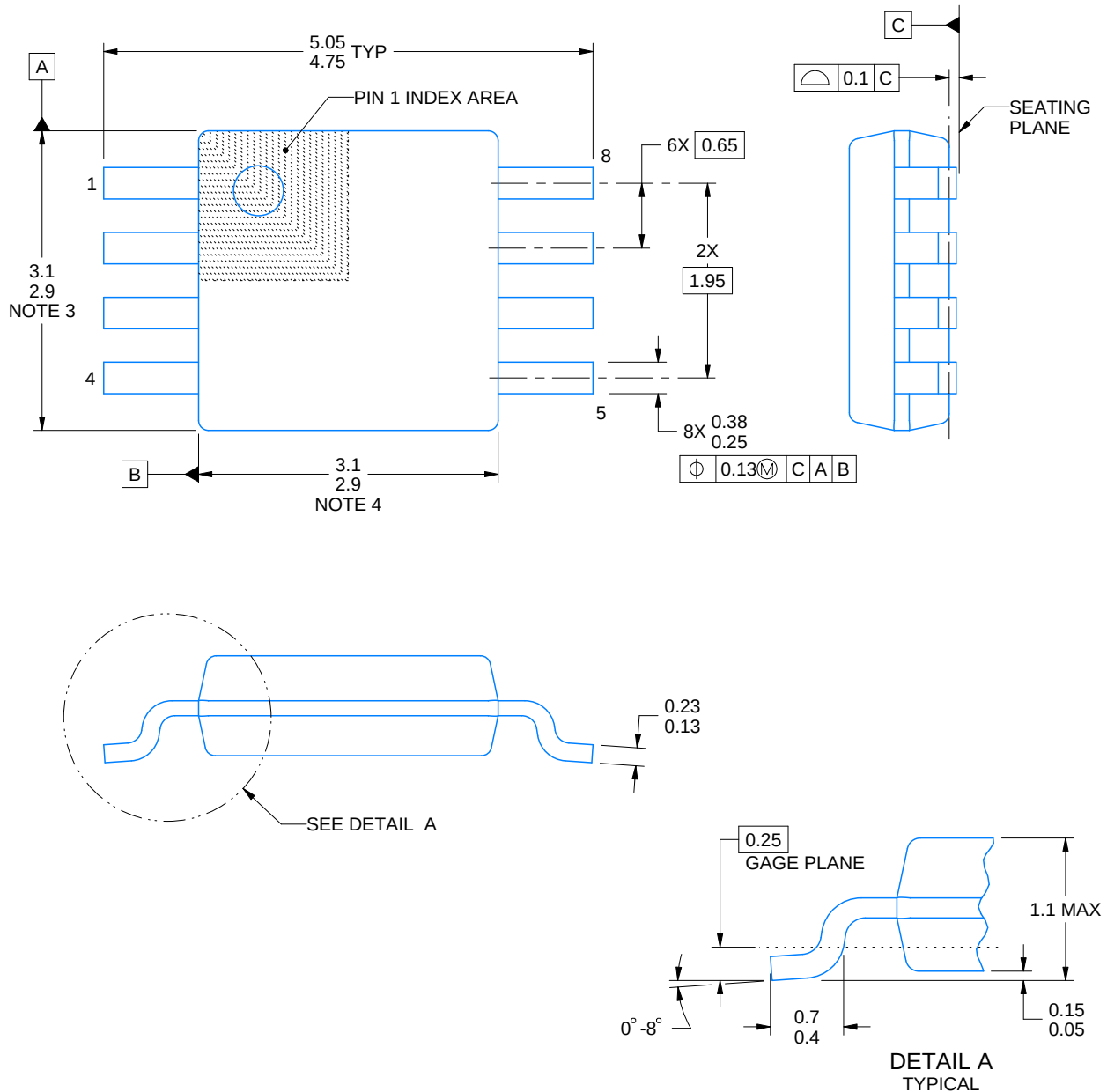


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TS12A12511DCNR | SOT-23       | DCN             | 8    | 3000 | 202.0       | 201.0      | 28.0        |
| TS12A12511DGKR | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| TS12A12511DRJR | SON          | DRJ             | 8    | 1000 | 213.0       | 191.0      | 35.0        |

**DGK0008A****PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

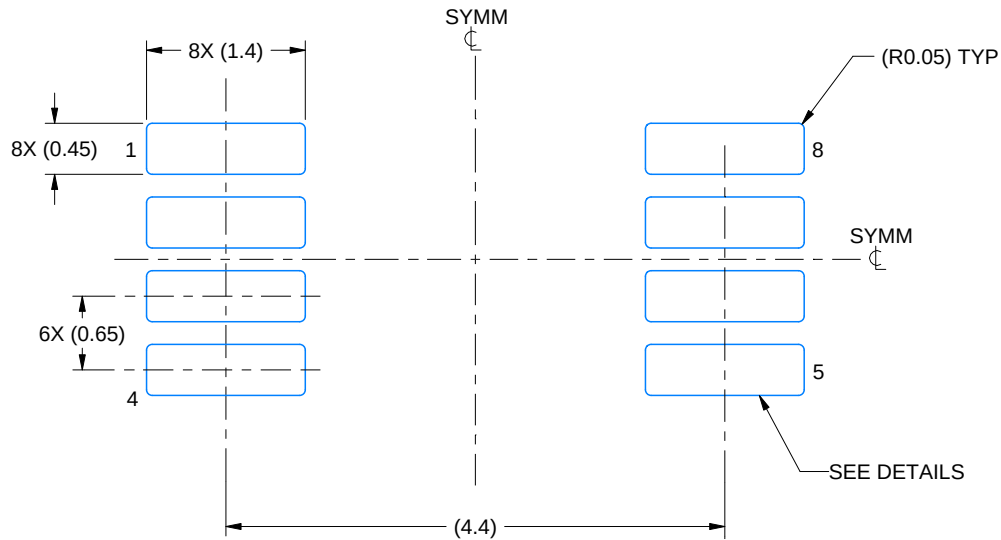
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

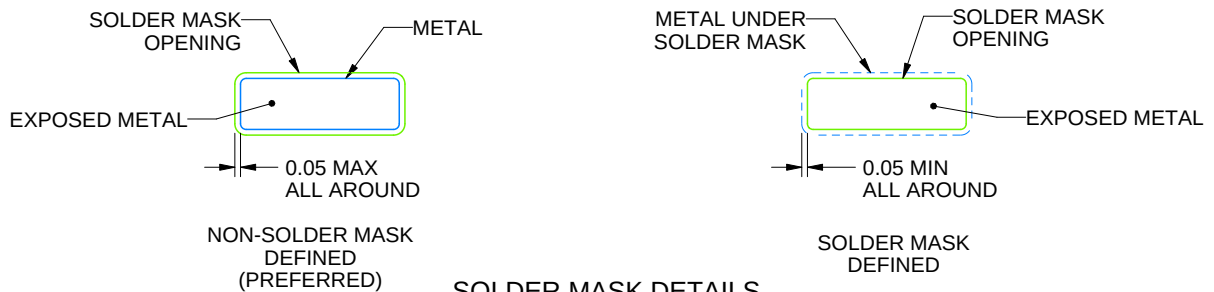
DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

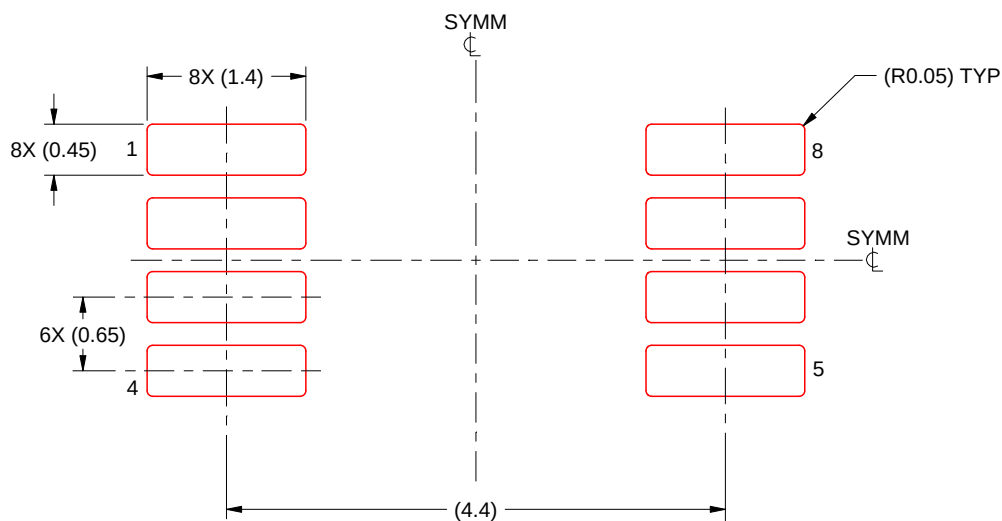


## EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

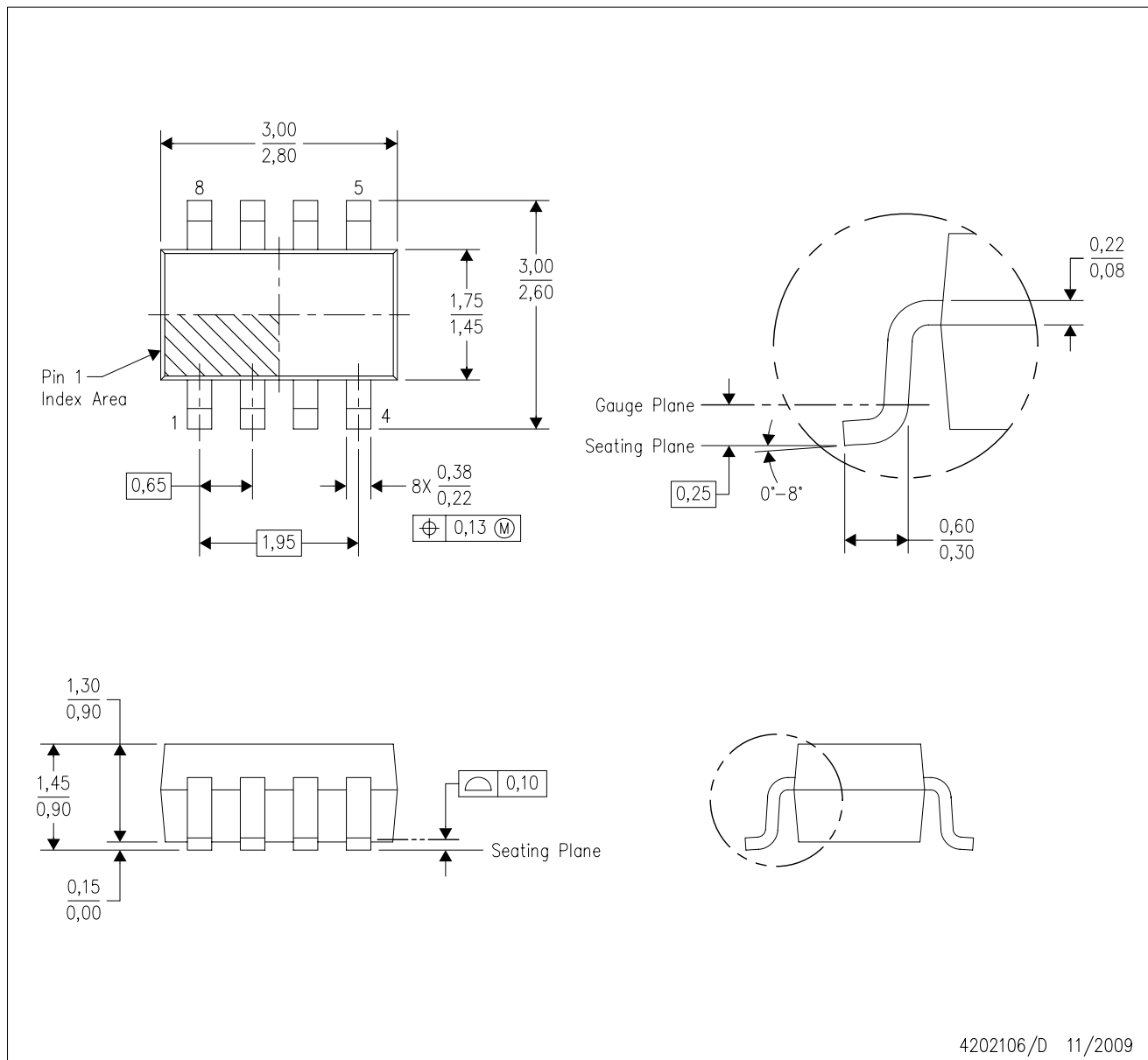
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DCN (R-PDSO-G8)

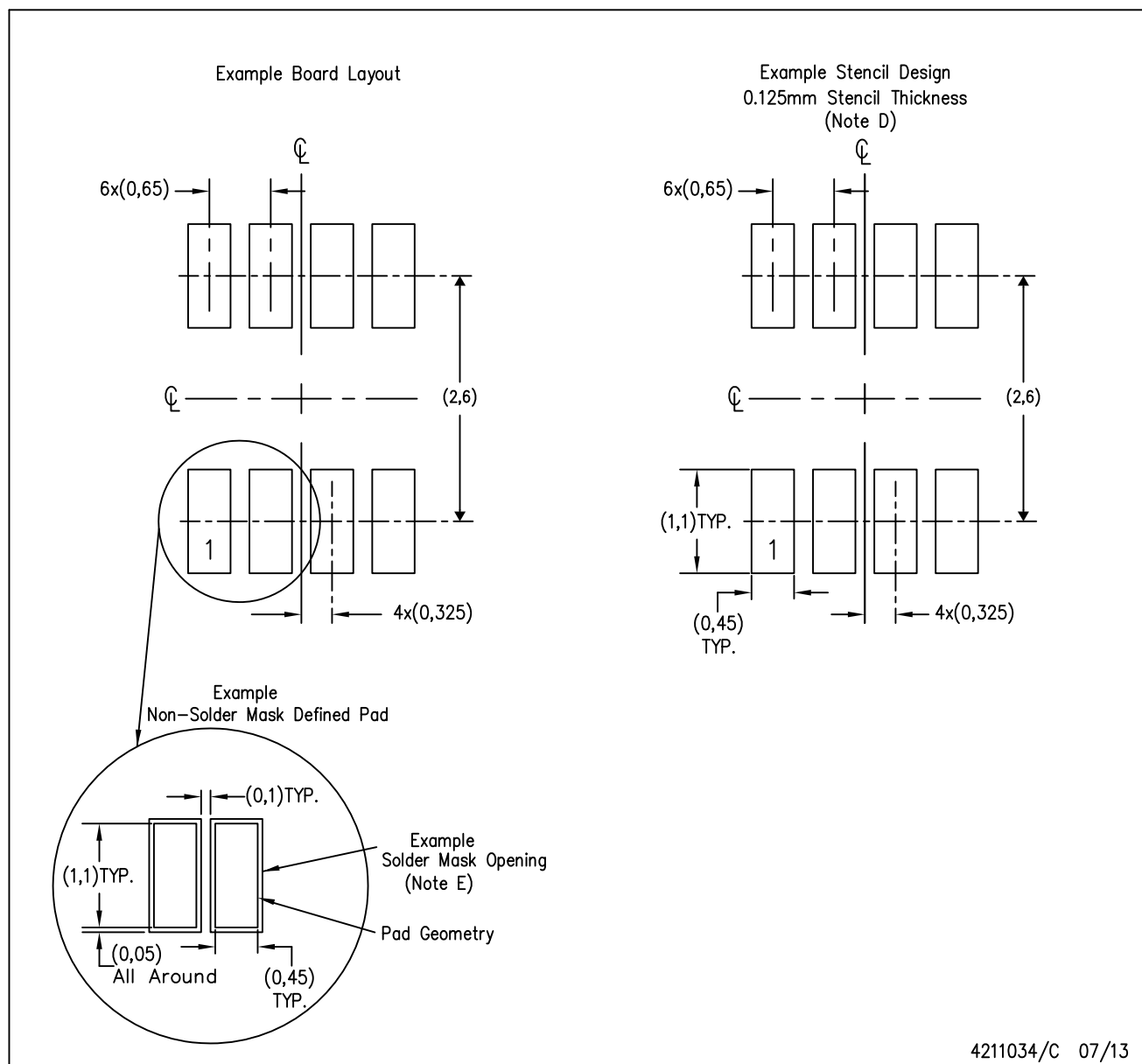
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
  - D. Package outline inclusive of solder plating.
  - E. A visual index feature must be located within the Pin 1 index area.
  - F. Falls within JEDEC MO-178 Variation BA.
  - G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8)

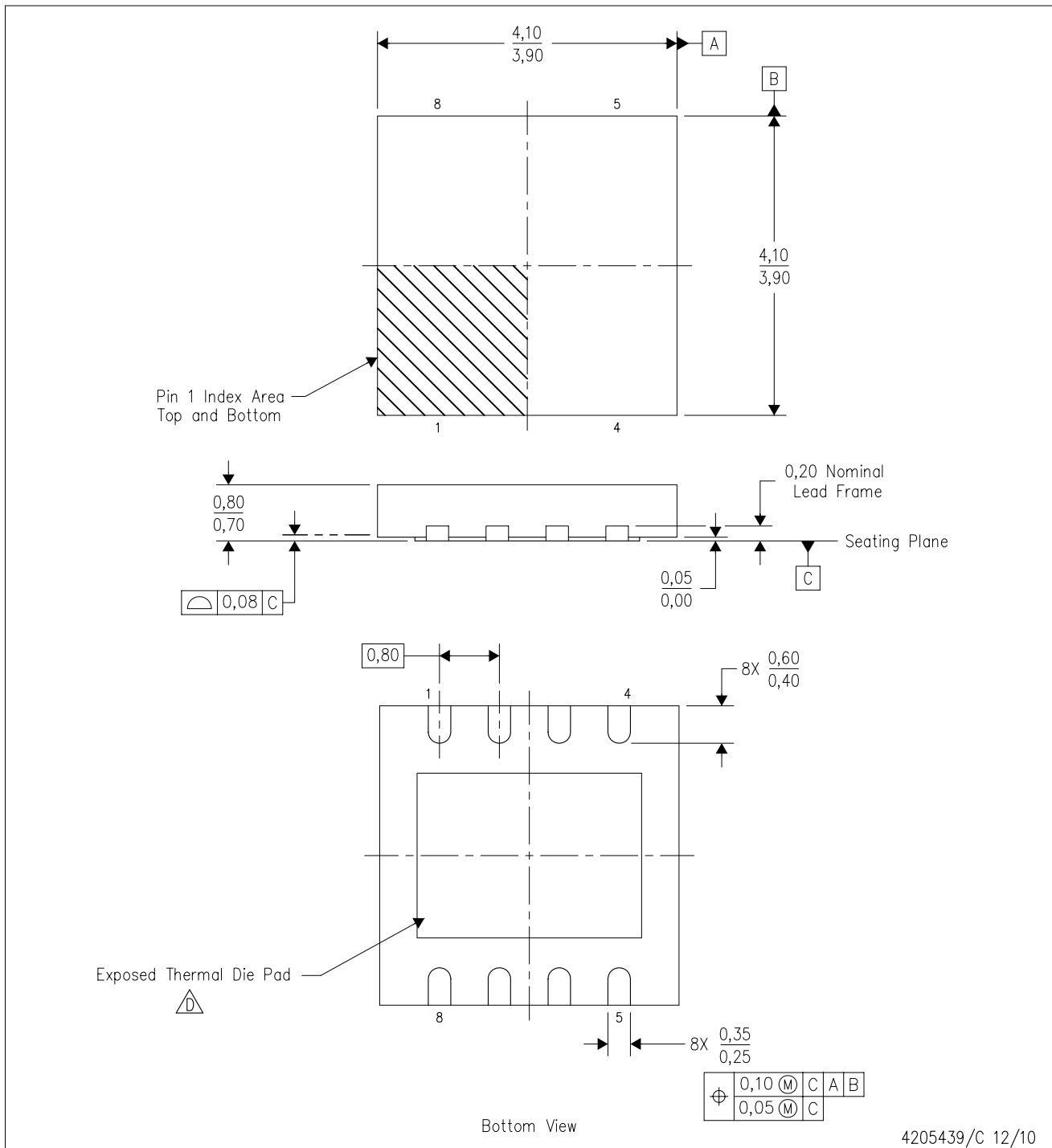
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRJ (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



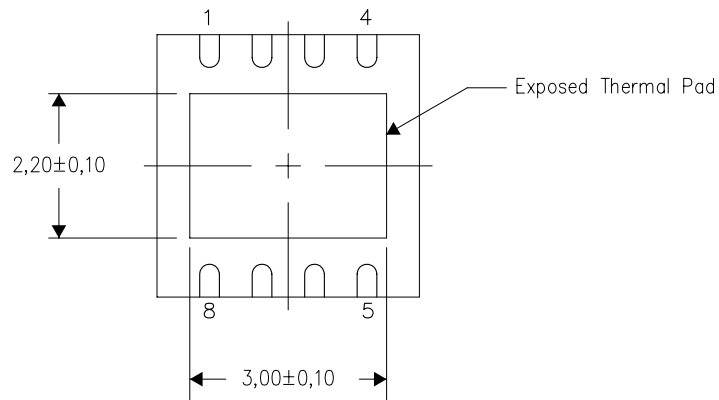
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Package complies to JEDEC MO-229 variation WGGB.

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

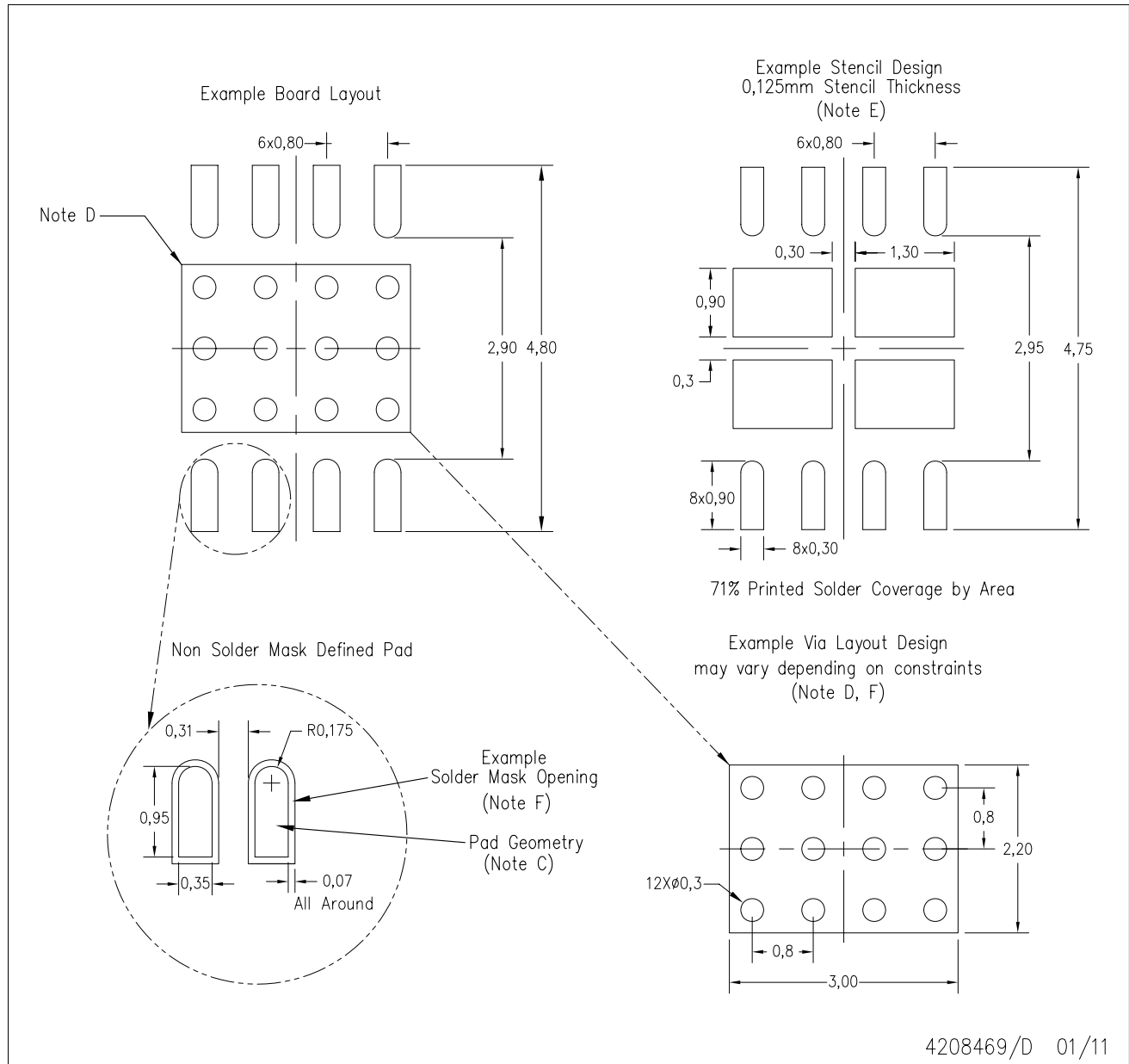
Exposed Thermal Pad Dimensions

4206882/F 01/11

NOTE: All linear dimensions are in millimeters

DRJ (S-PWSON-N8)

SMALL PACKAGE OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
版权所有 © 2025，德州仪器 (TI) 公司