

具有 $\pm 15\text{kV}$ IEC ESD 保护功能的 TRS3243E 3V 至 5.5V 多通道 RS-232 线路驱动器或接收器

1 特性

- 用于 IBM™ PC/AT™ 串行端口的单芯片和单电源接口
- 为 RS-232 总线引脚提供 ESD 保护
 - $\pm 15\text{kV}$ 人体放电模型 (HBM)
 - $\pm 8\text{kV}$ IEC61000-4-2 接触放电
 - $\pm 15\text{kV}$ IEC61000-4-2 气隙放电
- 符合或超出 TIA/EIA-232-F 和 ITU v.28 标准的要求
- 由 3V 至 5.5V V_{CC} 电源供电
- 始终有效同相接收器输出 (ROUT2B)
- 旨在以高达 500kbit/s 的数据速率传输数据
- 低待机电流: $1\mu\text{A}$ (典型值)
- 外部电容器: $4 \times 0.1\mu\text{F}$
- 接受 5V 逻辑输入及 3.3V 电源
- 设计为可与业界通用 '3243E 器件互换
- 串行鼠标驱动能力
- 自动断电功能, 在没有检测到有效 RS-232 信号时禁用驱动器输出
- 封装选项包括塑料小外形封装 (DW)、紧缩小外形封装 (DB) 和薄型紧缩小外形封装 (PW)

2 应用

- 电池供电型系统
- 个人电子产品
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

3 说明

TRS3243E 器件由三个线路驱动器、五个线路接收器和一个双电荷泵电路组成, 在串行端口连接引脚上具有 $\pm 15\text{kV}$ ESD (HBM 和 IEC61000-4-2, 空气间隙放电) 和 $\pm 8\text{kV}$ ESD (IEC61000-4-2, 接触放电) 保护。该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。这种驱动器和接收器的组合可满足对在 IBM PC/AT 中使用的典型串行端口的需求或与之兼容。电荷泵和四个小型外部电容器支持由 3V 至 5.5V 单电源供电。另外, 该器件包括一个始终有效同相输出 (ROUT2B), 这使得使用振铃指示的应用能够在器件断电的情况下发送数据。该器件以高达 250kbit/s 的数据信号传输速率运行, 驱动器输出压摆率最高为 $30\text{V}/\mu\text{s}$ 。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
TRS3243E	SSOP (DB)	10.20mm × 5.30mm
	SOIC (DW)	17.90 mm × 7.50mm
	TSSOP (PW)	9.70 mm × 4.40 mm
	VQFN (RHB)	5.00mm × 5.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

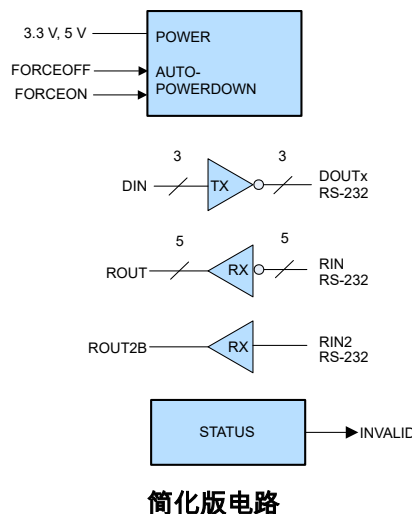


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4 Revision History

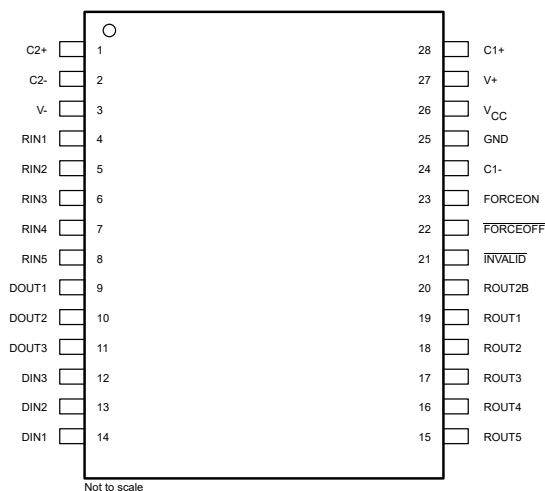
注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (October 2022) to Revision E (December 2022)	Page
• Changed 表 9-1 to match revision C of the data sheet. V_{CC} column: 3 V $\pm$ 5.5 V to: 3 V to 5.5 V and C1 column value: 0.47 μ F to: 0.047 μ F	15

Changes from Revision C (September 2011) to Revision D (October 2022)	Page
• 删除了 订购信息 表.....	1
• 添加了 器件信息 表、引脚配置和功能 部分、特性说明 部分、器件功能模式、应用和实施 部分、器件和文档支持 部分以及 机械、封装和可订购信息 部分。	1
• 将首页图像从“方框图”更改为“简化电路”.....	1
• Added the ESD Ratings - IEC Specifications table.....	6
• Changed the I_{CC} Supply current auto-powerdown disabled MAX value from 1 mA to 1.2 mA in the <i>Electrical Characteristics</i>	8

Changes from Revision B (July 2009) to Revision C (September 2011)	Page
• Deleted "VALID RIN RS-232 LEVEL" from INPUTS.....	14
• Deleted "ROUT2B is active" RECEIVER STATUS and combined ROUT outputs.....	14
• Added table "ROUT2B and INVALID Outputs" defining truth for ROUT2B and INVALID outputs.	14

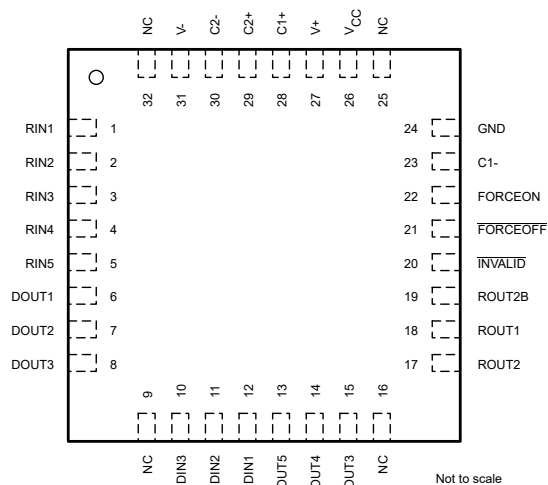
5 Pin Configuration and Functions



**图 5-1. DB, DW, or PW Package, 28 Pin (SSOP, SOIC, TSSOP)
(Top View)**

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the voltage-doubler charge-pump capacitor
2	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
3	V-	—	Negative charge pump output voltage
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active noninverting receiver output;
21	INVALID	O	Invalid Output Pin
22	FORCEOFF	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
25	GND	—	Ground
26	V _{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor



**图 5-2. RHB Package, 32 Pin (VQFN)
(Top View)**

表 5-2. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	RIN1	I	RS-232 receiver inputs
2	RIN2		
3	RIN3		
4	RIN4		
5	RIN5		
6	DOUT1	O	RS-232 driver outputs
7	DOUT2		
8	DOUT3		
9	NC	—	Not connected internally
10	DIN3	I	Driver inputs
11	DIN2		
12	DIN1		
13	ROUT5	O	Receiver outputs
14	ROUT4		
15	ROUT3		
16	NC	—	Not connected internally
17	ROUT2	O	Receiver outputs
18	ROUT1		
19	ROUT2B	O	Always-active noninverting receiver output
20	INVALID	O	Invalid Output Pin
21	FORCEOFF	I	Auto Powerdown Control input (Refer to Truth Table)
22	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
23	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
24	GND	—	Ground
25	NC	—	Not connected internally
26	V _{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage

表 5-2. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor
29	C2+	—	
30	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
31	V-	—	Negative charge pump output voltage
32	NC	—	Not connected internally

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		−0.3	6	V
V+	Positive output supply voltage ⁽²⁾		−0.3	7	V
V−	Negative output supply voltage ⁽²⁾		0.3	−7	V
V+ − V−	Output supply voltage difference ⁽²⁾			13	V
V _I	Input voltage	Driver (FORCEOFF, FORCEON)	−0.3	6	V
		Receiver	−25	25	
V _O	Output voltage	Driver	−13.2	13.2	V
		Receiver (INVALID)	−0.3	V _{CC} + 0.3	
T _{stg}	Storage temperature		−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to network GND.

6.2 ESD Ratings

			VALUE	UNIT
Driver Section				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ Driver output pins	±15,000	V
Receiver Section				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ Receiver input pins	±15,000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
Driver Section					
V _(ESD)	Electrostatic discharge	IEC61000-4-2, Air-Gap Discharge ⁽¹⁾	Driver outputs pins	±15	kV
		IEC61000-4-2, Contact Discharge ⁽¹⁾		±8	
Receiver Section					
V _(ESD)	Electrostatic discharge	IEC61000-4-2, Air-Gap Discharge ⁽¹⁾	Receiver input pins	±15	kV
		IEC61000-4-2, Contact Discharge ⁽¹⁾		±8	

- (1) For the DB, PW and RHB package only: A minimum of 1-μF capacitor between V_{CC} and GND is required to meet the specified IEC 61000-4-2 rating

6.4 Recommended Operating Conditions

See [Figure 9-1](#) ⁽¹⁾

			MIN	NOM	MAX	UNIT
Supply voltage		V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	
V _{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON	V _{CC} = 3.3 V		2	V
			V _{CC} = 5 V		2.4	
V _{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON			0.8	V
V _I	Driver and control input voltage	DIN, FORCEOFF, FORCEON	0		5.5	V
V _I	Receiver input voltage		–25		25	V
T _A	Operating free-air temperature	TRS3243EC	0		70	°C
		TRS3243EI	–40		85	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		VQFN (RHB)	TSSOP (PW)	SOIC (DW)	DB (SSOP)	UNIT
		32 PINS	28 PINS	28 PINS	28 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	34.1	70.3	59.0	76.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	25.9	21.0	28.8	35.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	14.6	29.2	30.3	37.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.5	1.3	7.8	7.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	14.6	28.8	30.0	37.0	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	5.1	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 9-1](#))⁽²⁾

PARAMETER			TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
I _I	Input leakage current	FORCEOFF, FORCEON				±0.01	±1	μA
I _{CC}	Supply current (T _A = 25°C)	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V _{CC} For DB, PW and RHB package			0.3	1.2	mA
		Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V _{CC} For DW package			0.3	1	mA
		Powered off	No load, FORCEOFF at GND			1	10	μA
		Auto-powerdown enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded, All DIN are grounded			1	10	
DRIVER SECTION								
V _{OH}	High-level output voltage	All DOUT at R _L = 3 kΩ to GND			5	5.4		V
V _{OL}	Low-level output voltage	All DOUT at R _L = 3 kΩ to GND			–5	–5.4		V
V _O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V _{CC} , 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA			±5			V
I _{IH}	High-level input current	V _I = V _{CC}			±0.01		±1	μA
I _{IL}	Low-level input current	V _I at GND			±0.01		±1	μA
V _{hys}	Input hysteresis						±1	V
I _{OS}	Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V,	V _O = 0 V				±60	mA
		V _{CC} = 5.5 V,	V _O = 0 V					
r _O	Output resistance	V _{CC} , V+, and V– = 0 V,		V _O = ±2 V	300	10M		Ω
I _{off}	Output leakage current	FORCEOFF = GND,	V _O = ±12 V,		V _{CC} = 0 to 5.5 V		±25	μA
RECEIVER SECTION								
V _{OH}	High-level output voltage	I _{OH} = –1 mA			V _{CC} – 0.6	V _{CC} – 0.1		V
V _{OL}	Low-level output voltage	I _{OH} = 1.6 mA					0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V				1.6	2.4	V
		V _{CC} = 5 V				1.9	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V			0.6	1.1		V
		V _{CC} = 5 V			0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})					0.5		V
I _{off}	Output leakage current (except ROUT2B)	FORCEOFF = 0 V				±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V or ±25 V			3	5	7	kΩ
AUTO-POWERDOWN SECTION								
V _{IT+(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}					2.7	V
V _{IT–(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}			–2.7			V
V _{T(invalid)}	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}			–0.3		0.3	V
V _{OH}	INVALID high-level output voltage	I _{OH} = -1 mA, FORCEON = GND, FORCEOFF = V _{CC}			V _{CC} – 0.6			V
V _{OL}	INVALID low-level output voltage	I _{OL} = 1.6 mA, FORCEON = GND, FORCEOFF = V _{CC}					0.4	V

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

(2) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF, C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

6.7 Switching Characteristics

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 9-1](#)) ⁽²⁾

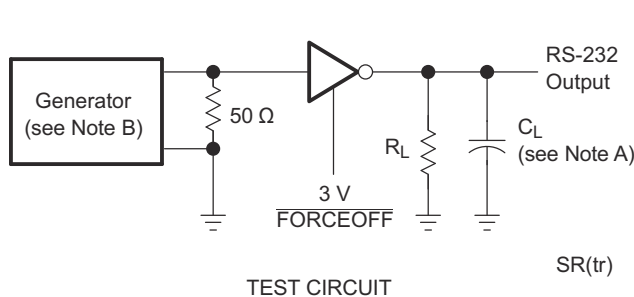
PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
DRIVER SECTION						
	Maximum data rate	$C_L = 1000\text{ pF}$, One DOUT switching, $R_L = 3\text{ k}\Omega$ See Figure 1	250	500		kbit/s
$t_{sk(p)}$	Pulse skew ⁽³⁾	$C_L = 150\text{ pF}$ to 2500 pF , $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, See Figure 2		100		ns
$SR_{(tr)}$	Slew rate, transition region (see Figure 1)	$V_{CC} = 3.3\text{ V}$, $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, PRR = 250 kbit/s				V/ μs
		$C_L = 150\text{ pF}$ to 1000 pF	6		30	
		$C_L = 150\text{ pF}$ to 2500 pF	4		30	
RECEIVER SECTION						
t_{PLH}	Propagation delay time, low-to high-level output	$C_L = 150\text{ pF}$, See Figure 7-2		150		ns
t_{PHL}	Propagation delay time, high-to low-level output			150		ns
t_{en}	Output enable time	$C_L = 150\text{ pF}$, $R_L = 3\text{ k}\Omega$, See Figure 7-3		200		ns
t_{dis}	Output disable time			200		ns
$t_{sk(p)}$	Pulse skew ⁽³⁾	See Figure 7-2		50		ns
AUTO-POWERDOWN SECTION						
t_{valid}	Propagation delay time, low-to high-level output	$V_{CC} = 5\text{ V}$		1		μs
$t_{invalid}$	Propagation delay time, high-to low-level output	$V_{CC} = 5\text{ V}$		30		μs
t_{en}	Supply enable time	$V_{CC} = 5\text{ V}$		100		μs

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

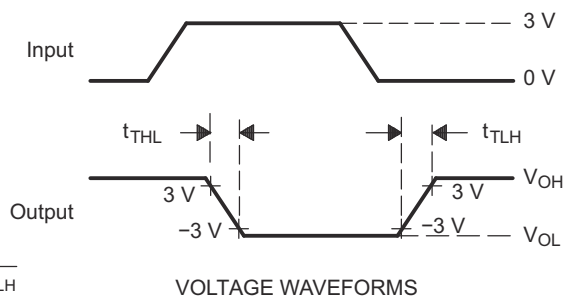
(2) Test conditions are $C1-C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} + 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2-C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

7 Parameter Measurement Information



$$SR(tr) = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

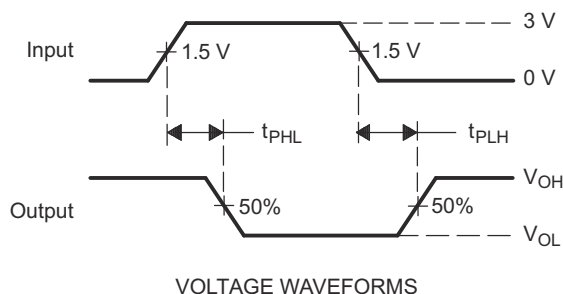
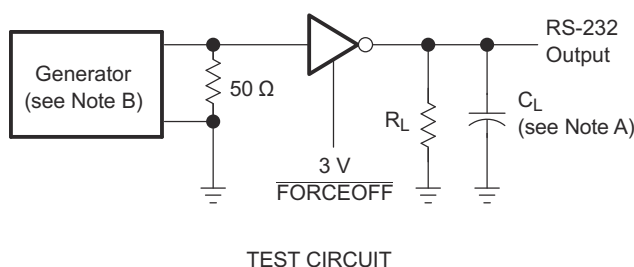


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A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 7-1. Driver Slew Rate

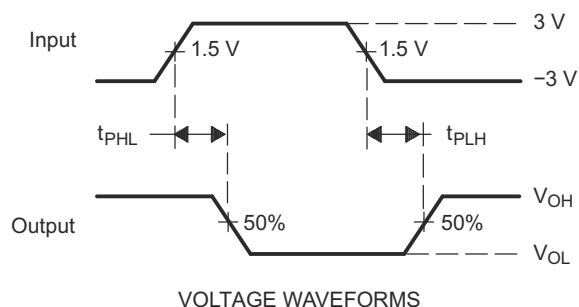
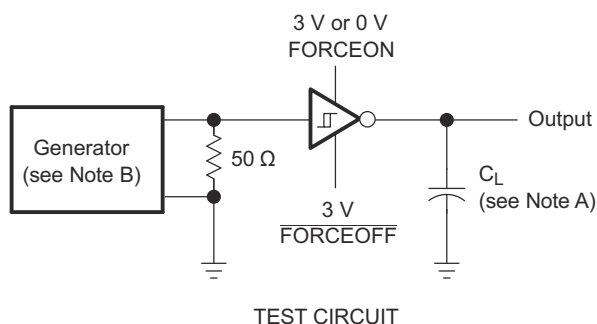


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A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 7-2. Driver Pulse Skew

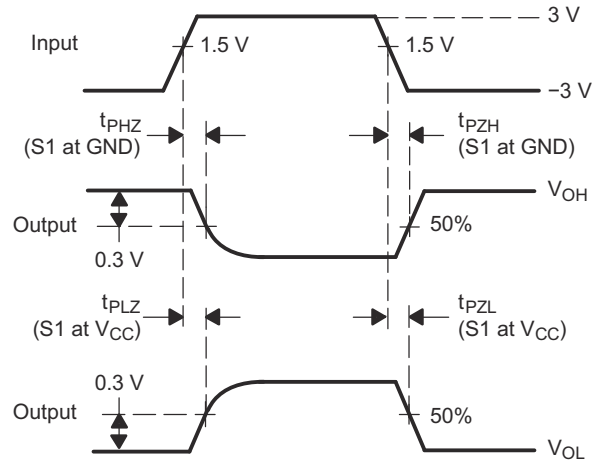
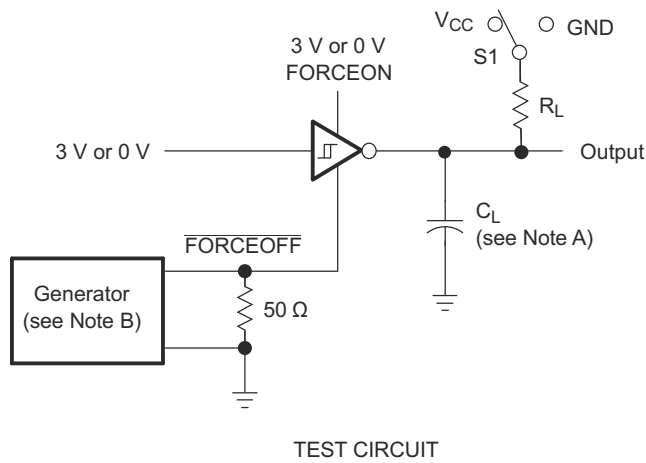


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A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

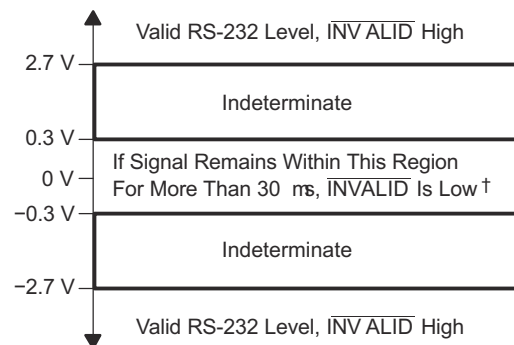
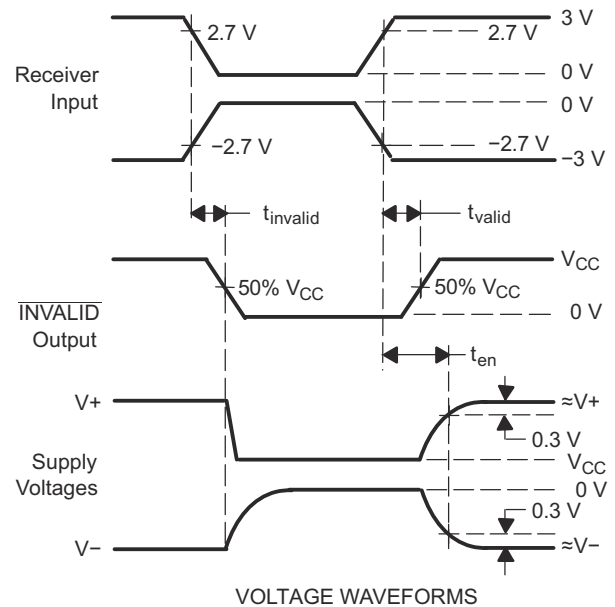
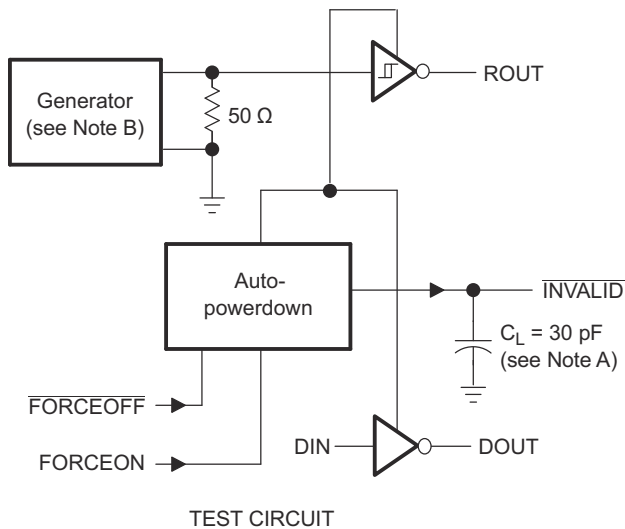
图 7-3. Receiver Propagation Delay Times



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- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\ \text{ns}$, $t_f \leq 10\ \text{ns}$.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

图 7-4. Receiver Enable And Disable Times



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A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

图 7-5. $\overline{\text{INVALID}}$ Propagation Delay Times And Supply Enabling Time

8 Detailed Description

8.1 Overview

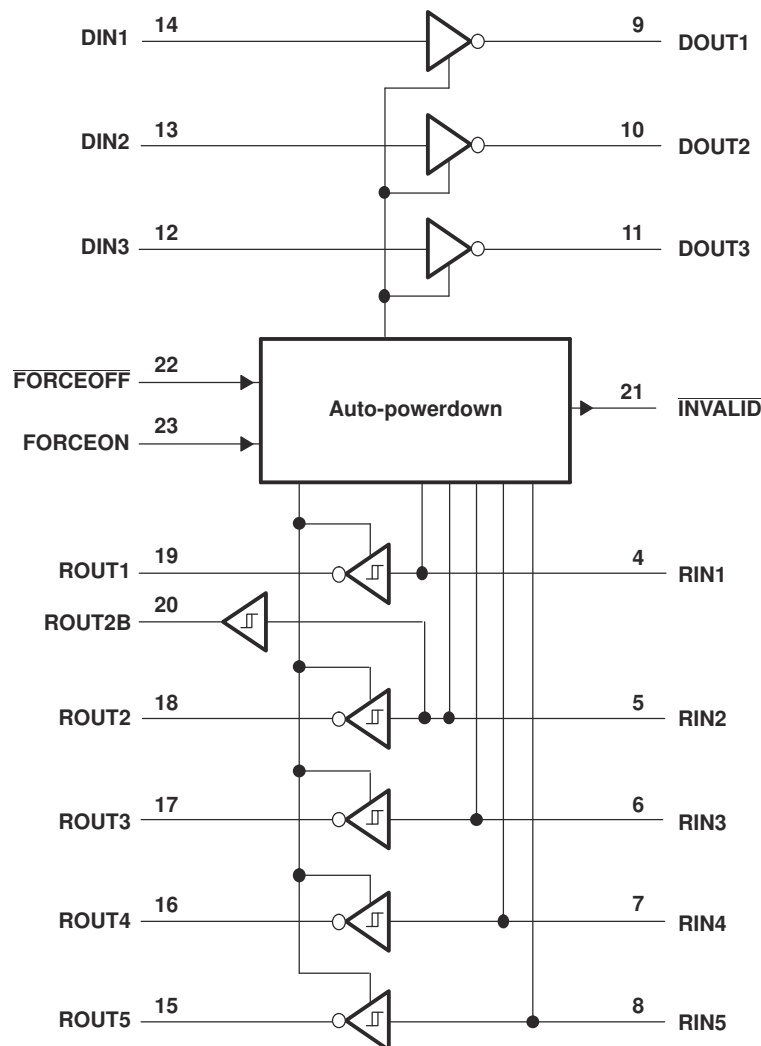
Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when **FORCEON** is low and **FORCEOFF** is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If **FORCEOFF** is set low, both drivers and receivers (except **ROUT2B**) are shut off, and the supply current is reduced to 1 μ A.

Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when **FORCEON** and **FORCEOFF** are high, and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The **INVALID** output is used to notify the user if an RS-232 signal is present at any receiver input. **INVALID** is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V or has been between -0.3 V and 0.3 V for less than 30 μ s. **INVALID** is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30 μ s. Refer to [Figure 7-5](#) for receiver input levels.

The TRS3243E is characterized for operation from 0°C to 70°C. The TRS3243EI is characterized for operation from -40°C to +85°C.

8.2 Functional Block Diagram



Logic Diagram (Positive Logic)

8.3 Device Functional Modes

表 8-1 through 表 8-3 show the device functional modes.

表 8-1. Each Driver

INPUTS ⁽¹⁾				OUTPUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
X	L	H	No	Z	Powered off by auto-powerdown feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 8-2. Each Receiver

INPUTS ⁽¹⁾			OUTPUT	RECEIVER STATUS
RIN	FORCEON	FORCEOFF	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation with auto-powerdown disabled/enabled
H	X	H	L	
Open	X	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

表 8-3. ROUT2B And Outputs $\overline{\text{INVALID}}$

INPUTS ⁽¹⁾				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	FORCEOFF	$\overline{\text{INVALID}}$	ROUT2B	
Yes	L	X	X	H	L	Always active
Yes	H	X	X	H	H	
Yes	Open	X	X	H	L	
No	Open	X	X	L	L	

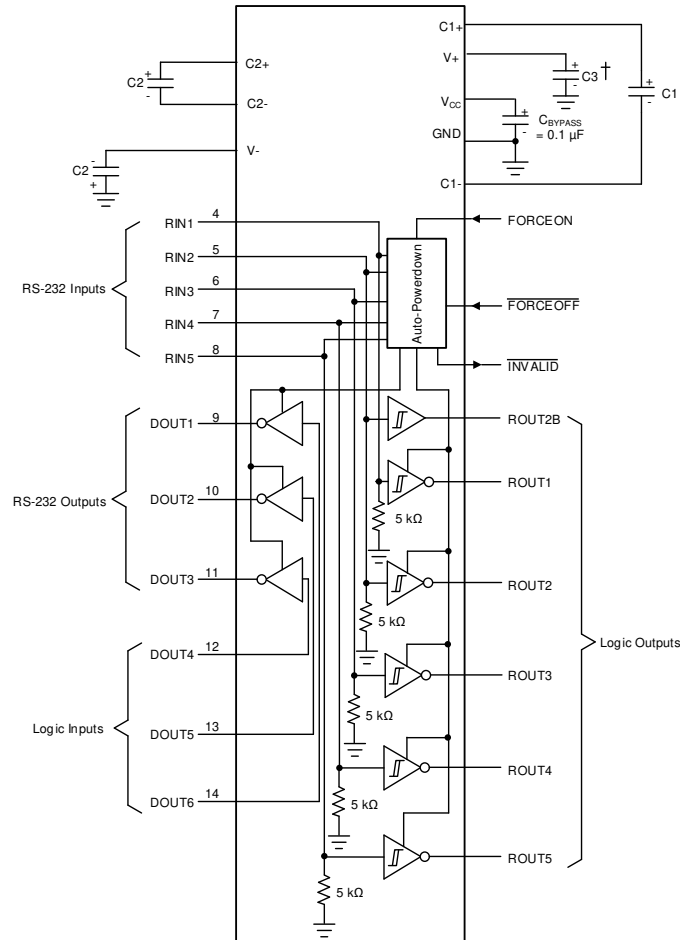
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Typical Application



- A. C3 can be connected to V_{CC} or GND.
- B. Resistor values shown are nominal.
- C. Nonpolarized ceramic capacitors are acceptable. If using polarized tantalum or electrolytic capacitors, connect them as shown.

图 9-1. Typical Operating Circuit and Capacitor Values

表 9-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	0.1 μ F	0.1 μ F
5 V $\pm$ 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

9.1.1 Detailed Design Procedure

9.1.1.1 ESD Protection

TI TRS3243E devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver

outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ± 15 -kV in all states: normal operation, shutdown, and powered down. The TRS3243E devices are designed to continue functioning properly after an ESD occurrence without any latchup.

The TRS3243E devices have three specified ESD limits on the driver outputs and receiver inputs, with respect to GND:

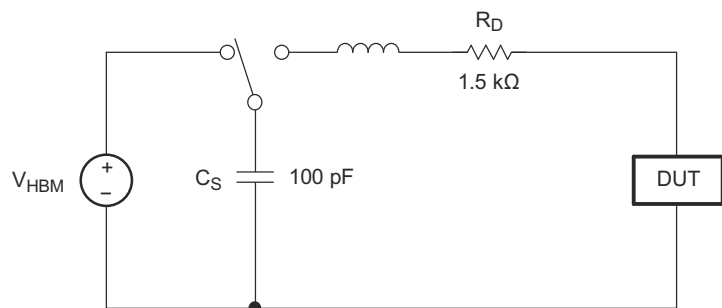
- ± 15 -kV Human-Body Model (HBM)
- ± 15 -kV IEC61000-4-2, Air-Gap Discharge (formerly IEC1000-4-2)
- ± 8 -kV IEC61000-4-2, Contact Discharge

9.1.1.2 ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

9.1.1.3 Human-Body Model (HBM)

The HBM of ESD testing is shown in 图 9-2, while 图 9-3 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-k Ω resistor.



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图 9-2. HBM ESD Test Circuit

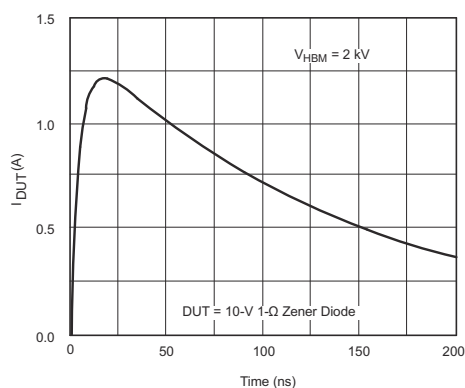


图 9-3. Typical HBM Current Waveform

9.1.1.4 IEC61000-4-2 (Formerly Known as IEC1000-4-2)

Unlike the HBM, MM, and CDM ESD tests that apply to component level integrated circuits, the IEC61000-4-2 is a system-level ESD testing and performance standard that pertains to the end equipment. The TRS3243E is designed to enable the manufacturer in meeting the highest level (Level 4) of IEC61000-4-2 ESD protection with no further need of external ESD protection circuitry. The more stringent IEC test standard has a higher peak current than the HBM, due to the lower series resistance in the IEC model.

图 9-4 shows the IEC61000-4-2 model, and 图 9-5 shows the current waveform for the corresponding ± 8 -kV contact-discharge (Level 4) test. This waveform is applied to a probe that has been connected to the DUT. On the other hand, the corresponding ± 15 -kV (Level 4) air-gap discharge test involves approaching the DUT with an already energized probe.

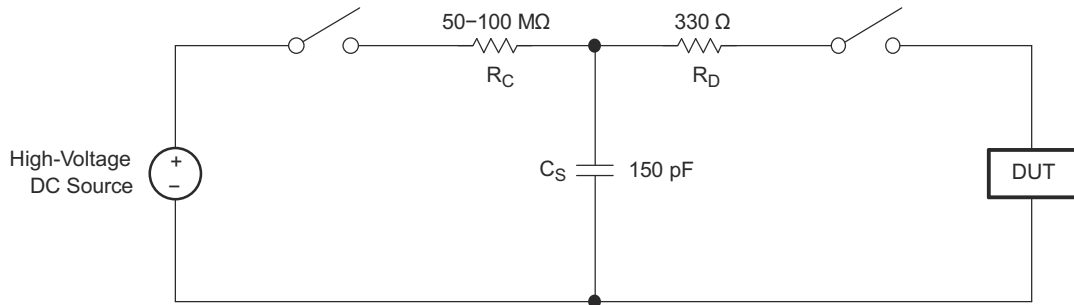


图 9-4. Simplified IEC61000-4-2 ESD Test Circuit

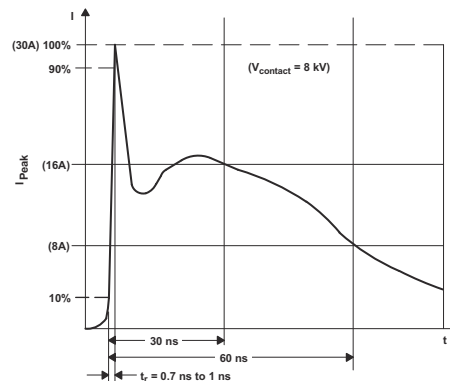


图 9-5. Typical Current Waveform Of IEC61000-4-2 ESD Generator

10 Device and Documentation Support

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

10.3 商标

IBM™ and PC/AT™ are trademarks of International Business Machines Corporation.

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS3243ECDBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC
TRS3243ECDBR.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EC
TRS3243ECDW	Obsolete	Production	SOIC (DW) 28	-	-	Call TI	Call TI	0 to 70	TRS3243EC
TRS3243ECDWR	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC
TRS3243ECDWR.A	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EC
TRS3243ECPW	Obsolete	Production	TSSOP (PW) 28	-	-	Call TI	Call TI	0 to 70	RS43EC
TRS3243ECPWR	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43EC
TRS3243ECPWR.A	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EC
TRS3243ECRHBR	Active	Production	VQFN (RHB) 32	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	RS43EC
TRS3243ECRHBR.A	Active	Production	VQFN (RHB) 32	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EC
TRS3243EIDBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIDBR.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIDBRG4.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIDW	Obsolete	Production	SOIC (DW) 28	-	-	Call TI	Call TI	-40 to 85	TRS3243EI
TRS3243EIDWR	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIDWR.A	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIPWR	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EI
TRS3243EIPWR.A	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EI
TRS3243EIRHBR	Active	Production	VQFN (RHB) 32	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EI
TRS3243EIRHBR.A	Active	Production	VQFN (RHB) 32	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EI
TRS3243EIRHBRG4	Active	Production	VQFN (RHB) 32	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EI

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

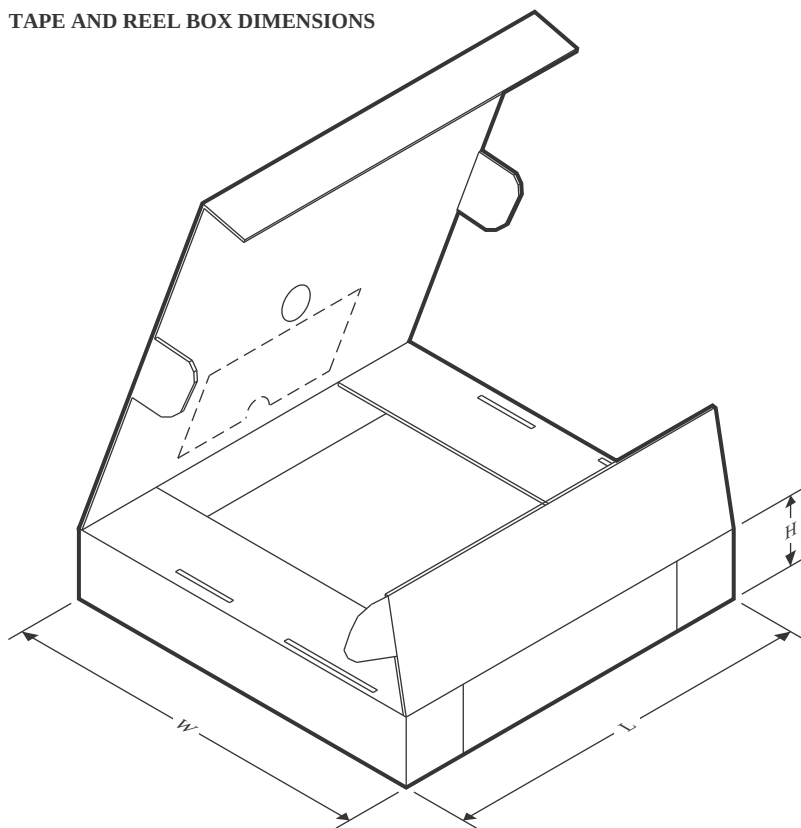
TAPE AND REEL INFORMATION



*All dimensions are nominal

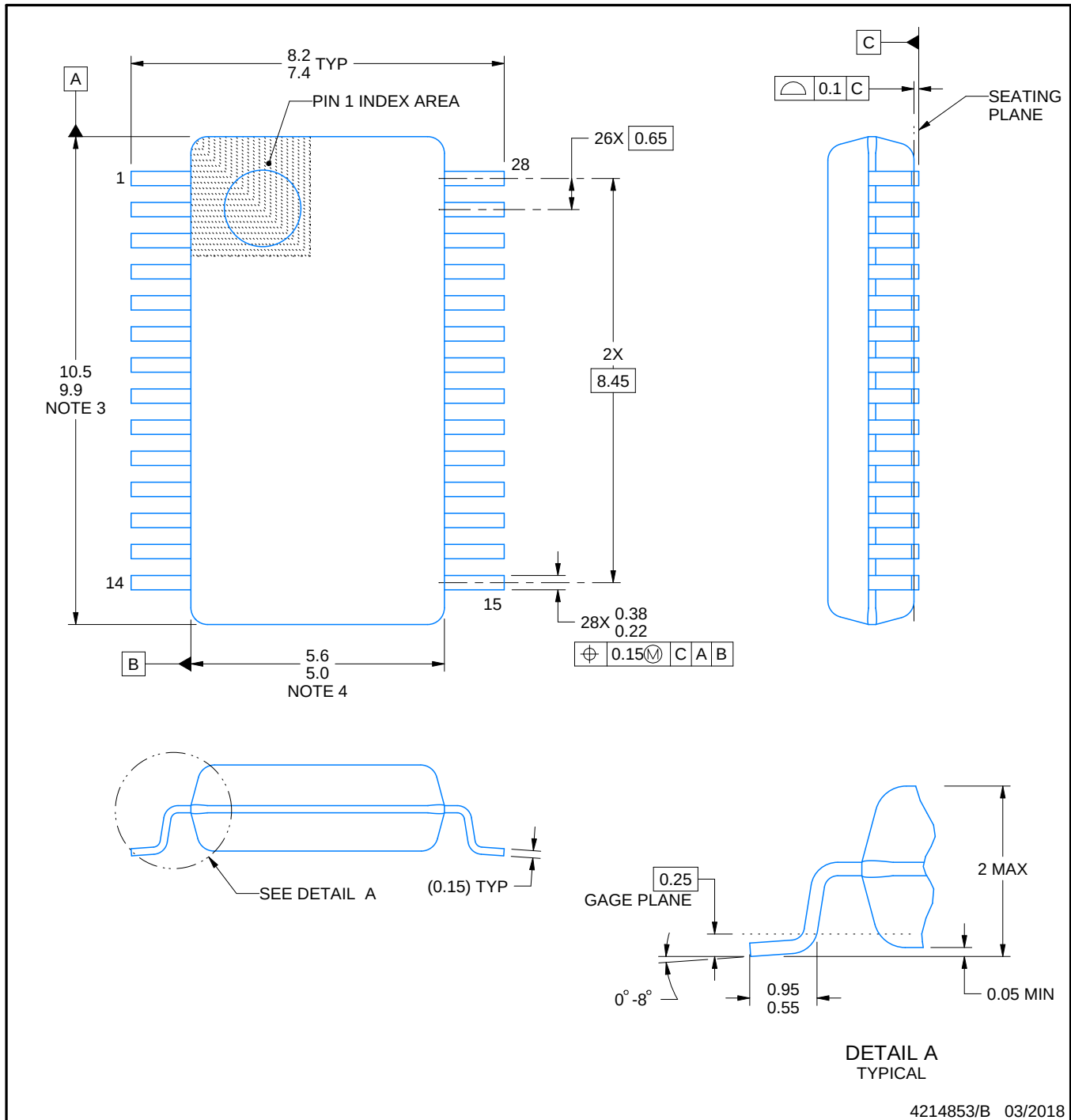
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3243ECDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243ECDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TRS3243ECDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243ECPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRS3243ECPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRS3243ECRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TRS3243EIDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243EIDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TRS3243EIDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243EIPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRS3243EIPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRS3243EIRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3243ECDDBR	SSOP	DB	28	2000	356.0	356.0	35.0
TRS3243ECDDBR	SSOP	DB	28	2000	356.0	356.0	35.0
TRS3243ECDWR	SOIC	DW	28	1000	350.0	350.0	66.0
TRS3243ECPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
TRS3243ECPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
TRS3243ECRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TRS3243EIDBR	SSOP	DB	28	2000	356.0	356.0	35.0
TRS3243EIDBR	SSOP	DB	28	2000	356.0	356.0	35.0
TRS3243EIDWR	SOIC	DW	28	1000	350.0	350.0	66.0
TRS3243EIPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
TRS3243EIPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
TRS3243EIRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0



4214853/B 03/2018

NOTES:

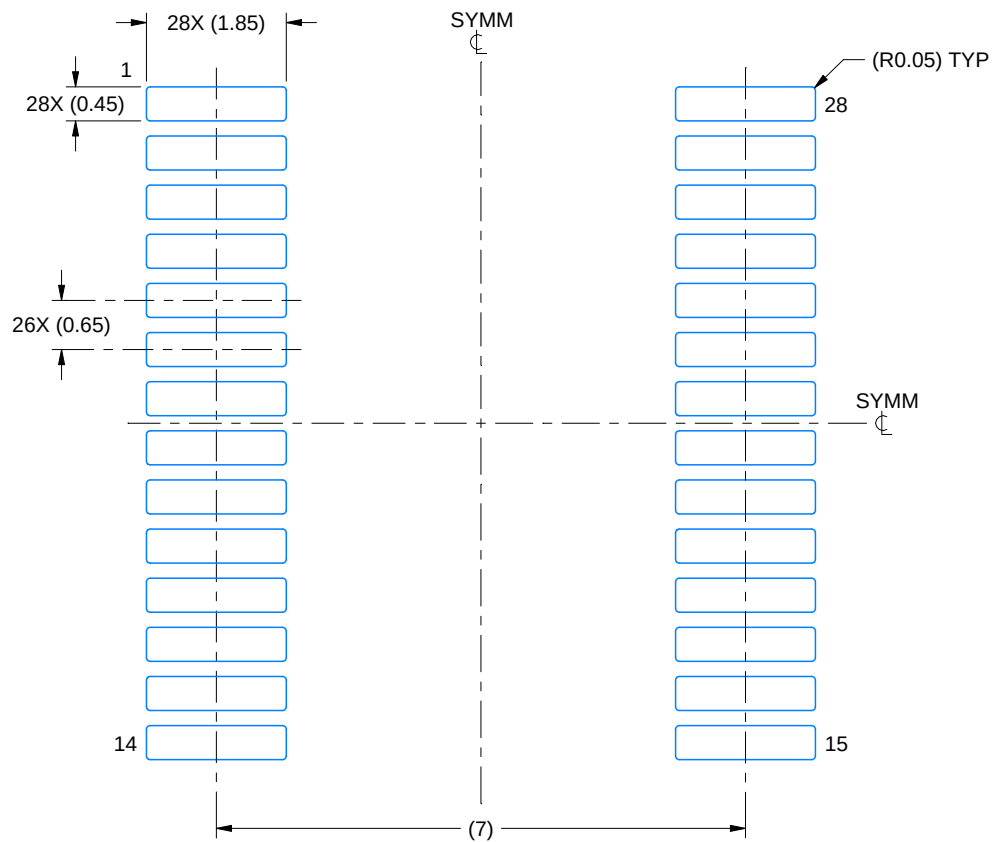
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

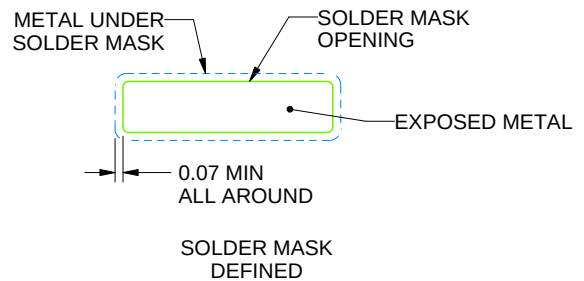
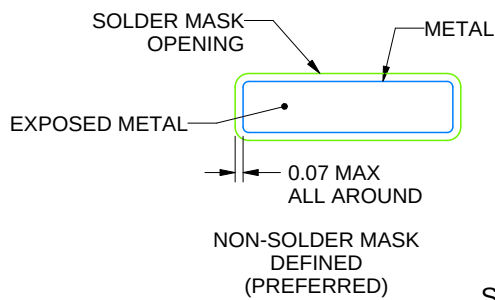
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214853/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

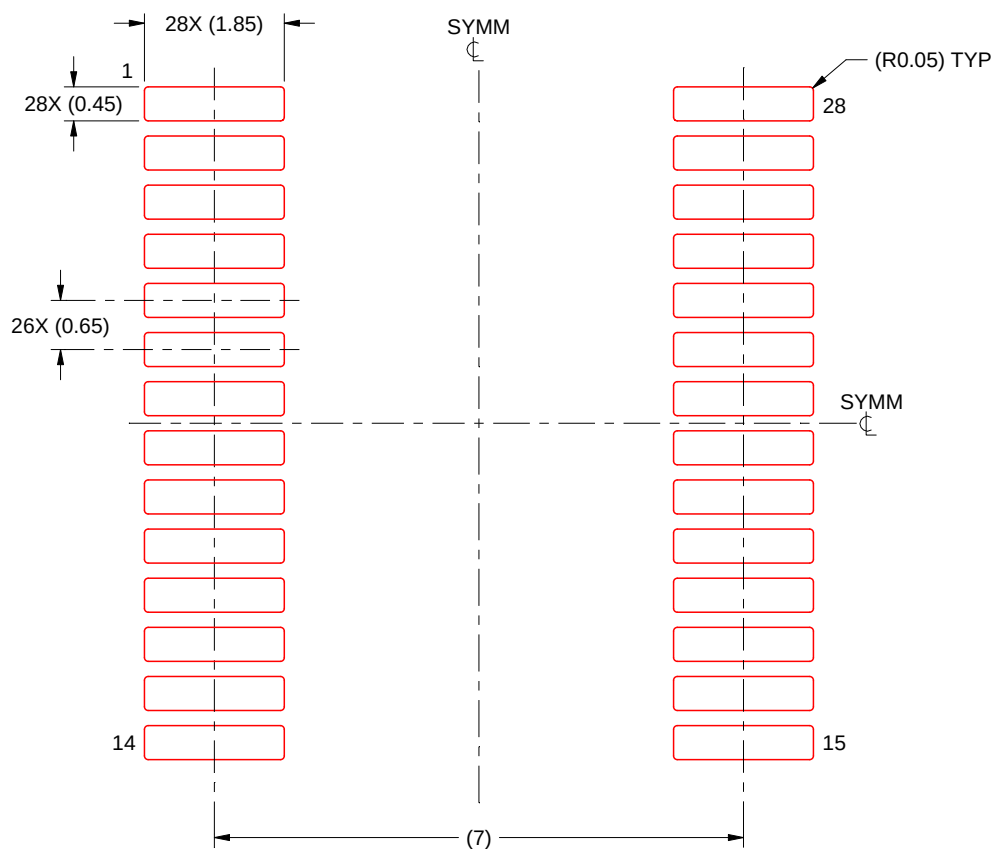
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

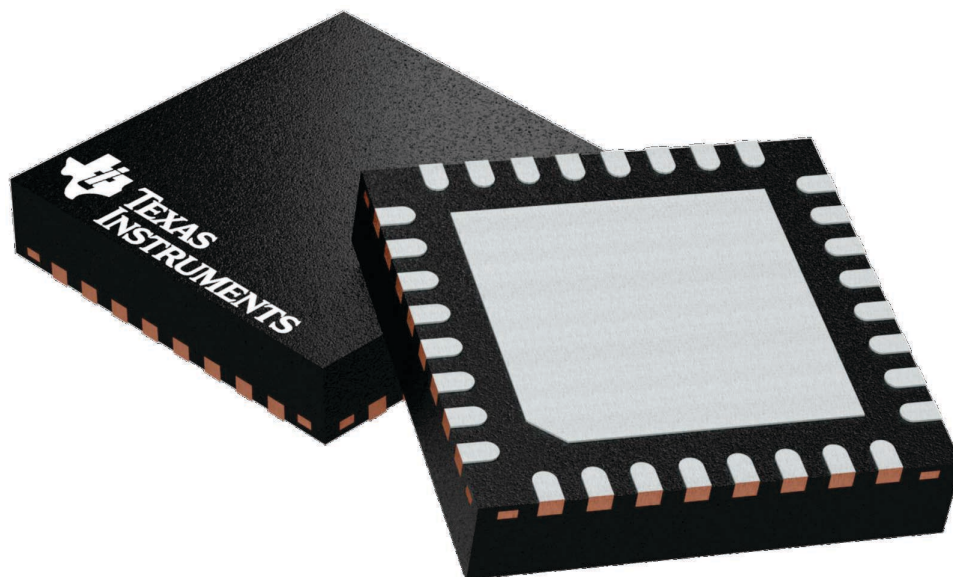
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

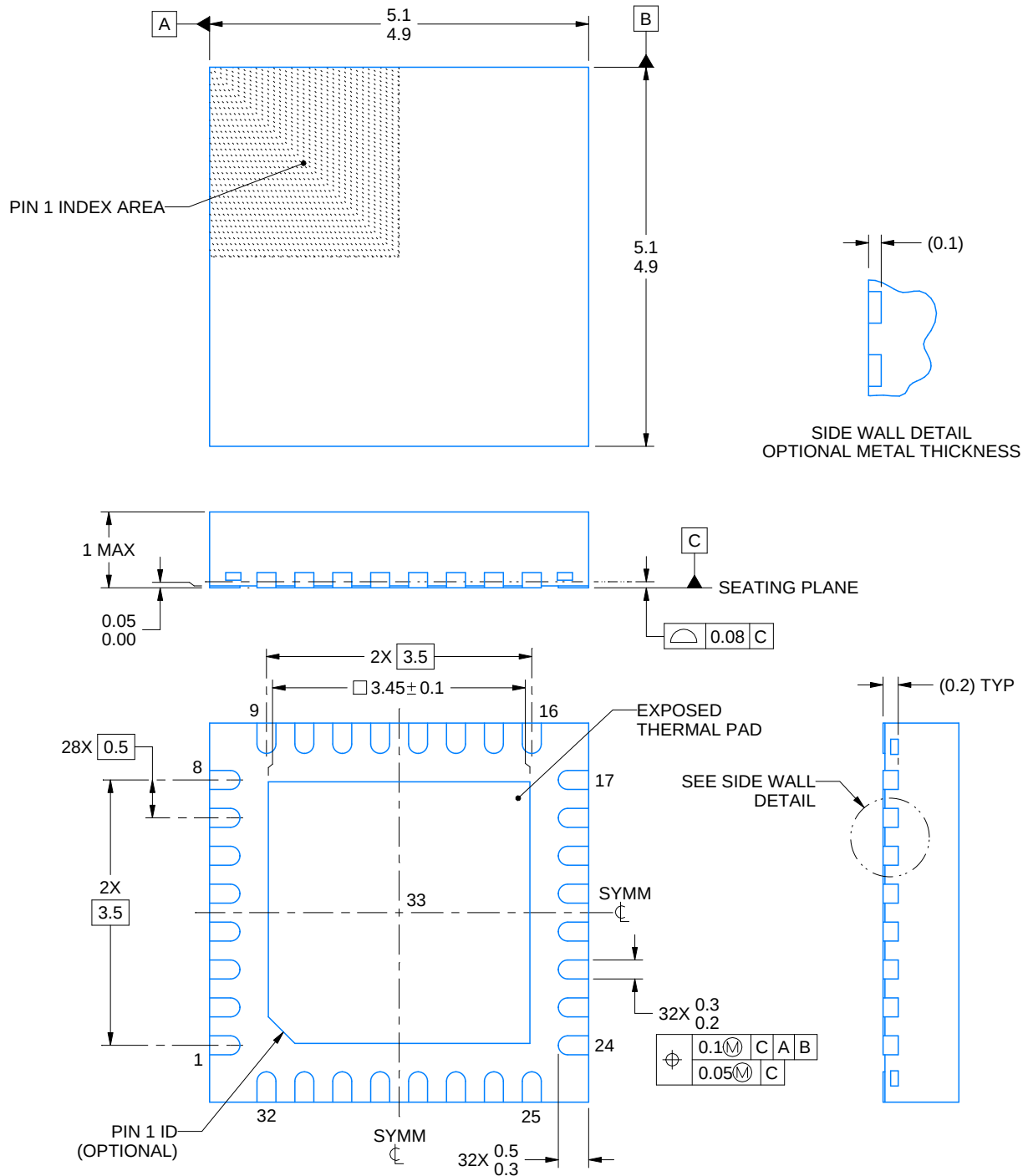
4224745/A

RHB0032E

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4223442/B 08/2019

NOTES:

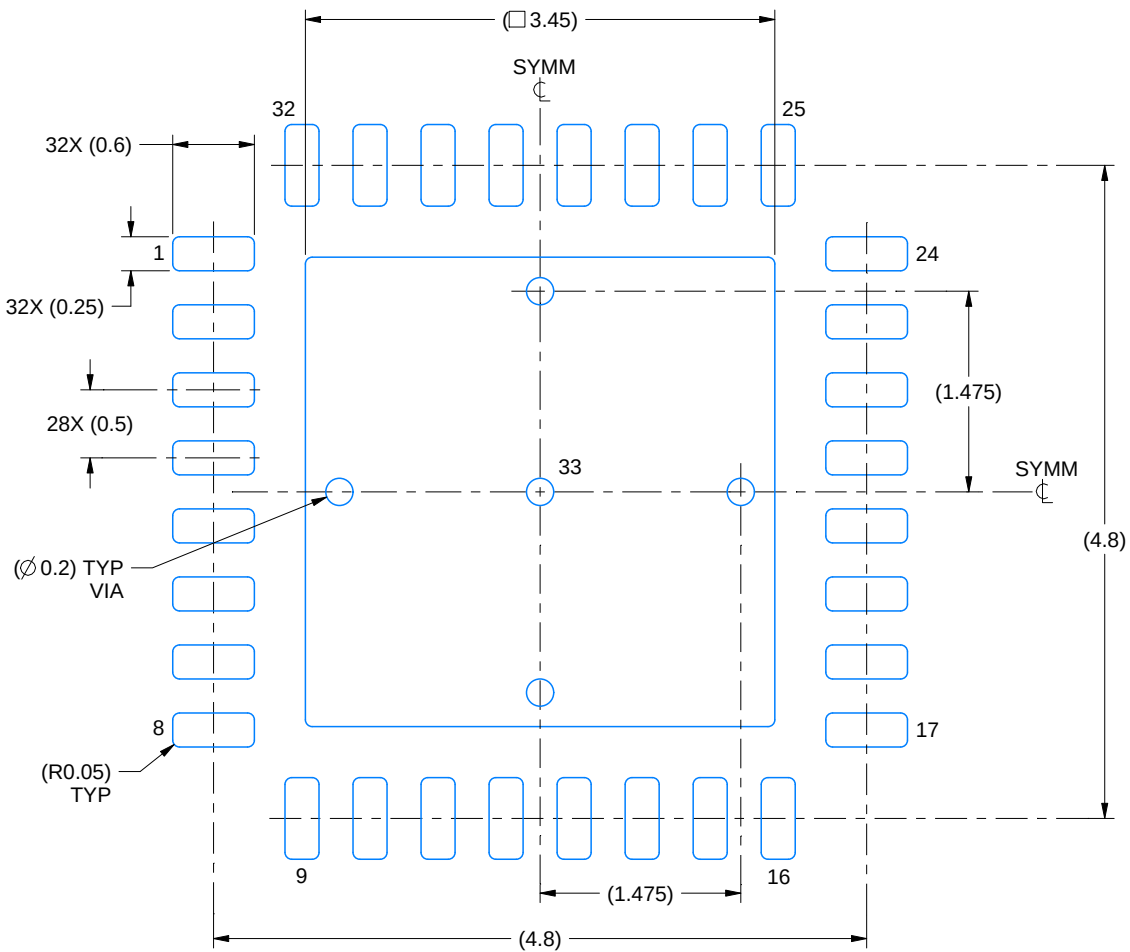
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

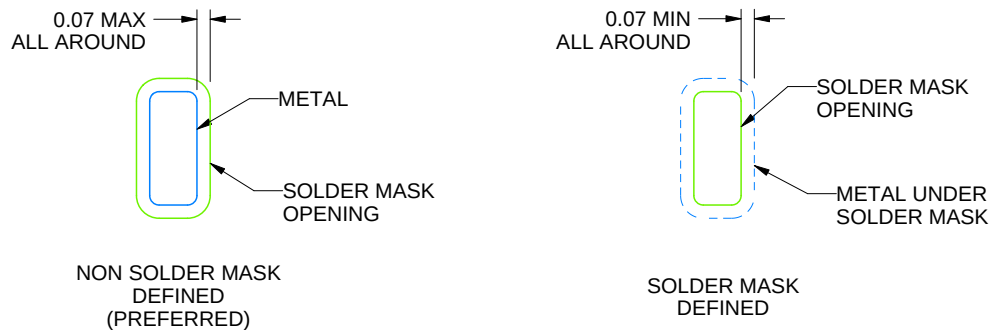
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

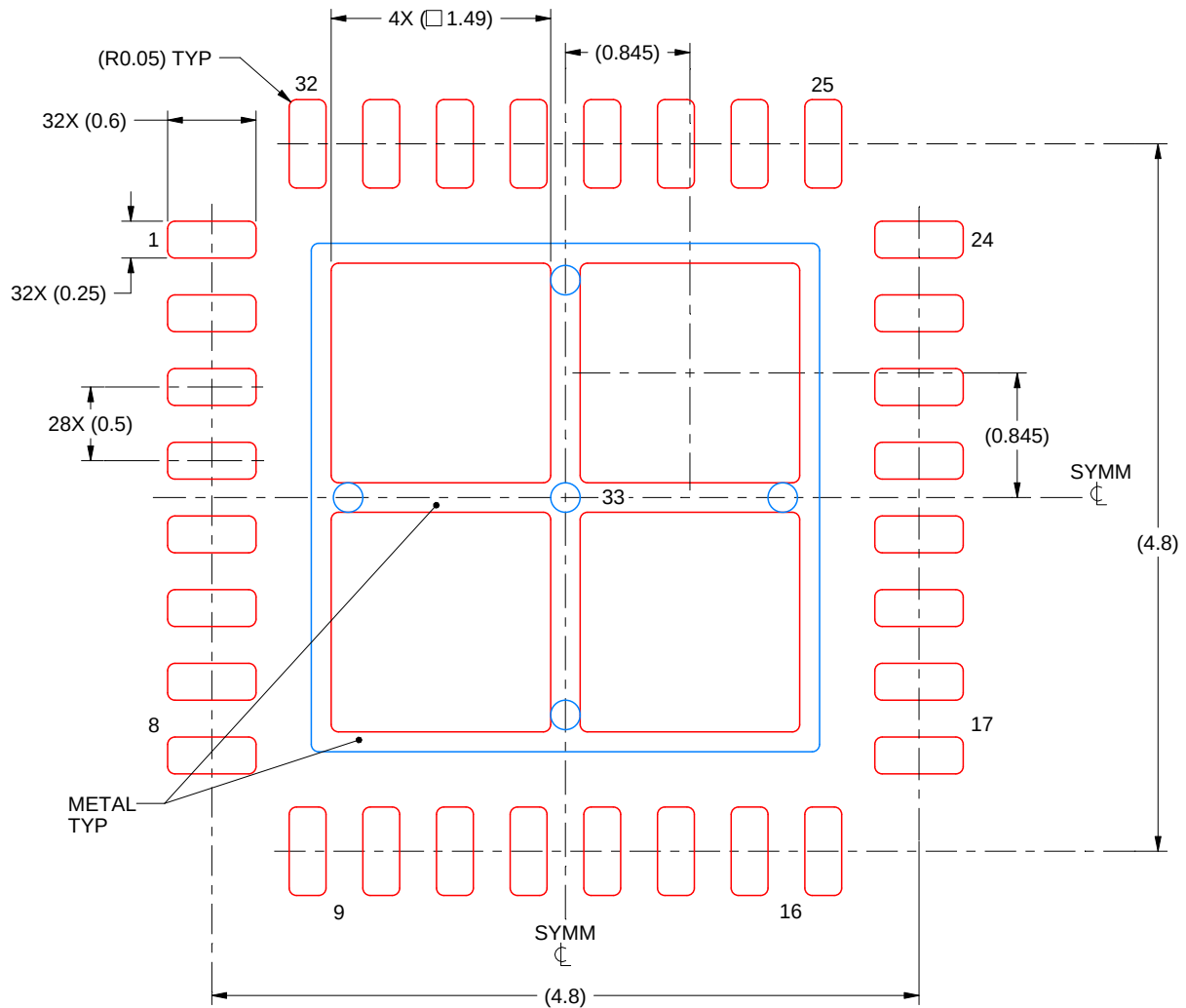
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
 75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

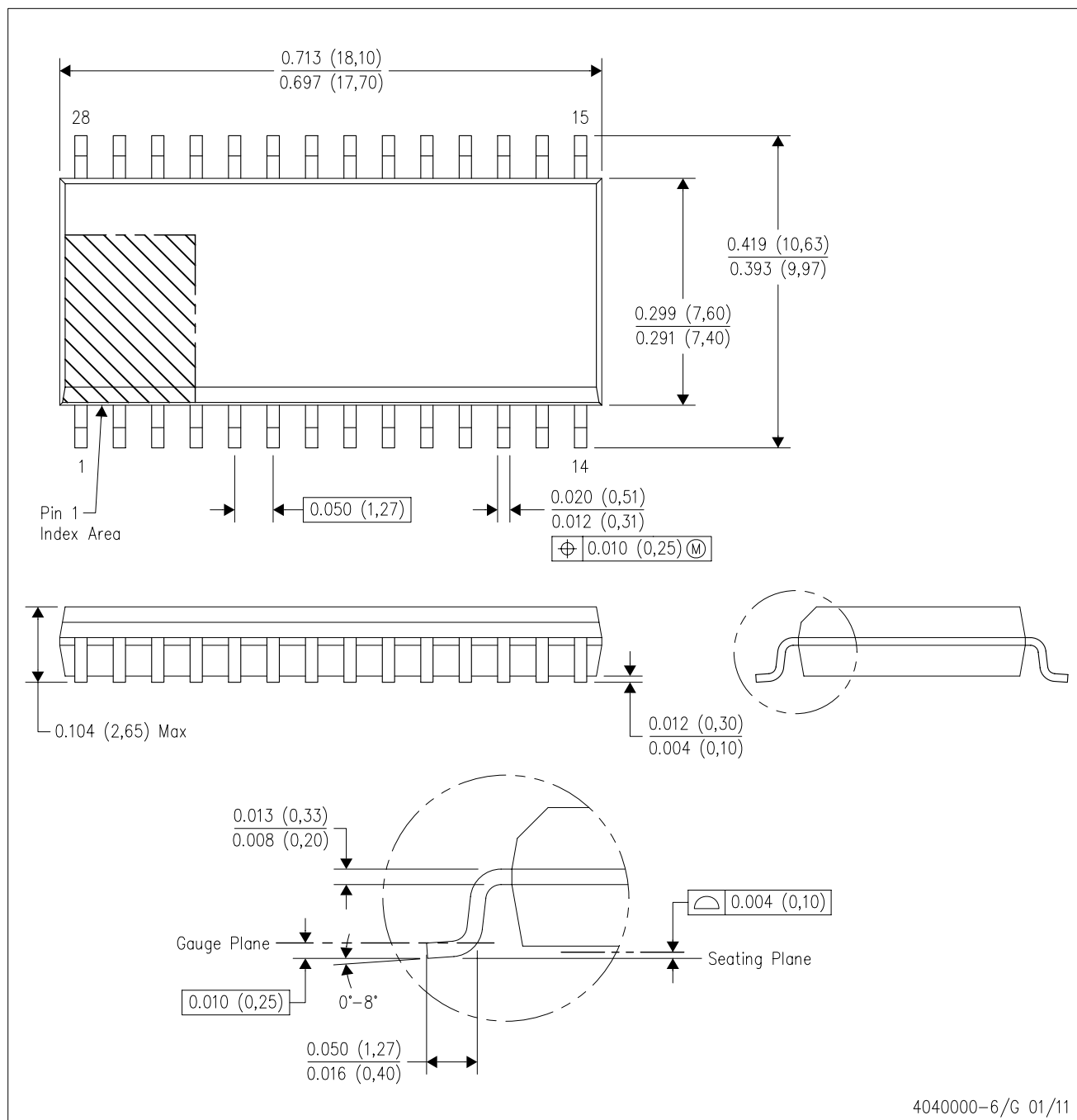
4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DW (R-PDSO-G28)

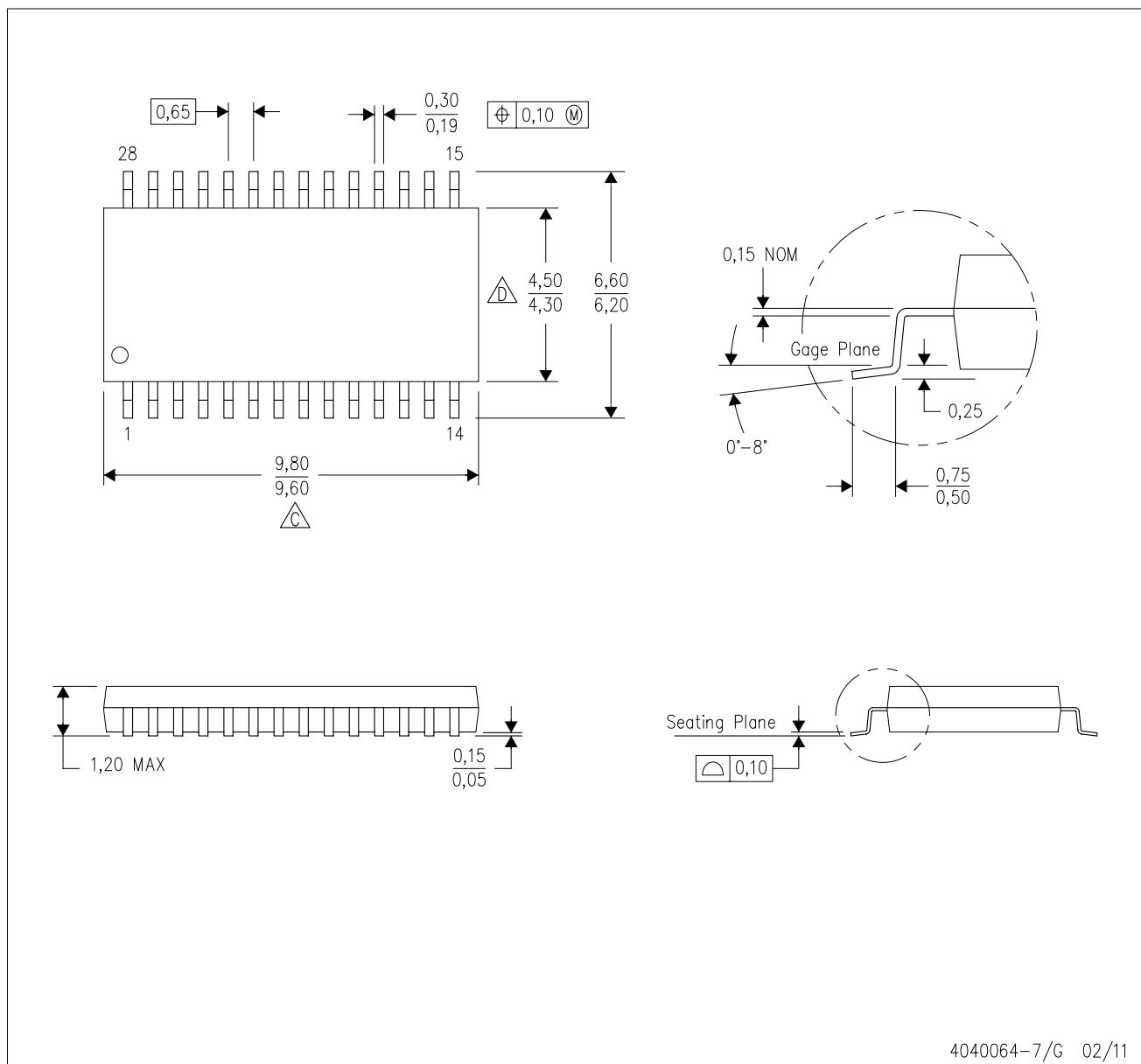
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AE.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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