

TRS3122E 1.8V 低功耗双路 RS-232 收发器

1 特性

- 扩展 V_{CC} 工作节点：1.8V、3.3V 或 5.0V
 - 独特的三倍频器电荷泵架构，与 3.3V 和 5V 电源保持兼容的同时实现低至 1.8V 的 V_{CC}
- 集成电平转换功能，连接低电压 MCU 时无需使用外部电源或附加电平转换器
- RIN 输入和 DOUT 输出端的增强型 ESD 保护
 - $\pm 15\text{kV}$ IEC 61000-4-2 气隙放电
 - $\pm 8\text{kV}$ IEC 61000-4-2 接触放电
 - $\pm 15\text{kV}$ 人体放电模式
- 数据速率指定为 1000Kbps
- 自动断电增强特性
- 关断电源电流低至 $0.5\mu\text{A}$
- 满足甚至超过 RS-232 接口的兼容性要求
- 对于 2.5V 单电源应用，可以考虑选用 TRS3318E 作为优化解决方案

2 应用

- 远程射频单元 (RRU)
- 基带装置 (BBU)
- 电子销售点 (EPOS)
- 诊断和数据传输
- 电池供电类设备

3 说明

TRS3122E 是一款具有双驱动器、双接收器的 RS-232 接口器件，配有分离电源引脚以支持混合电压运行。使用 IEC 61000-4-2 气隙放电方法，IEC 61000-4-2 接触放电方法和人体放电模型分别保护全部 RS-232 输入和输出不受 $\pm 15\text{kV}$ 、 $\pm 8\text{kV}$ 和 $\pm 15\text{kV}$ 电压的影响。

电荷泵需要使用 5 个 $0.1\mu\text{F}$ 小电容，以便器件能够在低至 1.8V 的电源供电下运行。TRS3122E 能够以高达 1000kbps 的数据速率运行，同时保持与 RS-232 相兼容的输出水平。

TRS3122E 具有一个独特的 V_L 引脚，可实现在混合逻辑电压系统内运行。可通过 V_L 引脚设定驱动器输入 (DIN) 和接收器输出 (ROUT) 逻辑电平。当连接低电压微控制器或通用异步收发器 (UART) 时，不再需要使用附加电压电平转换器。

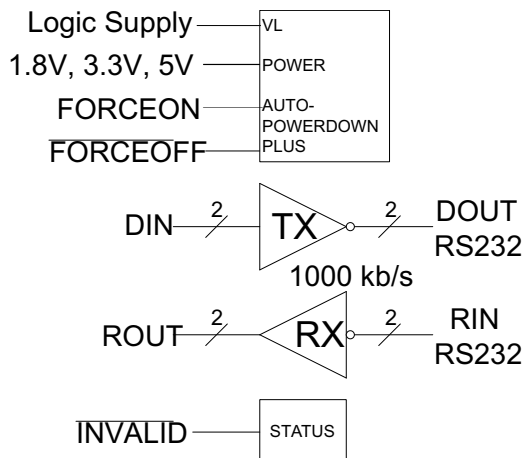
该器件具备“自动省电增强”(Auto Powerdown Plus) 功能，如果连续 30 秒未收发任何数据，则自动进入低功耗模式。该功能使得该器件备受电池供电类应用或其他功率敏感型应用的青睐。

器件信息⁽¹⁾

器件型号	封装 (引脚)	封装尺寸 (标称值)
TRS3122ERGER	RGE (24)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

功能图



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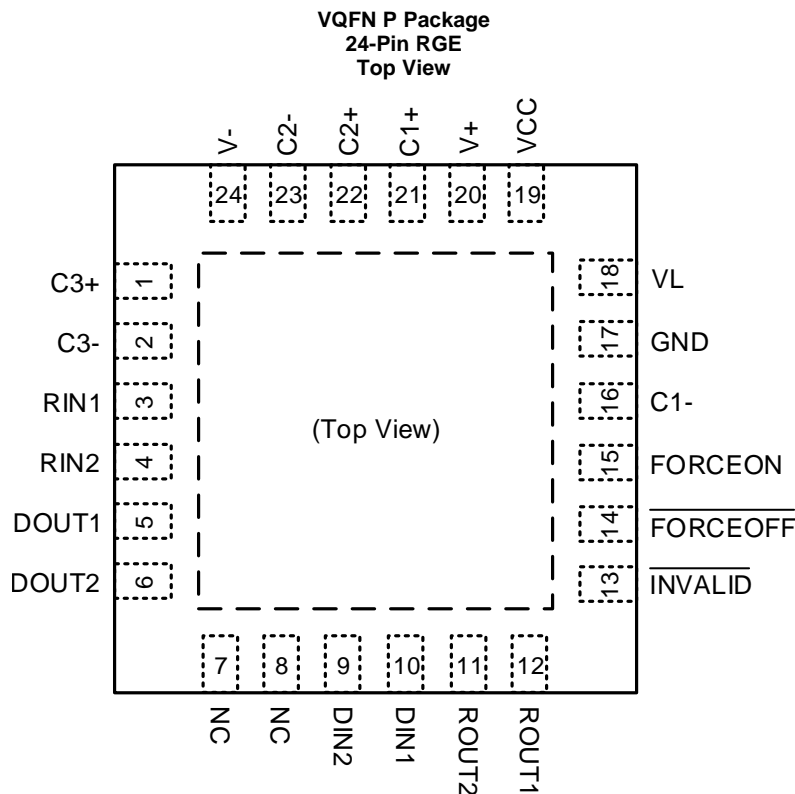
4 修订历史记录

Changes from Revision B (May 2016) to Revision C	Page
• 已按优先级对特性部分各要点进行了重新排序 1	1
• 已删除 首页应用部分的数据电缆，为首页图片留出空间 1	1
• 已更改 已更正描述文本中的 已交换的 ESD 级别 1	1

Changes from Revision A (May 2016) to Revision B	Page
• Updated ESD ratings values to reflect current device specifications 4	4
• 已添加 all Typical Characteristic graphs and schematics to the <i>Typical Characteristics</i> section 8	8
• 已添加 Application Curve image to <i>Application Curves</i> section 18	18

Changes from Original (June 2014) to Revision A	Page
• Added Pin Functions table. 3	3

5 Pin Configuration and Functions



Pin Functions

Pin		I/O	DESCRIPTION
NAME	NO.		
C1+, C2+	21, 22	-	Positive terminals of voltage-doubler charge-pump capacitors (required)
C3+	1	-	Positive terminal of voltage-tripler charge-pump capacitor (Not needed for VCC 3V to 5.5V)
C1-, C2-	16, 23	-	Negative terminals of voltage-doubler charge-pump capacitors (required)
C3-	2	-	Negative terminal of voltage-tripler charge-pump capacitor (Not needed for VCC 3V to 5.5V)
V+	20	-	Positive charge pump storage capacitor (required)
V-	24	-	Negative charge pump storage capacitor (required)
GND	17	-	Ground
V _{CC}	19	-	1.8-V or 3-V to 5-V supply voltage
V _L	18	-	Logic-level supply. All CMOS inputs (DIN) and outputs (ROUT) are referenced to this supply.
$\overline{\text{FORCEOFF}}$	14	I	Auto Powerdown Control input (Refer to Truth Table)
FORCEON	15	I	Auto Powerdown Control input (Refer to Truth Table)
$\overline{\text{INVALID}}$	13	O	Invalid Output Pin
DIN1, DIN2	10,9	I	Driver inputs
DOUT1, DOUT2	5, 6	O	RS-232 driver outputs
RIN1, RIN2	3, 4	I	RS-232 receiver inputs
ROUT1, ROUT2	12, 11	O	Receiver outputs; swing between 0 and V _L
NC	7, 8	I	Factory pins, can be unconnected or connected to GND

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CC}	Charge pump power supply	-0.3	6	V	
V _L	Logic power supply	-0.3	6	V	
V+	Positive storage capacitor voltage	-0.3	7	V	
V-	Negative storage capacitor voltage	0.3	-7	V	
V+ + V- ⁽²⁾			13	V	
V _I	Input voltage	FORCEOFF , FORCEON		V	
		DIN	-0.3		V _L + 0.3
		RIN (0Ω series resistance)			±20
		RIN (≥250Ω series resistance)			±25
V _O	Output voltage	DOUT		V	
		ROUT			±13.2
T _J	Junction temperature		150	°C	
T _{stg}	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- (2) V+ and V- can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.

6.2 ESD Ratings

			VALUE	UNIT		
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	All pins except RS-232 bus	±2000	V	
			RS-232 bus pins	±15000		
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	All pins	±500		
			IEC 61000-4-2 Air-Gap Discharge	RS-232 bus pins		±15000
						IEC 61000-4-2 Contact Discharge

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

				MIN	TYP	MAX	UNIT
V _{CC}	Charge pump power supply	Tripler Mode		1.65	1.8	2	V
		Doubler Mode		3	3.3	3.6	
V _L	Logic power supply			1.65		V _{CC}	V
R _{IN}	RS-232 Receiver interface			-15		15	V
D _{OUT}	RS-232 Transmitter interface			-12		12	V
V _{IL}	GPIO Input logic threshold low	D _{IN} , $\overline{\text{FORCEOFF}}$, FORCEON	V _L = 5.0 V	0		1.7	V
			V _L = 3.3V	0		1.1	
			V _L = 1.8 V	0		0.6	
V _{IH}	GPIO Input logic threshold high	D _{IN} , $\overline{\text{FORCEOFF}}$, FORCEON	V _L = 5.0V	3.3		V _L	V
			V _L = 3.3V	2.2		V _L	
			V _L = 1.8V	1.2		V _L	
V _{OZ}	ROUT disabled	FORCEOFF = 0V		0		V _L	V
Operating temperature				-40		85	°C

6.4 Thermal Characteristics

THERMAL METRIC		TRS3122E		UNIT
		RGE		
R _{θJA}	Junction-to-ambient thermal resistance	34.2		°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	27.2		
R _{θJB}	Junction-to-board thermal resistance	11.4		
ψ _{JT}	Junction-to-top characterization parameter	0.4		
ψ _{JB}	Junction-to-board characterization parameter	11.4		
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	3.6		

6.5 Power and Status Electrical Characteristics

V_{CC} = V_L = (1.65 V to 2.0 V) & (3.0V to 5.5V), T_A = -40°C to 85°C (unless otherwise noted). Typical data is T_A = 25°C, V_{CC} = V_L = 3.3V unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _{CC} (Static)		D _{IN1} = GND or V _L ; D _{IN2} = GND or V _L ; $\overline{\text{FORCEOFF}}$ = V _L FORCEON = V _L	No load	V _{CC} = 1.65V to 2.0V	1.0	1.9	mA
				V _{CC} = 3.0V to 3.6V	0.7	1.4	
				V _{CC} = 4.5V to 5.5V	0.8	1.9	
I _{CC} (off)		$\overline{\text{FORCEOFF}}$ = GND		0.4		10	μA
V _{IT+}	R _{IN} positive voltage threshold for INVALID output change	R _{IN1} = R _{IN2}		0.3		2.4	V
V _{IT-}	R _{IN} negative voltage threshold for INVALID output change			-2.4		-0.3	
V _{OH}	INVALID high-level output voltage	I _{OH} = -1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V _L		V _L -0.4	V _L -0.08	V _L	V
V _{OL}	INVALID low-level output voltage	I _{OL} = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V _L		0	0.06	0.4	V

6.6 Driver Electrical Characteristics

$V_{CC} = V_L = (1.65\text{ V to }2.0\text{ V}) \& (3.0\text{ V to }5.5\text{ V})$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted). Typical data is $T_A = 25^\circ\text{C}$, $V_{CC} = V_L = 3.3\text{ V}$ unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT} Output voltage swing	All driver outputs loaded with 3 k Ω to ground C3 = 100 nF, $V_{CC} = 1.8\text{ V}$	± 4.25	± 4.7		V
	All driver outputs loaded with 3 k Ω to ground C3 = 0 F, $V_{CC} = 3.3\text{ V}$ or 5 V	± 5	± 5.4		
r_O Output resistance	($V_{CC} = V_+ = V_- = 0$); Driver output = $\pm 2\text{ V}$	300	10M		Ω
I_{OS} Output short-circuit current	$V_{DOUT} = 0$			± 60	mA
I_{OZ} Output leakage current	$V_{DOUT} = \pm 12\text{ V}$, $\overline{\text{FORCEOFF}} = \text{GND}$	0		± 25	μA
Driver input hysteresis			0.5	1	V
Input leakage current	DIN = GND to V_L ; $\overline{\text{FORCEOFF}} = \text{GND to } V_L$; FORCEON = GND to V_L		0	± 5	μA

6.7 Receiver Electrical Characteristics

$V_{CC} = V_L = (1.65\text{ V to }2.0\text{ V}) \& (3.0\text{ V to }5.5\text{ V})$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted). Typical data is $T_A = 25^\circ\text{C}$, $V_{CC} = V_L = 3.3\text{ V}$ unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I_{off} Output leakage current	ROUT, receivers disabled		± 0.01	± 10	μA	
V_{OL} Output voltage low	$I_{OUT} = 2.0\text{ mA}$		0.04	0.3	V	
V_{OH} Output voltage high	$I_{OUT} = -2.0\text{ mA}$	$V_L - 0.3$	$V_L - 0.04$		V	
V_{IT-} Input threshold low	$T_A = 25^\circ\text{C}$	$V_L = 5\text{ V}$	0.8	1.5	V	
		$V_L = 3.3\text{ V}$	0.7	1.1		
		$V_L = 1.8\text{ V}$	0.6	0.7		
V_{IT+} Input threshold high	$T_A = 25^\circ\text{C}$	$V_L = 5\text{ V}$		2.0	2.4	V
		$V_L = 3.3\text{ V}$		1.5	2.4	
		$V_L = 1.8\text{ V}$		0.9	1.4	
V_{hys} Input hysteresis	$T_A = 25^\circ\text{C}$	$V_L = 5\text{ V}$		0.45	V	
		$V_L = 3.3\text{ V}$		0.35		
		$V_L = 1.8\text{ V}$		0.26		
Input resistance	$T_A = -40\text{ to }85^\circ\text{C}$	3	5	7	k Ω	

6.8 Driver Switching Characteristics

$V_{CC} = V_L = (1.65\text{ V to }2.0\text{ V}) \& (3.0\text{ V to }5.5\text{ V})$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted). Typical data is $T_A = 25^\circ\text{C}$, $V_{CC} = V_L = 3.3\text{ V}$ unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum data rate	$R_L = 3\text{ k}\Omega$, $C_L = 500\text{ pF}$ (one driver)	1000			kbps
	$R_L = 3\text{ k}\Omega$, $C_L = 1000\text{ pF}$ (one driver)	500			
Time-to-exit powerdown	$ V_{DOUT} > 3.7\text{ V}$		30	150	μs
$ t_{PHL} - t_{PLH} $ Driver skew ⁽¹⁾	$R_L = 3\text{ k}\Omega$	0	50	100	ns
Transition-region slew rate	$R_L = 3\text{ k}\Omega$ to 7 k Ω , $T_A = 25^\circ\text{C}$ Measured from 3 V to -3 V or -3 V to 3 V	$V_{CC} = 1.8\text{ V}$, $C_L = 200\text{ pF}$		33	V/ μs
		$V_{CC} = 1.8\text{ V}$, $C_L = 1000\text{ pF}$		25	
		$V_{CC} = 3.3\text{ V}$, $C_L = 200\text{ pF}$		38	
		$V_{CC} = 3.3\text{ V}$, $C_L = 1000\text{ pF}$		28	
		$V_{CC} = 5\text{ V}$, $C_L = 200\text{ pF}$		41	
		$V_{CC} = 5\text{ V}$, $C_L = 1000\text{ pF}$		30	

(1) Driver skew is measured at the driver zero crosspoint.

6.9 Receiver Switching Characteristics

$V_{CC} = V_L = (1.65\text{ V to }2.0\text{ V}) \& (3.0\text{V to }5.5\text{V})$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted). Typical data is $T_A = 25^\circ\text{C}$, $V_{CC} = V_L = 3.3\text{V}$ unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Receiver propagation delay, high to low	Receiver input to receiver output $C_L = 150\text{ pF}$		0.15	0.4	μs
t_{PLH}	Receiver propagation delay, low to high			0.15	0.4	
$t_{PHL} - t_{PLH}$	Receiver skew			50	300	ns
t_{en}	Receiver output enable time	From $\overline{\text{FORCEOFF}}$ to $R_{OUT} = V_L/2$ $C_L = 150\text{ pF}$, $R_L = 3\text{ k}\Omega$		200	400	ns
t_{dis}	Receiver output disable time			200	400	ns

6.10 Power and Status Switching Characteristics

$V_{CC} = V_L = (1.65\text{ V to }2.0\text{ V}) \& (3.0\text{V to }5.5\text{V})$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted). Typical data is $T_A = 25^\circ\text{C}$, $V_{CC} = V_L = 3.3\text{V}$ unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		1		μs
$t_{invalid}$	Propagation delay time, high- to low-level output		30		μs
t_{dis}	Receiver or driver edge to auto-powerdown plus	15	30	60	s

6.11 Typical Characteristics

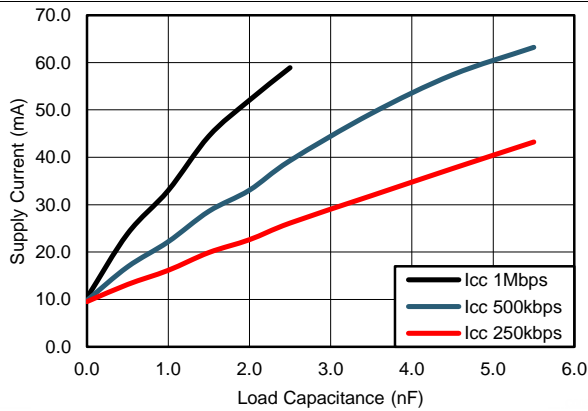


图 1. Supply Current vs. Load Capacitance
 $V_{CC} = 3.3\text{ V}$, $V_L = 1.8\text{ V}$, $R_{LOAD} = 3\text{ k}\Omega$, $CH2 = 32\text{ kbps}$

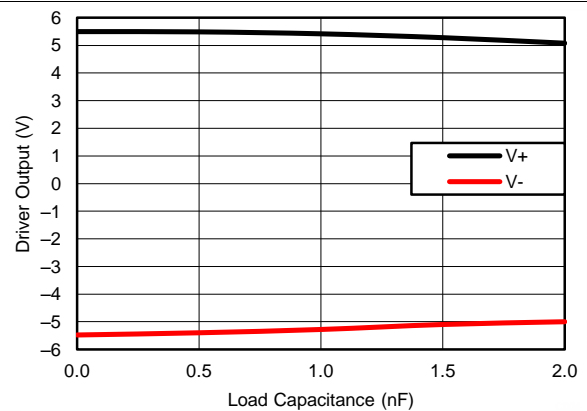


图 2. Driver Output vs. Load Capacitance, $V_{CC} = 3.3\text{ V}$
 $V_L = 1.8\text{ V}$, $R_{LOAD} = 3\text{ k}\Omega$, $CH1 = 1\text{ Mbps}$, $CH2 = 32\text{ kbps}$

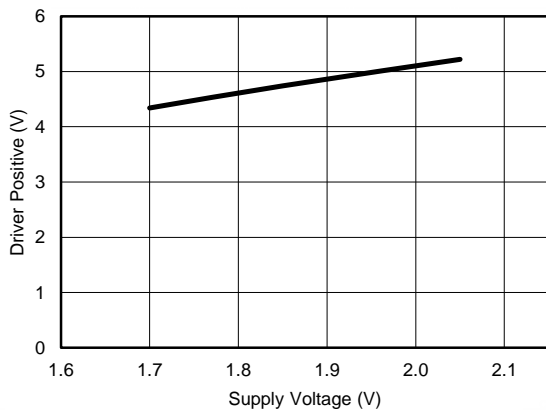


图 3. Driver Positive vs. Supply Voltage (Tripler Mode)
 1 Mbps , $R_{LOAD} = 3\text{ k}\Omega$, $C_{LOAD} = 560\text{ pF}$

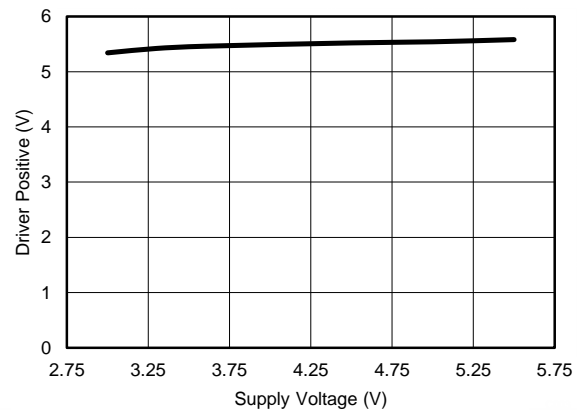


图 4. Driver Positive vs. Supply Voltage (Doubler Mode)
 1 Mbps , $R_{LOAD} = 3\text{ k}\Omega$, $C_{LOAD} = 560\text{ pF}$

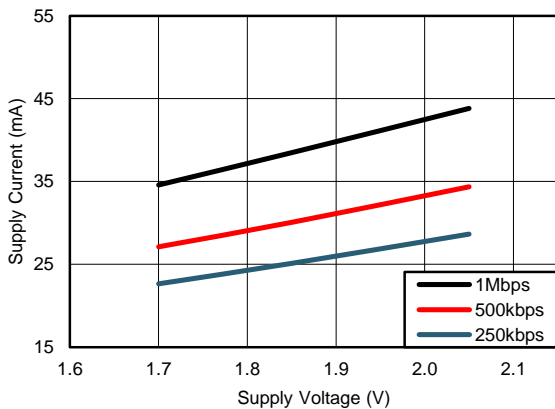


图 5. Supply Current vs. Supply Voltage (Tripler Mode)
 $V_L = 1.8\text{ V}$, $R_{LOAD} = 3\text{ k}\Omega$, $C_{LOAD} = 1\text{ nF}$, $CH2 = 32\text{ kbps}$

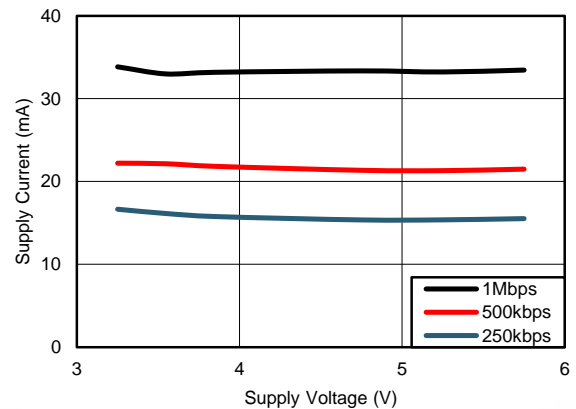
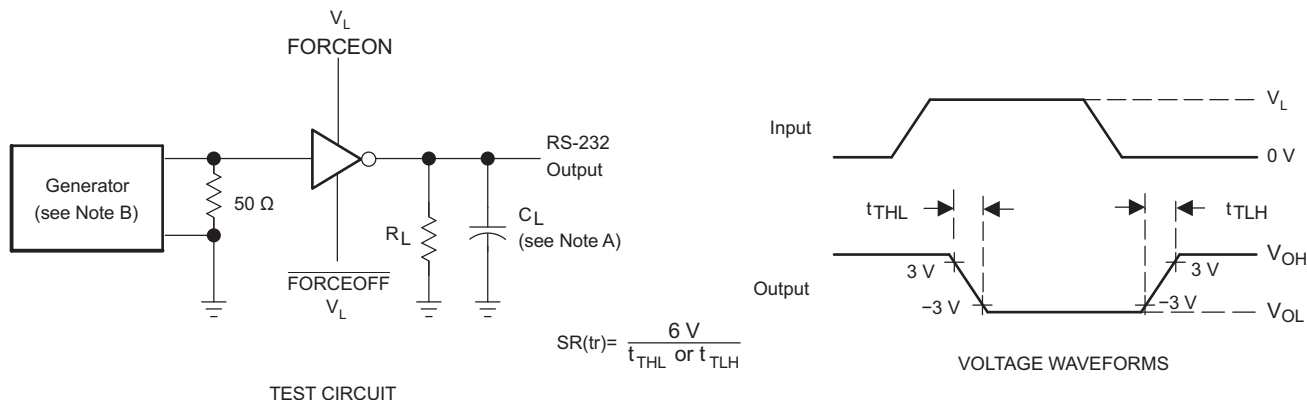


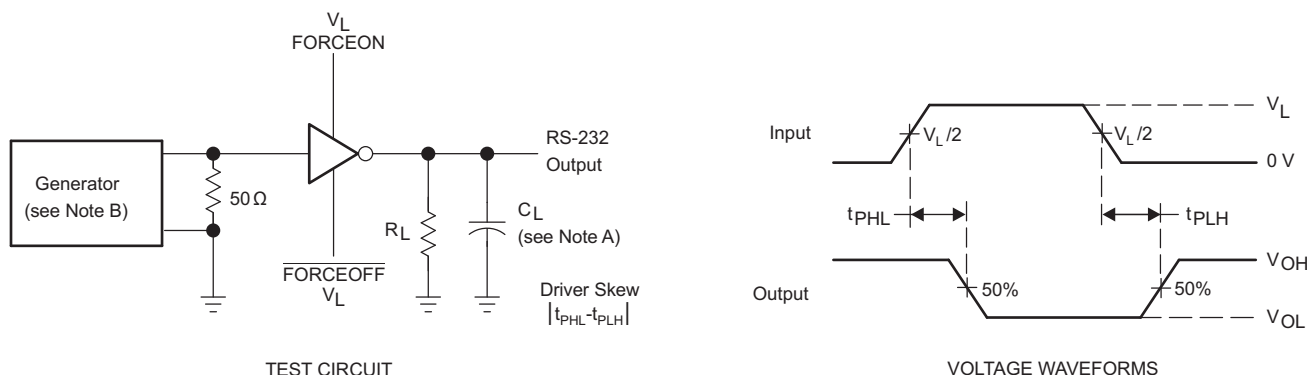
图 6. Supply Current vs. Supply Voltage (Doubler Mode)
 $V_L = 1.8\text{ V}$, $R_{LOAD} = 3\text{ k}\Omega$, $C_{LOAD} = 1\text{ nF}$, $CH2 = 32\text{ kbps}$

7 Parameter Measurement Information



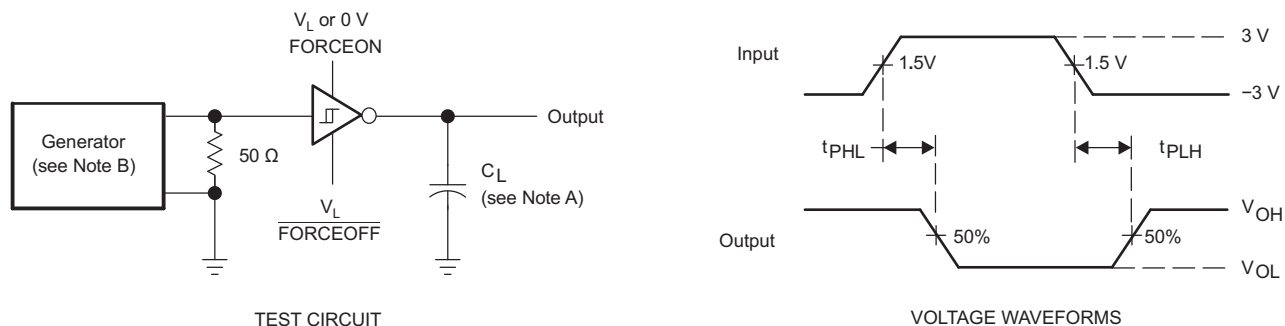
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 1000 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

图 7. Driver Slew Rate



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 1000 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

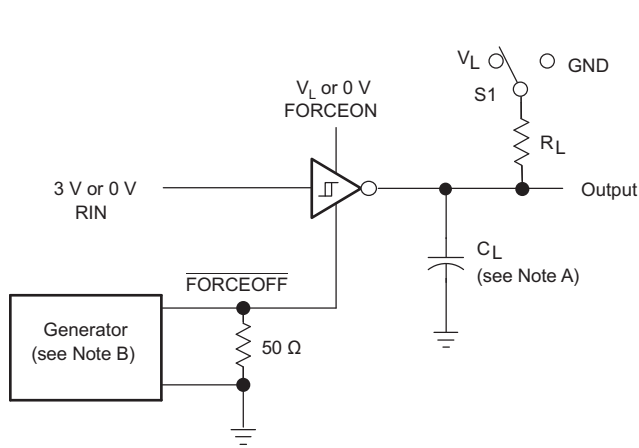
图 8. Driver Pulse Skew



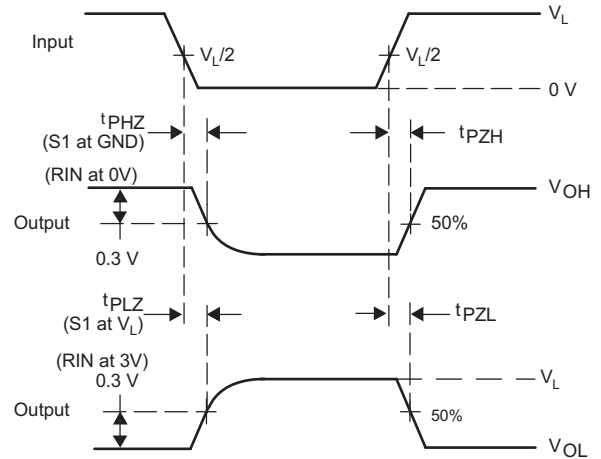
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

图 9. Receiver Propagation Delay Times

Parameter Measurement Information (接下页)



TEST CIRCUIT

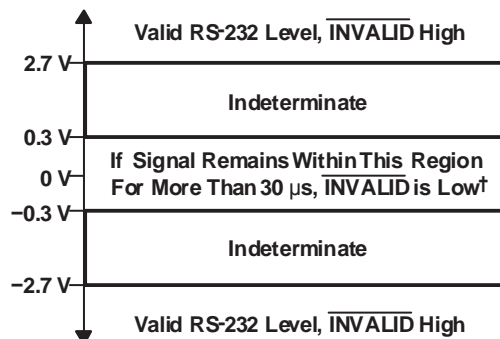
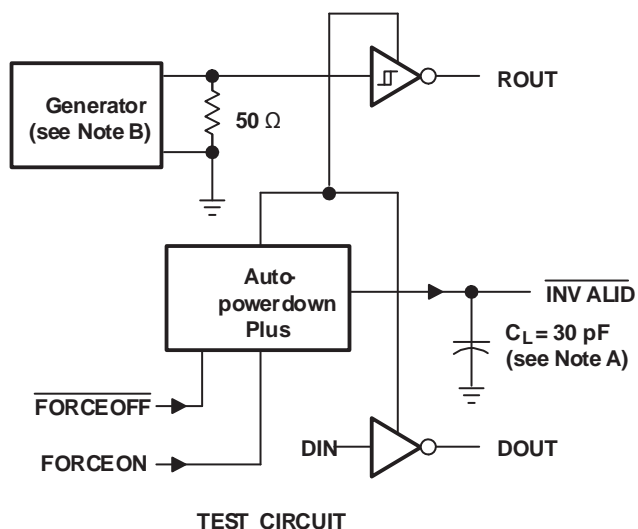


VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

图 10. Receiver Enable and Disable Times

Parameter Measurement Information (接下页)



† Auto-powerdown plus disables drivers and reduces supply current to 1 μ A.

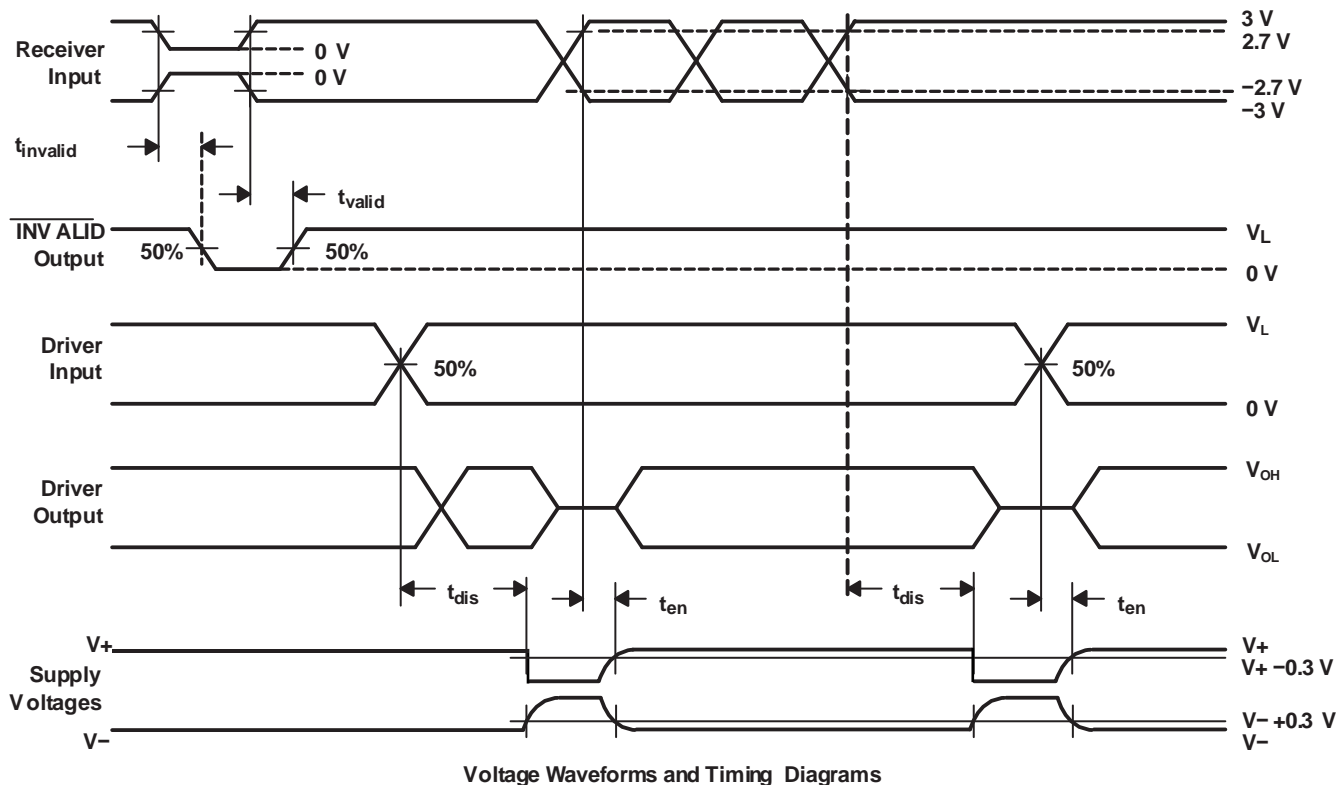


图 11. INVALID Propagation-Delay Times and Supply-Enabling Time

8 Detailed Description

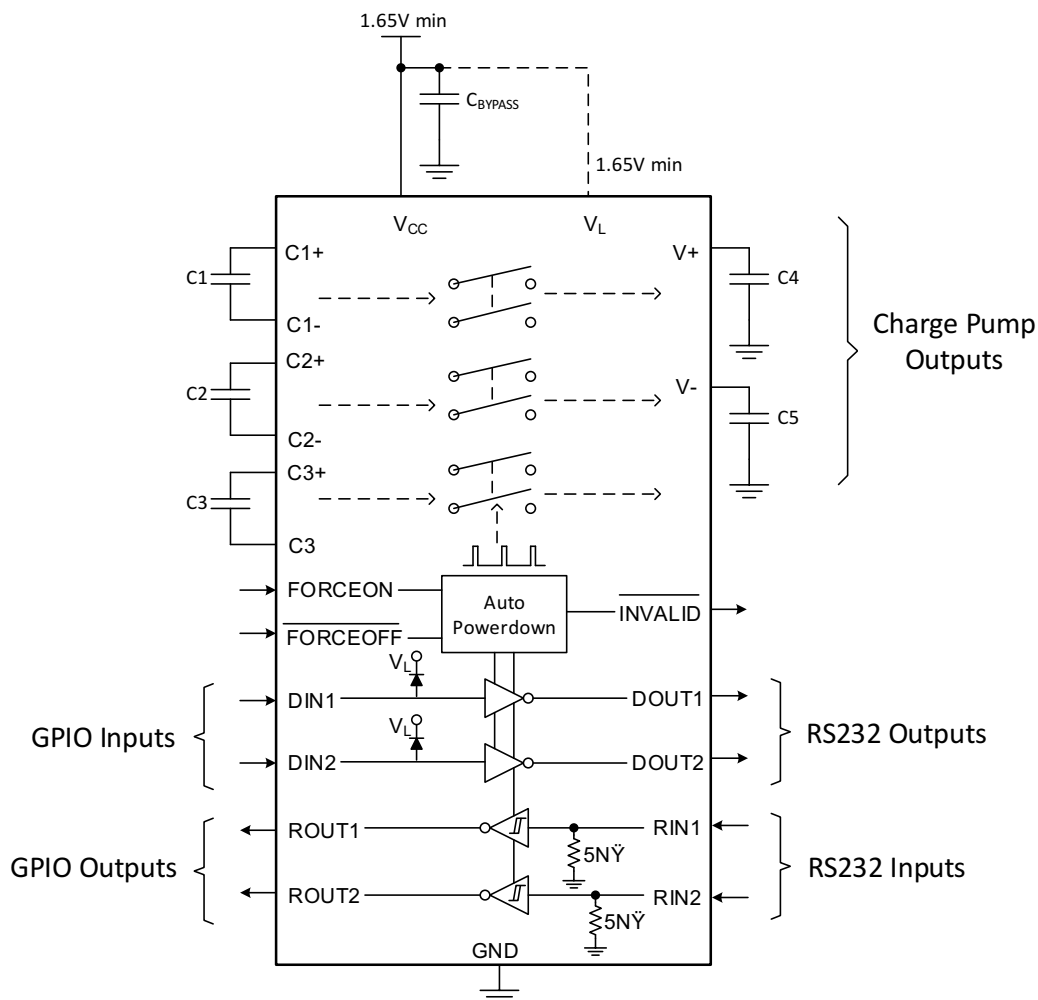
8.1 Overview

The TRS3122E is an upgrade to standard RS232 transceivers, offering compatibility with modern system needs like 1.8-V GPIO capability, enhanced ESD & ultra low stand-by current. The majority of RS-232 transceivers with 1.8-V GPIO compatibility require a logic supply pin for the I/O translation, in addition to a minimum 3.3 V V_{CC} for all of the other active circuitry on the chip. Unlike these transceivers, TRS3122E can operate with both V_L and V_{CC} equal to 1.8 V. When V_{CC} = 3.0 V to 5.5 V, the charge pump will sense V_{CC} and switch to doubler mode. C1 & C2 are the necessary flying capacitors, C3 is not needed, and the charge pump outputs V+ & V- will regulate to $\sim\pm 5.4$ V. When V_{CC} = 1.65 V to 2.0 V, the charge pump will sense V_{CC} and switch to tripler mode. C1, C2 & C3 are all necessary, and the charge pump outputs V+ & V- will regulate to $\sim\pm 2.65 \cdot V_{CC}$ from V_{CC} = 1.65 V to 2.0 V.

With many modern applications expanding into products that use RS232 as a backup communication protocol, it is important for the transceiver to have efficient standby operation. In order to accommodate this, Auto Powerdown Plus has been integrated to shut-off all active circuitry, allowing TRS3122E to achieve an I_{off} of 1 μ A.

In order to comply with common interface system needs and environments, the RS-232 receive and transmit I/O pins comply with IEC 61000-4-2 ratings.

8.2 Functional Block Diagram



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图 12. Schematic

8.3 Feature Description

8.3.1 Charge Pump

The internal power supply consists of a regulated auto-sensing charge pump that provides RS-232 compatible output voltages, over the 1.65 V to 2.0 V and 3.0 V to 5.5 V V_{CC} ranges. The charge pump operates in two modes to efficiently accommodate low voltage (1.8 V) and higher voltage (3.3 V & 5.0 V) supplies.

8.3.1.1 Doubler Mode

The charge pump requires two flying capacitors (C1, C2) and reservoir capacitors (C4, C5) to generate the V_+ and V_- supplies of approximately ± 5.4 V when V_{CC} is greater than 3 V. When V_{CC} is >2.9 V, TRS3122E will sense the supply voltage level and switch the charge pump to a doubler. Hence, no need for a third flying capacitor. C3+ & C3- pins can be left open for proper operation. If a capacitor is placed between C3+ & C3-, the charge pump will ignore this capacitor and still behave as a doubler.

For capacitor choice recommendations, please refer to [表 1](#).

8.3.1.2 Tripler Mode

The charge pump requires three flying capacitors (C1, C2 & C3) and reservoir capacitors (C4, C5) to generate the V_+ and V_- supplies of approximately $\pm 2.65 * V_{CC}$ when V_{CC} is greater than 1.65 V. When V_{CC} is <2.1 V, TRS3122E will sense the supply voltage level and switch the charge pump to a tripler.

For capacitor choice recommendations, please refer to [表 1](#).

8.3.2 Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to RS-232 levels. For $V_{CC}=3.0$ V to 5.0 V, the RS-232 output voltage swing is typically ± 5.4 V fully loaded and ± 5 V minimum fully loaded. For $V_{CC} = 1.8$ V, the RS-232 output voltage swing is typically ± 4.7 V fully loaded and ± 4.25 V minimum fully loaded.

The driver outputs are protected against indefinite short-circuits to ground without degradation in reliability. These drivers are compatible with RS-232 logic levels and all previous RS-232 versions. Unused driver inputs should be connected to GND or V_{CC} .

8.3.3 Receivers

The receivers convert EIA/TIA-232 levels to TTL or CMOS logic output levels. Receivers have an inverting output that can be disabled by using the FORCEOFF pin. Receivers remain active when the Auto Powerdown Plus circuitry autonomously enters a low power state. See [Auto Powerdown Plus](#) for more information on the Auto Powerdown mode. If the FORCEOFF pin is manually set low, the receivers will be disabled and put into 3-state mode. In either of these powerdown modes, the device will typically consume about 0.5 μ A. The truth table logic of the TRS3122E driver and receiver outputs can be found in [Device Functional Modes](#). Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300 mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5k Ω pull-down resistor to ground will commit the output of the receiver to a HIGH state.

8.3.4 ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The bus pins (driver outputs and receiver inputs) have extra protection structures, which have been tested up to ± 15 kV.

ESD protection is tested in various ways. TI uses the following standards to qualify the ESD structures designed into TRS3122E:

- ± 8 kV using IEC 61000-4-2 Contact Discharge (on RINx and DOUTx pins)
- ± 15 kV using IEC 61000-4-2 Airgap Discharge (on RINx and DOUTx pins)
- ± 15 kV using the Human Body Model (HBM) (on RINx and DOUTx pins)
- ± 2 kV using the Human Body Model (HBM) (on all pins except RINx and DOUTx pins)
- ± 0.5 kV using the Charged Device Model (CDM) (on all pins)

Feature Description (接下页)

The IEC 61000-4-2 standard is more rigorous than HBM, resulting in lower voltage levels compared with HBM for the same level of ESD protection. Because IEC 61000-4-2 specifies a lower series resistance, the peak current is higher than HBM. The TRS3122E has passed both HBM and IEC 61000-4-2 testing.

8.3.5 Auto Powerdown Plus

Powerdown is engaged in two separate cases: automatically, when no activity has occurred for a period of time, and manually, using the $\overline{\text{FORCEOFF}}$ device pin.

8.3.5.1 Automatic Powerdown

Auto Powerdown Plus is enabled when FORCEON is set LOW and $\overline{\text{FORCEOFF}}$ is set HIGH. Using TRS3122E's integrated edge detection circuitry and timer, the device can sense when there is no activity on the driver or receiver inputs for 30 seconds. When this condition is sensed by the device, it automatically shuts the charge pump off, reducing supply current to 0.5 μA . When a valid transition is sensed on one of the driver or receiver inputs, the charge pump turns back on and TRS3122E exits powerdown. The typical time to exit powerdown is typically in 30 μs , but can be as long as 150 μs . As a result, the system saves power without requiring any software control. [Device Functional Modes](#) summarizes the operating modes in truth table form.

While in the low power mode with Automatic Powerdown enabled ($\overline{\text{FORCEOFF}} = \text{HIGH}$ and $\text{FORCEON} = \text{LOW}$), the receiver inputs are still enabled.

8.3.5.2 Manual Powerdown

The device can be manually powered down by externally setting $\overline{\text{FORCEOFF}}$ pin to low logic level. Both the drivers and receivers will be powered off. [Device Functional Modes](#) summarizes the operating modes in truth table form.

8.3.5.3 Forced On

If the $\overline{\text{FORCEOFF}}$ and FORCEON pins are both set HIGH, the device will power on with Auto Powerdown Plus disabled. Both the drivers and receiver will be active regardless of inactivity. Because powerdown is autonomous, FORCEON can be used ensure drivers are ready for new data transmission if the time since last transmission (or receive data) was more than 15 seconds. [Device Functional Modes](#) summarizes the operating modes in truth table form.

8.4 Device Functional Modes

8.4.1 Each Driver⁽¹⁾

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown plus disabled
H	H	H	X	L	
L	L	H	<30 s	H	Normal operation with auto-powerdown plus enabled
H	L	H	<30 s	L	
L	L	H	>30 s	Z	Powered off by auto-powerdown plus feature
H	L	H	>30 s	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), 30s is typical inactivity time

8.4.2 Each Receiver⁽¹⁾

INPUTS			OUTPUTS	RECEIVER STATUS
RIN	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	ROUT	
X	L	X	Z	Powered off
L	H	X	H	Normal operation with auto-powerdown plus disabled/enabled
H	H	X	L	
Open	H	X	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

8.4.3 $\overline{\text{INVALID}}$ Status Truth Table⁽¹⁾

INPUTS				OUTPUT
RIN1, RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	$\overline{\text{INVALID}}$
Any L or H	X	X	X	H
All Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

8.4.4 Capacitor Selection Table

表 1. Capacitor Selection

$V_{CC} = V_L$	C1 Capacitor Value	C2 Capacitor Value	C3 Capacitor Value	C4 Capacitor Value	C5 Capacitor Value
1.65 V to 2 V ⁽¹⁾	100 nF				
3.0 V to 3.6 V ⁽¹⁾	100 nF		100 nF or open	100 nF	
4.5 V to 5.5 V ⁽¹⁾	47 nF	330 nF	100 nF or open	330 nF	
3 V to 5.5 V ⁽²⁾	47 nF	470 nF	100 nF or open	470 nF	

(1) For optimized performance, we recommend using these configurations.

(2) For applications where the V_{CC} variation is larger, this configuration is acceptable.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

RS232 is used to communicate between two electrical units on separate PCBs across cables <40 ft. Common RS232 cables are RJ45, DB9 & DB25.

9.2 Typical 1.8-V Application

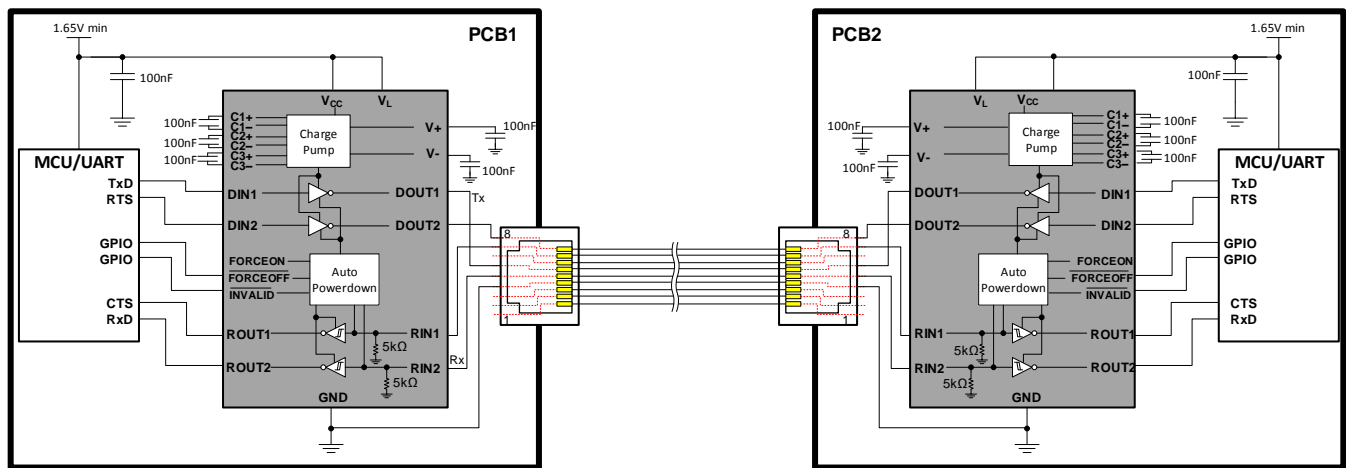


图 13. TRS3122E Typical Application

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
MCU GPIO Supply Voltage	1.8 V
Transmission Voltage	+/-4.7 V
Data-rate	1 Mbps
Number of Transmitters / Receivers	2
Charge Pump Capacitor Values	100nF (see 表 3)

9.2.2 Detailed Design Procedure

When using TRS3122E, determine the following:

- All DIN, FORCEOFF, and FORCEON inputs must be connected to valid low or high logic levels.
- Select capacitor values based on V_{CC} level for best performance. (see 表 3)

9.2.2.1 Data-Rate and Cable Length

RS-232 intended is for short range data transmission. The rise time for RS-232 driver edges is slow enough that the data cable appears as a capacitor instead of a transmission line impedance. The elapsed time for one bit of data far exceeds the transit time of any practical RS-232 cable length. The capacitance of the cable is the limiting factor. Therefore the capacitance per foot (or meter) of the cable is important if long data cables are used. Capacitance slows the rise and fall time of the signal. For low data rates, the delay is insignificant. However, high data rates will have reduced percentage of time that the output is at V_{OL} or V_{OH} and more time in the transitions. The timing of the UART (universal asynchronous receiver/transmitter) must sample the signal at the right time to coincide with V_{OL} and V_{OH} plateaus. At some point data reliability will be impacted. There are no hard limits for cable capacitance and data rate.

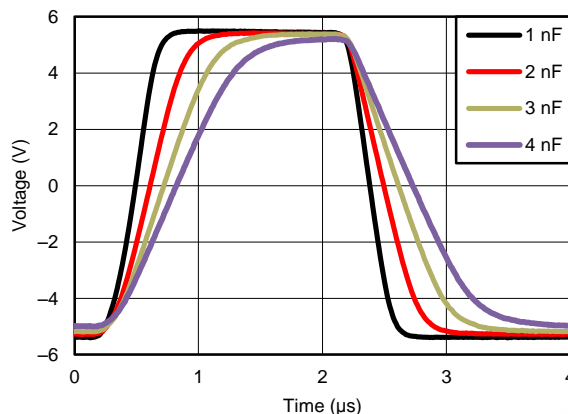


图 14. Typical Waveform with Capacitive Load
 $V_{CC} = 3.3\text{ V}$, $R_{LOAD} = 3\text{ k}\Omega$, Date Rate = 500kbps

The maximum cable length depends on the cable used (pf/ft), data rate, timing of receiving UART, system tolerance to data errors.

9.2.2.2 Capacitor Selection

The capacitor type used for C1–C5 is not critical for proper operation; polarized or non-polarized capacitors can be used, though lower ESR capacitors are preferred. The charge pump requires 0.1 μF capacitors for $V_{CC} = 1.8\text{-V}$ or $V_{CC} = 3.3\text{-V}$ operation. For other supply voltages, see 表 1 for required capacitor values. Do not use values smaller than those listed in 表 1. Increasing the capacitor values(e.g., by a factor of 2), except for C1, reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, C4 and C5 can be increased without changing C1’s value. However, do not increase C1 without also increasing the values of C2, C3, C4, C5, $C_{BYPASS1}$, and $C_{BYPASS2}$ to maintain the proper ratios (C1 to the other capacitors). When using the minimum required capacitor values, make sure the capacitor value does not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor’s equivalent series resistance (ESR) usually increases at low temperatures.

For best charge pump efficiency locate the charge pump and bypass capacitors as close as possible to the IC. Surface mount capacitors are best for this purpose. Using capacitors with lower equivalent series resistance (ESR) and self-inductance, along with minimizing parasitic PCB trace inductance will optimize charge pump operation. Designers are also advised to consider that capacitor values may shift over time and operating temperature.

表 3. Capacitor Selection

$V_{CC} = V_L$	C1 Capacitor Value	C2 Capacitor Value	C3 Capacitor Value	C4 Capacitor Value	C5 Capacitor Value
1.65 V to 2 V ⁽¹⁾	100 nF				
3.0 V to 3.6 V ⁽¹⁾	100 nF		100 nF or open	100 nF	
4.5 V to 5.5 V ⁽¹⁾	47 nF	330 nF	100 nF or open	330 nF	
3 V to 5.5 V ⁽²⁾	47 nF	470 nF	100 nF or open	470 nF	

(1) For optimized performance, we recommend using these configurations.

(2) For applications where the V_{cc} variation is larger, this configuration is acceptable.

9.2.3 Application Curves

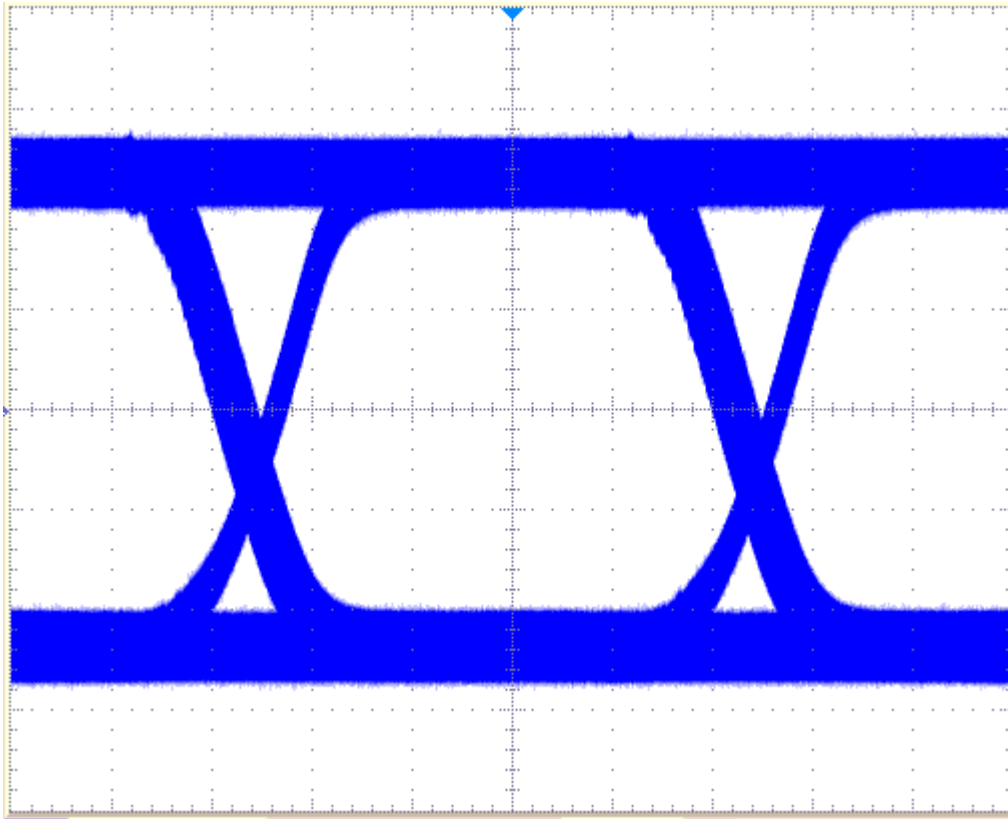


图 15. 1 Mbps Eye Diagram, 2 V/div, 200 ns/ div
 $V_{CC} = 1.8\text{ V}$, $C_{LOAD} = 500\text{ pF}$, $R_{LOAD} = 3\text{ k}\Omega$

10 Power Supply Recommendations

In most circumstances, a $0.1\text{-}\mu\text{F}$ V_{CC} bypass capacitor and a $1\text{-}\mu\text{F}$ V_L bypass capacitor are adequate. In applications that are sensitive to power-supply noise, use larger value V_{CC} bypass capacitor. There is no maximum limit for bypass capacitor. Place bypass capacitors as close to the IC as possible.

It is not recommended to use this device when V_{CC} is powered and $V_L = 0\text{ V}$ or floating for an extended period of time because operation is undefined. V_{CC} and V_L must be powered to guarantee charge pump operation.

Also, to achieve full functionality as described in [Specifications](#), it is recommended to not use a higher voltage on V_L than V_{CC} . Full functionality can be achieved when V_{CC} is greater than or equal to V_L .

11 Layout

11.1 Layout Guidelines

Minimize the length of all capacitor traces to ensure the device can maintain quick rising and falling transitions. Vias are recommended to accommodate layouts for the capacitors.

11.2 Layout Example

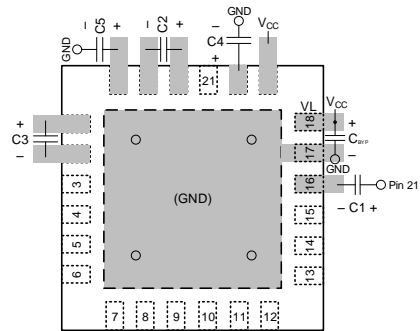


图 16. TRS3122E Typical Layout

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS3122ERGER	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3122
TRS3122ERGER.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3122
TRS3122ERGERG4	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3122
TRS3122ERGERG4.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3122
TRS3122ERGET	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3122
TRS3122ERGET.A	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3122

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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RGE 24

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

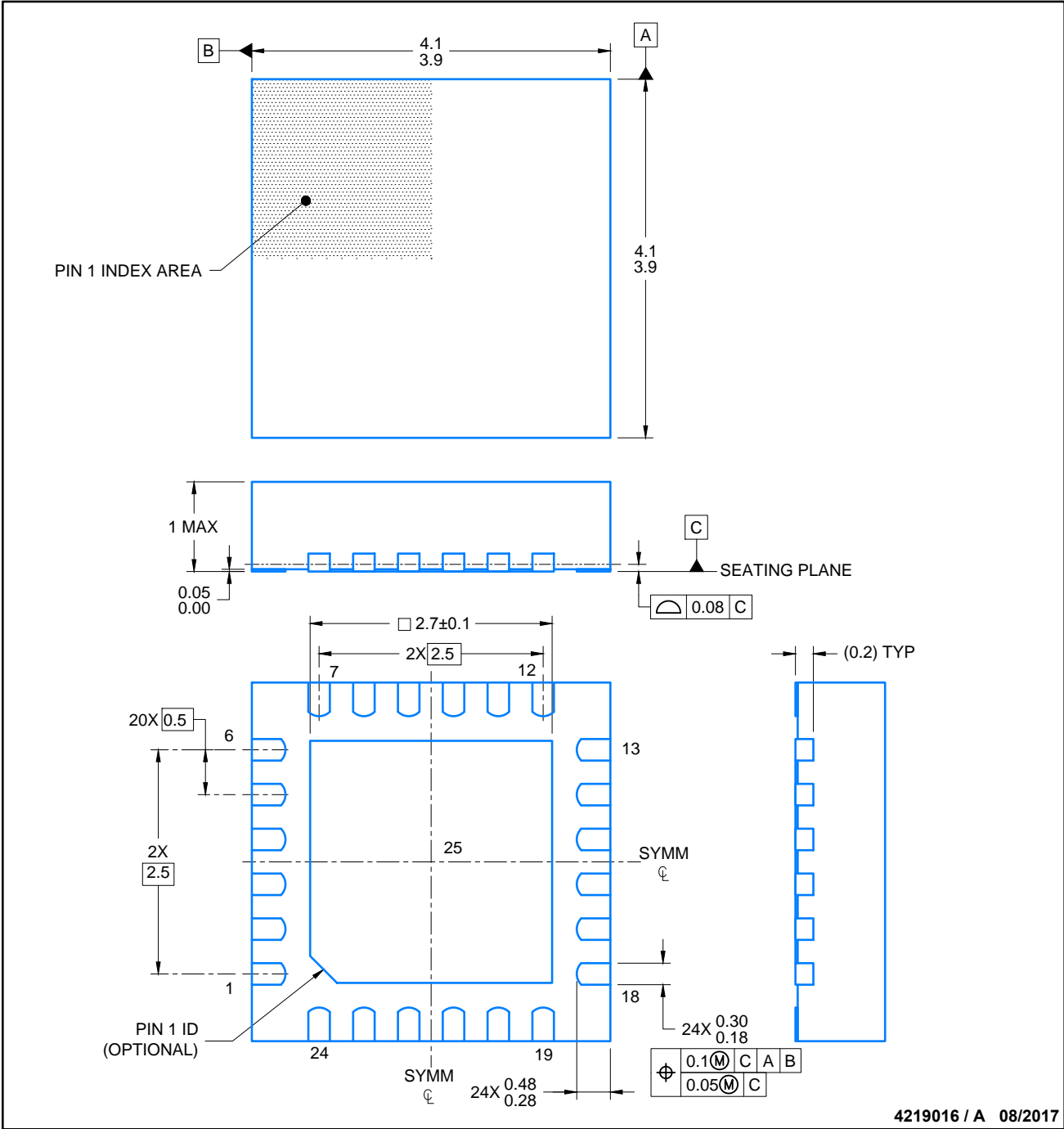
4204104/H

RGE0024H

PACKAGE OUTLINE

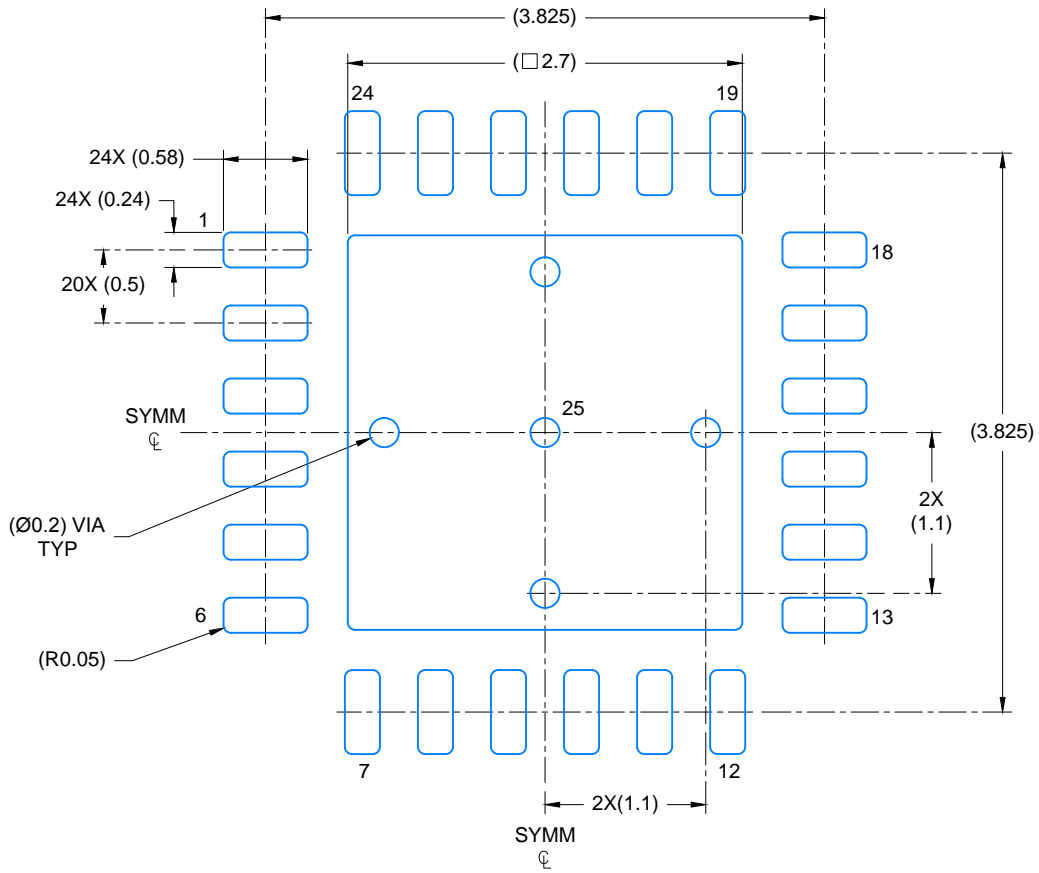
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



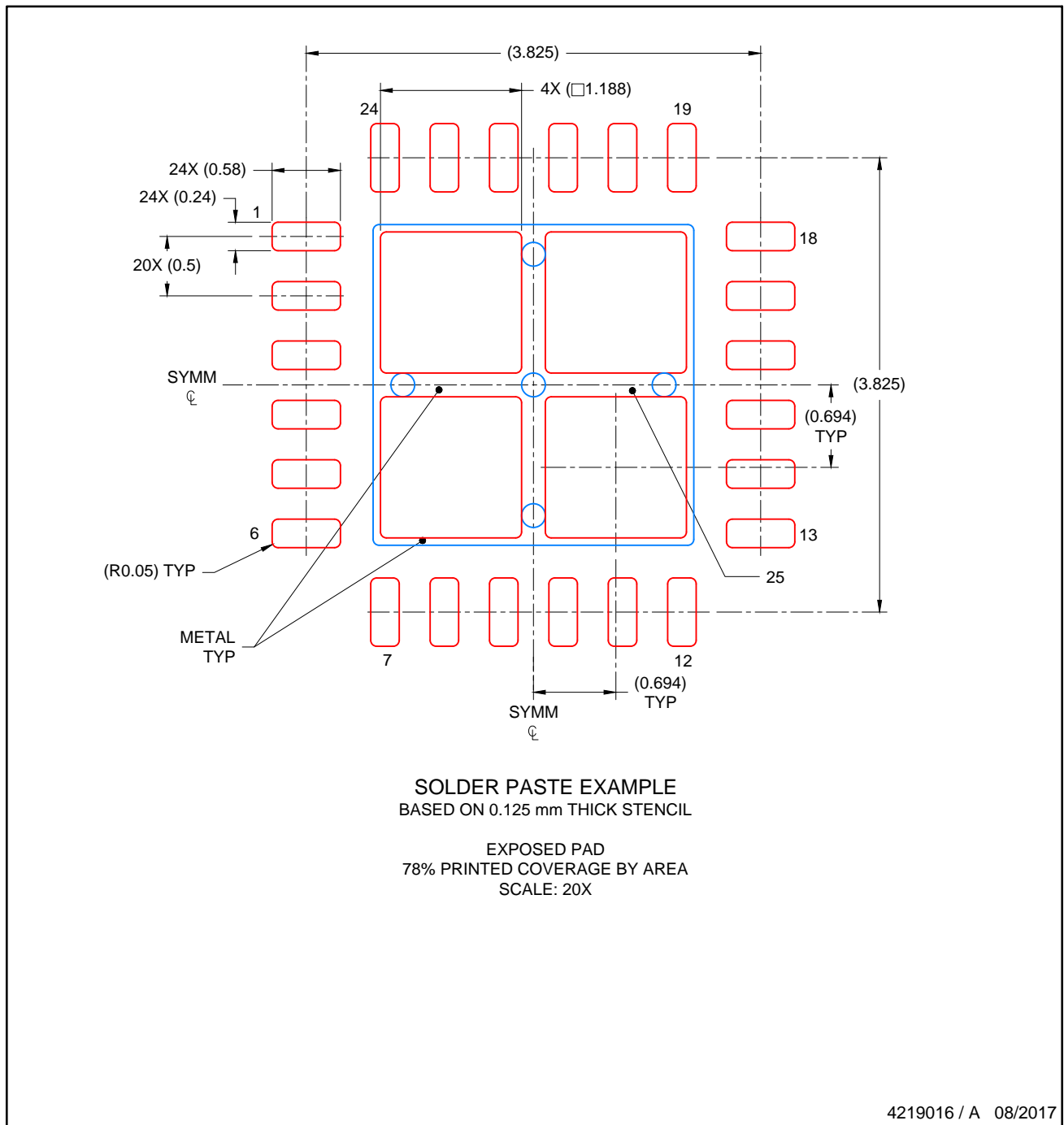
LAND PATTERN EXAMPLE
SCALE: 20X



4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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