TPS99001-Q1 系统管理控制器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 温度等级 2：–40°C 至 +105°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 适用于 DLP® 产品的汽车系统管理器件：
  - 高级电源监控、排序和保护电路
  - 两个裸片温度监控器、MCU 外部看门狗计时器和时钟频率监控器
  - 具有奇偶校验、校验和密码寄存器保护的 SPI 端口
  - 另一个用于独立系统监控的 SPI 端口
- 片上 DMD 镜像电压稳压器
  - 可生成 +16V、+8.5V 和 -10V DMD 控制电压
- 每帧高达 63 个时间序列样本的 12 位 ADC

2 应用

- 汽车高级照明应用（高分辨率前照灯）
- 自适应远光灯 (ADB)

3 说明

TPS99001-Q1 系统管理控制器是 DLP553x-Q1 和 DLP462x-Q1 芯片组的组成部分，其中还包含 DLPC23x-Q1 DMD 显示控制器。集成式 DMD 高压稳压器电源可提供 DMD 镜像基准电压，满足严格容差的要求。电源序列发生器和监控器为整个芯片组的加电和断电事件提供可靠协同。

TPS99001-Q1 控制器集成了一个 12 位 ADC，是控制系统的核心元件之一。该 ADC 能够自动对每个视频帧进行高达 63 次事件采样。

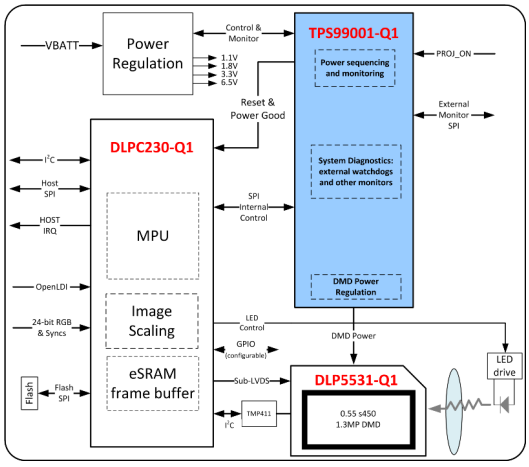
先进的系统状态监控电路可帮助实时了解显示子系统的运行情况，包括两个处理器看门狗电路、两个裸片温度监控器、用于过压和欠压检测的综合电源监控、在 SPI 总线事务上通过字节级奇偶校验获得校验和以及密码寄存器保护、以及其他内置测试功能。

为了帮助设计和制造基于 DLP 技术的符合汽车标准的投影仪，可利用多家老牌光学模块制造商和设计公司来支持您的设计。

器件信息

器件型号	封装(1)	封装尺寸
TPS99001-Q1	HTQFP (100)	14.00mm × 14.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型的独立系统

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4 Pin Configuration and Functions

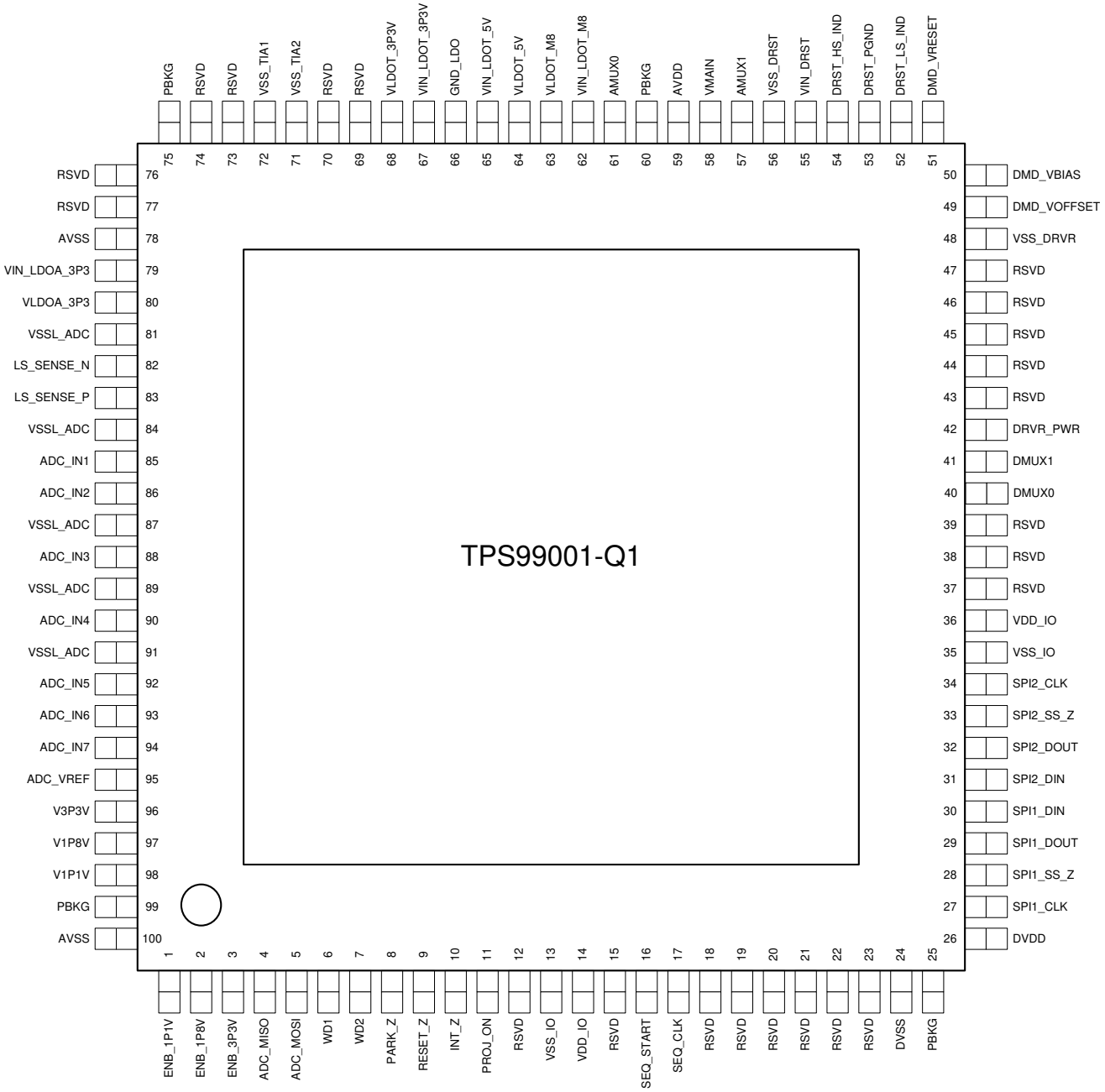


图 4-1. PZP Package 100-Pin HTQFP Top View

表 4-1. Pin Functions—Initialization, Clock, and Diagnostics

PIN		TYPE	DESCRIPTION
NO.	NAME		
6	WD1	I	Watchdog interrupt channel 1
7	WD2	I	Watchdog interrupt channel 2
8	PARK_Z	O	DMD mirror parking signal (active low)
9	RESET_Z	O	Reset output to the DLPC23x-Q1. TPS99001-Q1 controlled.
10	INT_Z	O	Interrupt output signal to DLPC23x-Q1 (open drain). Recommended to pull up to the DLPC23x-Q1 3.3V rail controlled by the TPS99001-Q1's ENB_3P3V signal.
11	PROJ_ON	I	Input signal to enable/disable the IC and DLP projector
16	SEQ_START	I	PWM shadow latch control; indicates a start of sequence
17	SEQ_CLK	I	Sequencer clock
40	DMUX0	O	Digital test point output
41	DMUX1	O	Digital test point output
57	AMUX1	O	Analog test mux output 1
61	AMUX0	O	Analog test mux output 0

表 4-2. Pin Functions—Power and Ground

PIN		TYPE	DESCRIPTION
NO.	NAME		
13, 35	VSS_IO	GND	Ground connection for digital IO interface
14, 36	VDD_IO	POWER	3.3V power input for IO rail supply
24	DVSS	GND	Digital core ground return
25, 60, 75, 99	PBKG	GND	Substrate tie and ESD ground return
26	DVDD	POWER	3.3V power input for digital core supply
42	DRVR_PWR	POWER	6V power input
48	VSS_DRVR	GND	Ground connection for driver power
49	DMD_VOFFSET	POWER	VOFFSET output rail. Connect a 1 µF ceramic capacitor to ground
50	DMD_VBIAS	POWER	VBIAS output rail. Connect a 0.47 µF ceramic capacitor to ground
51	DMD_VRESET	POWER	VRESET output rail. Connect a 1 µF ceramic capacitor to ground. Connect to DRST_HS_IND through external diode. Connect anode of diode to DMD_VRESET.
53	DRST_PGND	GND	Power ground for DMD power supply. Connect to ground plane
55	VIN_DRST	POWER	6V input for DMD power supply
56	VSS_DRST	GND	Ground supply for DMD power supply
59	AVDD	POWER	3.3V power supply input for analog circuit
63	VLDOT_M8	POWER	Unused. Leave open or unconnected.
64	VLDOT_5V	POWER	Filter cap interface for 5V LDO
65	VIN_LDOT_5V	POWER	6V power input for 5V LDO
66	GND_LDO	GND	Power ground return for LDO
67	VIN_LDOT_3P3V	POWER	6V power input for 3.3V LDO
68	VLDOT_3P3V	POWER	Filter cap interface for 3.3V LDO
71	VSS_TIA2	GND	Ground
72	VSS_TIA1	GND	Ground
78, 100	AVSS	GND	Analog ground
79	VIN_LDOA_3P3	POWER	6V power input for dedicated ADC interface 3.3V LDO supply
80	VLDOA_3P3	POWER	Dedicated ADC interface 3.3V LDO filter cap output
81, 84, 87, 89, 91	VSSL_ADC	GND	External ADC channel bondwire and lead frame isolation ground
95	ADC_VREF	POWER	ADC reference voltage output

表 4-3. Pin Functions—Power Supply Management

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	ENB_1P1V	O	External 1.1V buck enable. 3.3V output
2	ENB_1P8V	O	External 1.8V buck enable. 3.3V output
3	ENB_3P3V	O	External 3.3V buck enable. 3.3V output
52	DRST_LS_IND	ANA	Connection for the DMD power supply inductor (10 µH). Connect a 330pF, 50V capacitor to ground. X7R recommended
54	DRST_HS_IND	ANA	Connection for the DMD power supply inductor (10 µH)
58	VMAIN	I	Main intermediate voltage monitor input. Use an external resistor divider to set voltage input for brownout monitoring.
62	VIN_LDOT_M8	O	Unused. Leave open or unconnected.
96	V3P3V	I	External 3.3V buck voltage monitor input
97	V1P8V	I	External 1.8V buck voltage monitor input
98	V1P1V	I	External 1.1V buck voltage monitor input

表 4-4. Pin Functions—Reserved Pins

PIN		TYPE	DESCRIPTION
NO.	NAME		
12	Reserved	O	Reserved. Leave unconnected.
15	Reserved	O	Reserved. Leave unconnected.
18	Reserved	I	Reserved. Connect to ground.
19	Reserved	I	Reserved. Connect to ground.
20	Reserved	I	Reserved. Connect to ground.
21	Reserved	I	Reserved. Connect to ground.
22	Reserved	I	Reserved. Connect to ground.
23	Reserved	I	Reserved. Connect to ground.
37	Reserved	I	Reserved. Connect to ground
38	Reserved	O	Reserved. Leave unconnected.
39	Reserved	O	Reserved. Leave unconnected.
43	Reserved	O	Reserved. Leave unconnected.
44	Reserved	O	Reserved. Leave unconnected.
45	Reserved	O	Reserved. Leave unconnected.
46	Reserved	O	Reserved. Leave unconnected.
47	Reserved	O	Reserved. Leave unconnected.
69	Reserved	O	Reserved. Leave unconnected.
70	Reserved	I	Reserved. Leave unconnected.
73	Reserved	I	Reserved. Leave unconnected.
74	Reserved	O	Reserved. Leave unconnected.
76	Reserved	ANA	Reserved. Connect to ground.
77	Reserved	ANA	Reserved. Connect to ground.

表 4-5. Pin Functions—Serial Peripheral Interfaces

PIN		TYPE	DESCRIPTION
NO.	NAME		
27	SPI1_CLK	I	SPI control interface (DLPC23x-Q1 primary, TPS99001-Q1 secondary), clock input
28	SPI1_SS_Z	I	SPI control interface (DLPC23x-Q1 primary, TPS99001-Q1 secondary), chip select (active low)
29	SPI1_DOUT	O	SPI control interface (DLPC23x-Q1 primary, TPS99001-Q1 secondary), transmit data output
30	SPI1_DIN	I	SPI control interface (DLPC23x-Q1 primary, TPS99001-Q1 secondary), receive data input
31	SPI2_DIN	I	SPI diagnostic port (secondary), receive data input. For read-only monitoring
32	SPI2_DOUT	O	SPI diagnostic port (secondary), transmit data output. For read-only monitoring
33	SPI2_SS_Z	I	SPI diagnostic port (secondary), chip select (active low). For read-only monitoring
34	SPI2_CLK	I	SPI diagnostic port (secondary), clock input. For read-only monitoring

表 4-6. Pin Functions—Analog to Digital Converter

PIN		TYPE	DESCRIPTION
NO.	NAME		
4	ADC_MISO	O	ADC 2-wire interface - data output. DLPC23x-Q1 primary, TPS99001-Q1 secondary.
5	ADC_MOSI	I	ADC 2-wire interface - data input. DLPC23x-Q1 primary, TPS99001-Q1 secondary.
82	LS_SENSE_N	I	Low side current sense ADC negative input, see 表 6-1
83	LS_SENSE_P	I	Low side current sense ADC positive input, see 表 6-1
85	ADC_IN1	I	External ADC channel 1, see 表 6-1
86	ADC_IN2	I	External ADC channel 2, see 表 6-1
88	ADC_IN3	I	External ADC channel 3, see 表 6-1
90	ADC_IN4	I	External ADC channel 4, see 表 6-1
92	ADC_IN5	I	External ADC channel 5, see 表 6-1
93	ADC_IN6	I	External ADC channel 6, see 表 6-1
94	ADC_IN7	I	External ADC channel 7, see 表 6-1

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VDD_IO to VSS_IO	–0.3	4	V
	DVDD to DVSS	–0.3	4	
	AVDD to DVSS	–0.3	4	
	All "VSS" to other "VSS" (grounds)	–0.1	0.1	
	All digital input signals to ground (WD1, WD2, ADC_MOSI, PROJ_ON, SEQ_START, SEQ_CLK, SPI1_CLK, SPI1_DIN, SPI1_SS, SPI2_DIN, SPI2_CLK, SPI2_SS, EXT_SMPL)	–0.3	3.6	
	DRVR_PWR to ground	–0.3	7.5	
	VIN_LDO_5V	–0.3	7.5	
	V3P3V to ground	–0.3	5	
	V1P8V to ground	–0.3	5	
	V1P1V to ground	–0.3	5	
	VIN_LDOA_3P3 to ground	–0.3	7.5	
	VIN_LDOT_3P3 to ground	–0.3	7.5	
	ADC_IN(7:1) to ground	–0.3	3.6	
	DRST_LS_IND to DRST_PGND	–0.3	27	
	VIN_DRST to ground	–0.3	7.5	
	VMAIN	–0.3	7.5	
Outputs	INT_Z	–0.3	7.5	V
Operating junction temperature, T_J		–40	130	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
	Charged-device model (CDM), per AEC Q100-011	All pins	±500	
		Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
TEMPERATURE					
T_A	Operating ambient temperature(1)	– 40		105	°C
T_J	Operating junction temperature	– 40		125	°C
VOLTAGE					
VDD_IO	IO 3.3V voltage supply	3	3.3	3.6	V
DVDD	Digital 3.3V supply	3	3.3	3.6	V
AVDD	Analog 3.3V supply	3	3.3	3.6	V
ADC	ADC(7:1) inputs	0.1		1.6	V
VIN_DRST	DMD reset regulator input	5.5	6	7	V
VIN_LDOT_5V	Power supply input to 5V LDO	5.5	6	7	V
VIN_LDOA_3P3V	Power supply input to 3.3V ADC LDO	5.5	6	7	V
VIN_LDOT_3P3V	Power supply input to 3.3V LDO	5.5	6	7	V
DRVR_PWR	Gate driver power supply	3	6	7	V

(1) – 40°C to 105°C ambient, free air convection, AEC Q100 grade 2.

5.4 Thermal Information

THERMAL METRIC(1) (2)		TPS99001-Q1 PZP (HTQFP) 100 PINS	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) Operating ambient temperature is dependent on system thermal design. Operating junction temperature may not exceed its specified range across ambient temperature conditions.

5.5 Electrical Characteristics—Analog to Digital Converter

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
12-BIT ADC(1)						
V_{INPUT}	Input range(2)		0.1		1.6	V
INL	Integral non-linearity	Over valid input range VINPUT	–4		4	LSB
DNL	Differential non-linearity		–2.5		2.5	LSB
ENOB	Effective number Of bits		10	12		bits
t_{SAMPLE}	S/H sampling period		0.4	5.2	12.8	µs
t_{DELAY}	S/H delay before conversion starts		0.4		2.8	µs
t_{SHOLD}	S/H holding period			102.4	245	µs
t_{CONV}	Conversion period			102.4		µs
V_{REF}	Measurement reference	ADC reference voltage is doubled to 1.6V	0.784	0.8	0.816	V
V_{OFFS}	Offset		–20		20	LSB
	Gain error	"ADC_IN(7:1) inputs	2		2	%FSR

(1) ADC specifications refer to ADC core behavior, presume ideal clocks and IC input power conditions, unless otherwise noted.
(2) Results in invalid ADC codes below 256

5.6 Electrical Characteristics—Voltage Regulators

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOFFSET REGULATOR						
V_{OUT}	Output voltage	Across load conditions	8.25	8.5	8.75	V
I_{OUT}	Output current(2)		0.1(4)		16.3	mA
$V_{PGTHRESHR}$	Powergood threshold, VOUT rising			86%		
$V_{PGTHRESHF}$	Powergood threshold, VOUT falling			66%		
C_{OUT}	Output capacitor(3)			1		µF
T_{DISC}	Discharge time	C_{OUT} = 1 µ F			260	µs
VBIAS REGULATOR						
V_{OUT}	Output voltage		15.5	16	16.5	V
I_{OUT}	Output current(2)		0.1(4)		1.5	mA
$V_{PGTHRESHR}$	Powergood threshold, VOUT rising			86%		
$V_{PGTHRESHF}$	Powergood threshold, VOUT falling			66%		
C_{OUT}	Output capacitor(3)			0.47		µF
T_{DISC}	Discharge time	C_{OUT} = 0.47 µ F			260	µs
VRESET REGULATOR						
V_{OUT}	Output voltage		– 10.5	– 10	– 9.5	V
I_{OUT}	Output current(1) (2)		– 17.6		– 0.1(4)	mA
$V_{PGTHRESHR}$	Powergood threshold			80%		
C_{OUT}	Output capacitor(3)			1		µF
T_{DISC}	Discharge time	C_{OUT} = 1 µ F			260	µs

(1) VRESET current supplies both DMD and negative 8V LDO.
(2) VOFFSET, VBIAS, and VRESET are designed to supply the DMD and negative 8V LDO only, and should not be connected to additional loads.
(3) The capacitance value of some ceramic capacitor types can diminish drastically depending on the applied DC voltage and temperature. TI recommends X7R dielectric capacitors to minimize capacitance loss over voltage bias and temperatures. Using a higher voltage rated part and/or a larger package size also helps minimize the capacitance reduction at the applied DC voltage. Refer to the DLP5531Q1EVM for suggested components.
(4) Pull down resistors required to meet minimum current requirement.

5.7 Electrical Characteristics—Temperature and Voltage Monitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE MONITOR						
$TEMP_{WARN}$	Thermal warning threshold	Junction temperature		135		°C
$TEMP_{EMRG}$	Thermal emergency threshold	Junction temperature		150		°C
1.1-V SUPPLY MONITOR						
V_{TRIPN}	Negative trip threshold	Negative going only	0.95	0.98	1.01	V
$V_{TRIPHYST}$	Hysteresis	Positive going threshold, amount higher than negative trip voltage		2%		
t_{GLITCH}	Glitch suppression	Size of glitch ignored (no reset) with 2% overdrive	20		1000	µs
1.8-V SUPPLY MONITOR						
V_{TRIPN}	Negative trip threshold	Negative going only	1.552	1.6	1.648	V
$V_{TRIPHYST}$	Hysteresis	Positive going threshold, amount higher than negative trip voltage		2%		
t_{GLITCH}	Glitch suppression	Size of glitch ignored (no reset) with 2% overdrive	20		1000	µs
3.3-V SUPPLY MONITOR						
V_{TRIPN}	Negative trip threshold	Negative going only	2.852	2.93	3.03	V
$V_{TRIPHYST}$	Hysteresis	Positive going threshold, amount higher than negative trip voltage		2%		
t_{GLITCH}	Glitch suppression	Size of glitch ignored (no reset) with 2% overdrive	20		1000	µs
VMAIN SYSTEM INPUT SUPPLY MONITOR						
$V_{MAINTHRSH}$	VMAIN threshold	External resistor divider used to translate VMAIN	1.2125	1.25	1.2875	V
$t_{MAINGLITCH}$	VMAIN glitch suppression	At 2% overdrive	20		1000	µs

5.8 Electrical Characteristics—Current Consumption

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
SUM OF 3.3V SUPPLY PINS: DVDD, VDD_IO, AND AVDD					
System off	PROJ_ON low		1.5	2	mA
System on	Display ON state		3.5	4	mA
SUM OF 6V SUPPLY PINS: DRVR_PWR, VIN_DRST, VIN_LDOT_5V, VIN_LDOT_3P3V, AND VIN_LDOA_3P3V					
System off	PROJ_ON low		1	2	mA
System on(3)	Display ON state		98	119	mA

(1) Typical measurements performed at 25°C and nominal voltage

(2) Measurements taken at –40°C, 25°C, and 105°C. 3.3V inputs measured at 3V, 3.3V, and 3.6V. 6V inputs measured at 5.5V, 6V, and 7V. The maximum current draw of all these conditions is shown.

(3) This number represents the current at the input to the TPS99001-Q1 when the DMD voltage rails output the maximum current as listed in the respective sections of this data sheet. This number is the combination of the measured current when the DMD voltage regulator is unloaded (3mA typical, 56mA max) and the estimated current draw on the 6V supply when the DMD voltage regulator outputs the maximum current (63mA). The estimated current draw is calculated by the equation $I_{6V} = [(16 / 6) \times I_{VBIAS} + (8.5 / 6) \times I_{VOFFSET} + (-10 / 6) \times I_{VRESET}] / \eta$ where $\eta = 0.9$. In order to calculate the power dissipation of the TPS99001-Q1 in this condition, multiply the current from the unloaded condition by the input voltage and add the current from the DMD voltage regulator multiplied by the input voltage multiplied by $(1 - \eta)$.

5.9 Power-Up Timing Requirements

			TYP	UNIT
t_{en_dly}	PROJ_ON to 1.1V enable. This includes PROJ_ON t_{glitch} time.	Rising edge of PROJ_ON to rising edge of 1.1V enable	11	ms
t_{mon1} (1) (2)	Maximum time for 1.1V rail to reach voltage threshold after enable has been asserted. This delay length will occur even if 1.1V meets threshold earlier.	Rising edge of ENB_1P1V to internal 1.1V monitor test (3)	10	ms
t_{mon2} (1) (2)	Maximum time for 1.8V rail to reach voltage threshold after enable has been asserted. This delay length will occur even if 1.8V meets threshold earlier.	Rising edge of ENB_1P8V to internal 1.8V monitor test (3)	10	ms
t_{mon3} (1) (2)	Maximum time for 3.3V rail to reach voltage threshold after enable has been asserted. This delay length will occur even if 3.3V meets threshold earlier.	Rising edge of ENB_3P3V to internal 3.3V monitor test (3)	10	ms
t_{w1} (4)	RESETZ delay after voltage testing completion.	Completion of 3.3V monitor test to RESETZ rising edge	10	ms

(1) V1P1V, V1P8V, and V3P3V rails may be enabled prior to the TPS99001-Q1 assertion of their respective enable signal if required for system power design. If necessary, ENB_1P1V may be connected to the 1.1V, 1.8V, and 3.3V external supply enables.
(2) If any voltage threshold is not met within the specified time, the TPS99001-Q1 will not deassert RESETZ. The power-up procedure must be fully restarted in this situation.
(3) Each TPS monitor *test* is performed approximately 10 ms from the voltage rail's respective voltage enable. The voltage rail may come to its threshold value any time before this. This means there should be approximately 10 ms between each enable. The time for the respective 1.1V, 1.8V, and 3.3V to come up will differ by design and parts chosen, but they must all be valid before the monitor test.
(4) t_{w1} starts after the 3.3V rail passes its internal monitor tests (~10 ms). This time does not start as soon as the 3.3V comes to its threshold value. This time starts after the internal TPS monitor check for 3.3V passes. After the test passes, there will be a 10 ms delay before RESETZ may be de-asserted. This means there will be approximately 20 ms delay from the time the 3.3V enable is valid to the time RESETZ is de-asserted.

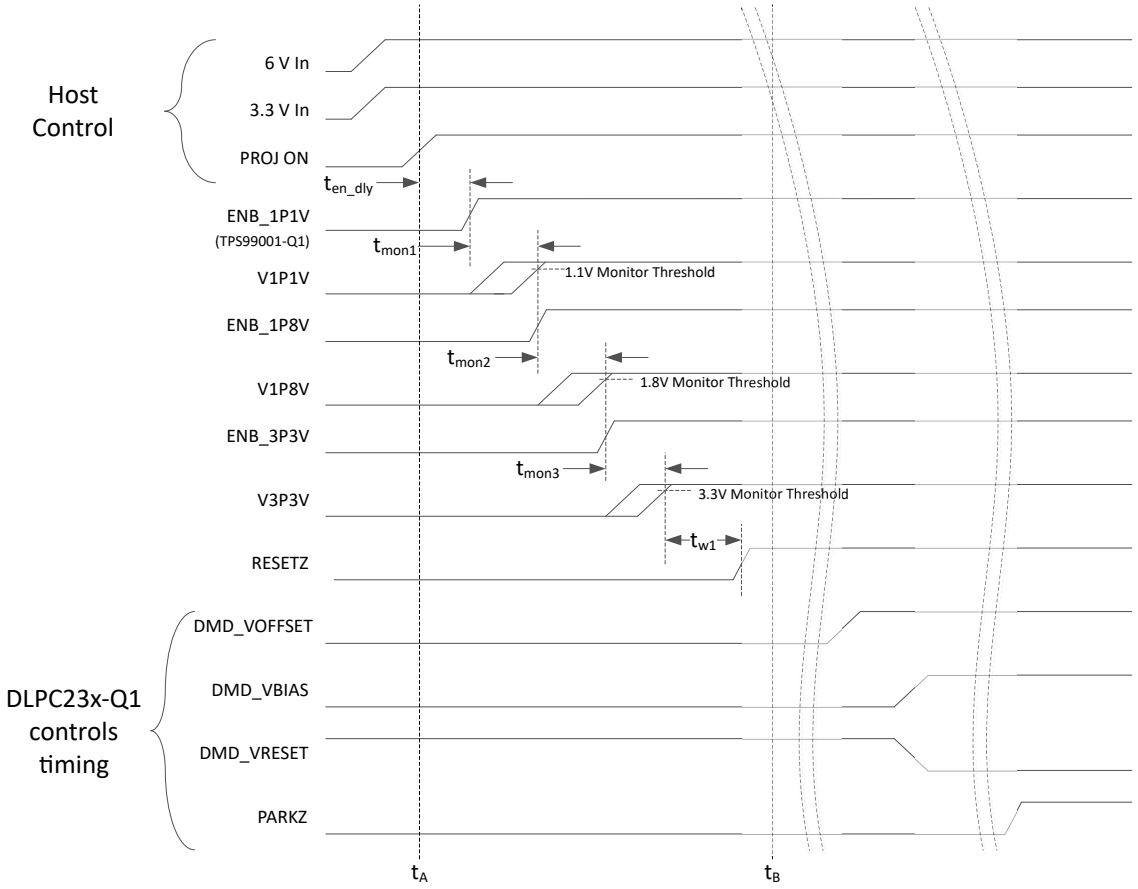


图 5-1. Power Up Timing

5.10 Power-Down Timing Requirements

See (1)

			MIN	MAX	UNIT
t_{vhold1}	Host voltage hold time after VMAIN minimum threshold reached. $t_{mon4}(max) + t_{park}(max) + t_{w2}(max)$	VMAIN threshold to 6V and 3.3V power loss(2) (3)	900		µs
t_{vhold2}	Host voltage hold time after PROJ_ON deasserted. $t_{mon5}(max) + t_{park}(max) + t_{w2}(max)$	VMAIN threshold to 6V and 3.3V power loss.(2) (3)	1.78		ms
t_{mon4}	VMAIN monitoring time	Minimum voltage trip threshold to PARKZ falling edge	52	120	µs
t_{mon5}	PROJ_ON deassertion reaction time	Falling edge of PROJ_ON to PARKZ falling edge		1	ms
t_{park}	DMD Park time	PARKZ falling edge to start DMD_VOFFSET discharge		280	µs
$t_{discharge}$ (4)	DMD voltage rail discharge time	VOFFSET C_{out} = 1 µF VRESET C_{out} = 1 µF VBIAS C_{out} = 0.47 µF		260	µs
t_{w2}	DMD voltage disables to RESETZ deassertion	Start of DMD voltage rail discharge to RESETZ falling edge		500	µs

(1) There are two methods for initiating the power-down sequence:
   a. VMAIN voltage decreases below its minimum threshold. This is typical if the TPS99001-Q1 is expected to initiate the power-down sequence when the main power is removed from the system. Note that the 6V and 3.3V input rails must remain within the operating range for a specified period of time after the power-down sequence begins.
   b. PROJ_ON low. This allows a host controller to initiate power down through a digital input to the TPS99001-Q1.

(2) 6V input rails include DRVR_PWR, VIN_DRST, VIN_LDOT_5V, VIN_LDOA_3P3V, VIN_LDOT3P3V.

(3) 3.3V input rails include VDD_IO, DVDD, AVDD.

(4) The DMD specifies a maximum absolute voltage difference between VBIAS and VOFFSET. To remain below this maximum voltage difference, VBIAS must discharge faster than VOFFSET. This is accomplished by using a smaller C_{out} capacitance for VBIAS to allow it to discharge quicker than VOFFSET.

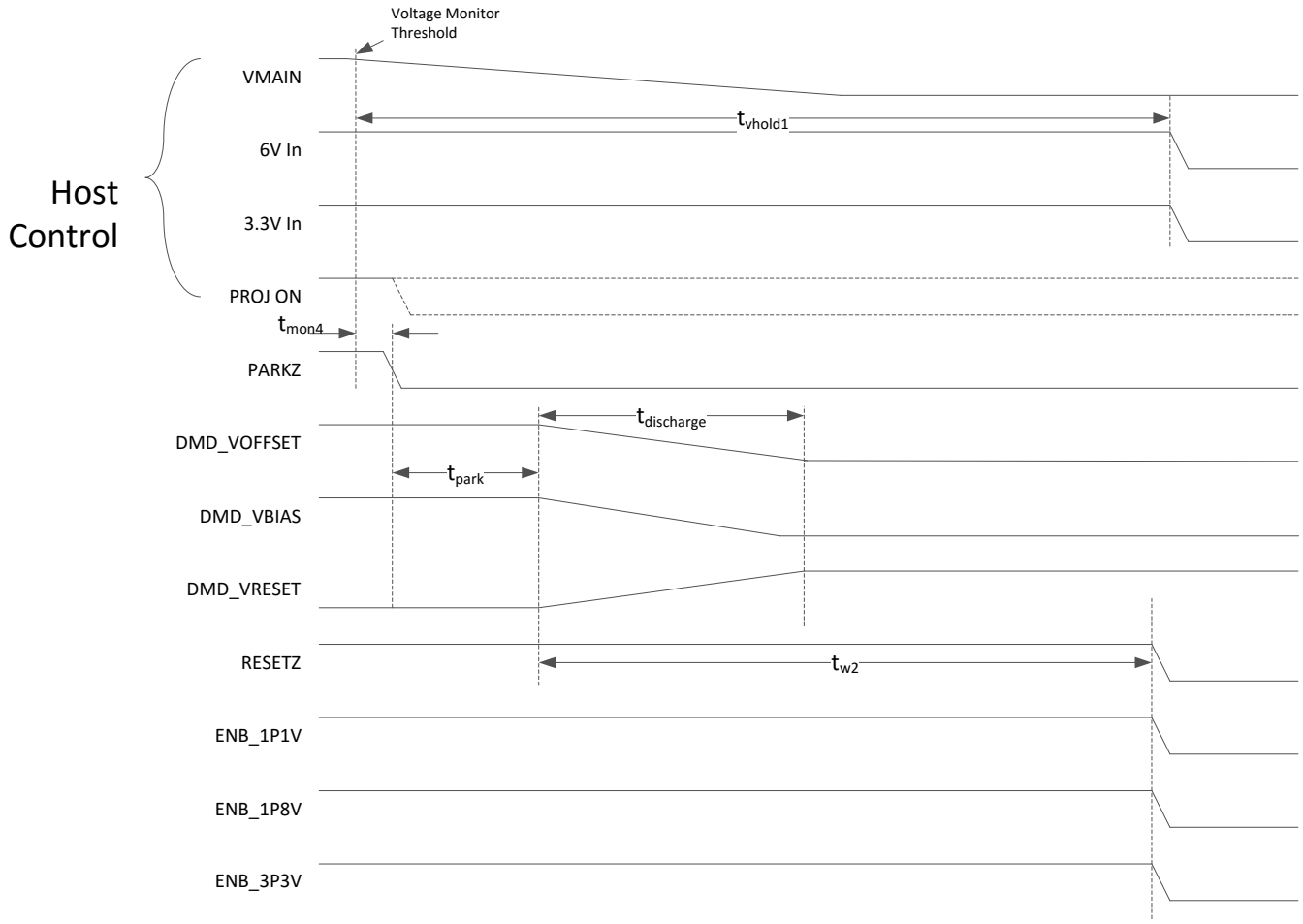


图 5-2. Power Down Timing—VMAIN Trigger

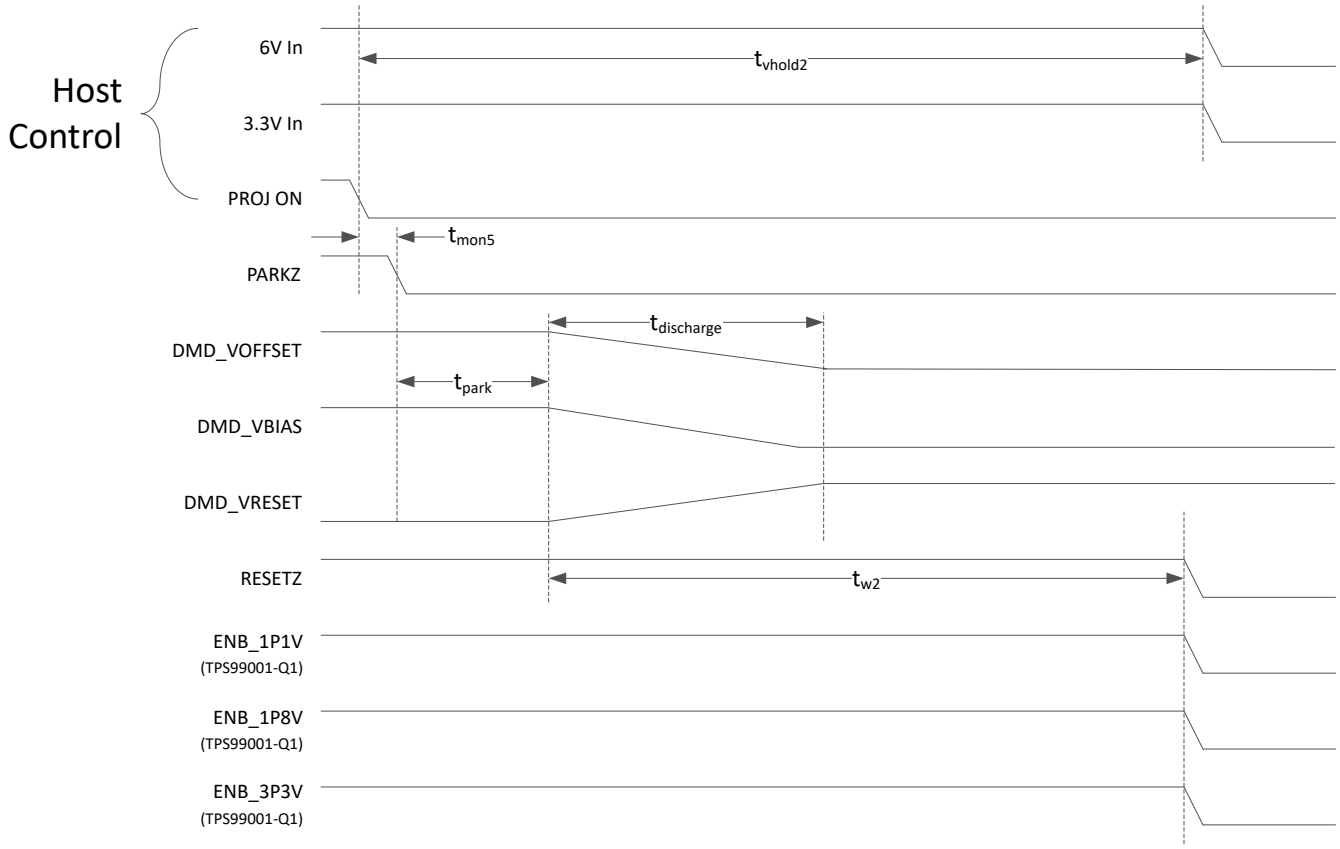


图 5-3. Power Down Timing—PROJ_ON Trigger

5.11 Timing Requirements—Sequencer Clock

		MIN	NOM	MAX	UNIT
f_{SEQ_CLK}	SEQ_CLK Frequency		30.00		MHz
t_{JPP}	SEQ_CLK Jitter (peak to peak)	– 3%		3%	
f_{SS}	SEQ_CLK allowable spread spectrum	– 2%		0%	
f_{SSMOD}	SEQ_CLK Spread Spectrum Modulation Frequency	25		100	kHz
$f_{SSSTEPS}$	SEQ_CLK Spread Spectrum Modulation Frequency Steps		50		steps

5.12 Timing Requirements—Host and Diagnostic Port SPI Interface

		MIN	NOM	MAX	UNIT
$t_{SPICPER}$	SPI CLK Cycle Time	31	33		ns
$t_{SPICHIGH}$	SPI CLK High Time	10			ns
$t_{SPICLOW}$	SPI CLK Low Time	10			ns
$t_{SPIDOUT}$	CLK Falling to DOUT	0		15	ns
$t_{SSSETUP}$	SPI SS_Z to CLK Rising Setup Time	5			ns
t_{SSHOLD}	SPI CLK Rising to SS_Z Hold Time	5			ns
$t_{DINSETUP}$	SPI DIN to CLK Rising Setup Time	5			ns
$t_{DINHOLD}$	SPI CLK Rising to DIN Hold Time	5			ns

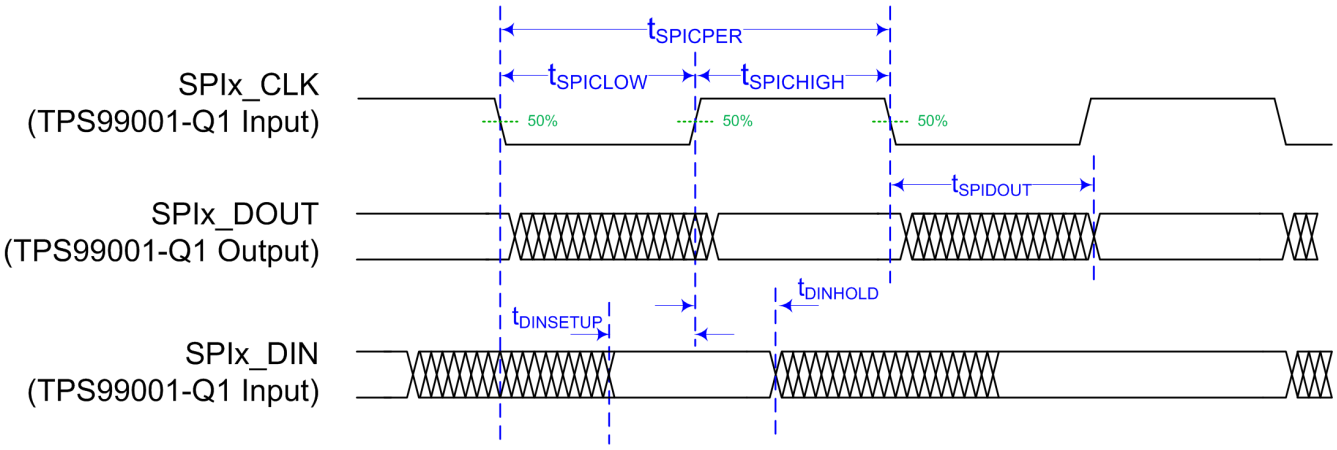


图 5-4. DLPC23x-Q1 Diagnostic Interface Timing

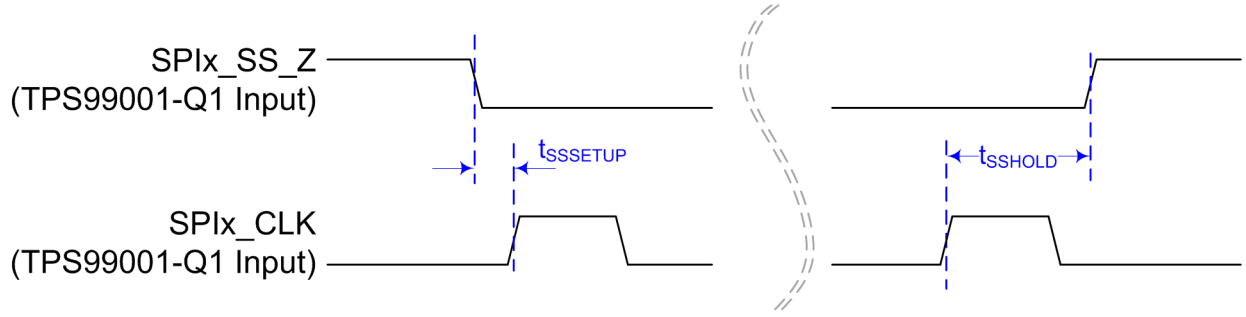


图 5-5. Chip Select Setup and Hold Timing

5.13 Timing Requirements—ADC Interface

		MIN	NOM	MAX	UNIT
$t_{ADCDINSETUP}$	ADC DIN to CLK Rising Setup Time	5			ns
$t_{ADCDINHOLD}$	ADC CLK Rising to DIN Hold Time	5			ns
$t_{ADCDOUT}$	CLK Rising to DOUT	0		15	ns

5.14 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL CLOCK						
f_{OSC}	Internal Oscillator Frequency		1.76	2	2.24	MHz

6 Detailed Description

6.1 Overview

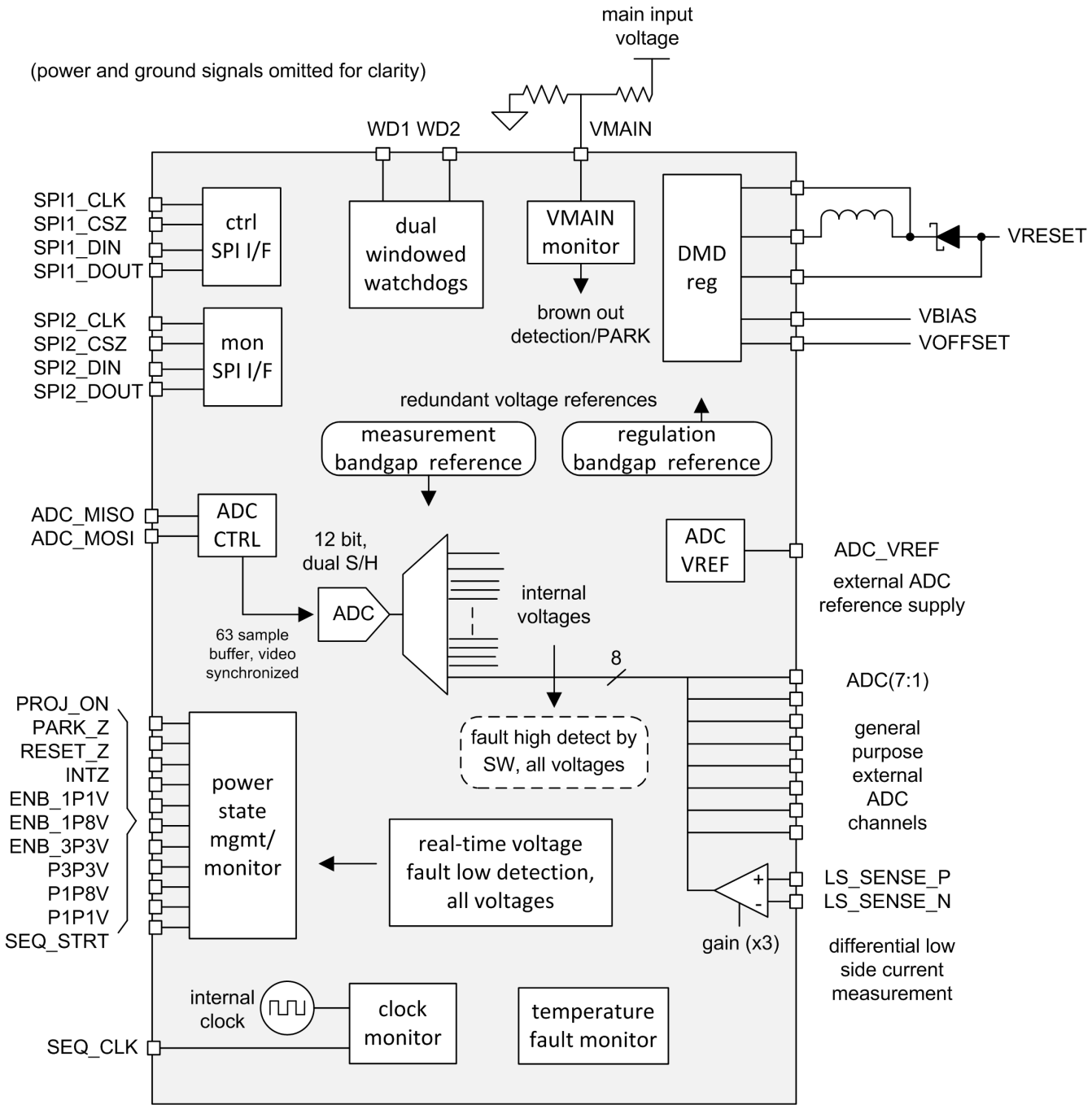
The TPS99001-Q1 is an integral component of the DLP553x-Q1 and DLP462x-Q1 chipset, which also includes the DLPC23x-Q1 DMD display controller. The TPS99001-Q1 provides a high-voltage, high-precision, three-rail regulator to cost-effectively create DMD mirror control voltages (16V, 8.5V, –10V). A complete system power monitor and DMD mirror parking solution is included to increase system robustness and reduce cost. In addition, the TPS99001-Q1 includes numerous system monitoring and diagnostic features, such as configurable ADCs and watchdogs.

An integrated 12-bit ADC provides useful information about the operating condition of the system. Several external ADC channels are included for general usage (LED temperature measurement, and so on). One of the external ADC channels includes a differential input amplifier and is dedicated to LED current measurement. The DLPC23x-Q1 and TPS99001-Q1 ADC control blocks support up to 63 samples per video frame, with precise hardware alignment of samples to the DMD sequence timeline.

Two SPI buses are included. The first bus is intended for command and control, and the second is a read-only bus for optional redundant system condition monitoring. The SPI ports include support for byte-level parity checking.

Two windowed watchdog circuits are included to provide validation of DLPC23x-Q1 microprocessor operation and monitoring of DMD sequencer activity. The TPS99001-Q1 also includes on-die temperature threshold monitoring and a monitor circuit to validate the external clock ratio (of the SEQ_CLK) against an internal oscillator.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog to Digital Converter

The TPS99001-Q1 includes a 12-bit analog to digital converter block with a 32:1 input mux and dual sample-and-hold circuits. It also includes a custom high speed serial control interface which when used in tandem with the DLPC23x-Q1 provides up to 63 DMD sequence-aligned samples per frame, with hardware-based sample timing and shadow-latched results. The hardware sample timing and shadow latch relieves the DLPC23x-Q1 processor from ADC timing tasks, freeing up processor resources for other uses.

图 6-1 illustrates the structure of the ADC controller blocks .

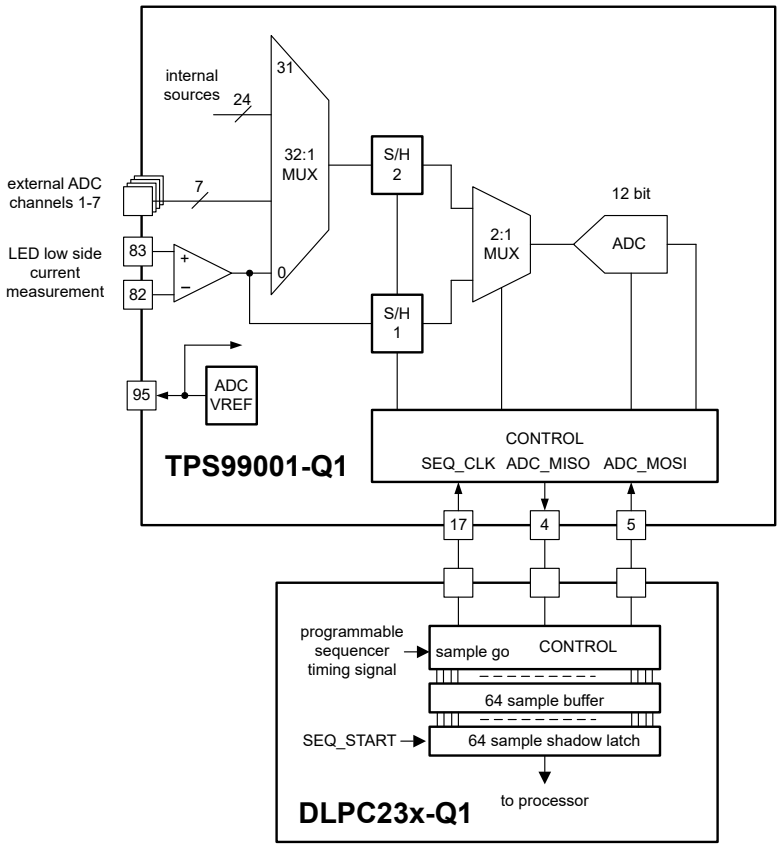


图 6-1. ADC Subsystem Block Diagram

The ADC block contains a dedicated channel reserved for differential low-side LED current measurements. Two sample-and-hold circuits are included to support paired LED current/voltage measurements. An additional seven external ADC channels are supported. The remaining 24 multiplexer inputs enable measurement of internal TPS99001-Q1 operating parameters.

备注

When performing paired samples, they are sampled simultaneously, but converted sequentially, so the conversion time doubles.

The DLPC23x-Q1 contains a custom ADC control block that supports up to 63 ADC samples per frame. The samples are aligned with DMD sequencer activity, configurable through system configuration tools. This alignment makes measurement of specific light pulses (LED current and voltage) within a sequence possible, with precise repeatability from frame to frame. Up to 63 samples per frame are supported. The 63 sample buffer includes a shadow latch that updates each frame. This latched output is held constant for a complete frame time, allowing time for the DLPC23x-Q1 to collect and process the information.

A reference voltage output is also included in the ADC block. This provides a low current voltage reference which matches the reference used by the ADC for conversion. This external reference can be used to bias thermistor voltage dividers, providing greater accuracy than would be possible using a mix of external and internal references. Regardless of whether the reference voltage is used, a 0.1 µF capacitor should be connected from this pin to ground.

备注

Current supply is limited. Loads which exceed the specified current maximum rating on ADC_VREF output may result in unpredictable ADC behavior.

6.3.1.1 Analog to Digital Converter Input Table

表 6-1. Analog to Digital Converter Input Table

PARAMETER		INTERNAL OR EXTERNAL	TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
Channel 0, Gain	Low side sense amp	External	Gain set to 24x	22.56	24	25.44	V/V
Channel 0, Gain	Low side sense amp	External	Gain set to 12x	11.28	12	12.72	V/V
Channel 0, Gain	Low side sense amp	External	Gain set to 9x	8.46	9	9.54	V/V
Channel 1, Gain	ADC_IN1_PAD (LED_ANODE)	External		0.980	1.000	1.020	V/V
Channel 2, Gain	ADC_IN2_PAD (VLED)	External		0.980	1.000	1.020	V/V
Channel 3, Gain	ADC_IN3_PAD	External		0.980	1.000	1.020	V/V
Channel 4, Gain	ADC_IN4_PAD	External		0.980	1.000	1.020	V/V
Channel 5, Gain	ADC_IN5_PAD (R_LED_THERM)	External		0.980	1.000	1.020	V/V
Channel 6, Gain	ADC_IN6_PAD (G_LED_THERM)	External		0.980	1.000	1.020	V/V
Channel 7, Gain	ADC_IN7_PAD (B_LED_THERM)	External		0.980	1.000	1.020	V/V
Channel 8, Gain	VBIAS	Internal		0.0596	0.0621	0.0646	V/V
Channel 9, Gain	VOFFSET	Internal		0.1112	0.117	0.1218	V/V
Channel 10, Gain	VRESET	Internal		–0.1978	–0.190	–0.1822	V/V
Channel 10, Offset	VRESET	Internal		–1.217	–1.1935	–1.169	V
Channel 11, Gain	VMAIN	Internal		0.52546	0.559	0.59254	V/V
Channel 12, Gain	DVDD	Internal		0.31302	0.333	0.35298	V/V
Channel 13, Gain	V1.1	Internal		0.65706	0.699	0.74094	V/V
Channel 14, Gain	V1.8	Internal		0.40326	0.429	0.45474	V/V
Channel 15, Gain	V3.3	Internal		0.2209	0.235	0.2491	V/V
Channel 17, Gain	ext ADC VREF	Internal		0.49	0.5	0.51	V/V
Channel 18, Gain	Driver Power	Internal		0.20398	0.217	0.23002	V/V
Channel 19, Gain	Die Temp1	Internal		0.490	0.500	0.510	V/V
Channel 20, Gain	Die Temp2	Internal		0.490	0.500	0.510	V/V
Channel 28, Gain	Channel not used	Internal					
Channel 29, Gain	Main Bandgap, 0.5V	Internal		0.980	1.000	1.020	V/V

(1) The conversionformula is (X + Offset) × Gain. X is the input voltage. Offset is 0V unless specified above.

6.3.2 Power Sequencing and Monitoring

The TPS99001-Q1 is specifically designed to perform correct power-up and power-down sequencing to ensure long term reliable operation of the DMD. The high voltage DMD mirror supplies require special power sequencing order, and restrictions on voltage differences between the power rails (VRESET, VBIAS, and VOFFSET) throughout power up, power down, and normal operation. The TPS99001-Q1 handles these requirements for the system designer.

6.3.2.1 Power Monitoring

Main asynchronous digital logic reset (DVDD_RSTZ) – Monitor of the main power of the 3.3V power supply input to the TPS99001-Q1. This monitor output is used as an asynchronous reset for all of the digital logic inside TPS99001-Q1.

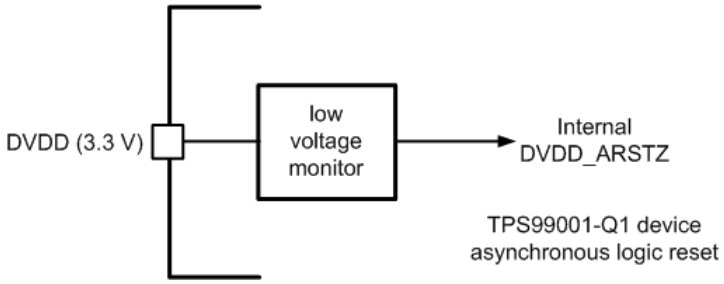


图 6-2. Internal DVDD Monitor

The PROJ_ON pin is the main on/off switch for the DLP subsystem. *1* is ON, *0* is OFF. Once DVDD_ARSTZ is released, TPS99001-Q1 will begin sampling the PROJ_ON pin. If it is low, the system stays in the OFF state. If it goes high, TPS99001-Q1 begins to progress through the power-on process.

The TPS99001-Q1 includes a VMAIN *brown out* monitor function. A voltage monitor observes the voltage on the VMAIN input pin, as shown in 图 6-3. The Zener may be necessary for overvoltage protection of the pin, in case the voltage being monitored has the potential to go high, such as a battery input.

Either PROJ_ON or VMAIN may be used to turn the system on and off, and doing so will remove power to the DLPC23x-Q1. For fast control of turning the display on and off without removing power to the DLPC23x-Q1, change the operating mode of the DLPC23x-Q1 embedded software between 'Standby' and 'Display'.

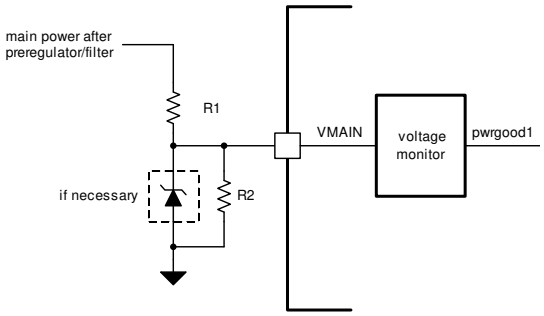


图 6-3. VMAIN *Brown Out* Monitor

This monitor is used to provide the DLP subsystem with an early warning that power to the unit is going away. The system will park the DMD mirrors and proceed to a ready-for-power-off state if the VMAIN input voltage falls below a fixed threshold. External resistors should be used to divide the input power rail. Once a VMAIN brownout occurs, the main power rails to the TPS99001-Q1 must remain within their operating ranges until the TPS99001-Q1 power-down is complete.

The main power rails to the chipset (6V, 3.3V, 1.8V, and 1.1V) are monitored with real-time power monitors as well. Each of these monitors is logically 'OR'ed together to produce the *pwrgood2* signal in 图 6-4.

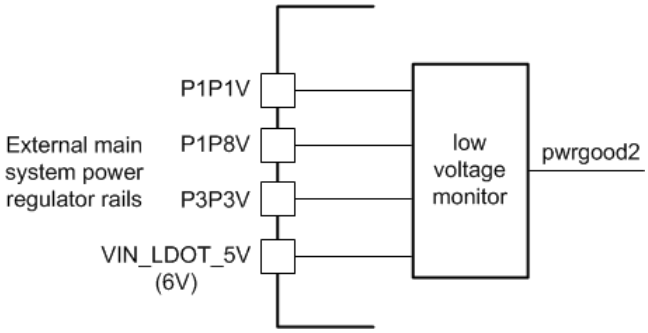


图 6-4. Real-Time Power Rail Monitors

Additionally, all power within the TPS99001-Q1 can be monitored by the ADC function. DLPC23x-Q1 software configures the ADC block to collect all voltage information in the system each frame. Any gross out of specification issues are captured and reported as system errors in the DLPC23x-Q1 system status.

6.3.3 DMD Mirror Voltage Regulator

The DMD mirror voltage regulator generates three high-voltage supply rails: DMD_VRESET, DMD_VBIAS, and DMD_VOFFSET. The DMD regulator uses a switching regulator where the inductor is time-shared between all three supplies. The inductor is charged up to a certain current level and then discharged into one of the three supplies. In cases where a supply does not need additional charge, the time slot normally allocated to that supply is skipped and the supplies requiring more charge receive all of the charging time.

For proper operation, specific bulk capacitance values are required for each supply rail. Refer to *Electrical Characteristics—Temperature and Voltage Monitors* for recommended values for the capacitors. The regulator contains active power down/discharge circuits. To meet timing requirements, total capacitance (actual capacitance, not the nominal) must not exceed these levels by substantial amounts, as defined in *Electrical Characteristics—Temperature and Voltage Monitors*. Power-down timing should be verified in each specific system design. Too low of a total capacitance will result in excessive ripple on the supply rails which may impact DMD mirror dynamic behavior. Care should be taken to use capacitors that maintain the recommended minimum capacitance over the expected operating device temperature range. Large-size packages are required here that do not lose so much capacitance at high voltages.

Although the average current drawn by the DMD on these supplies is small (10s of mA worst case), the peak currents can be several amps over 10s of nano-seconds. To supply this peak current, the use of small-value, high-frequency decoupling capacitors should be included as close as practical to the DMD power input pins.

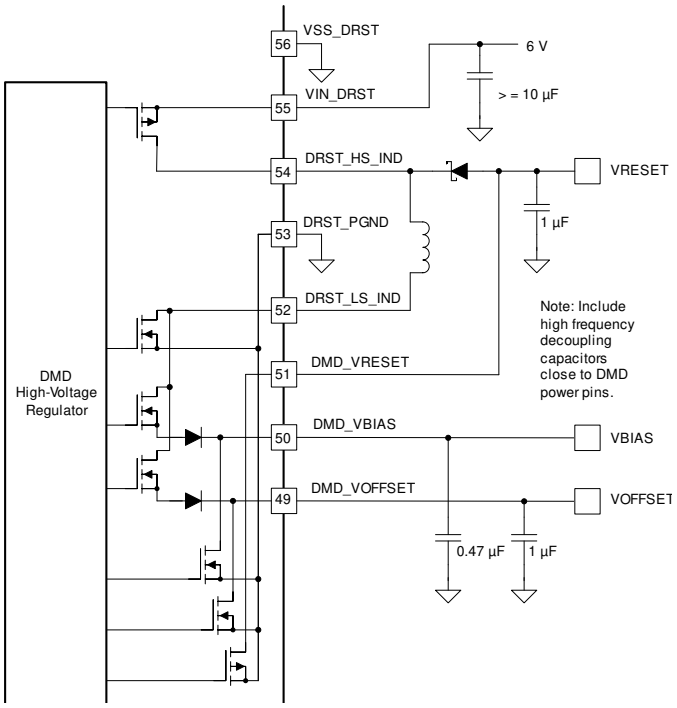


图 6-5. DMD Voltage Regulator Circuit

6.3.4 Low Dropout Regulators

The TPS99001-Q1 includes three low drop out regulators, dedicated to specific internal functions:

- A 5V output regulator for internal analog circuits (VIN_LDOT_5V input, VLDOT_5V output)
- A 3.3V output regulator for internal analog (VIN_LDOT_3P3V input, VLDOT_3P3V output)

- A 3.3V output regulator dedicated to the ADC block (VIN_LDOA_3P3 input, VLDOA_3P3 output)

The positive output LDO regulators are all designed to operate from the same nominal 6V input as is needed by the DMD mirror voltage regulator, VIN_DRST. However, care must be taken to isolate the sensitive analog circuit power supply inputs from switching noise, through dedicated sub-planes and supply filtering techniques.

6.3.5 System Monitoring Features

6.3.5.1 Windowed Watchdog Circuits

The TPS99001-Q1 contains two windowed watchdog circuits that can be used to detect malfunctions within the DLPC23x-Q1.

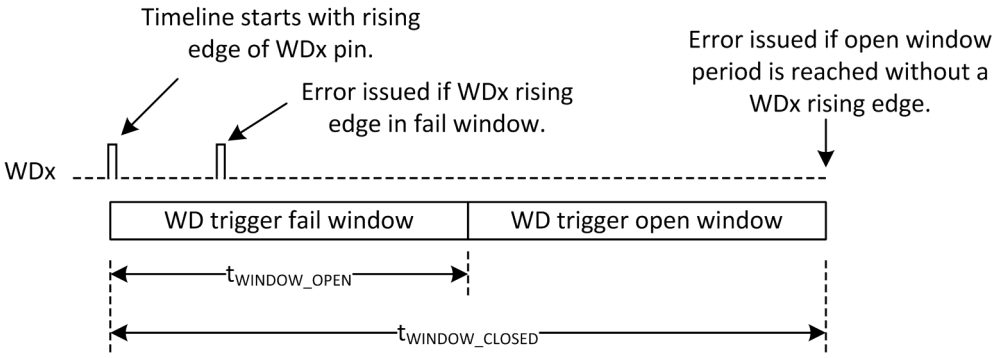


图 6-6. Windowed Watchdog Function

The DLPC23x-Q1 software uses both watchdog circuits. Watchdog #1 (WD1) monitors the internal microprocessor of the DLPC23x-Q1 through a wire connection to a dedicated GPIO line from DLPC23x-Q1. Watchdog #2 (WD2) is used to monitor the DLPC23x-Q1 sequencer operation (through monitoring of the SEQ_STRT pin, wired to WD2 input).

When this function is enabled, two registers control the timing of the opening and closing of a watchdog trigger window. Process is initiated by a rising edge on the respective WDx pin. If another rising edge occurs before the WD trigger window opens, a watchdog error is issued. If the end of the open window period is reached without receiving a rising edge on WDx, an error is issued. The process restarts any time a WDx rising edge is received. The two watchdogs are independent.

6.3.5.2 Die Temperature Monitors

The TPS99001-Q1 contains two on-chip die temperature monitors, for reduncy purposes, to monitor the internal temperature of the TPS99001-Q1. Each monitor has an output that indicates whether the die temperature has exceeded one of two thresholds. One monitors a warning threshold, and the other monitors an over-temperature error threshold. If the warning threshold is exceeded, a processor interrupt may be generated. If the over-temperature error threshold is exceeded during operation, the TPS99001-Q1 will initiate an emergency shutdown procedure and then wait for a toggle of the PROJ_ON pin to initiate a system restart while operating in a low power state. The system does not proceed through the power-on initialization steps unless the on-die temperature is below the warning threshold. The status of these temperature monitor output bits is available over the SPI buses as long as DVDD and VDD_IO power supplies are up and stable.

6.3.5.3 External Clock Ratio Monitor

The TPS99001-Q1 operates from two primary clock sources: an internal low frequency oscillator (2 MHz, used for system initialization and other maintenance purposes), and an external high speed (30 MHz) clock, SEQ_CLK, used for most timing critical applications, such as the ADC. The TPS99001-Q1 includes a function that reports the ratio of this internal vs. external clock. This ratio is available over the SPI bus. The DLPC23x-Q1 can check this ratio and compare to expected value. If the ratio is incorrect, there is a possibility the DLPC23x-Q1 oscillator may have locked to an incorrect harmonic, or some other fault condition has occurred.

6.3.6 Communication Ports

6.3.6.1 Serial Peripheral Interface (SPI)

The TPS99001-Q1 provides two four-wire SPI ports that support transfers up to 30MHz clock rates. The primary port (SPI1) supports register reads and writes, and serves as the primary set up and control interface for the device. The DLPC23x-Q1 is the primary of SPI1 to control the TPS99001-Q1 during system operation. A secondary read-only four wire SPI port (SPI2) is available to provide status information to an optional second microcontroller in the system.

For both ports, the SPIx_SS_Z serves as the active low chip select for the SPI port. A SPI frame is initiated by SPIx_SS_Z pin going low, and is completed when SPIx_SS_Z pin is driven high.

The secondary SPI port serves as a read-only system monitor port. All registers in the address space are read accessible over this port. The protocol is effectively the same as the main port except for being read-only. Note that data is clocked in on the rising edge of the SPI2_CLK.

When using this port, one must always transmit the full transaction packet. Failure to do so may result in corruption of data.

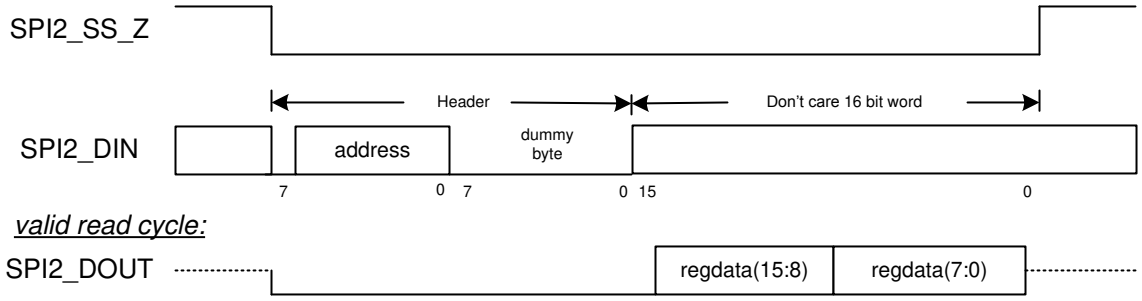


图 6-7. SPI Port 2 Protocol (Read Only)

6.4 Device Functional Modes

The following diagram in 图 6-8 illustrates the functional operating modes of the TPS99001-Q1.

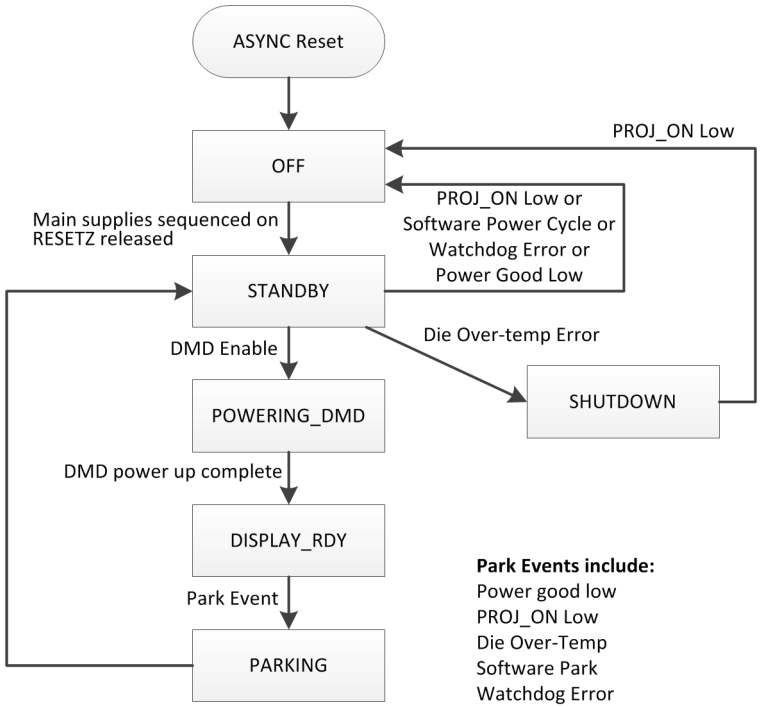


图 6-8. Top Level System States

6.4.1 OFF

The asynchronous internal reset of the device places system in this state. All supplies (DMD supplies, 1.1 V, 1.8 V, 3.3 V) are asynchronously disabled and RESETZ output to DLPC23x-Q1 is held low. Once the internal reset is released, communication over SPI2 is supported.

Exit from OFF state progresses to the STANDBY state. To exit OFF state, the following must all be true:

- VMAIN input monitor must show good status.
- PROJ_ON (projector on) input pin must be high.
- The die temperature warning must indicate the die temperature is below the warning threshold. Upon exit of OFF state and before entry to STANDBY, the external 1.1 V, 1.8 V, and 3.3 V supplies are powered on in sequence – first 1.1 V, then 1.8 V, then 3.3 V.

Internal monitors of 1.1 V, 1.8 V, and 3.3 V (and 6 V input on VIN_LDOT_5V) will hold off progression to STANDBY until all 4 rails are in operational range. After power is good, RESETZ output signal is held low for a specific period to ensure a proper reset cycle for the DLPC23x-Q1, and then it is released to transition to STANDBY.

6.4.2 STANDBY

Upon entry to STANDBY state, RESETZ is set high and DLPC23x-Q1 begins its boot process.

Exit options from STANDBY state include:

- A die over temp error sends system to SHUTDOWN state. An over temperature error in the STANDBY state means something is wrong with the system.
- PROJ_ON low sends to OFF state.
- Software commanded power cycle. System proceeds to OFF state.
- If either watchdog timers are enabled by software and an error occurs, system proceeds to OFF state.
- If power unexpectedly goes bad, system proceeds to OFF state.
- DLPC23x-Q1 software begins to enable DMD voltages. Sends to POWERING_DMD state. This is the first step in DMD voltage enabling process.

During the STANDBY phase, the DLPC23x-Q1 software performs DMD and DLPC23x-Q1 sequencer configuration steps. The software is in charge of DMD voltage enable timing, interleaving necessary DMD configuration register writes, and DLPC23x-Q1 ASIC block configuration steps. After the DLPC23x-Q1 software begins enabling DMD voltages, the TPS99001-Q1 proceeds to POWERING_DMD state.

6.4.3 POWERING_DMD

Once the DLPC23x-Q1 software begins enabling DMD voltages when in STANDBY, the system enters POWERING_DMD state. In this state, the DLPC23x-Q1 software performs all steps needed to properly configure and power up the DMD safely.

Exiting from POWERING_DMD state, the DLPC23x-Q1 software confirms that DMD is powered up. This sends the TPS99001-Q1 to DISPLAY_RDY state. This is the last step in DMD voltage enabling process.

If a PROJ_ON low is received during power on, the TPS99001-Q1 will still complete the power on sequence.

6.4.4 DISPLAY_RDY

In the display ready state, the DLPC23x-Q1 may enable illumination at any time.

Once the DLPC23x-Q1 software enables illumination, the TPS99001-Q1 enters the DISPLAY state.

Exit conditions:

- A *DMD park* event has occurred including power not good, PROJ_ON low, die over temp error, software park initiated, or software power cycle initiated. These events send the TPS99001-Q1 to PARKING state.

6.4.5 PARKING

DMD parking is taking place. PARKZ output signal (to DLPC23x-Q1) is asserted low in this state. Timers count down time then the control for the DMD voltage regulators is disabled. Once the final hardware delay elapses, the next state is STANDBY.

6.4.6 SHUTDOWN

The shutdown state is entered only when a die over temperature condition is experienced. All switchable on chip activity is halted. The only exit conditions from this state are PROJ_ON low (*0*) or true power off. This state is readable via the 2nd diagnostic SPI port. All power supplies are disabled.

6.5 Register Maps

6.5.1 System Status Registers

ADDRESS	NAME	BITS	DESCRIPTION
Chip Revision ID, R-only, Reset Value 0000			
0x00	Unused	[15:8]	Unused
	Major	[7:4]	Major revision
	Minor	[3:0]	Minor revision
Status Set, R/W, Reset Value 0000			
0x01	PG Fault Status	[15]	Asserted when any bin in user register 38h is set
	VXPG Init	[13]	Power good timer for VOFS, VRST, or VBIAS expired
	Main SPI parity error	[12]	Parity error on a SPI1 port transaction occurred (command or write data) on previous command
	ADC block error	[11]	"OR" of all errors in ADC block. Refer to x0D to determine specific error.
	Checksum error 3	[10]	Checksum error in LED section
	Checksum error 2	[9]	Checksum error in light sensor conditioning section
	Checksum error 1	[8]	Checksum error in ADC sub-system section
	WD2	[7]	Watchdog #2 error
	WD1	[6]	Watchdog #1 error
	Top level state change	[5]	Indicates top level state machine has changed state. Can be used to indicate that the TPS99001-Q1 has exited DISPLAY state unexpectedly due to a random fault
	VXPG Fault	[3]	Set 1 by hardware if power good fault occurs for VOFS, VRST, or VBIAS
	DIE Over temp warning	[2]	Thermal conditions on chip have reached the warning level. If temperature continues to rise, system will reach die over temp error temperature and emergency actions will be taken by TPS99001-Q1
	DIE Over temp error	[1]	Thermal conditions on chip have reached the emergency/error. Emergency actions will be taken by TPS99001-Q1 to protect the system. This error bit is non-maskable for PARKZ output
	PROJ_ON_LOW	[0]	Projector ON input pin is low (produces a *1* on this status bit).

ADDRESS	NAME	BITS	DESCRIPTION
General Status 1, R-only, Reset Value 0000			
0x05	Clock ratio monitor	[15:12]	Mid-scale reading (1000 ± 1) indicate approximately 30-MHz external signal has been applied
	Open	[11:8]	Reserved
	Last Reset (2:0)	[7:5]	Root cause of last reset cycle, last pass through the *OFF* state. “000” – true power on cycle, internal reset set/release “001” – PROJ_ON went low “010” – watchdog timer 1 error “011” – watchdog timer 2 error “100” – die over temperature error “101” – SW power cycle command all others unused
	Top State (4:0)	[4:0]	Top level state machine current state 0x00 = SHUTDOWN 0x01 = Internal initialization 0x02 = OFF 0x03 = Internal initialization 0x04 = Initializing 1P1V 0x05 = Initializing 1P8V 0x06 = Initializing 3P3V 0x07 = De-assert RESETZ 0x08 = STANDBY 0x09 = VOFFSET enabled 0x0A = VBIAS enabled 0x0B = VRESET enabled 0x0C = DISPLAY READY 0x0D = DISPLAY ON 0x0E = Parking initialized 0x0F = VBIAS and VRESET disabled 0x10 = VOFFSET disabled 0x11 = DMD voltage discharge

6.5.2 ADC Control

ADDRESS	NAME	BITS	DESCRIPTION
ADC Block Status SET, Read, Reset Value 0000			
0x0D	Unused	[15:8]	Reserved
	AD3 Command Stop-bit Error	[7]	Indicates that a stop bit was missing
	ADC Timeline Error	[6]	Indicates that a new command was received while previous command was still in progress
	Command error	[5]	An error was detected on a serial bus command
	Parity error detected	[4]	A parity error in bit stream was detected
	Ch2 underflow	[3]	ADC conversion results presented in channel two register experienced an underflow
	Ch2 saturated	[2]	ADC conversion results presented in channel two register are saturated
	Ch1 underflow	[1]	ADC conversion results presented in channel one register experienced an underflow
	Ch1 saturated	[0]	ADC conversion results presented in channel one register are saturated

6.5.3 General Fault Status

ADDRESS	NAME	BITS	DESCRIPTION
General Fault Status, R-only, Reset Value 0000, Value of 1 indicates a Fault			
0x38	VBIAS Powergood Fault	[15]	VBIAS is below the minimum specified voltage
	VRST Powergood Fault	[14]	VRESET is below the minimum specified voltage
	VOFS Powergood Fault	[13]	VOFFSET is below the minimum specified voltage
	Powergood 1 Fault	[12]	VMAIN or AVDD rail is below the minimum specified voltage (Logical OR).
	Powergood 2 Fault	[10]	At least one of 1.1V, 1.8V, 3.3V, and 6V supplies is below the minimum specified voltage (Logical OR).
	ADC 3V LDO Powergood Fault	[9]	ADC 3V LDO is below the minimum specified voltage
	ADC 3V LDO Over Voltage Fault	[8]	ADC 3V LDO is above the maximum specified voltage
	3V LDO Powergood Fault	[7]	3V LDO is below the minimum specified voltage
	3V LDO Over Voltage Fault	[6]	3V LDO is above the maximum specified voltage
	LDO Over Voltage Fault	[5]	LDO is above the maximum specified voltage
	V3P3 Powergood Fault	[2]	3.3V is below the minimum specified voltage
	V1P8 Powergood Fault	[1]	1.8V is below the minimum specified voltage
	V1P1 Powergood Fault	[0]	1.1V is below the minimum specified voltage

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The DLP553x-Q1 and DLP462x-Q1 chipset is designed to support projection-based automotive applications such as high resolution headlights.

The DLP553x-Q1 chipset consists of three components—the DLP553x-Q1 (DMD), the DLPC23x-Q1, and the TPS99001-Q1. The DLP462x-Q1 chipset consists of three components—the DLP462x-Q1 (DMD), the DLPC23x-Q1, and the TPS99001-Q1. The DMD is a light modulator consisting of tiny mirrors used to form and project images. The DLPC23x-Q1 is a controller for the DMD; it formats incoming video and controls the timing of the DMD illumination sources and the DMD to display the incoming video. The TPS99001-Q1 is a management IC for the entire chipset. In conjunction, the DLPC23x-Q1 and the TPS99001-Q1 can also be used for system-level monitoring, diagnostics, and failure detection features.

7.2 Typical Applications

Pulldown resistors are required on the pins in the below table to avoid a floating input during the power-up and power-down conditions.

表 7-1. Pulldown Resistor Requirements

PIN	NAME	TYP
5	ADC_MOSI	10 kΩ
6	WD1	10 kΩ
16	SEQ_START	10 kΩ
17	SEQ_CLK	10 kΩ
27	SPI1_CLK	10 kΩ
30	SPI1_DIN	10 kΩ
31	SPI2_DIN	10 kΩ
34	SPI2_CLK	10 kΩ
49	DMD_VOFFSET(1)	56 kΩ
50	DMD_VBIAS(1)	110 kΩ
51	DMD_VRESET(1)	68 kΩ

(1) Resistor pulldowns are required to create a minimum load for DMD_VOFFSET, DMD_VBIAS, and DMD_VRESET. Each of these pulldowns should provide a load from 0.1mA to 1mA. If the -8V LDO is used, then the pull down for DMD_VRESET may be eliminated.

7.2.1 Headlight

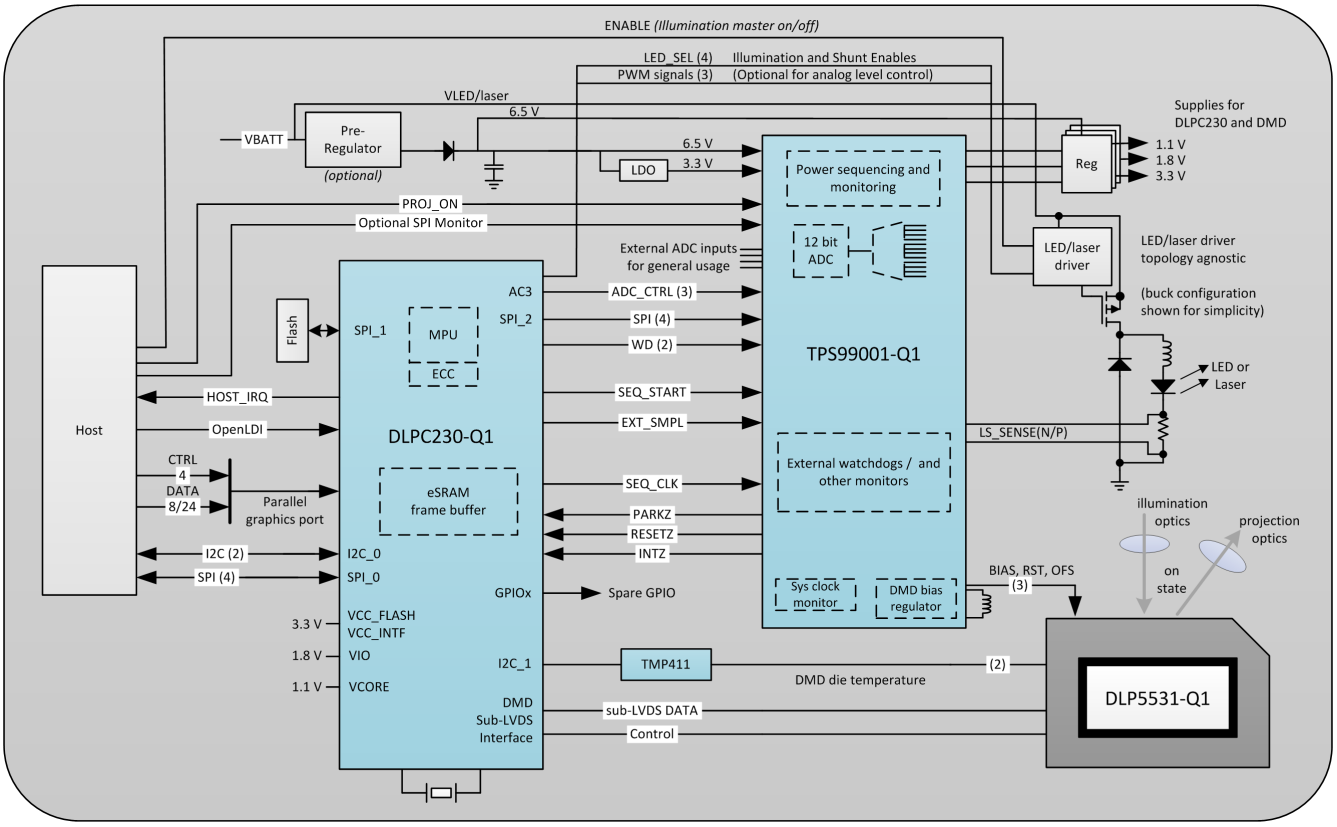


图 7-1. Headlight System Block Diagram

备注

The TPS99001-Q1 system management and illumination controller is part of the DLP553x-Q1 and DLP462x-Q1 chipset, which also includes the DLPC23x-Q1 DMD display controller.

7.2.1.1 Design Requirements

The DLPC23x-Q1 1 is a controller for the DMD and the light sources in headlight applications. It receives input video from the host and synchronizes DMD and light source timing in order to achieve the desired video. The DLPC23x-Q1 formats input video data that is displayed on the DMD. It synchronizes these video segments with light source timing in order to create video with grayscale shading.

The DLPC23x-Q1 receives inputs from a host processor in the vehicle. The host provides commands and input video data. R/W commands can be sent using either the I^2C bus or SPI bus. The bus that is not being used for R/W commands can be used as a read-only bus for diagnostic purposes. Input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The 24-bit bus can be limited to only 8-bits of data for single light source systems such as headlights. The SPI flash memory provides the embedded software for the DLPC23x-Q1’s ARM core, any calibration data, and default settings. The TPS99001-Q1 provides diagnostic and monitoring information to the DLPC23x-Q1 using an SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The TMP411 uses an I^2C interface to provide the DMD array temperature to the DLPC23x-Q1.

The outputs of the DLPC23x-Q1 are configuration and monitoring commands to the TPS99001-Q1, timing controls to the LED or laser driver, control signals to the DMD, and monitoring and diagnostics information to the host processor. The DLPC23x-Q1 communicates with the TPS99001-Q1 over an SPI bus. It uses this to configure the TPS99001-Q1 and to read monitoring and diagnostics information from the TPS99001-Q1. The

DLPC23x-Q1 sends drive-enable signals to the LED or laser driver, and synchronizes this with the DMD mirror timing. The control signals to the DMD are sent using a SubLVDS interface.

The TPS99001-Q1 is a highly integrated mixed-signal IC that controls DMD power and provides monitoring and diagnostics information for the headlight system. The power sequencing and monitoring blocks of the TPS99001-Q1 properly power up the DMD and provide accurate DMD voltage rails, and then monitor the system’s power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The TPS99001-Q1 also has several general-purpose ADCs that designers can use for system-level monitoring.

The TPS99001-Q1 receives inputs from the DLPC23x-Q1, the power rails it monitors, the host processor, and potentially several other ADC ports. The DLPC23x-Q1 sends configuration and control commands to the TPS99001-Q1 over an SPI bus and several other control signals. The TPS99001-Q1 includes watchdogs to monitor the DLPC23x-Q1 and ensure that it is operating as expected. The power rails are monitored by the TPS99001-Q1 to detect power failures or glitches and request a proper power down of the DMD in case of an error. The host processor can read diagnostics information from the TPS99001-Q1 using a dedicated SPI bus. Additionally, the host can request the image to be turned on or off using a PROJ_ON signal. Lastly, the TPS99001-Q1 has several general-purpose ADCs that can be used to implement system-level monitoring functions.

The outputs of the TPS99001-Q1 are diagnostic information and error alerts to the DLPC23x-Q1, and control signals to the LED or laser driver. The TPS99001-Q1 can output diagnostic information to the host and the DLPC23x-Q1 over two SPI busses. In case of critical system errors, such as power loss, it outputs signals to the DLPC23x-Q1 that trigger power down or reset sequences. It also has output signals that can be used to implement various LED or laser driver topologies.

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as an input (video data) and produces a mechanical output (mirror position). The electrical interface to the DMD is a SubLVDS interface with the DLPC23x-Q1. The mechanical output is the state of more than 1.3 million mirrors in the DMD array that can be tilted ±12°. In a projection system, the mirrors are used as pixels to display an image.

8 Power Supply Recommendations

The TPS99001-Q1 requires two power inputs and also provides several power outputs, as well as controlling additional external power supplies. The power supply architecture is explained in 节 8.3 .

8.1 TPS99001-Q1 Power Supply Architecture

- 6.5V
- 3.3V (LDO recommended)

8.2 TPS99001-Q1 Power Outputs

- DMD Required Voltages:
  - DMD_VOFFSET
  - DMD_VBIAS
  - DMD_VRESET
- Internally used LDOs. These are not designed to be used externally, but are listed here as they require external bypass capacitors:
  - 5V
  - 3.3V
  - 3.3V ADC

8.3 Power Supply Architecture

TI recommends the following power supply architecture:

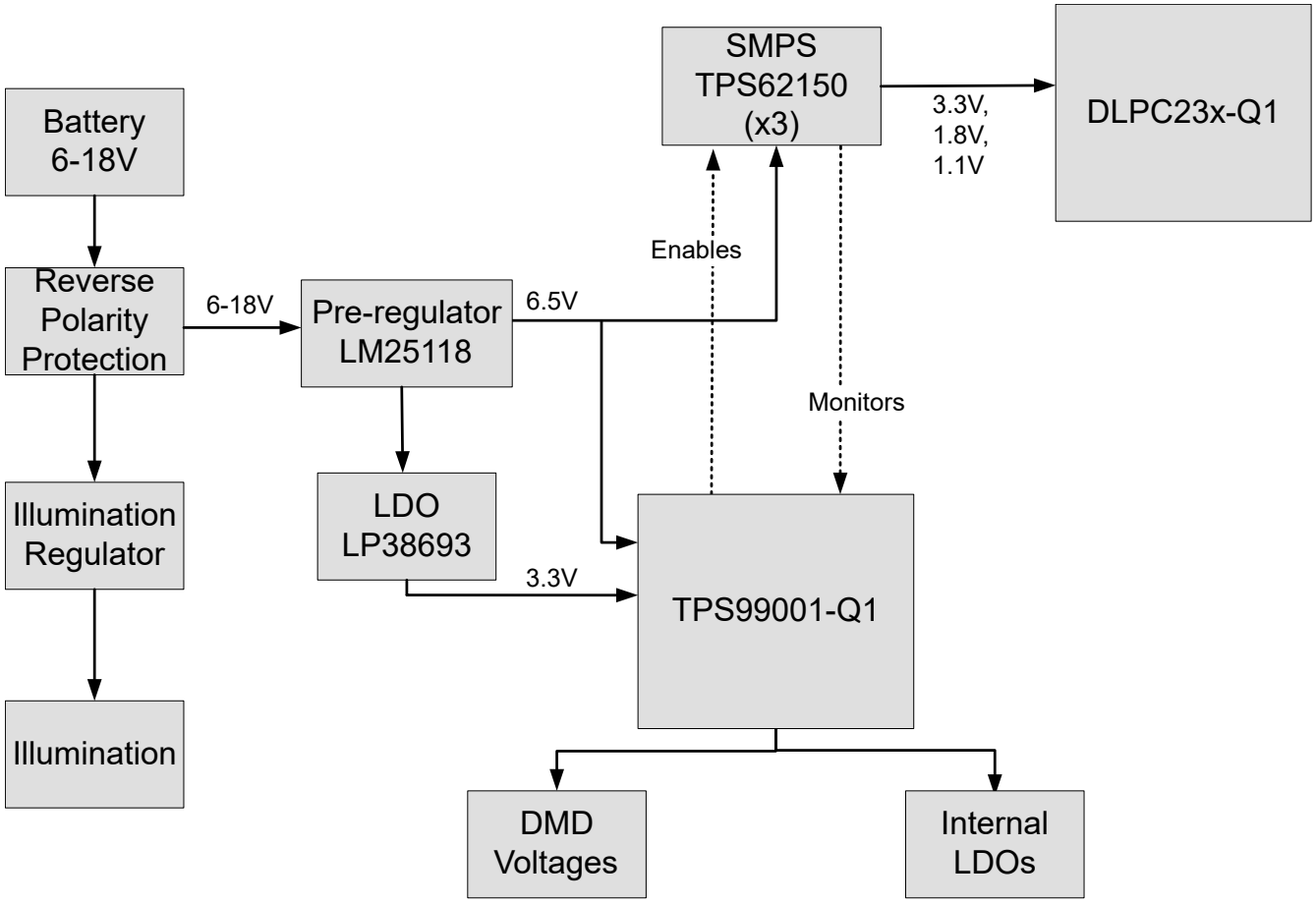


图 8-1. Headlight Power Supply Architecture

9 Layout

9.1 Layout Guidelines

The TPS99001-Q1 is both a power and precision analog IC. As such, care must be taken to the layout of certain signals and circuits within the system. Along with general layout best practices, pay attention to the following areas of detail, which are discussed in this document.

- Power/high current signals
- Sensitive analog signals
- High-speed digital signals
- High-power current loops
- Kelvin sensing connections
- Ground separation

9.1.1 Power/High Current Signals

The TPS99001-Q1 switches a relatively high amount of current via the switching regulator which generates the voltages used by the DMD.

The DMD regulator consists of the following pins of the TPS99001-Q1:

表 9-1. TPS99001-Q1 DMD Regulator Pins

PIN	NAME	PEAK BOARD CURRENT
49	DMD_VOFFSET	800mA
50	DMD_VBIAS	800mA
51	DMD_VRESET	800mA
52	DRST_LS_IND	800mA
53	DRST_PGND	800mA
54	DRST_HS_IND	800mA
55	VIN_DRST	800mA
56	VSS_DRST	800mA

The value of 800mA for these pins relates to the peak current through the inductor due to the nature of the switching regulator architecture. The DC for these paths will be closer to the load current drawn by the DMD.

In addition to these high current signals that are driven by the TPS99001-Q1, the LED driver electronics will likely have other circuits that handle the high currents required by the LEDs. These currents may be as high as 6A and therefore also requires special consideration by the layout engineer. As a guide for the PCB trace width requirements, the reader is referred to TI’s Application Note (SLUA366). The PCB trace widths used in TI’s design were:

表 9-2. PCB Trace Widths

SIGNAL GROUP	PCB TRACE WIDTH
DMD Regulator	10 mils

9.1.2 Sensitive Analog Signals

The following signals are analog inputs to TPS99001-Q1. Most of these analog inputs are DC levels and are somewhat insensitive to noise, but others are part of the real-time color control algorithm of the TPS99001-Q1 and therefore must be kept immune from noise injection from other signals. The list of analog input pins is as follows:

表 9-3. TPS99001-Q1 Analog Input Pins

PIN	NAME	SIGNAL TYPE
82	LS_SENSE_N	Real-time

表 9-3. TPS99001-Q1 Analog Input Pins（续）

PIN	NAME	SIGNAL TYPE
83	LS_SENSE_P	Real-time
85	ADC_IN1	Real-time
86	ADC_IN2	DC
88	ADC_IN3	DC
90	ADC_IN4	DC
92	ADC_IN5	DC
93	ADC_IN6	DC
94	ADC_IN7	DC
96	V3P3V	DC
97	V1P8V	DC
98	V1P1V	DC

9.1.3 High-Speed Digital Signals

The TPS99001-Q1 has three serial interfaces that transmit data into and out of the device. All of these interfaces have a maximum clock speed of 30MHz. To help prevent high levels of EMI emissions, these signals should be laid out with impedance-matched, low-inductance traces. In particular, the three clocks for these interfaces should be low inductance, and if a cable or a connector is used, the clock signal should be adjacent to the ground signal return.

表 9-4. SPI1 Interface from DLPC23x-Q1 to TPS99001-Q1

PIN	NAME	FUNCTION
27	SPI1_CLK	Clock (30MHz)
28	SPI1_SS_Z	Secondary Select
29	SPI1_DOUT	Data
30	SPI1_DIN	Data

表 9-5. SPI2 Interface from Customer MCU to TPS99001-Q1

PIN	NAME	FUNCTION
31	SPI2_DIN	Data
32	SPI2_DOUT	Data
33	SPI2_SS_Z	Secondary Select
34	SPI2_CLK	Clock (up to 30MHz)

表 9-6. ADC3 Interface from DLPC23x-Q1 to TPS99001-Q1

PIN	NAME	FUNCTION
4	ADC_MISO	Data
5	ADC_MOSI	Data
17	SEQ_CLK	Clock (30MHz)

To avoid crosstalk, a PCB trace spacing requirement is suggested, such as the “3 W rule” which specifies that if the trace width is 5 mils, then traces should be spaced out at least 15 mils from center to center. On TI’s PCB design, the typical trace spacing was 20 mils.

9.1.4 Kelvin Sensing Connections

There are many places in the system design where the current through a signal path is measured by using a sense resistor in series with the signal path. In these cases, the resistor should be connected by using a “Kelvin” connection, or a “Force-Sense” connection. This means that two connections are made to the

resistor that carry the high level of current, and two connections are made separately to measure the voltage across the resistor. This prevents the sense lines from being affected by the extra resistance of the copper traces, and makes the measurement more accurate. An example of the “Force-Sense” connection is shown in 图 9-1.

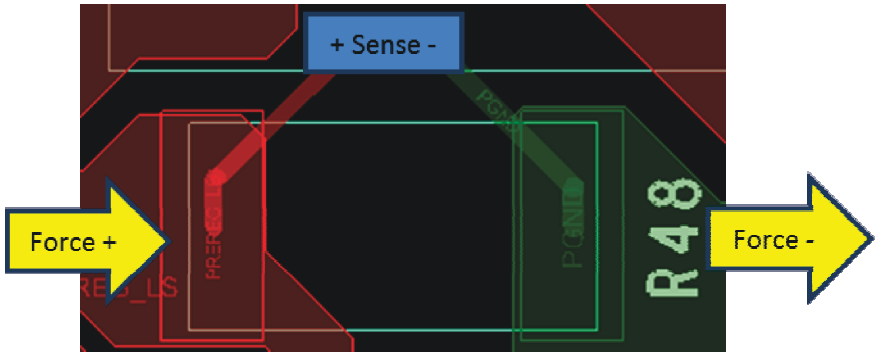


图 9-1. Kelvin Sensing Layout

The TPS99001-Q1 uses a sense resistor to measure the current delivered to the LEDs. These differential sense lines are the inputs to the part LS_SENSE_P and LS_SENSE_N. It is important to notice that although LS_SENSE_N may be electrically connected to ground by the netlist, this signal must be routed as a separate trace to prevent it from being affected by changes in the ground plane.

9.1.5 Ground Separation

Separated ground planes are good for isolating noise from different parts of the circuit to other. However, when designing with separate ground planes, one must be careful of how the signals are routed to avoid large inductive loops. If separate ground planes are used, TI recommends the following ground connections to the TPS99001-Q1. In addition, the grounds should be connected electrically by a via or a 0 Ω resistor. If a unified ground plane is used, the following can be used as a guideline for which groups of signals should be routed apart from other signals.

表 9-7. TPS99001-Q1 Ground Separation

PIN	NAME	GROUND
13, 35	VSS_IO	Digital
24	DVSS	Digital
25, 60, 75, 99	PBKG	Analog
48	VSS_DRVR	Power
53	DRST_PGND	Power
56	VSS_DRST	Power
66	GND_LDO	Analog
71, 72	VSS_TIA	Analog
78, 100	AVSS	Analog
81, 84, 87, 89, 91	VSSL_ADC	Analog
Thermal Pad	DAP	Analog

10 Device and Documentation Support

10.1 Device Support

10.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

10.4 Trademarks

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DLP® is a registered trademark of Texas Instruments.
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10.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Revision History

Changes from Revision A (January 2021) to Revision B (June 2024)	Page
• 将整个出版物中多个位置的 DMD 和控制器参考进行了归纳，以包括 TPS99001-Q1 系统管理控制器的所有可能组合。	1
• Footnote *(3)* and *(4)* added to Power-Up Timing Requirements Table explaining how to account for each internal TPS monitor test prior to RESETZ being de-asserted	16

Changes from Revision * (June 2019) to Revision A (January 2021)	Page
• 首次公开发布的数据表	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS9901TPZPQ1	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS9901TPZP
TPS9901TPZPQ1.A	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS9901TPZP
TPS9901TPZPRQ1	Active	Production	HTQFP (PZP) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS9901TPZP
TPS9901TPZPRQ1.A	Active	Production	HTQFP (PZP) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS9901TPZP
TPS9901TPZPRQ1.B	Active	Production	HTQFP (PZP) | 100	1000 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS9901TPZP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

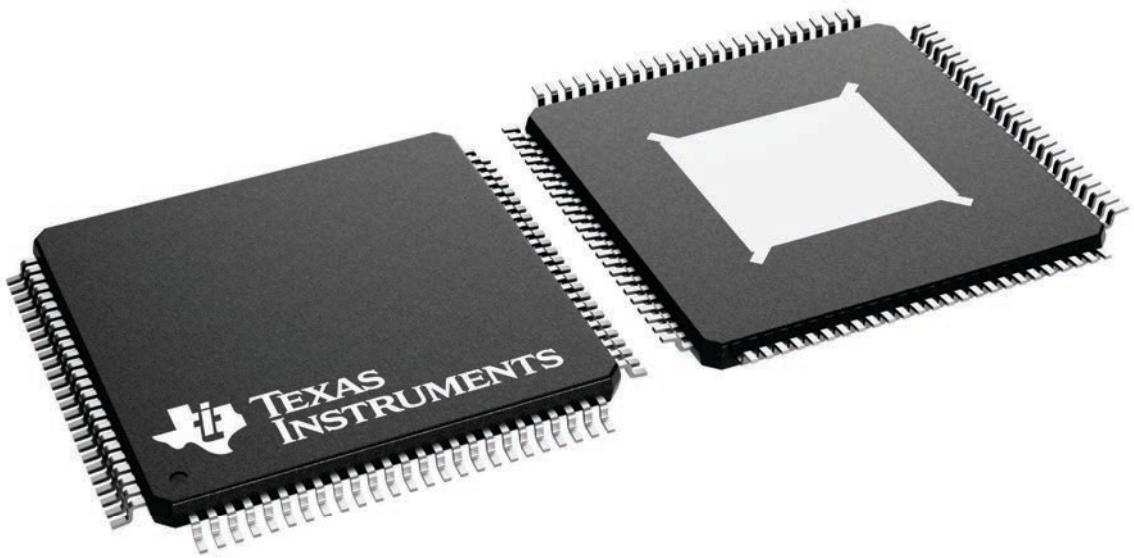
PZP 100

PowerPAD ™ TQFP - 1.2 mm max height

14 x 14 mm Pkg Body, 0.5 mm pitch
16 x 16 mm Pkg Area

PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



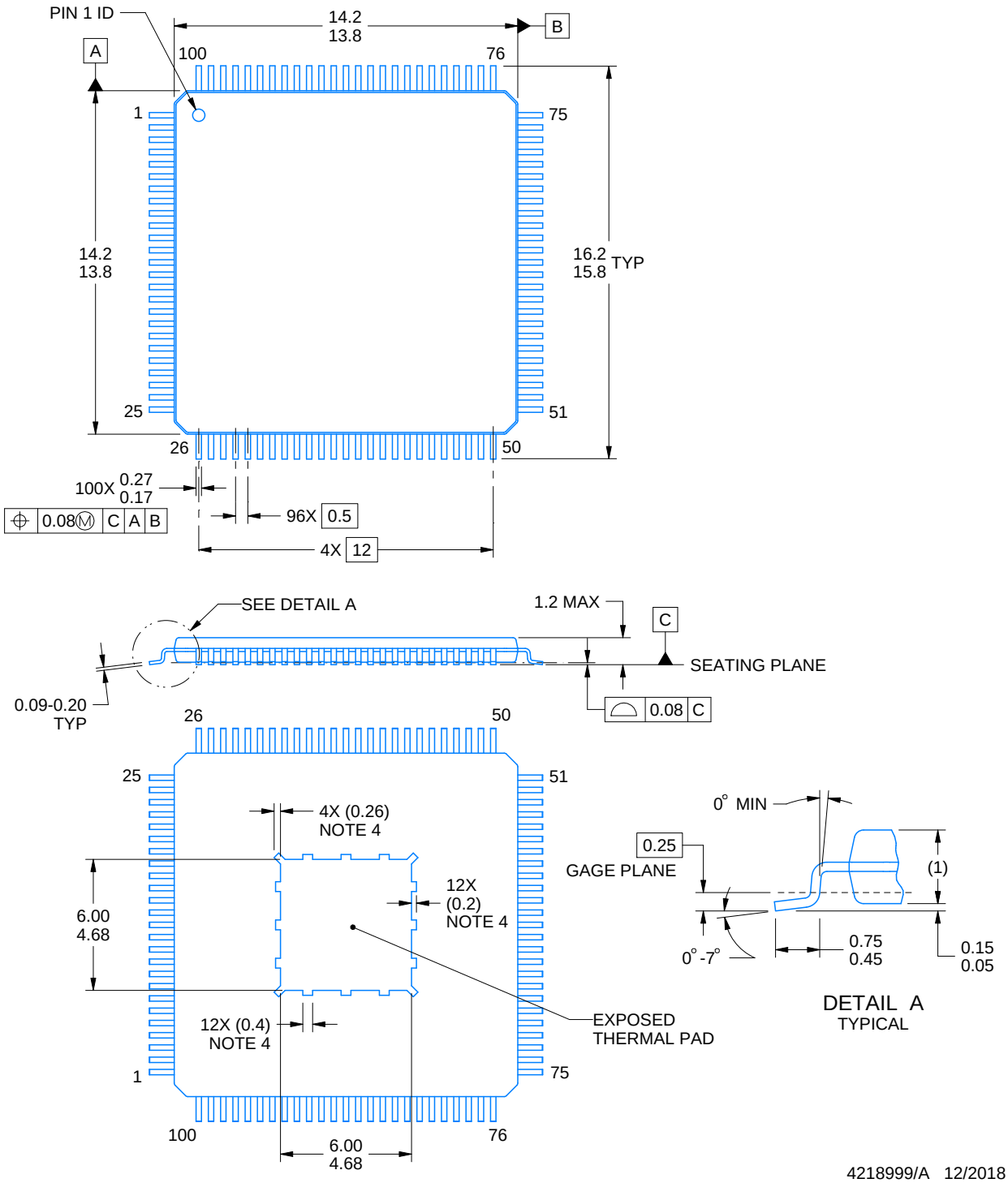
4224739/B

PACKAGE OUTLINE

PZP0100K

PowerPAD™ TQFP - 1.2 mm max height

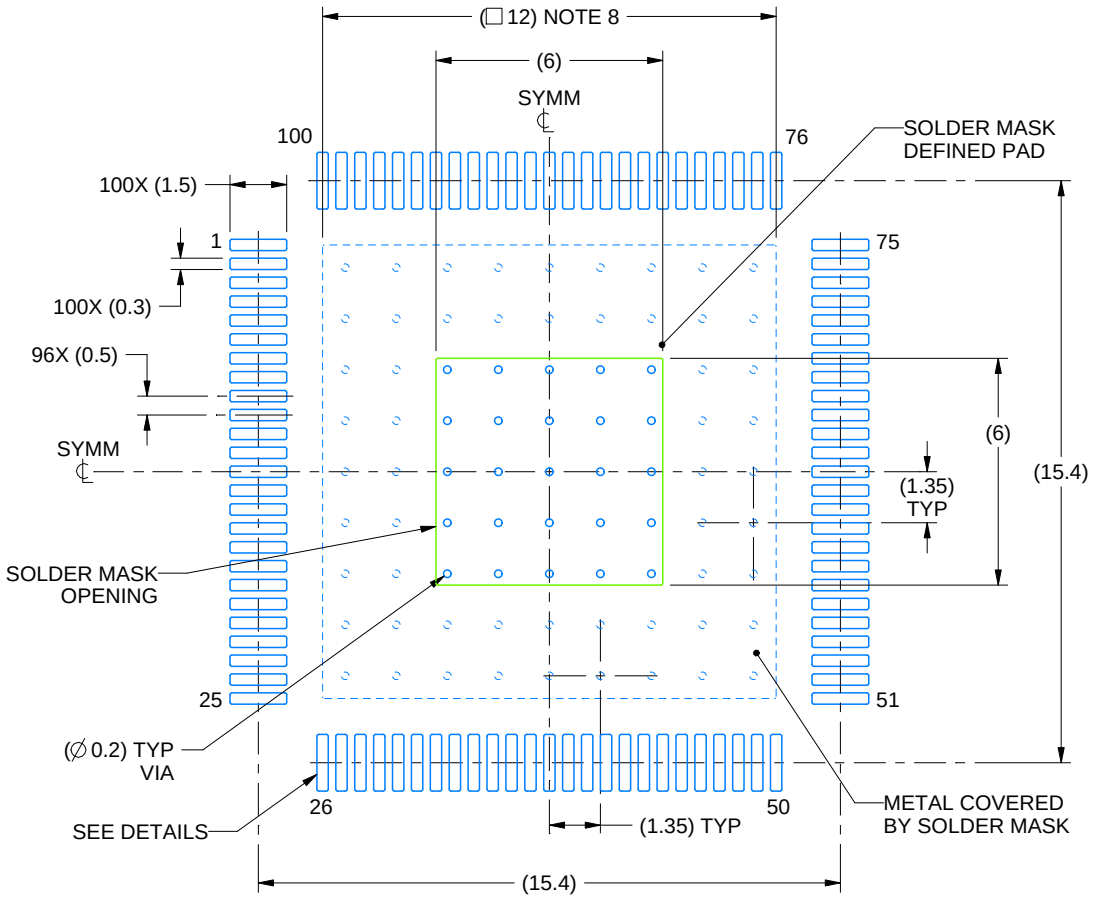
PLASTIC QUAD FLATPACK



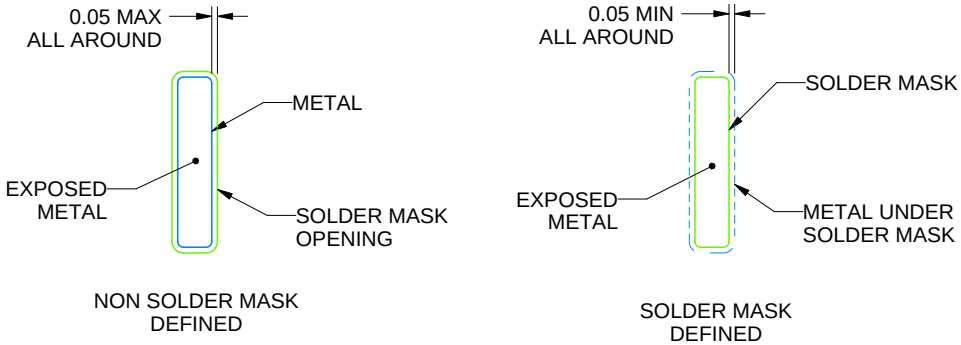
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026, variation ACD.
4. Strap features may not be present,



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X

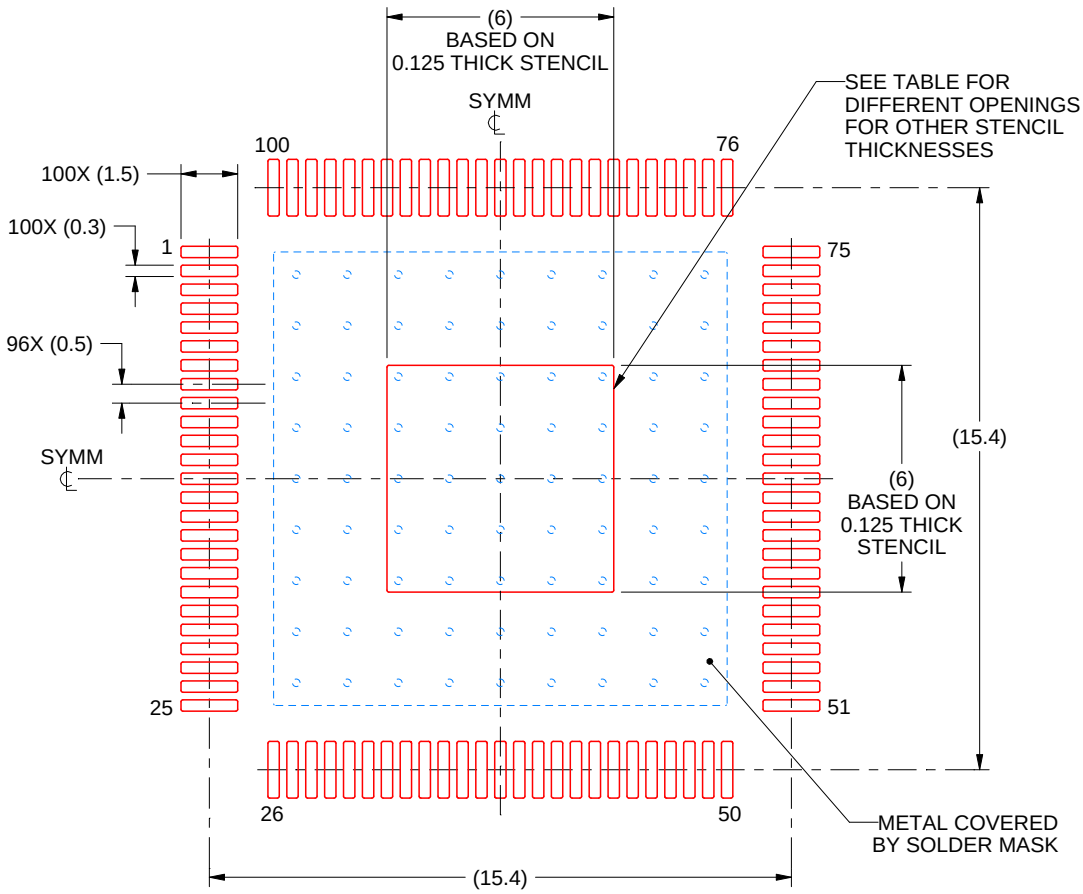


SOLDER MASK DETAILS

4218999/A 12/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:5X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	6.71 X 6.71
0.125	6 X 6 (SHOWN)
0.150	5.48 X 5.48
0.175	5.07 X 5.07

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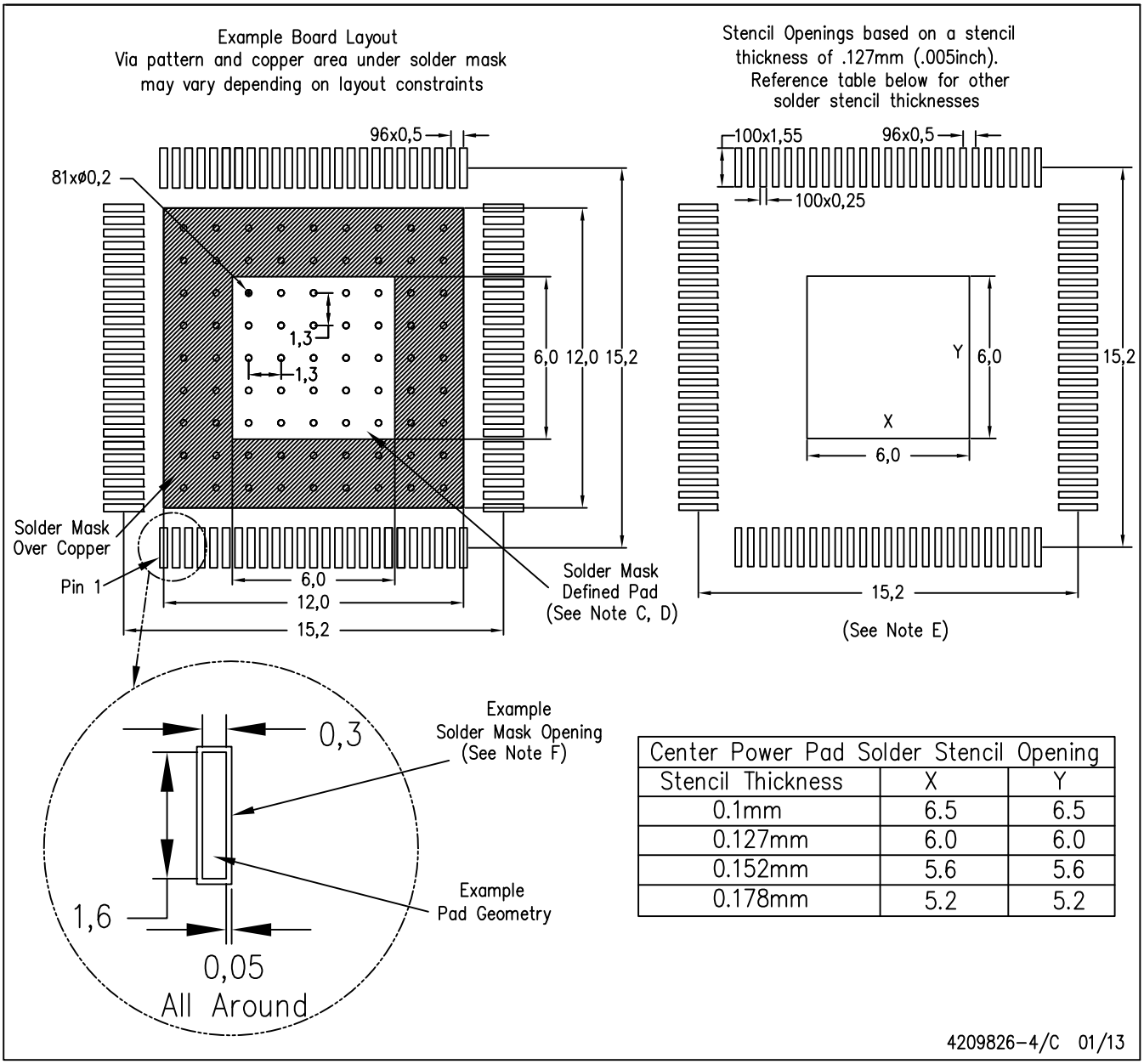
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.5	6.5
0.127mm	6.0	6.0
0.152mm	5.6	5.6
0.178mm	5.2	5.2

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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