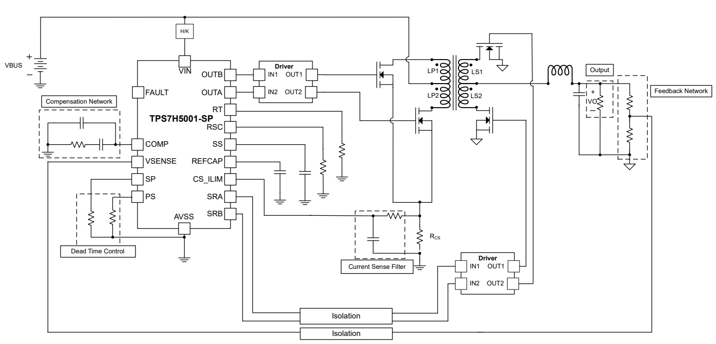
TPS7H500x-SP 耐辐射加固保障 2MHz 电流模式 PWM 控制器

1 特性

- 辐射性能：
  - 耐辐射加固保障 (RHA) 高达 TID 100krad(Si)
  - SEL、SEB 和 SEGR 对于 LET 的抗扰度 = 75MeV-cm²/mg
  - SET 和 SEFI 对于 LET 的额定抗扰度高达 75MeV-cm²/mg
  - SET 表征期间未发现控制器输出跨导事件
- 输入电压：4V 至 14V
- 在温度、辐射以及线路和负载调节范围内提供 0.613V +0.7%/–1% 的基准电压
- 开关频率范围为 100kHz 至 2MHz
- 外部时钟同步功能
- 同步整流输出
  - TPS7H5001-SP、TPS7H5002-SP、TPS7H5003-SP
- 可调死区时间
  - TPS7H5001-SP、TPS7H5002-SP
- 可调前沿消隐时间
  - TPS7H5001-SP、TPS7H5002-SP、TPS7H5004-SP
- 可配置的占空比限值
  - TPS7H5001-SP、TPS7H5002-SP、TPS7H5003-SP
- 可调斜坡补偿和软启动
- 封装选项包括 CFP 和 TSSOP

2 应用

- 用于 FPGA、微控制器、数据转换器和 ASIC 的太空卫星负载点电源
- 通信负载
- 命令和数据处理
- 卫星电力系统



TPS7H5001-SP 的典型应用

3 说明

TPS7H500x-SP 耐辐射加固保障高速 PWM 控制器系列。这些控制器提供的许多功能有助于设计面向太空应用的直流/直流转换器拓扑。控制器具有精密的内部基准 (0.613V +0.7%/-1%)，可配置开关频率高达 2MHz。每个器件都提供可编程斜坡补偿和软启动功能。

TPS7H500x-SP 系列可通过 SYNC 引脚使用外部时钟来驱动，也可使用内部振荡器以用户编程的频率来驱动。此控制器系列为用户提供了各种选项，用于选择开关输出、同步整流功能、死区时间（固定或可配置）、前沿消隐时间（固定或可配置）和占空比限制。TPS7H500x-SP 系列中的每个器件均采用 22 引脚 CFP 陶瓷封装和 24 引脚 TSSOP 塑料封装。

器件信息

器件型号[(1)]	等级	封装尺寸
5962R1822201VXC	QMLV-RHA	22 引脚陶瓷 6.21mm × 7.69mm 质量 = 415.6mg[(2)]
5962R1822202VXC		
5962R1822203VXC		
5962R1822204VXC		
TPS7H5001HFT/EM	工程样片	
TPS7H5002HFT/EM		
TPS7H5003HFT/EM		
TPS7H5004HFT/EM		
5962R1822201PYE	QMLP-RHA	24 引脚塑料 4.40mm × 7.80mm 质量 = 102.3mg[(2)]
5962R1822202PYE		
5962R1822203PYE		
5962R1822204PYE		
5962R1822201V9A	QMLV-RHA KGD	裸片
5962R1822202V9A		
5962R1822203V9A		
5962R1822204V9A		
TPS7H5001Y/EM	工程样片	
TPS7H5002Y/EM		
TPS7H5003Y/EM		
TPS7H5004Y/EM		

(1) 有关更多信息，请查看*器件选项*表。
(2) 质量误差在 ±10% 以内。

Table of Contents

4 Device Comparison Table

DEVICE	PRIMARY OUTPUTS	SYNCHRONOUS RECTIFIER OUTPUTS	DEAD-TIME SETTING	LEADING EDGE BLANK TIME SETTING	DUTY CYCLE LIMIT OPTIONS
TPS7H5001-SP	2	2	Resistor programmable	Resistor programmable	50%, 75%, 100%
TPS7H5002-SP	1	1	Resistor programmable	Resistor programmable	75%, 100%
TPS7H5003-SP	1	1	Fixed (50-ns typical)	Fixed (50-ns typical)	75%, 100%
TPS7H5004-SP	2	0	Not applicable	Resistor programmable	50%

5 Device Options

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER(3)
TPS7H5001-SP	TID of 100 krad(Si) RLAT, DSEE free to LET = 75 MeV-cm^2/mg	QMLV-RHA	22-pin CFP HFT	5962R1822201VXC
		KGD (QMLV-RHA)	Die	5962R1822201V9A
		QMLP-RHA	24-pin TSSOP PW	5962R1822201PYE
	None	Engineering sample(4)	22-pin CFP HFT	TPS7H5001HFT/EM
			Die	TPS7H5001Y/EM
TPS7H5002-SP	TID of 100 krad(Si) RLAT, DSEE free to LET = 75 MeV-cm^2/mg	QMLV-RHA	22-pin CFP HFT	5962R1822202VXC
		KGD (QMLV-RHA)	Die	5962R1822202V9A
		QMLP-RHA	24-pin TSSOP PW	5962R1822202PYE
	None	Engineering sample(4)	22-pin CFP HFT	TPS7H5002HFT/EM
			Die	TPS7H5002Y/EM
TPS7H5003-SP	TID of 100 krad(Si) RLAT, DSEE free to LET = 75 MeV-cm^2/mg	QMLV-RHA	22-pin CFP HFT	5962R1822203VXC
		KGD (QMLV-RHA)	Die	5962R1822203V9A
		QMLP-RHA	24-pin TSSOP PW	5962R1822203PYE
	None	Engineering sample(4)	22-pin CFP HFT	TPS7H5003HFT/EM
			Die	TPS7H5003Y/EM
TPS7H5004-SP	TID of 100 krad(Si) RLAT, DSEE free to LET = 75 MeV-cm^2/mg	QMLV-RHA	22-pin CFP HFT	5962R1822204VXC
		KGD (QMLV-RHA)	Die	5962R1822204V9A
		QMLP-RHA	24-pin TSSOP PW	5962R1822204PYE
	None	Engineering sample(4)	22-pin CFP HFT	TPS7H5004HFT/EM
			Die	TPS7H5004Y/EM
SN0022HFT	N/A	Mechanical "dummy" package (no die)	22-pin CFP HFT	SN0022HFT

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view SLYB235.
(3) For all available packages, see the orderable addendum at the end of the data sheet.
(4) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

6 Pin Configuration and Functions

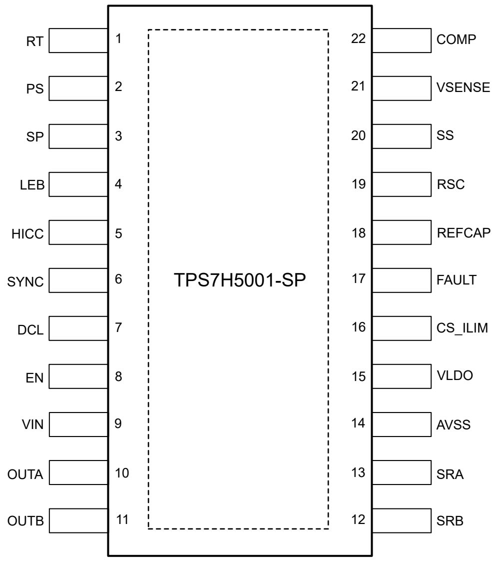


图 6-1. TPS7H5001-SP HFT Package 22-Pin CFP With Thermal Pad (Top View)

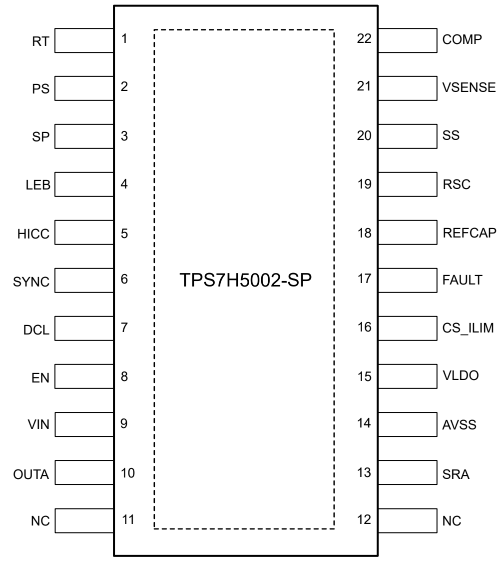


图 6-2. TPS7H5002-SP HFT Package 22-Pin CFP With Thermal Pad (Top View)

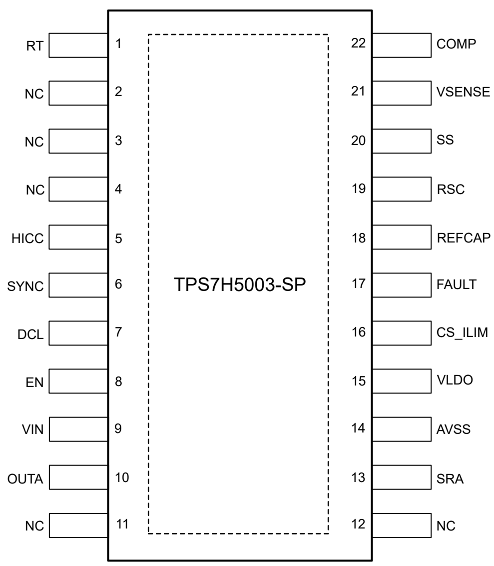


图 6-3. TPS7H5003-SP HFT Package 22-Pin CFP With Thermal Pad (Top View)

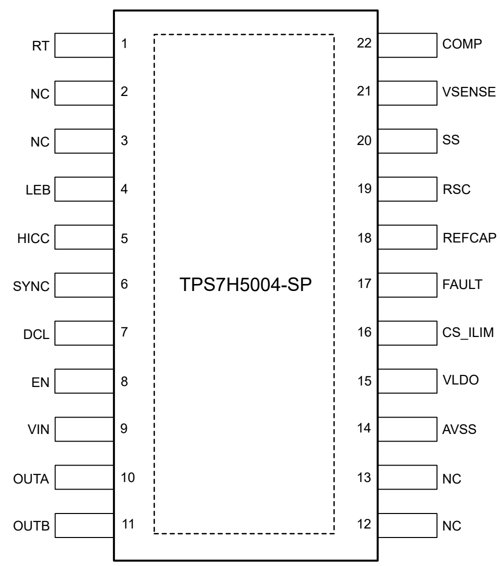


图 6-4. TPS7H5004-SP HFT Package 22-Pin CFP With Thermal Pad (Top View)

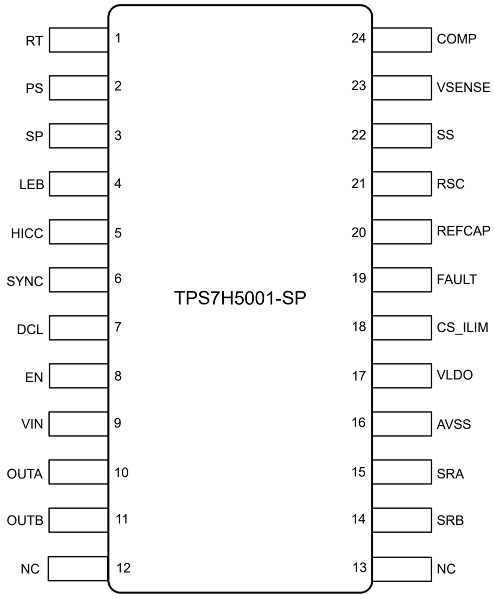


图 6-5. TPS7H5001-SP PW Package 24-Pin TSSOP (Top View)

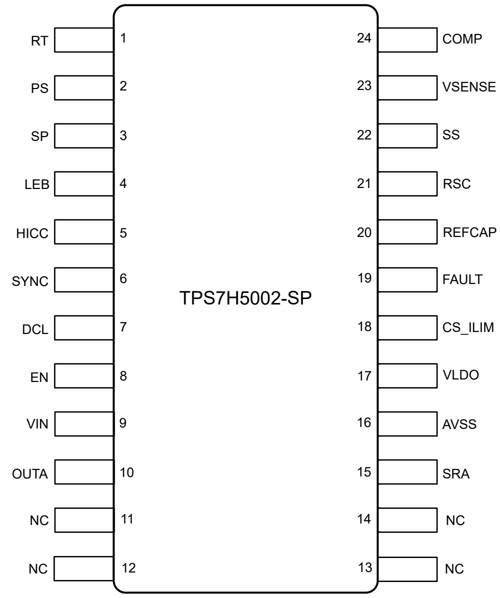


图 6-6. TPS7H5002-SP PW Package 24-Pin TSSOP (Top View)

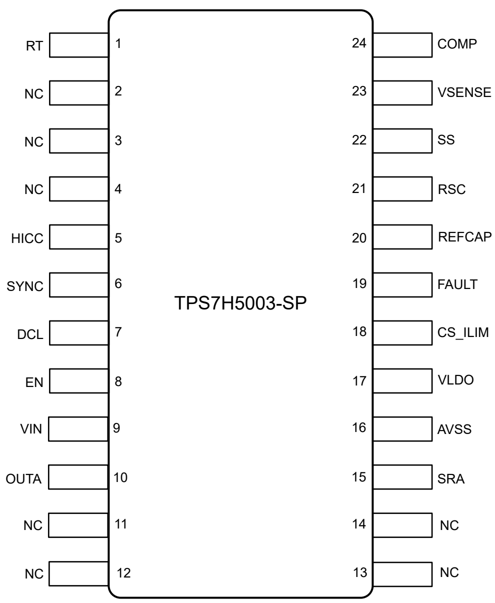


图 6-7. TPS7H5003-SP PW Package 24-Pin TSSOP (Top View)

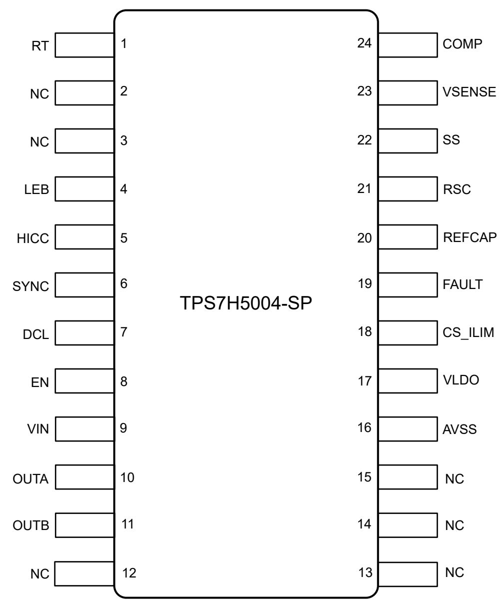


图 6-8. TPS7H5004-SP PW Package 24-Pin TSSOP (Top View)

表 **6-1. Pin Functions**

NAME	PIN								I/O	DESCRIPTION
	TPS7H5001-SP		TPS7H5002-SP		TPS7H5003-SP		TPS7H5004-SP			
	CFP	TSSOP	CFP	TSSOP	CFP	TSSOP	CFP	TSSOP		
RT	1	1	1	1	1	1	1	1	I/O	In internal oscillation mode, the RT pin must be populated with a resistor to AVSS. When the RT pin is floating, a 200-kHz to 4-MHz external clock is required at the SYNC pin. The frequency of the external clock must be twice the desired switching frequency.
PS	2	2	2	2	—	—	—	—	I/O	Primary off to synchronous rectifier on dead-time set. Programmable through an external resistor to AVSS.
SP	3	3	3	3	—	—	—	—	I/O	Synchronous rectifier off to primary on dead-time set. Programmable through an external resistor to AVSS.
LEB	4	4	4	4	—	—	4	4	I/O	Leading edge blank time set. Programmable through an external resistor to AVSS.
HICC	5	5	5	5	5	5	5	5	I/O	Cycle-by-cycle current limit time delay and hiccup time setting. Delay time and hiccup time determined by capacitor from HICC to AVSS. Connecting this pin to AVSS disables hiccup mode.
SYNC	6	6	6	6	6	6	6	6	I/O	When the RT pin is floating, SYNC is configured as an input for a 200-kHz to 4-MHz external clock. In this case, the external clock input gets inverted and the system clock will run at half the frequency of the external clock input. When the RT pin is populated with a resistor to AVSS, SYNC outputs a 200-kHz to 4-MHz clock signal at twice the device switching frequency in phase with the switching of the device.

表 6-1. Pin Functions （续）

NAME	TPS7H5001-SP CFP	TPS7H5001-SP TSSOP	TPS7H5002-SP CFP	TPS7H5002-SP TSSOP	TPS7H5003-SP CFP	TPS7H5003-SP TSSOP	TPS7H5004-SP CFP	TPS7H5004-SP TSSOP	I/O	DESCRIPTION
DCL	7	7	7	7	7	7	7	7	I/O	Duty cycle limit configurability. For TPS7H5001-SP, connect to AVSS for 50% duty cycle limit, floating for 75%, and VLDO for 100%. For TPS7H5002-SP and TPS7H5003-SP, the DCL pin can be left floating or connected to VLDO to set the maximum duty cycle to 75% or 100%, respectively. For TPS7H5004-SP, this pin must be connected to AVSS in order to obtain the 50% maximum duty cycle.
EN	8	8	8	8	8	8	8	8	I	Connecting the EN pin to the VLDO pin or external source greater than 0.6 V enables the device. In addition, input undervoltage lockout (UVLO) can be adjusted with two resistors.
VIN	9	9	9	9	9	9	9	9	I	Input supply to the device. Input voltage range is from 4 V to 14 V.
OUTA	10	10	10	10	10	10	10	10	O	Primary switching output A.
OUTB	11	11	—	—	—	—	11	11	O	Primary switching output B. Active only when DCL = AVSS.
SRB	12	14	—	—	—	—	—	—	O	Synchronous rectifier output B. Active only when DCL = AVSS.
SRA	13	15	13	15	13	15	—	—	O	Synchronous rectifier output A.
AVSS	14	16	14	16	14	16	14	16	—	Ground of the device. The thermal pad, lid, and seal ring of the device are internally connected to ground for the ceramic package (CFP).
VLDO	15	17	15	17	15	17	15	17	O	Output of internal regulator. Requires at least 1-μF external capacitor to AVSS.
CS_ILIM	16	18	16	18	16	18	16	18	I/O	Current sense for PWM control and cycle-by-cycle overcurrent protection. An input voltage over 1.05 V on CS_ILIM will trigger an overcurrent in the PWM controller. The sensed waveform on CS_ILIM contains a 150-mV offset when compared to the COMP/2 voltage at the input of the PWM comparator.

表 6-1. Pin Functions （续）

NAME	TPS7H5001-SP CFP	TPS7H5001-SP TSSOP	TPS7H5002-SP CFP	TPS7H5002-SP TSSOP	TPS7H5003-SP CFP	TPS7H5003-SP TSSOP	TPS7H5004-SP CFP	TPS7H5004-SP TSSOP	I/O	DESCRIPTION
FAULT	17	19	17	19	17	19	17	19	I	Fault protection pin. When the rising threshold of the FAULT pin is exceeded, the outputs will stop switching. After the external voltage drops below the falling threshold, the device will restart after a set delay. Connect this pin to AVSS to disable FAULT.
REFCAP	18	20	18	20	18	20	18	20	O	1.2-V internal reference. Requires a 470-nF external capacitor to AVSS.
RSC	19	21	19	21	19	21	19	21	I/O	A resistor from RSC to AVSS sets the desired slope compensation.
SS	20	22	20	22	20	22	20	22	I/O	Soft start. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
VSENSE	21	23	21	23	21	23	21	23	I	Inverting input of the error amplifier.
COMP	22	24	22	24	22	24	22	24	I/O	Error amplifier output. Connect frequency compensation to this pin.
NC	N/A	12, 13	11, 12	11, 12, 13, 14	2, 3, 4, 11, 12	2, 3, 4, 11, 12, 13, 14	2, 3, 12, 13	2, 3,12, 13, 14, 15	—	No connect. Can be connected to AVSS to avoid floating metal if desired.

表 6-2. TPS7H500x-SP Bare Die Information - Applicable for All Devices

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	GND	Al (0.5% Cu)	3000 nm

图 6-9. TPS7H500x-SP Bare Die Diagram - Applicable for All Devices

表 6-3. TPS7H5001-SP Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
RT	1	21.33	3775.77	111.33	3865.77
PS	2	21.33	3392.37	111.33	3482.37
SP	3	21.33	3233.115	111.33	3323.115
LEB	4	21.33	2955.015	111.33	3045.015
HICC	5	21.33	2695.905	111.33	2785.905
SYNC	6	32.13	2427.705	122.13	2517.705
DCL	7	32.13	2149.515	122.13	2239.515
NC	8	32.175	1923.165	122.175	2013.165
EN	9	32.13	1660.275	122.13	1750.275
VIN	10	28.665	1432.53	118.665	1522.53
VIN	11	28.665	1325.475	118.665	1415.475
OUTA	12	32.13	586.755	122.13	676.755
OUTB	13	32.13	433.35	122.13	523.35
SRB	14	2224.62	132.93	2314.62	222.93
SRA	15	2224.62	586.755	2314.62	676.755
AVSS	16	2235.42	1053.315	2325.42	1143.315
AVSS	17	2235.42	1221.435	2325.42	1311.435
AVSS	18	2235.42	1330.425	2325.42	1420.425
VLDO	19	2224.62	1803.51	2314.62	1893.51
VLDO	20	2224.62	1912.545	2314.62	2002.545
VLDO	21	2224.62	2021.58	2314.62	2111.58
CS_ILM	22	2224.62	2274.3	2314.62	2364.3
FAULT	23	2224.62	2513.16	2314.62	2603.16
REFCAP	24	2235.42	2766.285	2325.42	2856.285
RSC	25	2235.42	3033.36	2325.42	3123.36
SS	26	2235.42	3296.655	2325.42	3386.655
VSENSE	27	2235.42	3563.64	2325.42	3653.64
COMP	28	2235.42	3905.55	2325.42	3995.55

表 6-4. TPS7H5002-SP Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
RT	1	21.33	3775.77	111.33	3865.77
PS	2	21.33	3392.37	111.33	3482.37
SP	3	21.33	3233.115	111.33	3323.115
LEB	4	21.33	2955.015	111.33	3045.015
HICC	5	21.33	2695.905	111.33	2785.905
SYNC	6	32.13	2427.705	122.13	2517.705
DCL	7	32.13	2149.515	122.13	2239.515
NC	8	32.175	1923.165	122.175	2013.165
EN	9	32.13	1660.275	122.13	1750.275
VIN	10	28.665	1432.53	118.665	1522.53
VIN	11	28.665	1325.475	118.665	1415.475
OUTA	12	32.13	586.755	122.13	676.755
NC	13	32.13	433.35	122.13	523.35
NC	14	2224.62	132.93	2314.62	222.93

表 6-4. TPS7H5002-SP Bond Pad Coordinates in Microns （续）

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
SRA	15	2224.62	586.755	2314.62	676.755
AVSS	16	2235.42	1053.315	2325.42	1143.315
AVSS	17	2235.42	1221.435	2325.42	1311.435
AVSS	18	2235.42	1330.425	2325.42	1420.425
VLDO	19	2224.62	1803.51	2314.62	1893.51
VLDO	20	2224.62	1912.545	2314.62	2002.545
VLDO	21	2224.62	2021.58	2314.62	2111.58
CS_ILM	22	2224.62	2274.3	2314.62	2364.3
FAULT	23	2224.62	2513.16	2314.62	2603.16
REFCAP	24	2235.42	2766.285	2325.42	2856.285
RSC	25	2235.42	3033.36	2325.42	3123.36
SS	26	2235.42	3296.655	2325.42	3386.655
VSENSE	27	2235.42	3563.64	2325.42	3653.64
COMP	28	2235.42	3905.55	2325.42	3995.55

表 6-5. TPS7H5003-SP Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
RT	1	21.33	3775.77	111.33	3865.77
NC	2	21.33	3392.37	111.33	3482.37
NC	3	21.33	3233.115	111.33	3323.115
NC	4	21.33	2955.015	111.33	3045.015
HICC	5	21.33	2695.905	111.33	2785.905
SYNC	6	32.13	2427.705	122.13	2517.705
DCL	7	32.13	2149.515	122.13	2239.515
NC	8	32.175	1923.165	122.175	2013.165
EN	9	32.13	1660.275	122.13	1750.275
VIN	10	28.665	1432.53	118.665	1522.53
VIN	11	28.665	1325.475	118.665	1415.475
OUTA	12	32.13	586.755	122.13	676.755
NC	13	32.13	433.35	122.13	523.35
NC	14	2224.62	132.93	2314.62	222.93
SRA	15	2224.62	586.755	2314.62	676.755
AVSS	16	2235.42	1053.315	2325.42	1143.315
AVSS	17	2235.42	1221.435	2325.42	1311.435
AVSS	18	2235.42	1330.425	2325.42	1420.425
VLDO	19	2224.62	1803.51	2314.62	1893.51
VLDO	20	2224.62	1912.545	2314.62	2002.545
VLDO	21	2224.62	2021.58	2314.62	2111.58
CS_ILM	22	2224.62	2274.3	2314.62	2364.3
FAULT	23	2224.62	2513.16	2314.62	2603.16
REFCAP	24	2235.42	2766.285	2325.42	2856.285
RSC	25	2235.42	3033.36	2325.42	3123.36
SS	26	2235.42	3296.655	2325.42	3386.655
VSENSE	27	2235.42	3563.64	2325.42	3653.64

表 6-5. TPS7H5003-SP Bond Pad Coordinates in Microns （续）

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
COMP	28	2235.42	3905.55	2325.42	3995.55

表 6-6. TPS7H5004-SP Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
RT	1	21.33	3775.77	111.33	3865.77
NC	2	21.33	3392.37	111.33	3482.37
NC	3	21.33	3233.115	111.33	3323.115
LEB	4	21.33	2955.015	111.33	3045.015
HICC	5	21.33	2695.905	111.33	2785.905
SYNC	6	32.13	2427.705	122.13	2517.705
DCL	7	32.13	2149.515	122.13	2239.515
NC	8	32.175	1923.165	122.175	2013.165
EN	9	32.13	1660.275	122.13	1750.275
VIN	10	28.665	1432.53	118.665	1522.53
VIN	11	28.665	1325.475	118.665	1415.475
OUTA	12	32.13	586.755	122.13	676.755
OUTB	13	32.13	433.35	122.13	523.35
NC	14	2224.62	132.93	2314.62	222.93
NC	15	2224.62	586.755	2314.62	676.755
AVSS	16	2235.42	1053.315	2325.42	1143.315
AVSS	17	2235.42	1221.435	2325.42	1311.435
AVSS	18	2235.42	1330.425	2325.42	1420.425
VLDO	19	2224.62	1803.51	2314.62	1893.51
VLDO	20	2224.62	1912.545	2314.62	2002.545
VLDO	21	2224.62	2021.58	2314.62	2111.58
CS_ILM	22	2224.62	2274.3	2314.62	2364.3
FAULT	23	2224.62	2513.16	2314.62	2603.16
REFCAP	24	2235.42	2766.285	2325.42	2856.285
RSC	25	2235.42	3033.36	2325.42	3123.36
SS	26	2235.42	3296.655	2325.42	3386.655
VSENSE	27	2235.42	3563.64	2325.42	3653.64
COMP	28	2235.42	3905.55	2325.42	3995.55

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Input	VIN	–0.3	16	V
	RT, VSENSE, SS, RSC, COMP, PS, SP, HICC, LEB	–0.3	3.3	
	SYNC	–0.3	7.5	
	EN, FAULT	–0.3	7.5	
	DCL, CS_ILIM	–0.3	7.5	
Output	OUTA, OUTB, SRA and SRB	–0.3	7.5	V
	VLDO	–0.3	7.5	
	REFCAP	–0.3	3.3	
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[(2)]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply voltage	4		14	V
SR_{VIN}	Input voltage slew rate			0.03	V/µs
T_J	Junction temperature	–55		125	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		TP7H500x-SP		UNIT
		CFP	TSSOP	
		22 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.8	74.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.4	-	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.9	34.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (top) thermal resistance	16.5	17.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.6	30.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics: All Devices

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES AND CURRENTS						
VIN	Operating input voltage		4		14	V
IDD	Operating supply current	f_{SW} = 500 kHz, No load for OUTA, OUTB, SRA, and SRB		6.25	8	mA
		f_{SW} = 1 MHz, No load for OUTA, OUTB, SRA, and SRB		6.75	9.5	
		f_{SW} = 2 MHz, No load for OUTA, OUTB, SRA, and SRB		8.5	13.5	
		f_{SW} = 500 kHz, C_{LOAD} = 100 pF for OUTA, OUTB, SRA, and SRB		7.5	9.5	
		f_{SW} = 1 MHz, C_{LOAD} = 100 pF for OUTA, OUTB, SRA, and SRB		9	12	
		f_{SW} = 2 MHz, C_{LOAD} = 100 pF for OUTA, OUTB, SRA, and SRB		14	19.5	
$I_{DD(dis)}$	Standby current	EN = 0 V			3	mA
VLDO	Internal linear regulator output voltage	5 V ≤ VIN ≤ 14 V, f_{sw} ≤ 1 MHz	4.75	5	5.2	V
VLDO	Internal linear regulator output voltage	5 V ≤ VIN ≤ 14 V, f_{sw} = 2 MHz	4.65	5	5.2	V
ENABLE AND UNDERVOLTAGE LOCKOUT						
V_{ENR}	EN threshold rising		0.57	0.6	0.65	V
V_{ENF}	EN threshold falling		0.47	0.5	0.55	V
V_{ENH}	EN hysteresis voltage		85	95	105	mV
I_{EN}	EN pin input leakage current	VIN = 14 V, EN = 5 V		5	50	nA
$VLDO_{UVLOR}$	VLDO UVLO rising		3.44	3.55	3.66	V
$VLDO_{UVLOF}$	VLDO UVLO falling		3.29	3.4	3.51	V
$VLDO_{UVLOH}$	VLDO UVLO hysteresis		115	135	160	mV
SOFT START						
I_{SS}	Soft-start current	SS = 0.3 V	1.98	2.7	3.32	µA
ERROR AMPLIFIER						
EA_{gm}	Transconductance	–2 µA < I_{COMP} < 2 µA, $V_{(COMP)}$ = 1 V	1150	1800	2500	µA/V
EA_{DC}	DC gain	V_{SENSE} = 0.6 V		10000		V/V
EA_{ISRC}	Error amplifier source current	$V_{(COMP)}$ = 1 V, 100-mV input overdrive	100		190	µA
EA_{ISNK}	Error amplifier sink current	$V_{(COMP)}$ = 1 V, 100-mV input overdrive	100		190	µA
EA_{ro}	Error amplifier output resistance			7		MΩ
EA_{OS}	Error amplifier input offset voltage		–2		2	mV
EA_{IB}	Error amplifier input bias current				35	nA
EA_{BW}	Bandwidth			10		MHz
OSCILLATOR						
$SYNC_{IL}$	SYNC in low-level	VIN < 5 V			0.8	V
		VIN ≥ 5 V			0.8	
$SYNC_{IH}$	SYNC in high-level	VIN < 5 V	3.5			V
		VIN ≥ 5 V	3.5			
F_{SYNC}	SYNC in frequency range		200		4000	kHz
D_{SYNC}	SYNC in duty cycle	Duty cycle of external clock	40		60	%
$SYNC_{RT}$	SYNC out low-to-high rise time (10%/90%)	C_{LOAD} = 25 pF		6	15	ns

7.5 Electrical Characteristics: All Devices （续）

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$SYNC_{FT}$	SYNC out high-to-low fall time (10%/ 90%)	C_{LOAD} = 25 pF		6	17	ns
$SYNC_{OL}$	SYNC out low level	I_{OL} = 10 mA			500	mV
VLDO – $SYNC_{OH}$	SYNC out high level (1)	I_{OH} = 10 mA			0.5	V
EXT_{DT}	Externally set frequency detection time	RT = Open, f = 200 kHz			20	µs
FSW_{EXT}	Externally set frequency	RT = 1.07 MΩ	95	105	115	kHz
		RT = 511 kΩ	190	210	230	
		RT = 90.9 kΩ	900	1000	1100	
		RT = 34.8 kΩ	1700	2000	2300	
VOLTAGE REFERENCE						
VREF	Internal voltage reference initial tolerance	Measured at COMP, 25°C	0.609	0.613	0.615	V
	Internal voltage reference	Measured at COMP, –55°C	0.607	0.609	0.612	
		Measured at COMP, 125°C	0.611	0.614	0.617	
REFCAP	REFCAP voltage	REFCAP = 470 nF	1.213	1.225	1.237	V
CURRENT SENSE, CURRENT LIMIT AND HICCUP						
CCSR	COMP to CS_ILIM ratio		2.00	2.06	2.12	
V_{CS_ILIM}	Current limit (overcurrent) threshold			1.05	1.09	V
I_{HICC_DEL}	Hiccup delay current	CS_ILIM = 1.3 V, COMP = 3 V, VSENSE = REFCAP/2 V, C_{HICC} = 3 nF, LEB = 49.9 kΩ, f_{sw} = 100 kHz		80		µA
I_{HICC_RST}	Hiccup restart current			1		µA
V_{HICC_PU}	Hiccup pull-up threshold			1.0		V
V_{HICC_SD}	Hiccup shut-down threshold			0.6		V
V_{HICC_RST}	Hiccup restart threshold			0.3		V
SLOPE COMPENSATION						
	Slope compensation	f_{SW} = 100 kHz, RSC = 1.18 MΩ		0.033		V/µs
		f_{SW} = 200 kHz, RSC = 562 kΩ		0.066		
		f_{SW} = 1000 kHz, RSC = 100 kΩ		0.333		
		f_{SW} = 2000 kHz, RSC = 49.9 kΩ		0.666		
FAULT						
V_{FLTR}	FLT threshold rising		0.57	0.6	0.65	V
V_{FLTF}	FLT threshold falling		0.47	0.5	0.55	V
V_{FLTH}	FLT hysteresis voltage		90	100	110	mV
T_{FLT}	FLT minimum pulse width	V_{FLT} = 1 V	0.4		1.4	µs
t_{DFLT}	FLT delay duration	f_{sw} = 100 kHz	140	152	169	µs
		f_{sw} = 200 kHz	66	78	86	
		f_{sw} = 1 MHz	14	17	21	
		f_{sw} = 2 MHz	7	11	14	
THERMAL SHUTDOWN						
	Thermal shutdown		165	175	185	°C
	Thermal shutdown hysteresis		10	15	20	°C
PRIMARY AND SYNCHRONOUS RECTIFIER OUTPUTS						

7.5 Electrical Characteristics: All Devices （续）

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low-level threshold	I_{SINK} = 10 mA		0.5		V
	High-level threshold	I_{SOURCE} = 10 mA		4.5		V
	Rise/fall time	R_{LOAD} = 50 kΩ, C_{LOAD} = 100 pF, 10% to 90%		10	17	ns
R_{SRC_P}	Output source resistance	I_{OUT} = 20 mA, 5 V ≤ VIN ≤ 14 V		15		Ω
R_{SINK_P}	Output sink resistance	I_{OUT} = 20 mA, 5 V ≤ VIN ≤ 14 V		15		Ω

(1) Bench verified. Not tested in production.

7.6 Electrical Characteristics: TPS7H5001-SP

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MINIMUM ON-TIME AND DEAD TIME						
t_{MIN}	Minimum on-time	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V			85	ns
TD_{PS}	Primary off to secondary on dead time	PS = floating, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	5	8	11	ns
		PS = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	43	50	55	
		PS = 107 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	85	100	110	
TD_{SP}	Secondary off to primary on dead time	SP = floating, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating	5	8	11	ns
		SP = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising edge, OUTx and SRx floating	43	50	55	
		SP = 107 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating	85	100	110	
LEADING EDGE BLANK TIME AND DUTY CYCLE						
T_{LEB}	Leading edge blank time	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	12	15	19	ns
		LEB = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V	45	50	55	
		LEB = 110 kΩ, 5 V ≤ VIN ≤ 14 V	85	100	110	
D_{MAX}	Maximum duty cycle	DCL = AVSS	45	48	50	%
		DCL = floating, clock duty cycle = 50%	70	75	80	
		DCL = VLDO			100	

7.7 Electrical Characteristics: TPS7H5002-SP

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MINIMUM ON-TIME AND DEAD TIME						
t_{MIN}	Minimum on-time	LEB = 10 kΩ, 5 V ⩽ VIN ⩽ 14 V			85	ns
TD_{PS}	Primary off to secondary on dead time	PS = floating, 5 V ⩽ VIN ⩽ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	5	8	11	ns
		PS = 49.9 kΩ, 5 V ⩽ VIN ⩽ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	43	50	55	
		PS = 107 kΩ, 5 V ⩽ VIN ⩽ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	85	100	110	
TD_{SP}	Secondary off to primary on dead time	SP = floating, 5 V ⩽ VIN ⩽ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating	5	8	11	ns
		SP = 49.9 kΩ, 5 V ⩽ VIN ⩽ 14 V, 90% of SRx falling to 10% of OUTx rising edge, OUTx and SRx floating	43	50	55	
		SP = 107 kΩ, 5 V ⩽ VIN ⩽ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating	85	100	110	
LEADING EDGE BLANK TIME AND DUTY CYCLE						
T_{LEB}	Leading edge blank time	LEB = 10 kΩ, 5 V ⩽ VIN ⩽ 14 V	12	15	19	ns
		LEB = 49.9 kΩ, 5 V ⩽ VIN ⩽ 14 V	45	50	55	
		LEB = 110 kΩ, 5 V ⩽ VIN ⩽ 14 V	85	100	110	
D_{MAX}	Maximum duty cycle	DCL = floating, clock duty cycle = 50%	70	75	80	%
		DCL = VLDO			100	

7.8 Electrical Characteristics: TPS7H5003-SP

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MINIMUM ON-TIME AND DEAD TIME						
t_{MIN}	Minimum on-time	5 V ⩽ VIN ⩽ 14 V			115	ns
TD_{PS}	Primary off to secondary on dead time	5 V ⩽ VIN ⩽ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	40	50	60	ns
TD_{SP}	Secondary off to primary on dead time	5 V ⩽ VIN ⩽ 14 V, 90% of SRx falling to 10% of OUTx rising edge, OUTx and SRx floating	40	50	60	ns
LEADING EDGE BLANK TIME AND DUTY CYCLE						
T_{LEB}	Leading edge blank time	5 V ⩽ VIN ⩽ 14 V	40	50	60	ns
D_{MAX}	Maximum duty cycle	DCL = floating, clock duty cycle = 50%	70	75	80	%
		DCL = VLDO			100	

7.9 Electrical Characteristics: TPS7H5004-SP

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MINIMUM ON-TIME						
t_{MIN}	Minimum on-time	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V			85	ns
LEADING EDGE BLANK TIME AND DUTY CYCLE						
T_{LEB}	Leading edge blank time	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	12	15	19	ns
		LEB = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V	45	50	55	
		LEB = 110 kΩ, 5 V ≤ VIN ≤ 14 V	85	100	110	
D_{MAX}	Maximum duty cycle	DCL = AVSS	45	48	50	%

7.10 Typical Characteristics

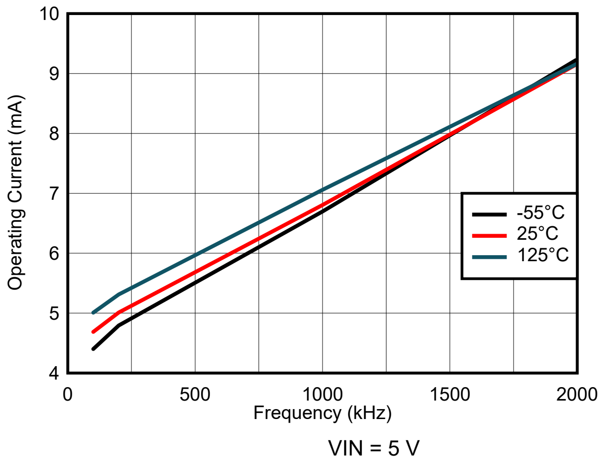


图 7-1. Operating Current Variation

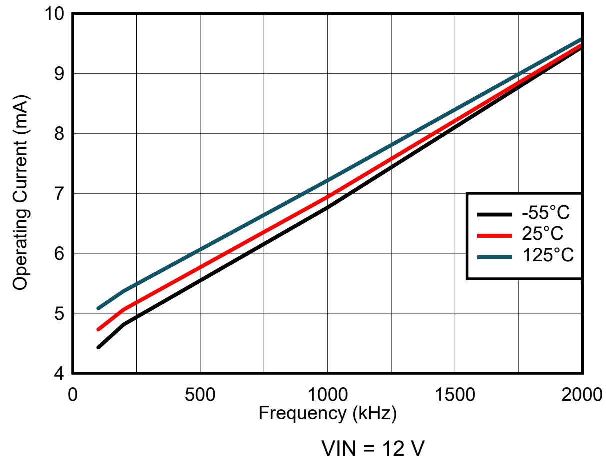


图 7-2. Operating Current Variation

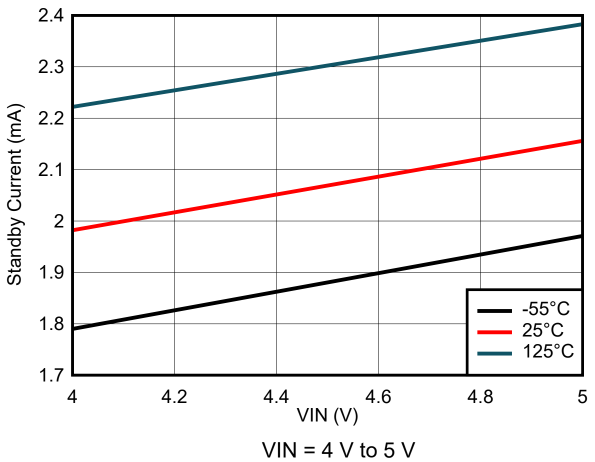


图 7-3. Standby Current Variation

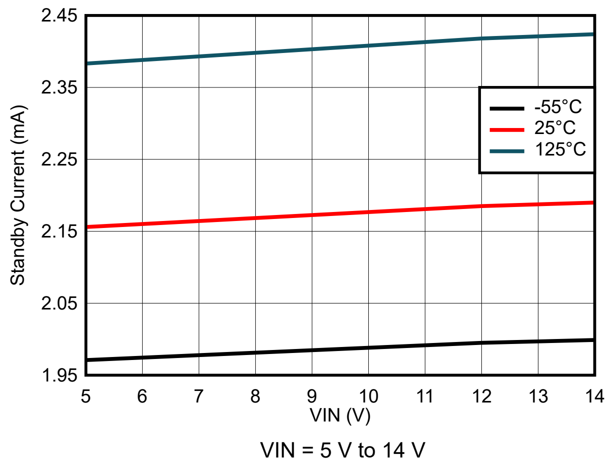


图 7-4. Standby Current Variation

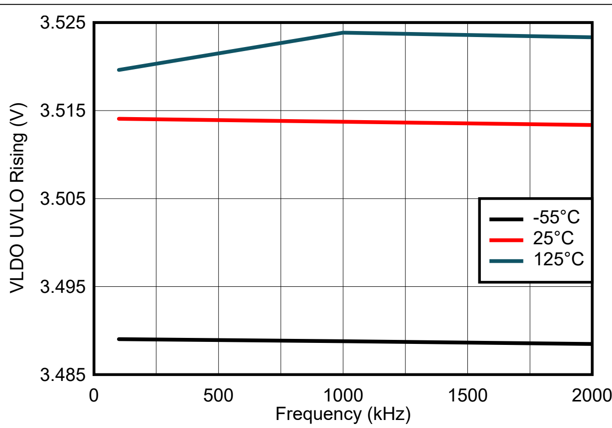


图 7-5. VLDO UVLO Rising Variation

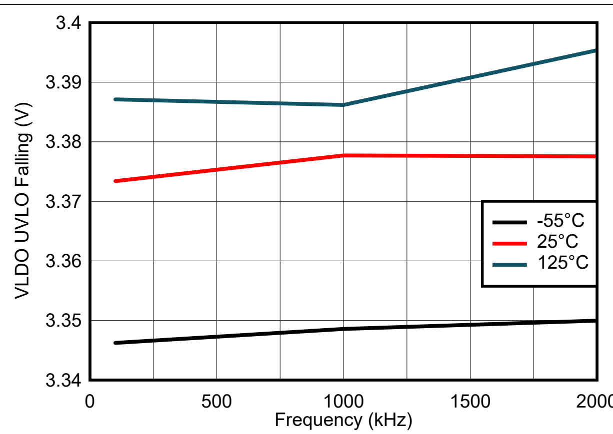


图 7-6. VLDO UVLO Falling Variation

7.10 Typical Characteristics (continued)

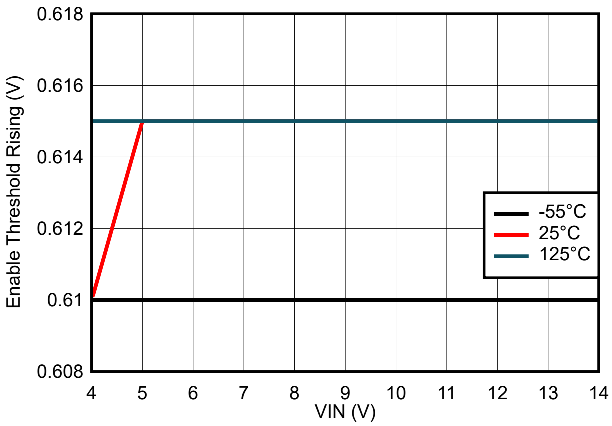


图 7-7. Enable Threshold Rising Variation

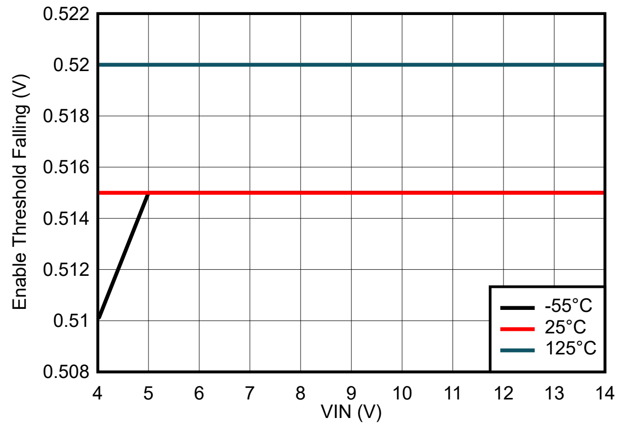
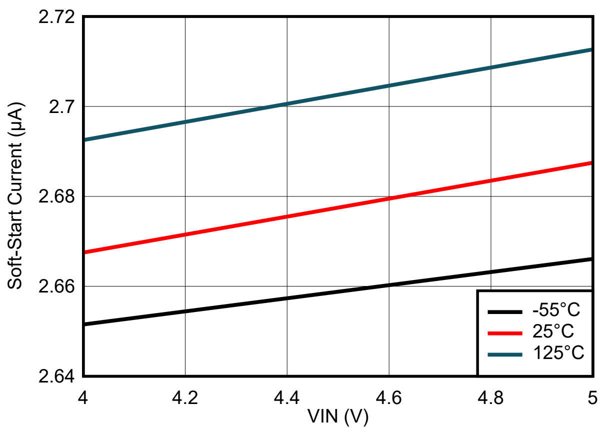
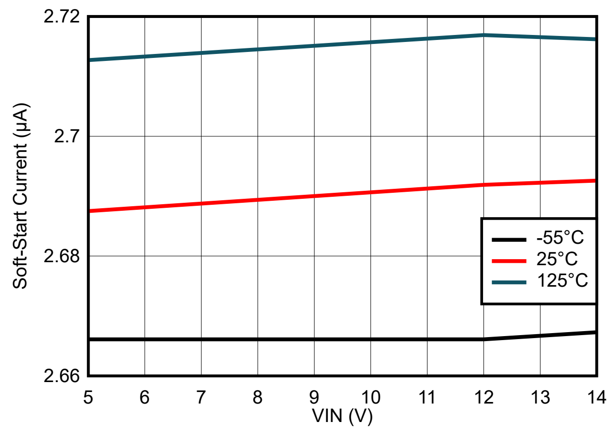


图 7-8. Enable Threshold Falling Variation



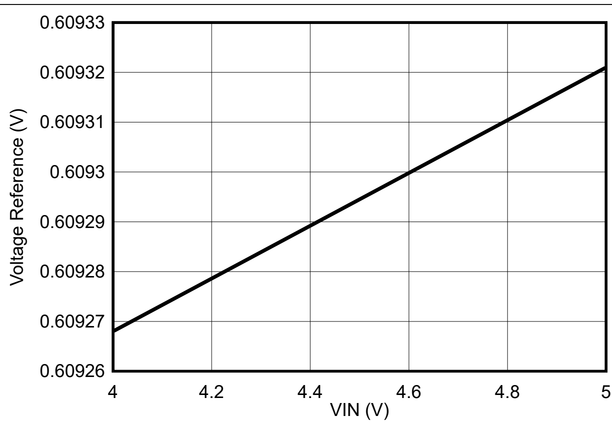
VIN = 4 V to 5 V

图 7-9. Soft-Start Current Variation



VIN = 5 V to 14 V

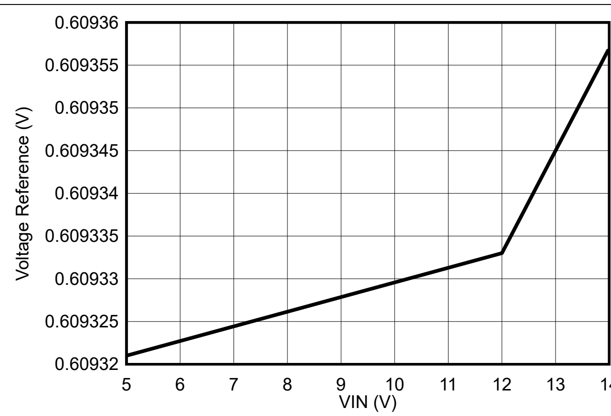
图 7-10. Soft-Start Current Variation



VIN = 4 V to 5 V

Temp. = – 55°C

图 7-11. Voltage Reference Variation

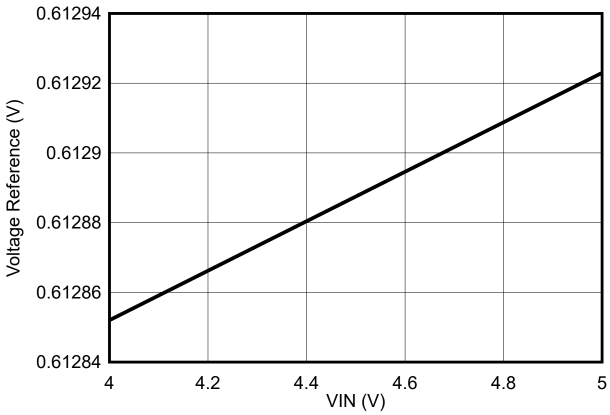


VIN = 5 V to 14 V

Temp. = – 55°C

图 7-12. Voltage Reference Variation

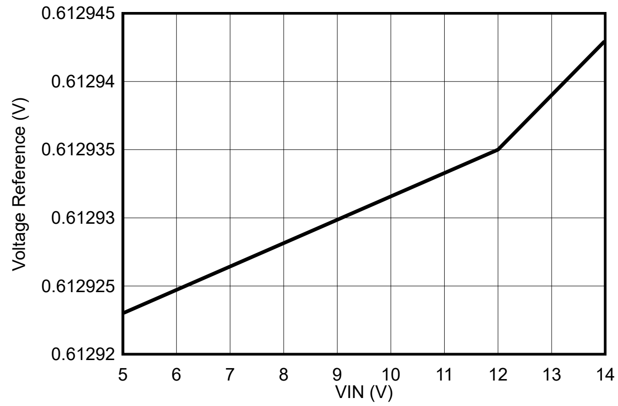
7.10 Typical Characteristics (continued)



VIN = 4 V to 5 V

Temp. = 25°C

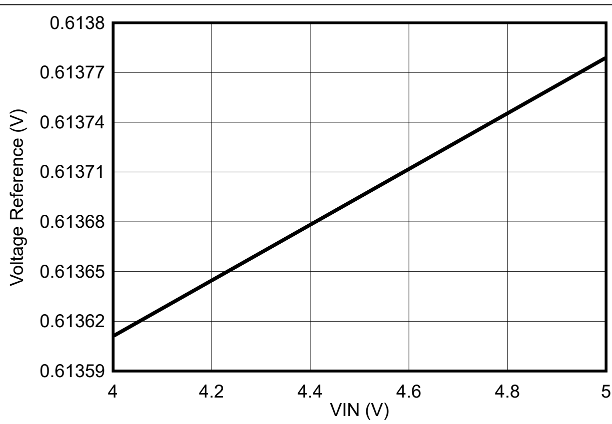
图 7-13. Voltage Reference Variation



VIN = 5 V to 14 V

Temp. = 25°C

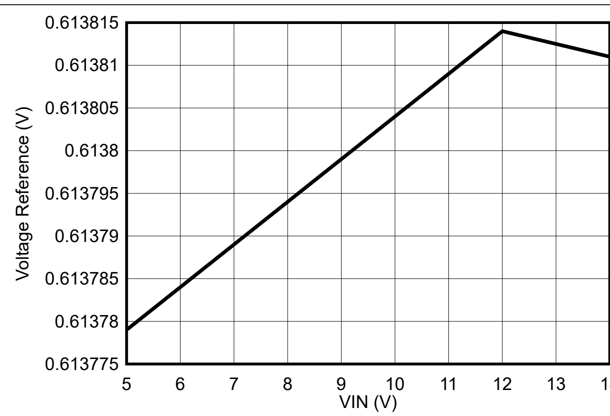
图 7-14. Voltage Reference Variation



VIN = 4 V to 5 V

Temp. = 125°C

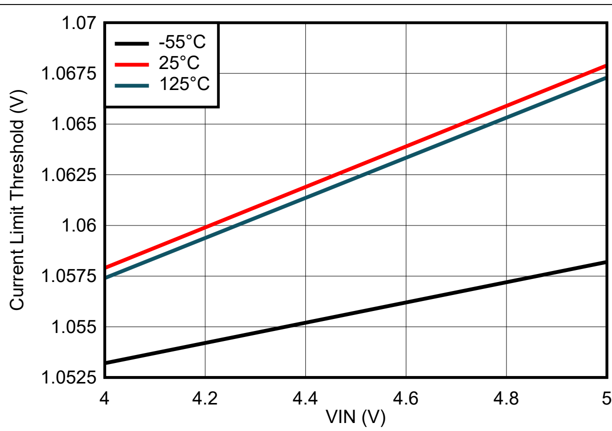
图 7-15. Voltage Reference Variation



VIN = 5 V to 14 V

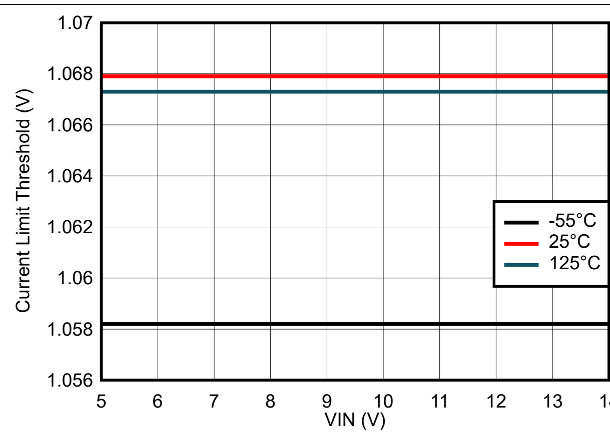
Temp. = 125°C

图 7-16. Voltage Reference Variation



VIN = 4 V to 5 V

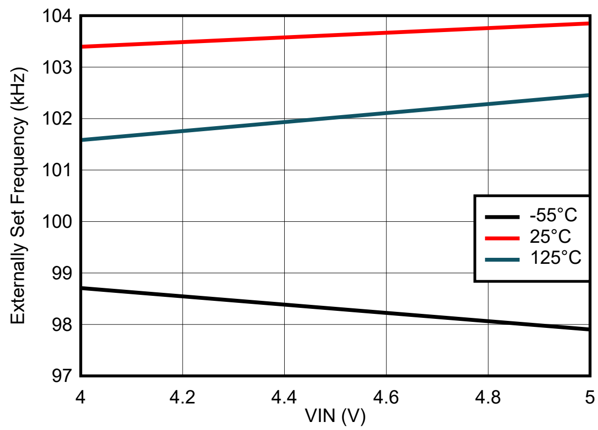
图 7-17. Current Limit Threshold Variation



VIN = 5 V to 14 V

图 7-18. Current Limit Theshold Variation

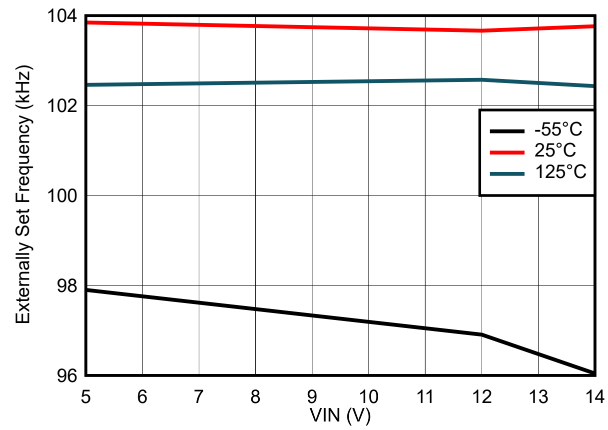
7.10 Typical Characteristics (continued)



VIN = 4 V to 5 V

RT = 1.07 MΩ

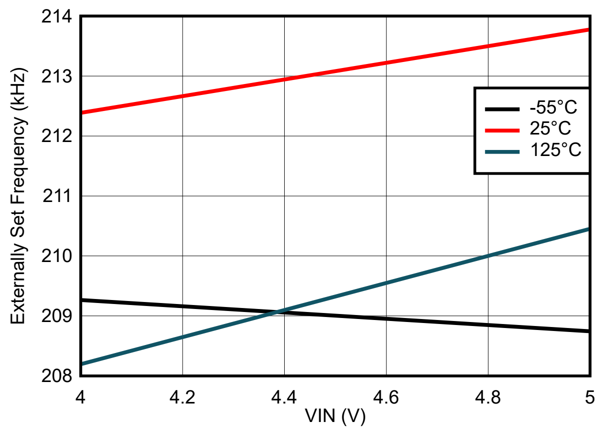
图 7-19. Externally Set Frequency Variation



VIN = 5 V to 14 V

RT = 1.07 MΩ

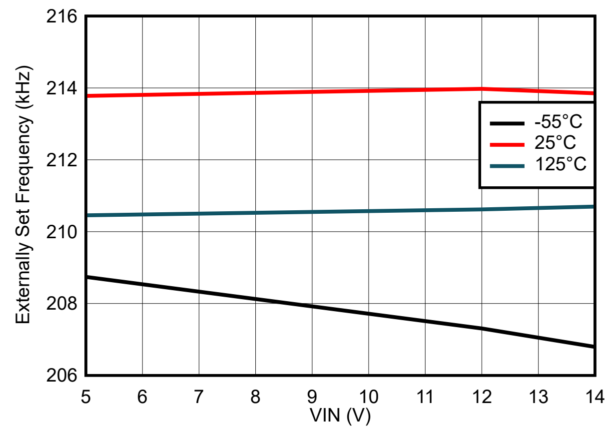
图 7-20. Externally Set Frequency Variation



VIN = 4 V to 5 V

RT = 511 kΩ

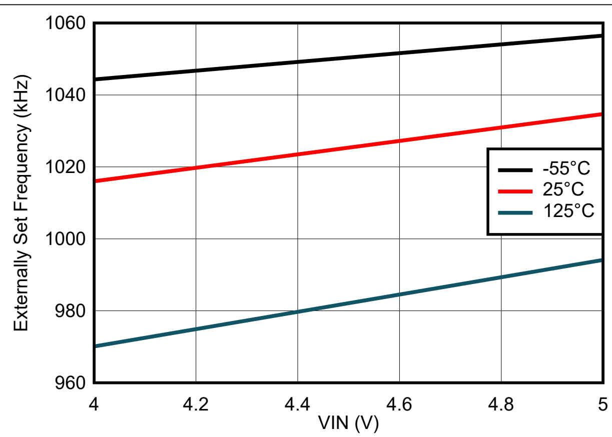
图 7-21. Externally Set Frequency Variation



VIN = 5 V to 14 V

RT = 511 kΩ

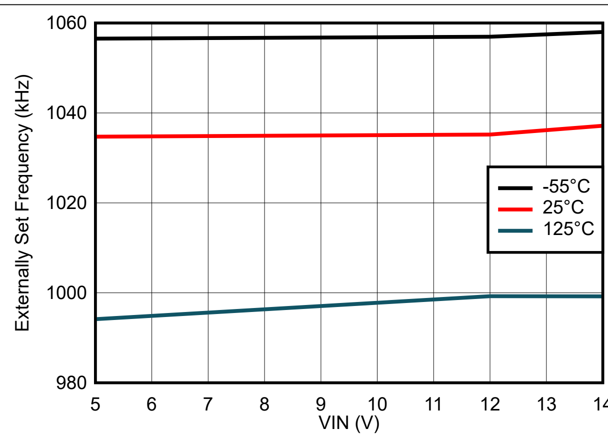
图 7-22. Externally Set Frequency Variation



VIN = 4 V to 5 V

RT = 90.9 kΩ

图 7-23. Externally Set Frequency Variation

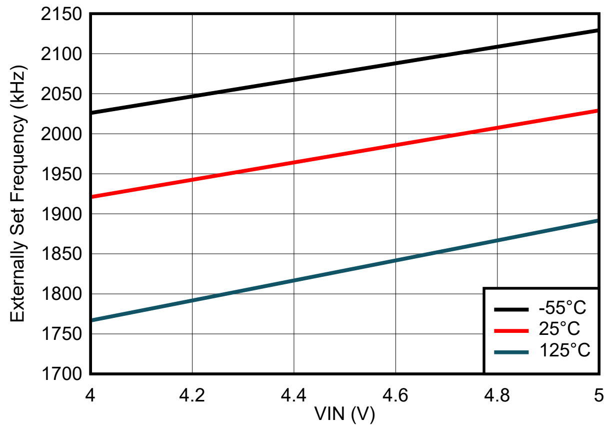


VIN = 5 V to 14 V

RT = 90.9 kΩ

图 7-24. Externally Set Frequency Variation

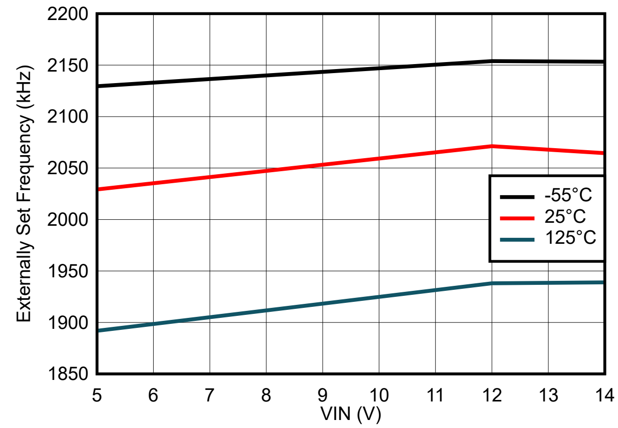
7.10 Typical Characteristics (continued)



VIN = 4 V to 5 V

RT = 34.8 kΩ

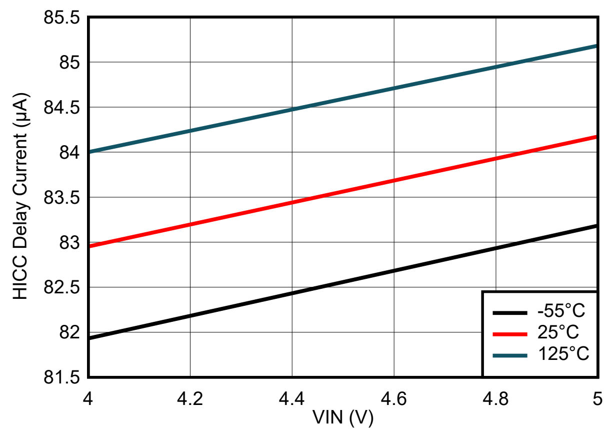
图 7-25. Externally Set Frequency Variation



VIN = 5 V to 14 V

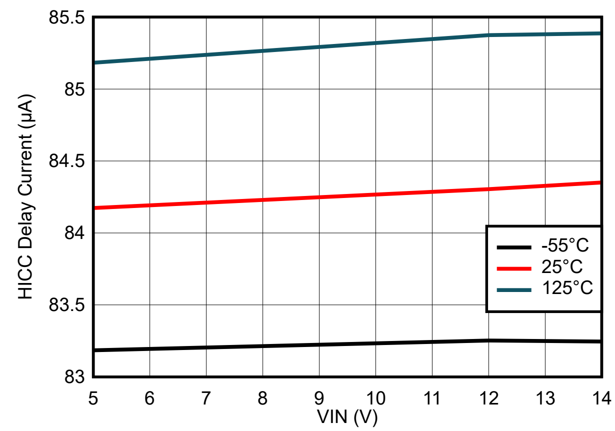
RT = 34.8 kΩ

图 7-26. Externally Set Frequency Variation



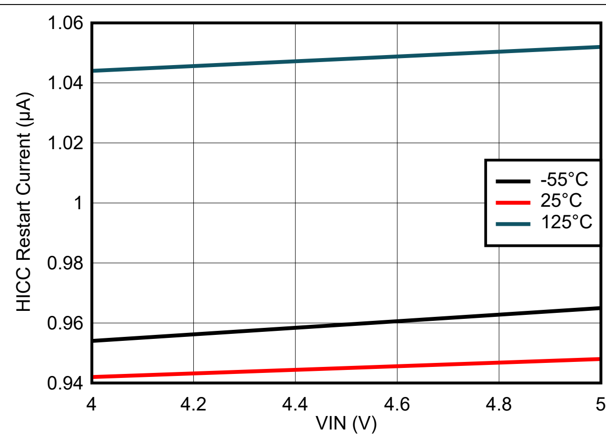
VIN = 4 V to 5 V

图 7-27. Hiccup Delay Current Variation



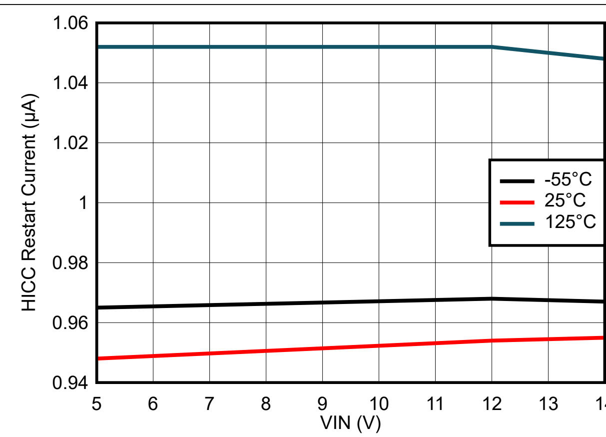
VIN = 5 V to 14 V

图 7-28. Hiccup Delay Current Variation



VIN = 4 V to 5 V

图 7-29. Hiccup Restart Current Variation



VIN = 5 V to 14 V

图 7-30. Hiccup Restart Current Variation

7.10 Typical Characteristics (continued)

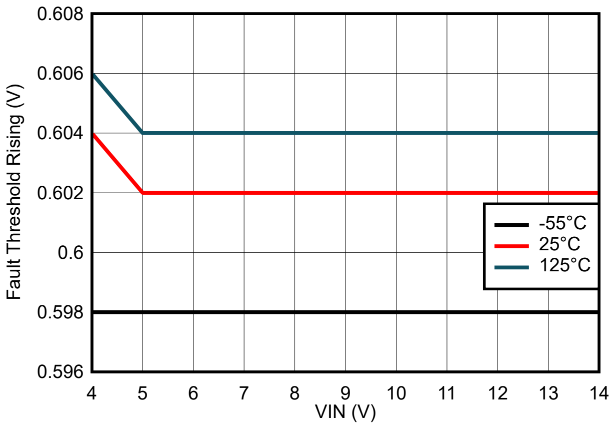


图 7-31. FAULT Threshold Rising Variation

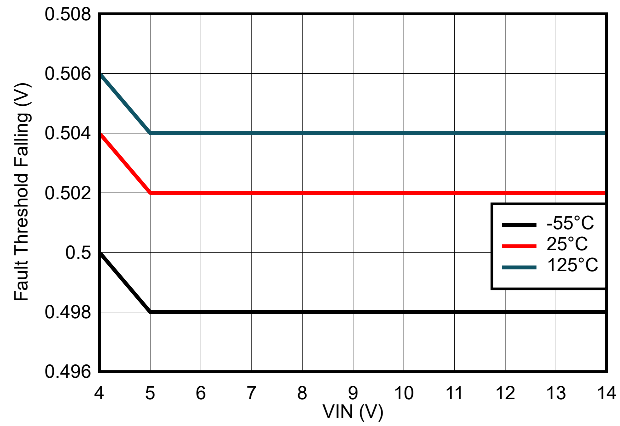
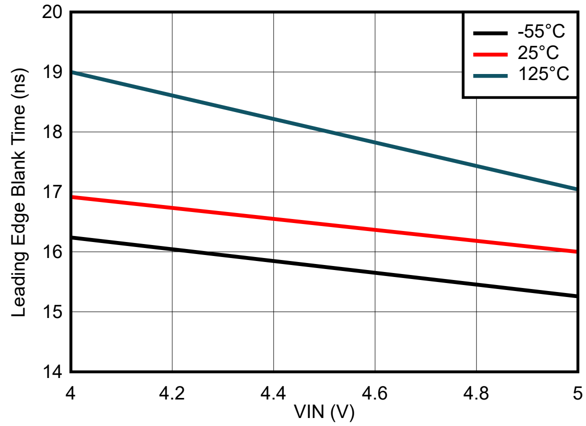


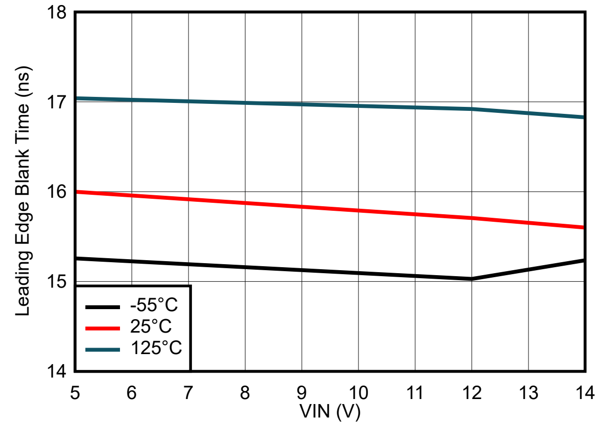
图 7-32. FAULT Threshold Falling Variation



VIN = 4 V to 5 V

RT = 10 kΩ

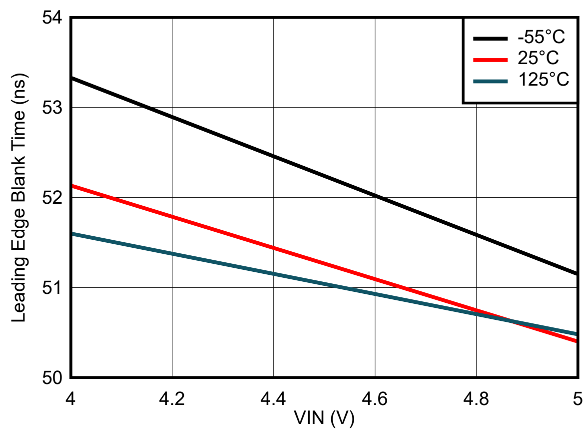
图 7-33. Leading Edge Blank Time Variation



VIN = 5 V to 14 V

RT = 10 kΩ

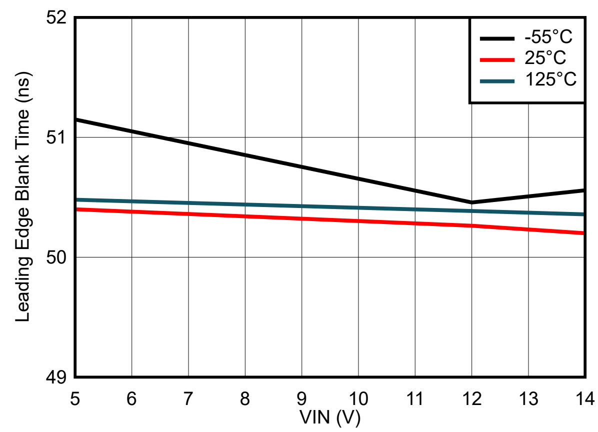
图 7-34. Leading Edge Blank Time Variation



VIN = 4 V to 5 V

RT = 49.9 kΩ

图 7-35. Leading Edge Blank Time Variation

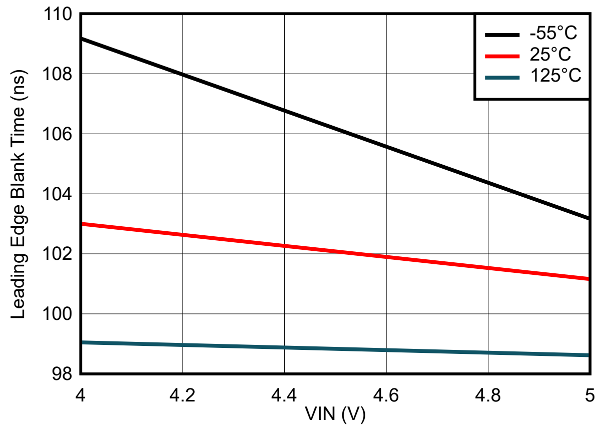


VIN = 5 V to 14 V

RT = 49.9 kΩ

图 7-36. Leading Edge Blank Time Variation

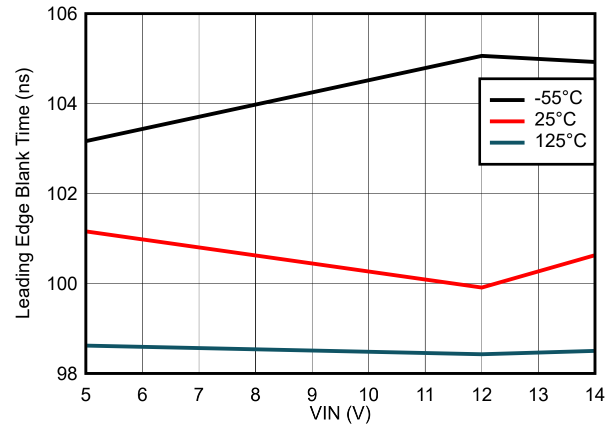
7.10 Typical Characteristics (continued)



VIN = 4 V to 5 V

RT = 100 kΩ

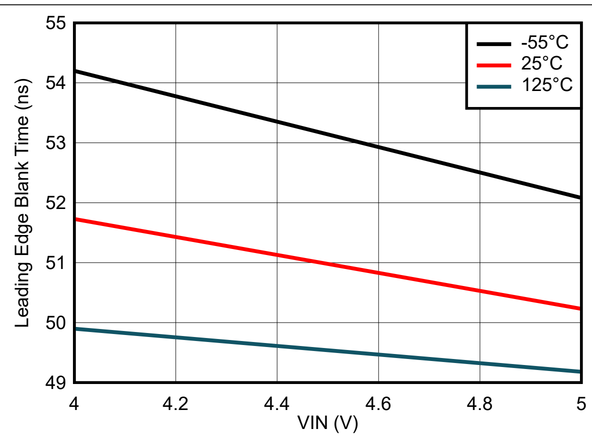
图 7-37. Leading Edge Blank Time Variation



VIN = 5 V to 14 V

RT = 100 kΩ

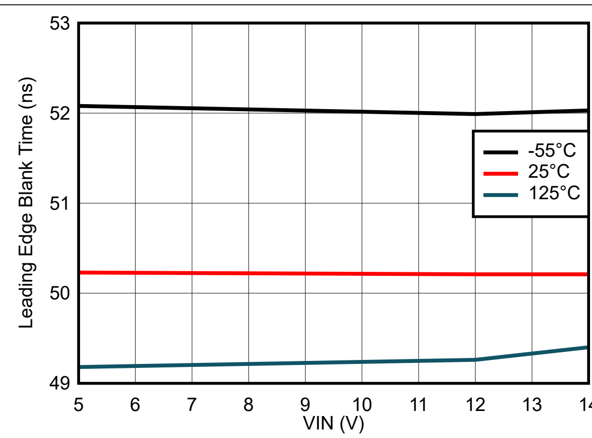
图 7-38. Leading Edge Blank Time Variation



VIN = 4 V to 5 V

TPS7H5003-SP

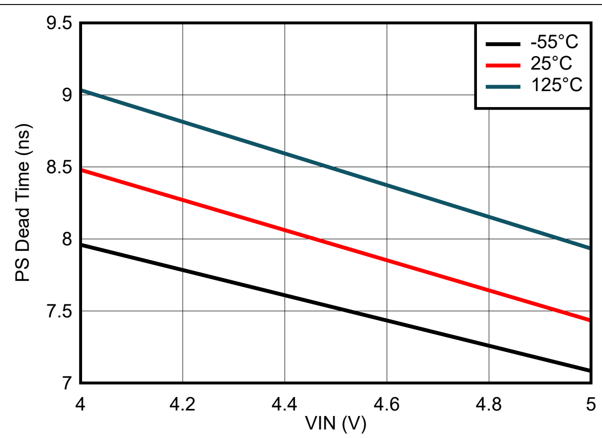
图 7-39. Leading Edge Blank Time Variation



VIN = 5 V to 14 V

TPS7H5003-SP

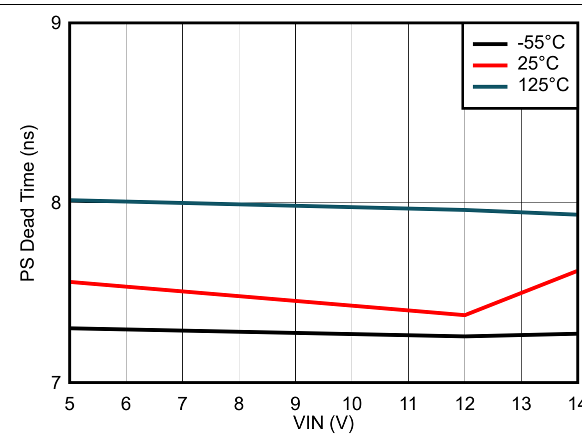
图 7-40. Leading Edge Blank Time Variation



VIN = 4 V to 5 V

RT = Floating

图 7-41. PS Dead Time Variation

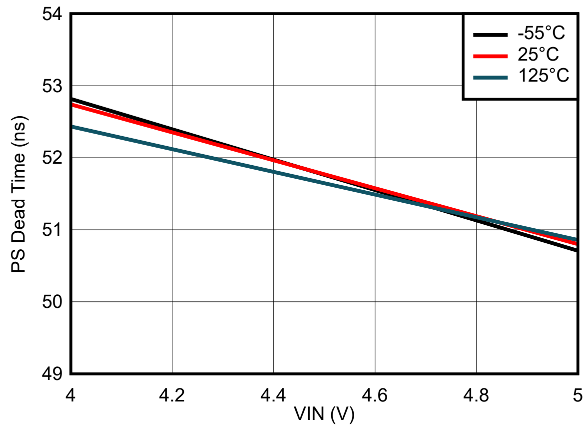


VIN = 5 V to 14 V

RT = Floating

图 7-42. PS Dead Time Variation

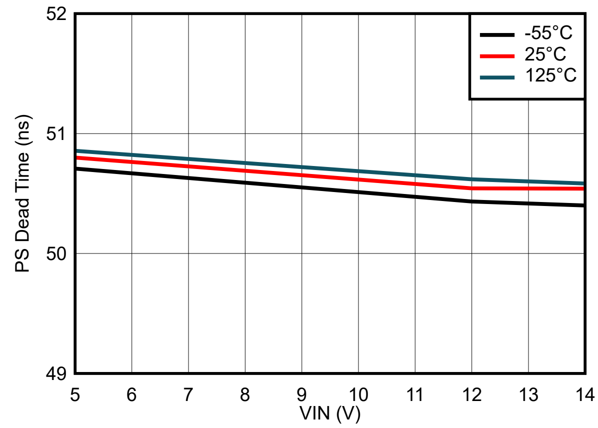
7.10 Typical Characteristics (continued)



VIN = 4 V to 5 V

RT = 49.9 kΩ

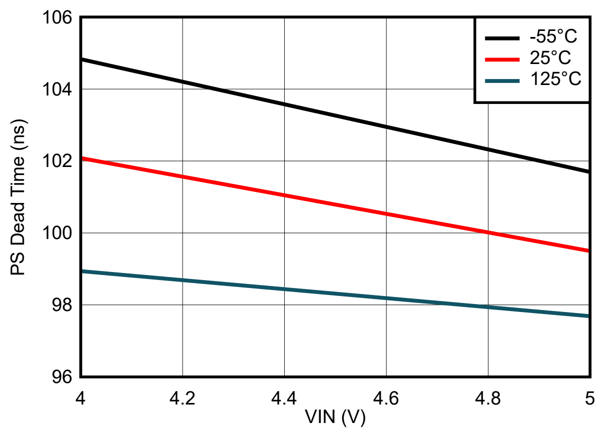
图 7-43. PS Dead Time Variation



VIN = 5 V to 14 V

RT = 49.9 kΩ

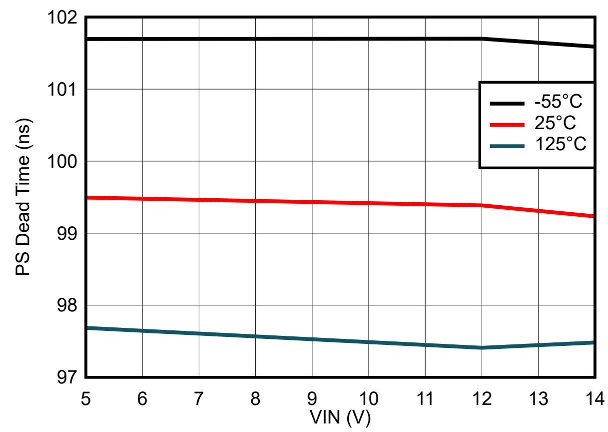
图 7-44. PS Dead Time Variation



VIN = 4 V to 5 V

RT = 100 kΩ

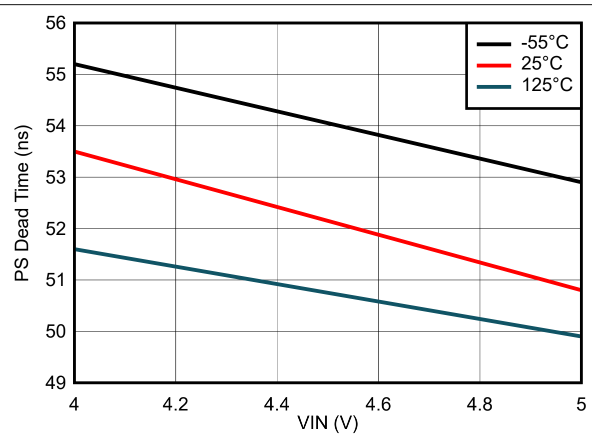
图 7-45. PS Dead Time Variation



VIN = 5 V to 14 V

RT = 100 kΩ

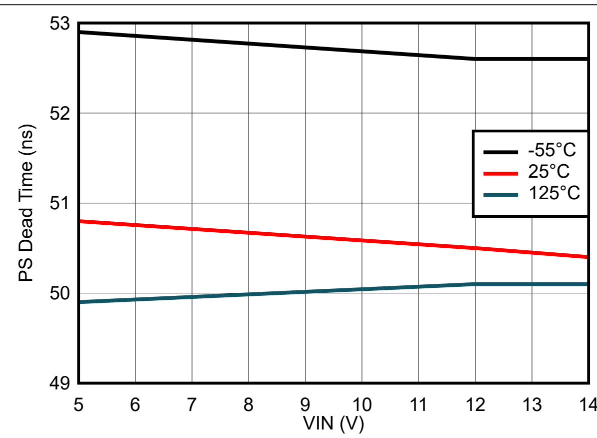
图 7-46. PS Dead Time Variation



VIN = 4 V to 5 V

TPS7H5003-SP

图 7-47. PS Dead Time Variation

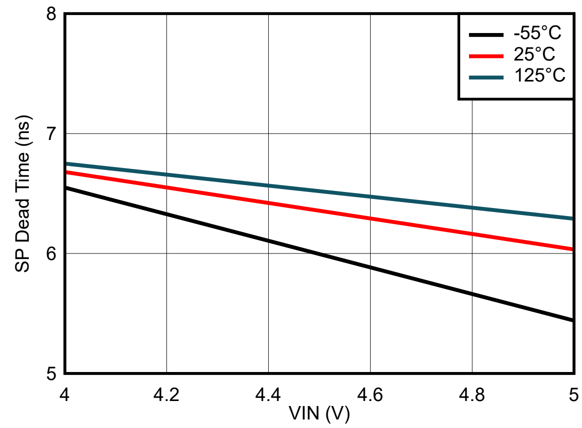


VIN = 5 V to 14 V

TPS7H5003-SP

图 7-48. PS Dead Time Variation

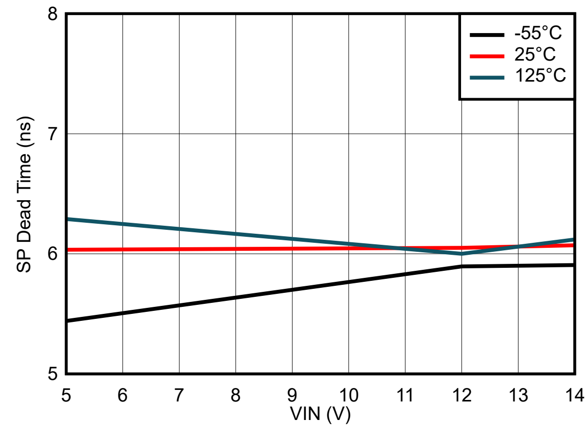
7.10 Typical Characteristics (continued)



VIN = 4 V to 5 V

RT = Floating

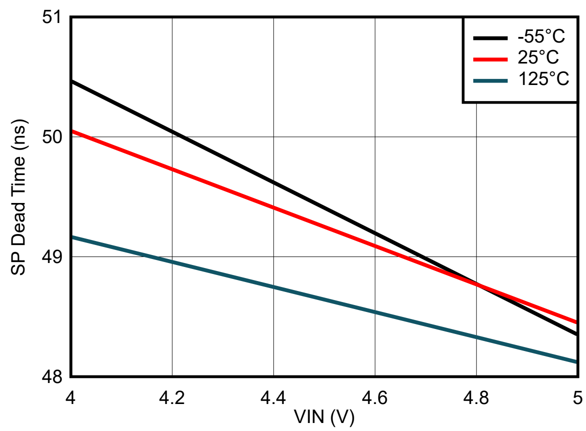
图 7-49. SP Dead Time Variation



VIN = 5 V to 14 V

RT = Floating

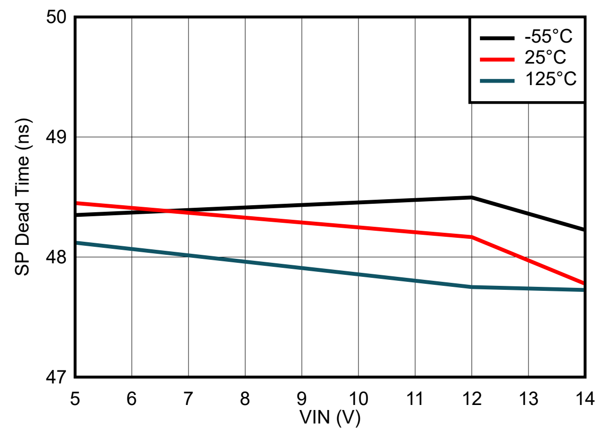
图 7-50. SP Dead Time Variation



VIN = 4 V to 5 V

RT = 49.9 kΩ

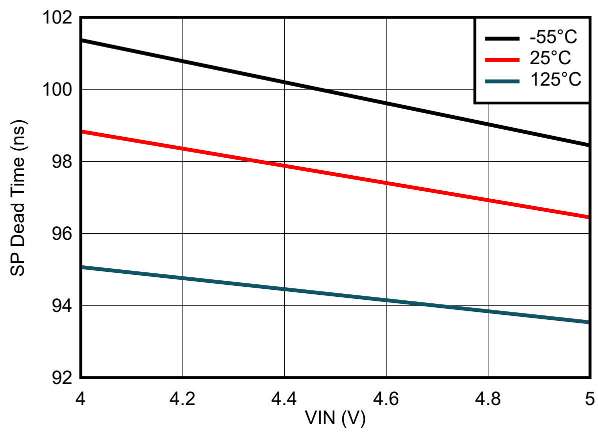
图 7-51. SP Dead Time Variation



VIN = 5 V to 14 V

RT = 49.9 kΩ

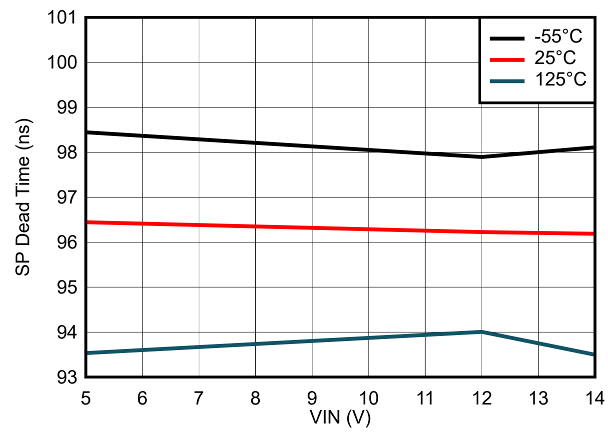
图 7-52. SP Dead Time Variation



VIN = 4 V to 5 V

RT = 100 kΩ

图 7-53. SP Dead Time Variation

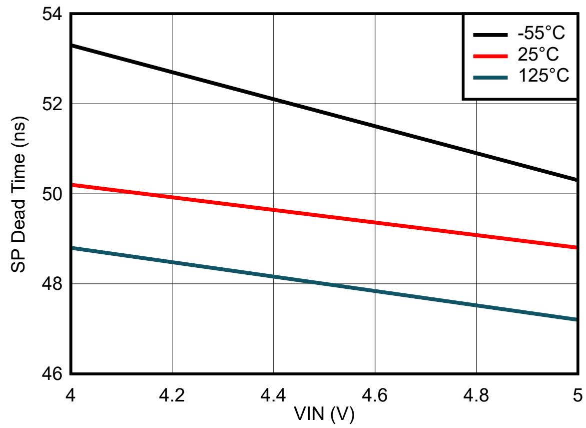


VIN = 5 V to 14 V

RT = 100 kΩ

图 7-54. SP Dead Time Variation

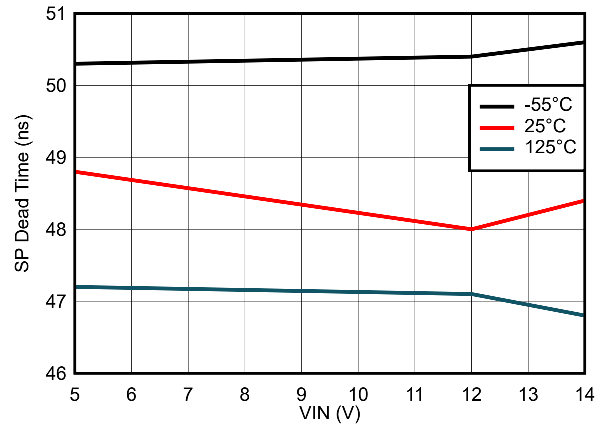
7.10 Typical Characteristics (continued)



VIN = 4 V to 5 V

TPS7H5003-SP

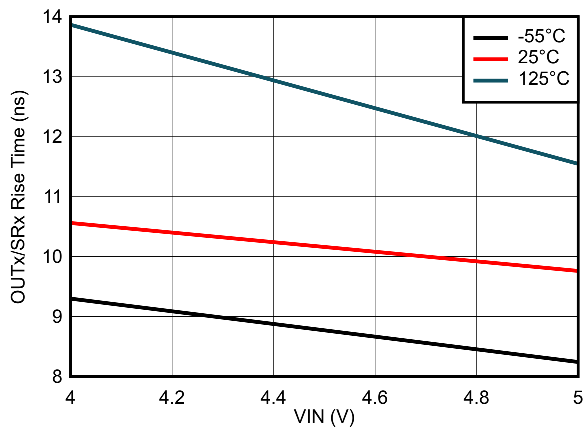
图 7-55. SP Dead Time Variation



VIN = 5 V to 14 V

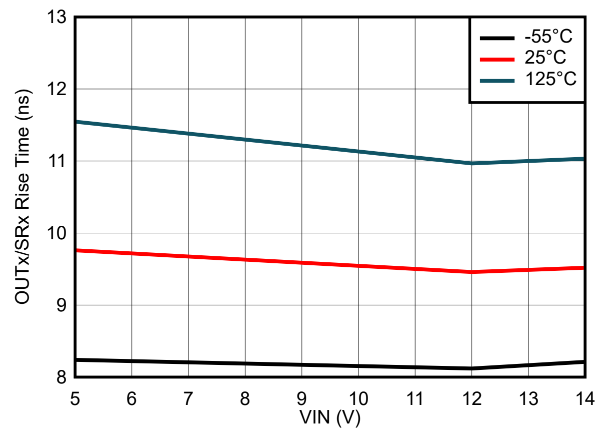
TPS7H5003-SP

图 7-56. SP Dead Time Variation



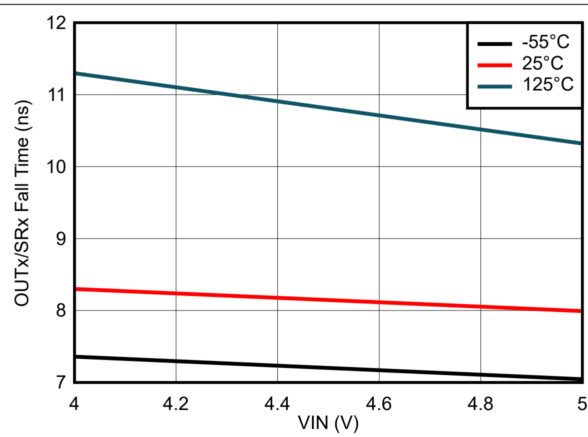
VIN = 4 V to 5 V

图 7-57. Output Rise Time Variation



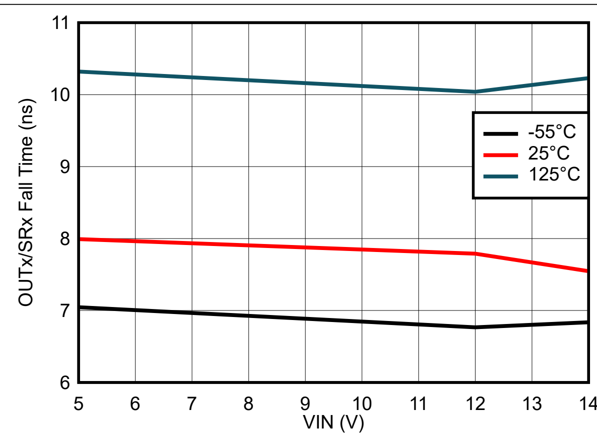
VIN = 5 V to 14 V

图 7-58. Output Rise Time Variation



VIN = 4 V to 5 V

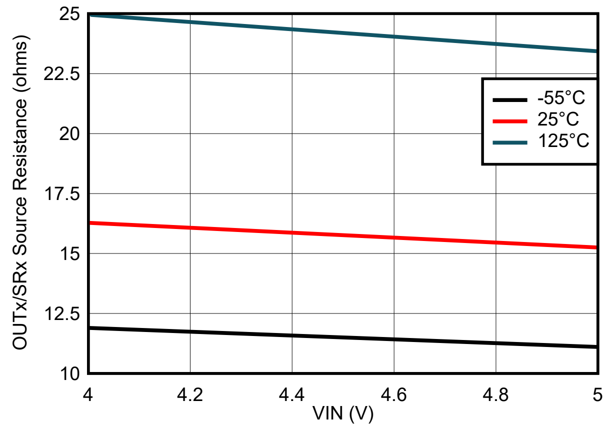
图 7-59. Output Fall Time Variation



VIN = 5 V to 14 V

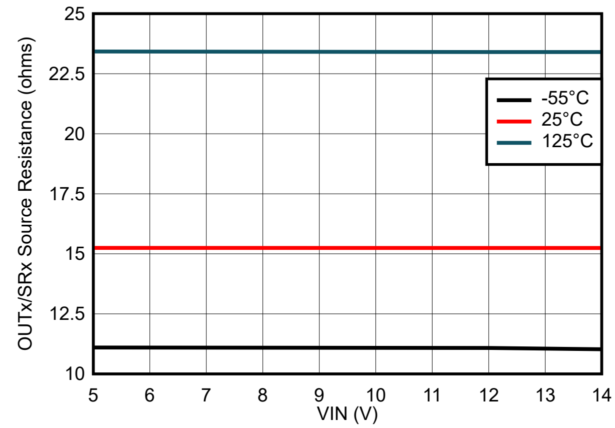
图 7-60. Output Fall Time Variation

7.10 Typical Characteristics (continued)



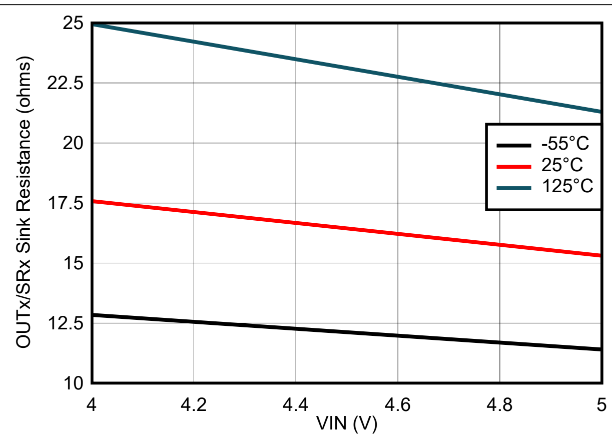
VIN = 4 V to 5 V

图 7-61. Output Source Resistance Variation



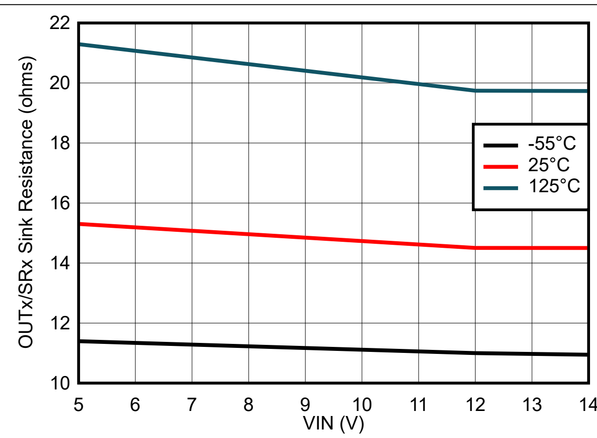
VIN = 5 V to 14 V

图 7-62. Output Source Resistance Variation



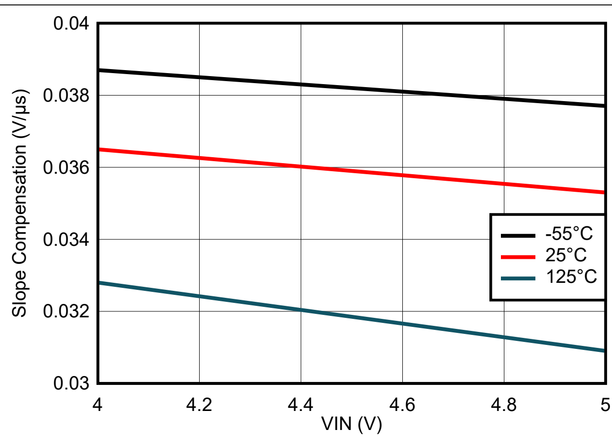
VIN = 4 V to 5 V

图 7-63. Output Sink Resistance Variation



VIN = 5 V to 14 V

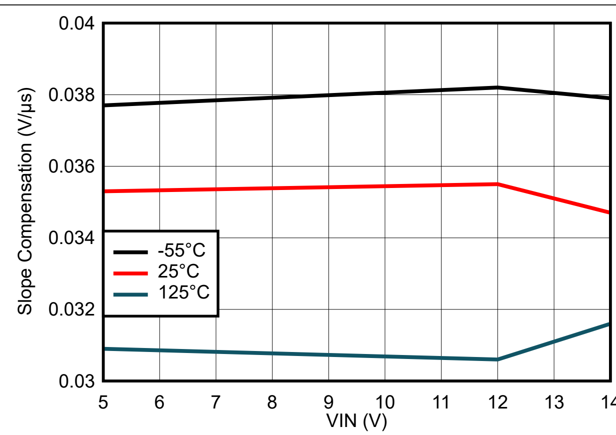
图 7-64. Output Sink Resistance Variation



VIN = 4 V to 5 V

RT = 1.18 MΩ

图 7-65. Slope Compensation Variation

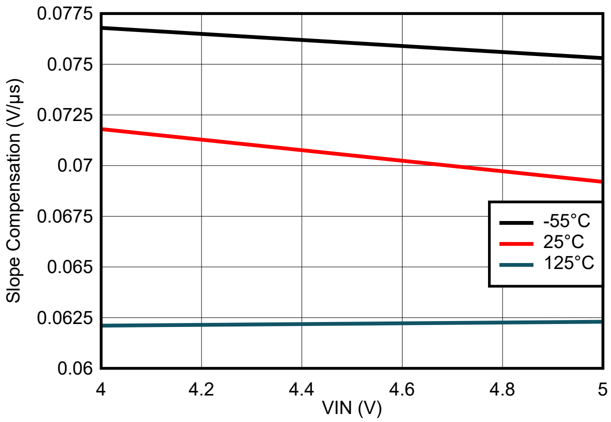


VIN = 5 V to 14 V

RT = 1.18 MΩ

图 7-66. Slope Compensation Variation

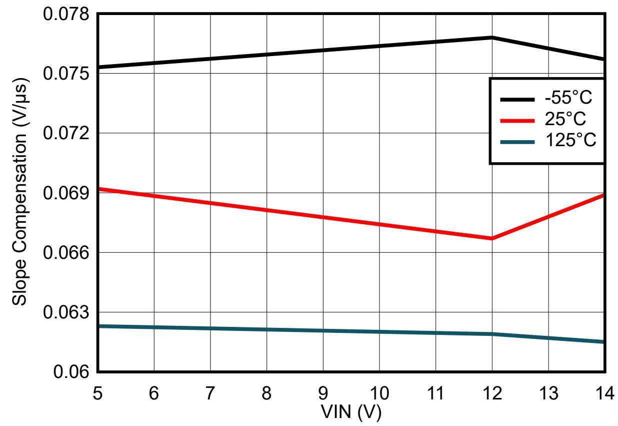
7.10 Typical Characteristics (continued)



VIN = 4 V to 5 V

RT = 562 kΩ

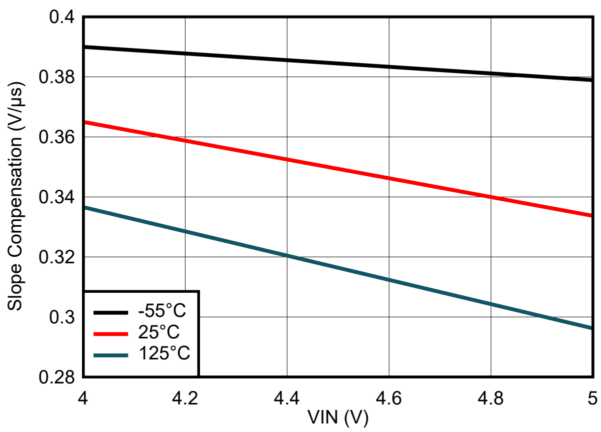
图 7-67. Slope Compensation Variation



VIN = 5 V to 14 V

RT = 562 kΩ

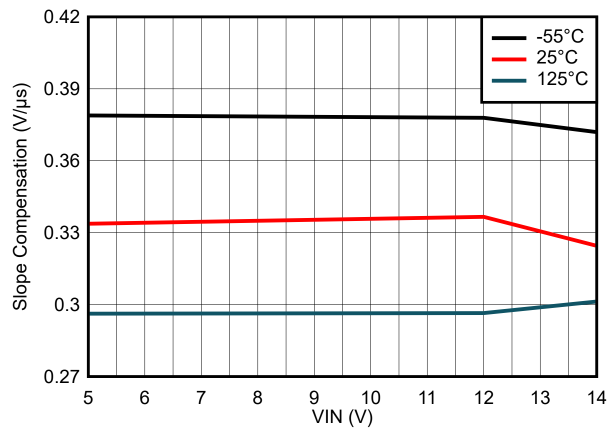
图 7-68. Slope Compensation Variation



VIN = 4 V to 5 V

RT = 100 kΩ

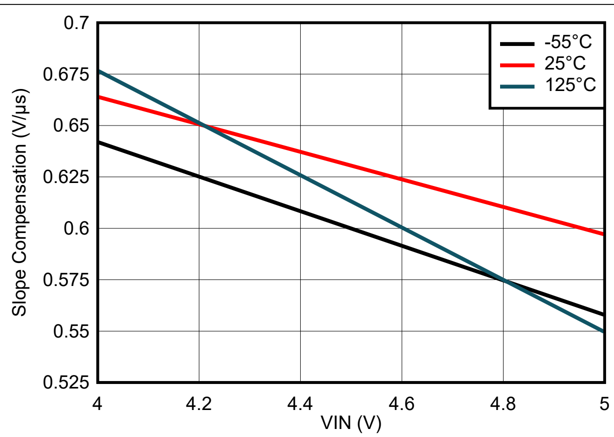
图 7-69. Slope Compensation Variation



VIN = 5 V to 14 V

RT = 100 kΩ

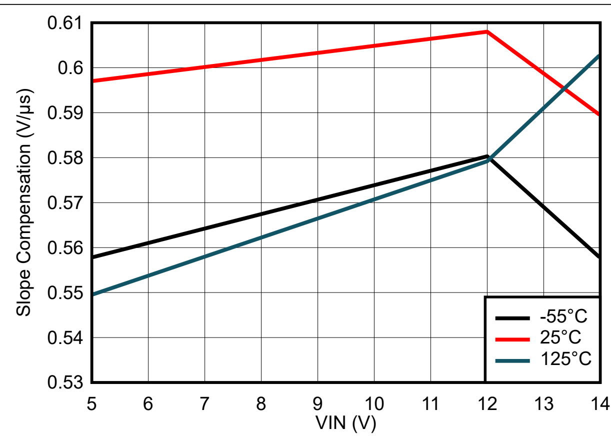
图 7-70. Slope Compensation Variation



VIN = 4 V to 5 V

RT = 49.9 kΩ

图 7-71. Slope Compensation Variation



VIN = 5 V to 14 V

RT = 49.9 kΩ

图 7-72. Slope Compensation Variation

8 Detailed Description

8.1 Overview

The TPS7H500x-SP series is a family of radiation-hardness-assured PWM controllers. Each controller features a voltage reference of 0.613 V with accuracy of +0.7%/-1%. The switching frequency is configurable from 100 kHz to 2 MHz, with external clock synchronization capability. The series consists of the full-featured device TPS7H5001-SP, as well as the three additional specialized controllers TPS7H5002-SP, TPS7H5003-SP, and TPS7H5004-SP.

The TPS7H5001-SP is a radiation-hardness-assured, current mode, dual output PWM controller optimized for silicon (Si) and gallium nitride (GaN) based DC-DC converters in space applications. The switching frequency of the TPS7H5001-SP can be configured from 100 kHz to 2 MHz while still maintaining a very low current consumption, which makes it ideal for fully exploiting the area reduction and high efficiency benefits of GaN based DC-DC converters. The device features integrated synchronous rectifier control outputs and dead-time programmability in order to target high efficiency and high performance topologies. In addition, the TPS7H5001-SP supports single-ended converter topologies by providing the user flexibility to control the maximum duty cycle. The 0.613-V +0.7%/-1% accurate internal reference allows design of high-current buck converters for FPGA core voltages.

The TPS7H5002-SP is a single output radiation-hardness-assured PWM controller that supports buck applications and single ended isolated topologies. The controller contains an integrated synchronous rectification output. Optimized for GaN power semiconductor based applications, the controller has configurable dead time and configurable leading edge blank time. The controller can be configured for maximum duty cycle of 75% or 100%. As such, the DCL pin can be left floating or connected to VLDO. Connection of the DCL pin to AVSS is not permissible for this device.

The TPS7H5003-SP is also a single output radiation-hardness-assured PWM controller that contains an integrated synchronous rectification output. The dead time and leading edge blank time are fixed at 50 ns for this device. The controller can be configured for maximum duty cycle of 75% or 100%. As such, the DCL pin can be left floating or connected to VLDO. Connection of the DCL pin to AVSS is not permissible for this device.

The TPS7H5004-SP is a dual output radiation-hardness-assured PWM controller suited for usage in non-synchronous push-pull and full-bridge topologies. The controller has configurable leading edge blank time. The maximum duty cycle for this device is 50% and the DCL pin must be connected to AVSS.

8.2 Functional Block Diagram

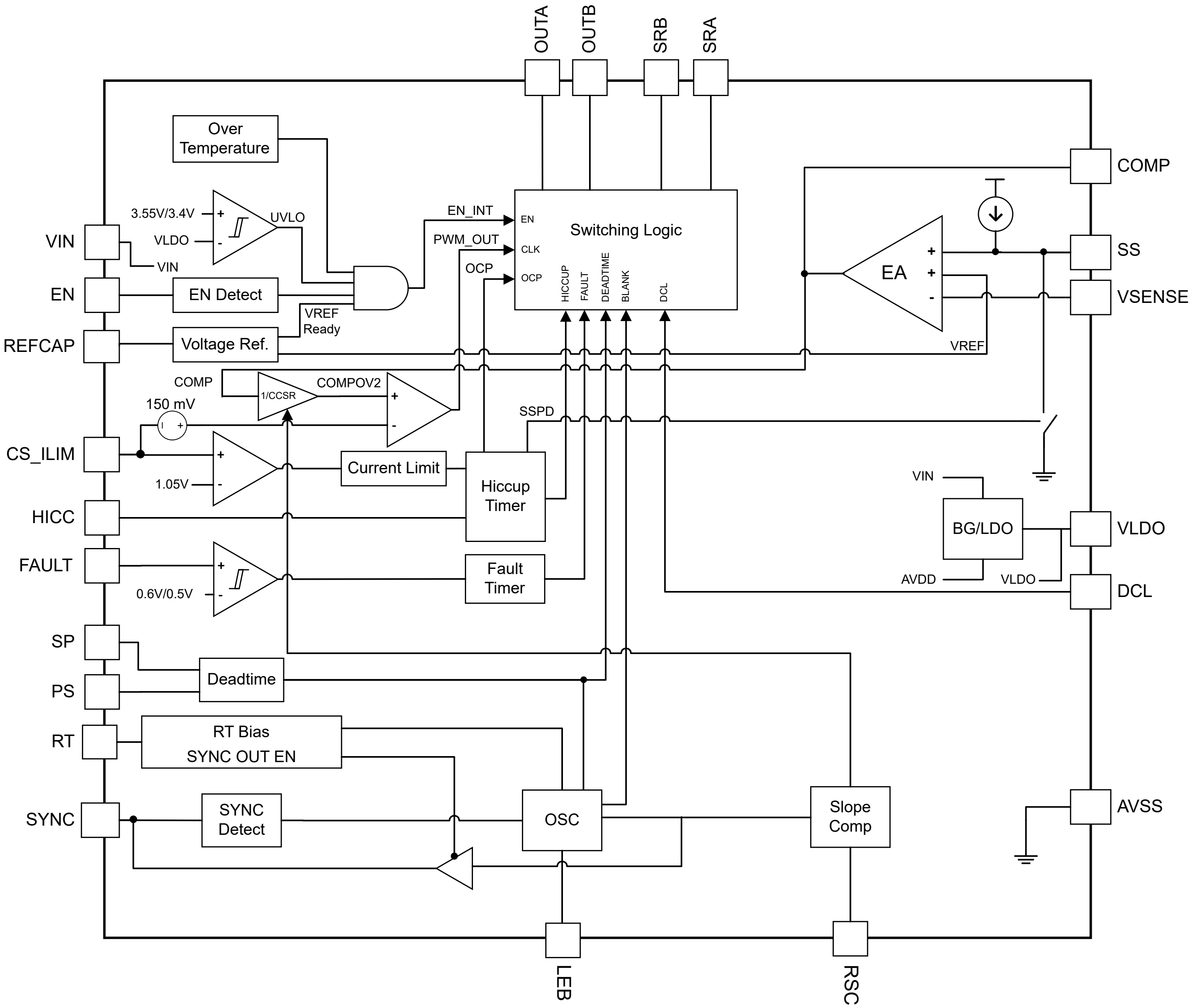


图 8-1. TPS7H5001-SP Functional Block Diagram

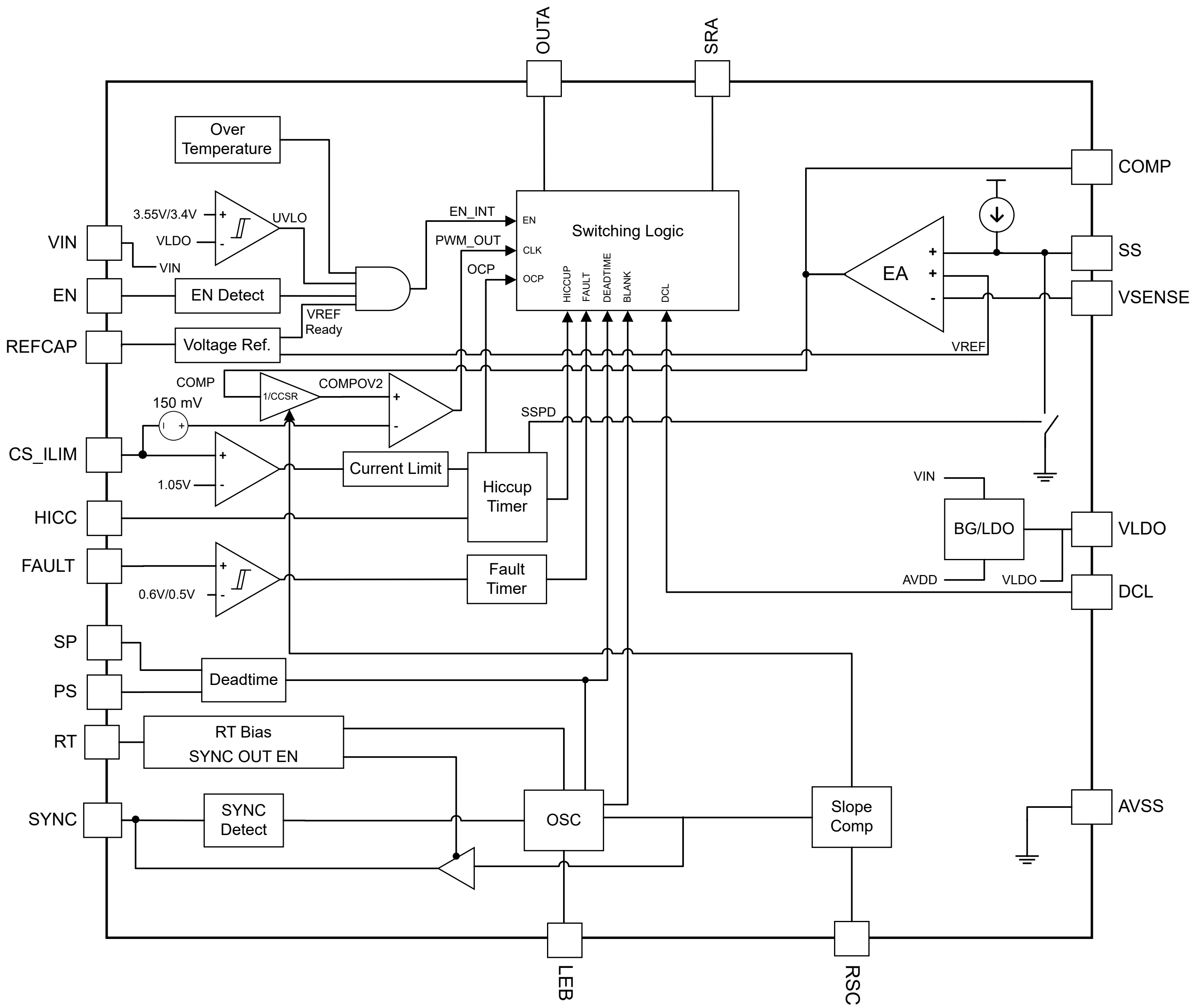


图 8-2. TPS7H5002-SP Functional Block Diagram

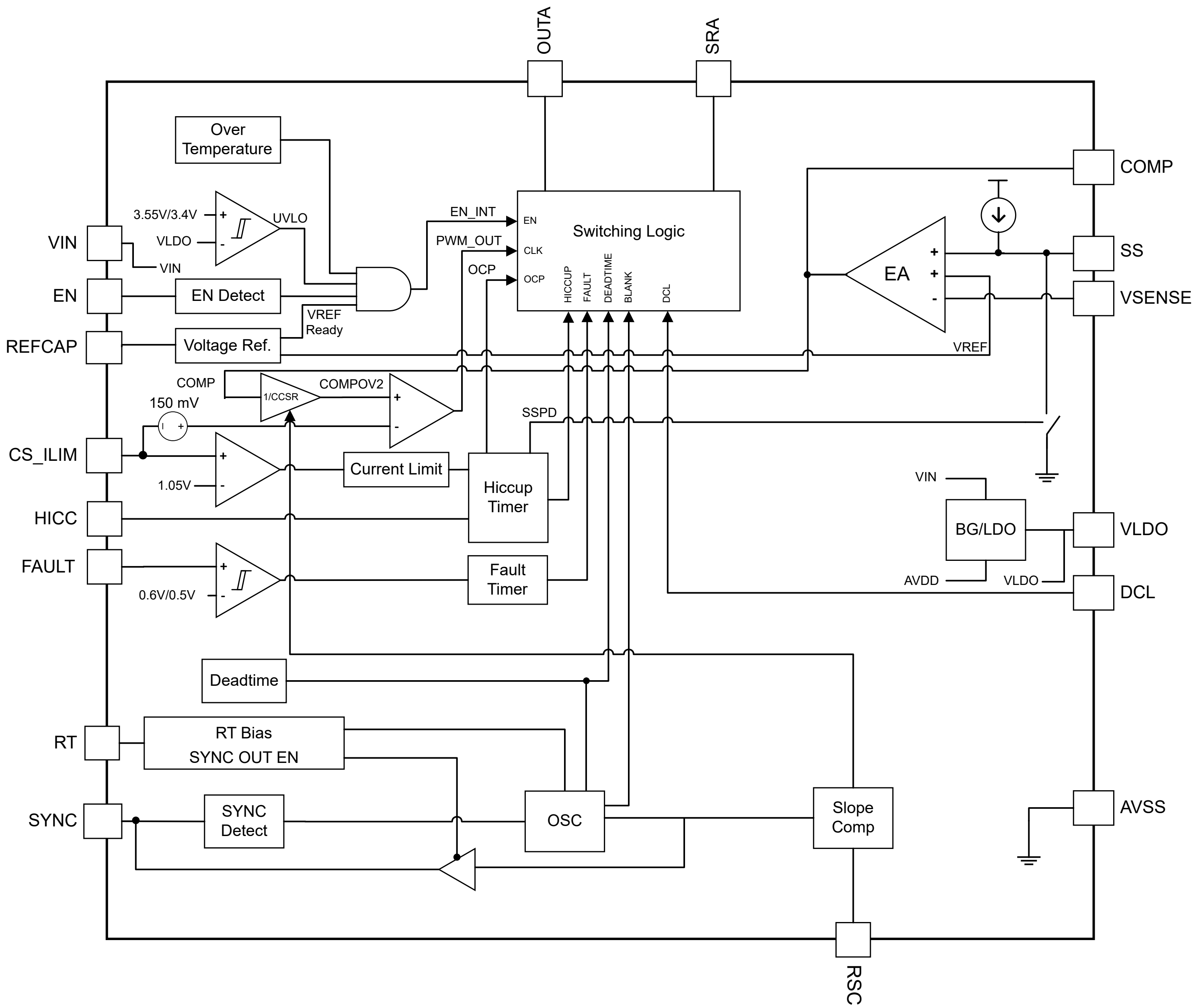


图 8-3. TPS7H5003-SP Functional Block Diagram

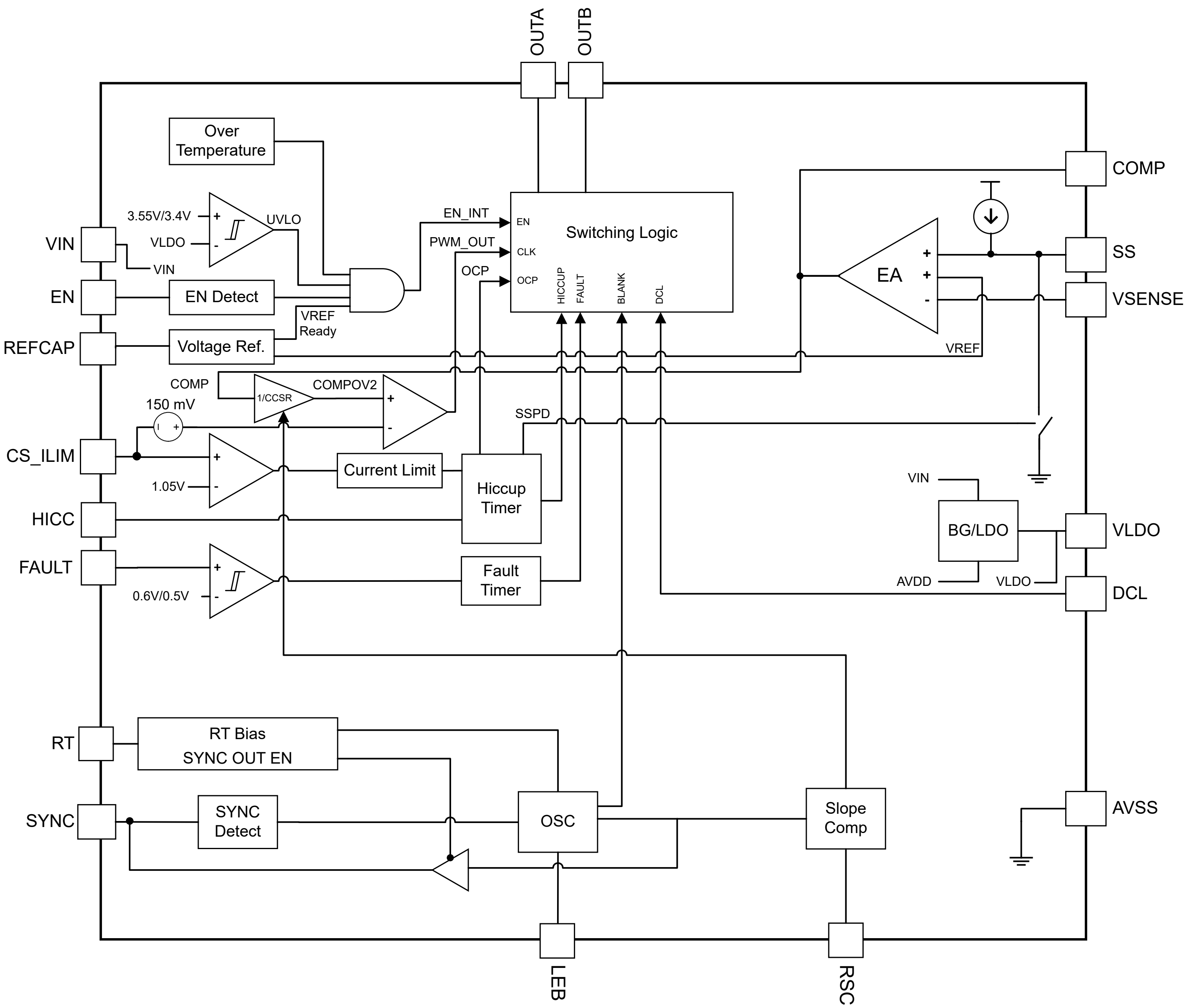


图 8-4. TPS7H5004-SP Functional Block Diagram

8.3 Feature Description

8.3.1 VIN and VLDO

During steady state operation, the input voltage of the TPS7H500x-SP must be between 4 V and 14 V. A minimum bypass capacitance of at least 0.1 µF is needed between VIN and AVSS. The input bypass capacitors should be placed as close to the controller as possible.

The voltage applied at VIN serves as the input for the internal regulator that generates the VLDO voltage (5 V). At input voltages less than 5 V, the VLDO voltage will follow the voltage at VIN. Recommended capacitance for VLDO is 1 µF. The EN and/or DCL pin can be tied to VLDO, but otherwise it is recommended to not externally load this pin due to limited output current capability.

A voltage divider connected between VIN and the EN pin can adjust the input voltage UVLO appropriately.

8.3.2 Start-Up

Before the primary outputs of the controller will start switching, the following conditions must be met:

- VLDO exceeds the rising UVLO threshold of 3.55 V (typical)
- The internal 0.613 V reference voltage is available
- The enable signal EN is above the rising voltage threshold of 0.6 V (typical)
- The FAULT pin voltage is below the rising voltage threshold of 0.6 V (typical)
- The device junction temperature is below the thermal shutdown threshold of 175°C (typical)

Once all of the aforementioned conditions are satisfied, the soft-start process will be initiated.

8.3.3 Enable and Undervoltage Lockout (UVLO)

There are several methods for enabling the TPS7H500x-SP through the EN pin. The pin can be tied directly to VLDO, which would allow for the device to be enabled as soon as the voltage on VLDO surpasses the rising edge voltage threshold of the EN pin. The pin can also be driven with an externally generated signal or a compatible PGOOD signal for instances in which sequencing is desired. Lastly, two resistors can be used to program the controller to enable when VIN surpasses a user determined threshold, as shown in 图 8-5 . The two resistors are configured as a divider, with one between VIN and EN and the other between EN and AVSS.

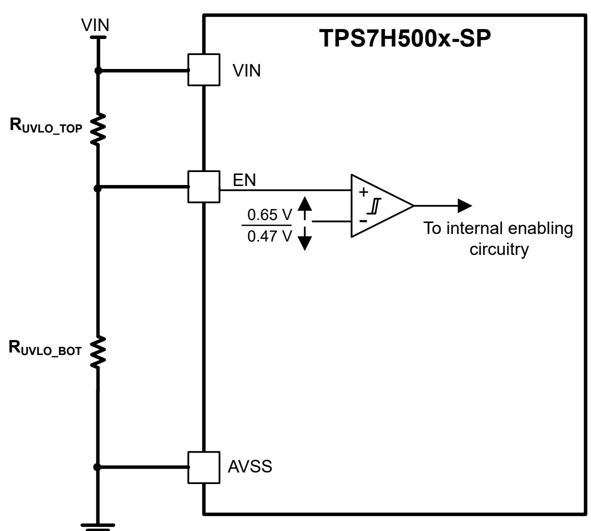


图 8-5. Enable Pin Configuration Using Two External Resistors

Using 方程式 1, the user can calculate the value for R_{UVLO_TOP} for a chosen value of R_{UVLO_BOT} based on the desired maximum start-up voltage for the device. With these selected resistors 方程式 2 can be used to determine the minimum start-up voltage.

$$R_{UVLO\_TOP} = R_{UVLO\_BOT} \times \left(\frac{V_{START,MAX}}{V_{EN\_RISING\_MAX}} - 1 \right) \tag{1}$$

$$V_{START,MIN} = V_{EN\_RISING\_MIN} \times \left(\frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right) \tag{2}$$

In the two-resistor configuration of 图 8-5, the controller will also shut down due to undervoltage lockout when the input voltage falls below a particular threshold. This is due to the hysteresis of the EN pin. In order to determine the voltages at which shutdown is expected to occur, use 方程式 3 and 方程式 4.

$$V_{STOP,MAX} = V_{EN\_FALLING\_MAX} \times \left(\frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right) \tag{3}$$

$$V_{STOP,MIN} = V_{EN\_FALLING\_MIN} \times \left(\frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right) \tag{4}$$

It is important to note that the user should take care when selecting the values for R_{UVLO_TOP} and R_{UVLO_BOT}. It is recommended to optimize the selection of these resistors for start-up in order to ensure proper operation. The UVLO value must be approximately 75% or less of the input voltage in order to ensure that the device turns on as expected under all circumstances. Setting the UVLO any higher may cause issues with the turn-on of the device. 图 8-6 shows the expected start-up and UVLO voltages on a 12-V rail where the maximum start-up voltage is 90% of the nominal input voltage. In this instance, turn-off will occur when the input voltage falls to between 75% and 65% of its nominal value.

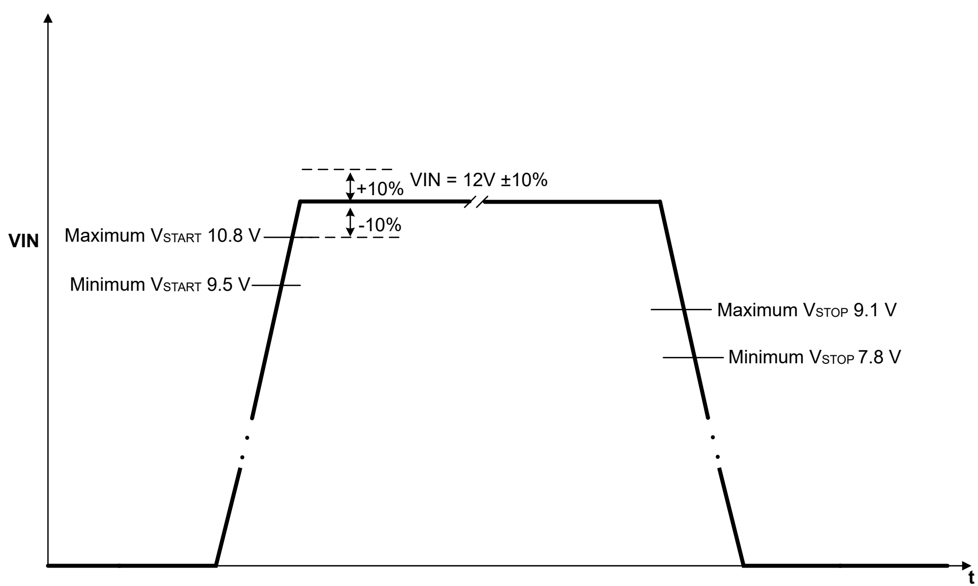


图 8-6. Start-Up and UVLO Values for Two-Resistor Configuration With VIN = 12 V

8.3.4 Voltage Reference

Each device generates an internal 1.23-V bandgap reference that is utilized throughout the various control logic blocks. This is the voltage present on the REFCAP pin during steady state operation. This voltage is divided down to 0.613 V to produce the reference for the error amplifier. The error amplifier reference is measured at the COMP pin to account for offsets in the error amplifier and maintains regulation within +0.7%/-1% across line, load, temperature, and TID as shown in 节 7. This tight reference tolerance allows for the user to design a highly accurate power converter. A 470-nF capacitor to ground is required at the REFCAP pin for proper electrical operation as well as to ensure robust SET performance of the device.

8.3.5 Error Amplifier

Each TPS7H500x-SP controller uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS pin voltage or the internal 0.613-V voltage reference. The transconductance of the error amplifier is 1800 µA/V during normal operation. The frequency compensation network is connected between COMP pin and AVSS. The error amplifier DC gain is typically 10,000 V/V.

8.3.6 Output Voltage Programming

The output voltage of the power converter is set by using a resistor divider from V_{OUT} of the converter to the VSENSE pin. The output voltage must be divided down to nominal voltage reference of 0.613 V. 方程式 5 can be used to select R_{BOTTOM}.

$$R_{BOTTOM} = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{TOP} \tag{5}$$

where:

- V_{REF} is 0.613 V (typical)
- V_{OUT} is the desired output voltage
- R_{TOP} is the value of the top resistor, selected by the user (i.e. 10 kΩ)

The recommendation is to use high tolerance resistors (1% or less) for R_{BOTTOM} and R_{TOP} for improved output voltage setpoint accuracy.

8.3.7 Soft Start (SS)

The soft-start circuit increases the output voltage of the converter gradually until the steady-state programmed output is reached. During soft start, the error amplifier uses the voltage on the soft-start pin as its reference until the SS pin voltage rises above V_{REF}. Once the voltage at SS pin is above V_{REF}, the soft-start period is complete. Note that the voltage at SS pin will continue to rise and once it reaches 1 V, the synchronous rectifier outputs of the controller will become active.

A capacitor between the SS pin and AVSS controls the soft-start time of the PWM controller. The following equation can be used to select the capacitor for the desired soft-start time:

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}} \tag{6}$$

where:

- t_{SS} is the desired soft-start time
- V_{REF} is voltage reference of 0.613 V (typical)
- I_{SS} is the soft-start charging current of 2.7 µA (typical)

8.3.8 Switching Frequency and External Synchronization

Each TPS7H500x-SP controller has three modes for setting the switching frequency of the device: internal oscillator, external synchronization, and primary-secondary. The device is placed on one of these modes through unique configurations of the RT and SYNC pins. Primary-secondary mode can be used when it is desired for two controllers to have synchronized switching without the use of the external clock.

8.3.8.1 Internal Oscillator Mode

A resistor from the RT pin to AVSS sets the switching frequency of the device. The TPS7H500x-SP controller has a switching frequency range of 100 kHz to 2 MHz. In internal oscillator mode, the RT pin must be populated or the controller will not perform any switching. 方程式 7 shows the calculation determining the RT value for a desired switching frequency. The curve in 图 8-7 shows the RT value that corresponds to a given switching frequency for the TPS7H5001-SP.

$$RT = \frac{112000}{f_{sw}} - 19.7 \tag{7}$$

where:

- RT is in kΩ
- f_{sw} is in kHz

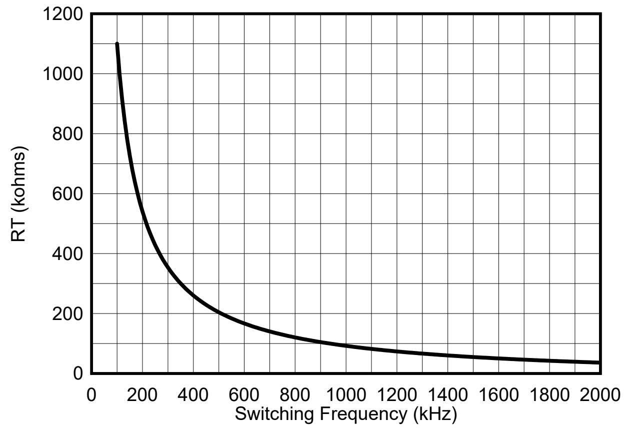


图 8-7. RT vs Switching Frequency

In this mode, the SYNC pin is configured as an output and produces a clock signal with a frequency that is twice that of the switching frequency set by RT. As such, this clock signal has a range of 200 kHz to 4 MHz. This SYNC output clock signal is in phase with the switching frequency of the device. 图 8-8 shows typical waveforms for the controller in this mode of operation. Note that the OUTB waveform is only applicable for TPS7H5001-SP and TPS7H5004-SP.

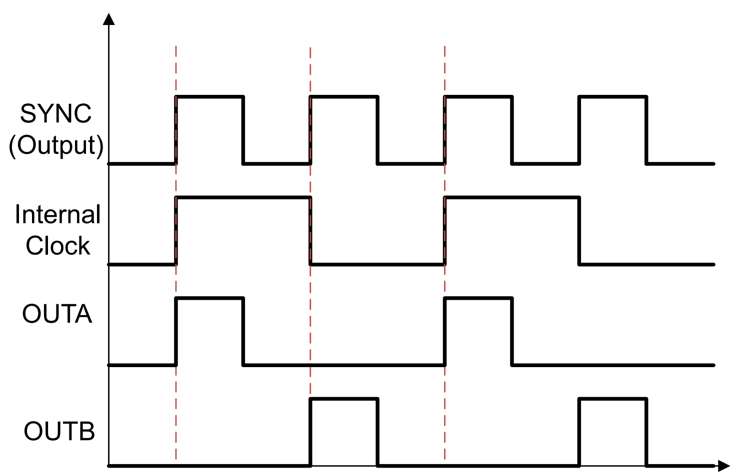


图 8-8. Switching Waveforms for Internal Oscillator Mode

8.3.8.2 External Synchronization Mode

Each controller can be used in external synchronization mode by leaving the RT pin floating and applying a clock to the SYNC pin. Note than the RT pin configuration sets the oscillator mode of the controller and must be left floating for this mode of operation. The external clock that is applied must be set to twice the desired switching frequency (i.e. a 1-MHz applied clock is needed for 500-kHz switching frequency). The external clock must be in the range of 200 kHz to 4 MHz with a duty cycle between 40% and 60%. It is recommended to use an external clock with 50% duty cycle. The controller will internally invert the clock signal that is applied at the SYNC pin during this mode. Since the controller does not perform any switching with RT floating, the applied clock must be present before OUTA and OUTB will become active for external synchronization mode. 图 8-9 shows the switching waveforms for the controller in external synchronization mode. Note that the OUTB waveform is only applicable for TPS7H5001-SP and TPS7H5004-SP.

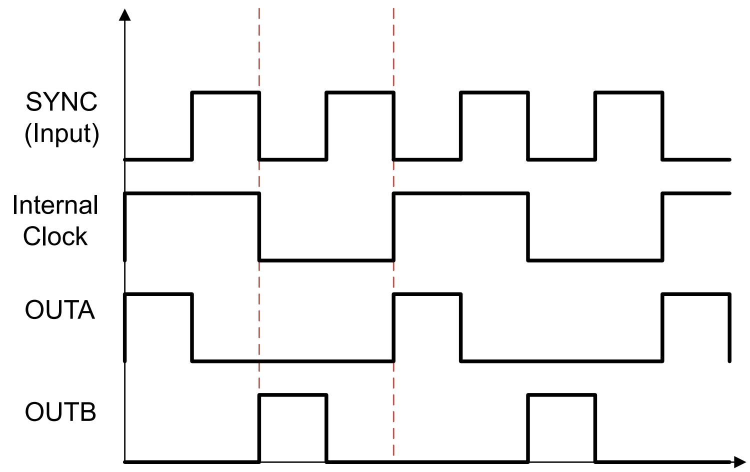


图 8-9. Switching Waveforms for External Synchronization Mode

8.3.8.3 Primary-Secondary Mode

Two TPS7H500x-SP controllers can be operated in a primary-secondary mode by utilizing the SYNC pin. As mentioned in the *Internal Oscillator* section, when RT is selected to provide the desired switching frequency, SYNC outputs a clock signal at twice the switching frequency. As such, the clock input generated by the primary device be used as the clock input at SYNC for the secondary controller, which would operate in external synchronization mode. This means that the RT pin of the primary device should be populated while the corresponding pin of the secondary device would be left floating.

The primary-secondary mode would be useful in a couple of scenarios. The first is for two independent converters that need to be synchronized to the same switching frequency. In this instance, the converters can be two converters can have different operating conditions or topologies. Besides the shared SYNC signal, there are no connections between the two converters.

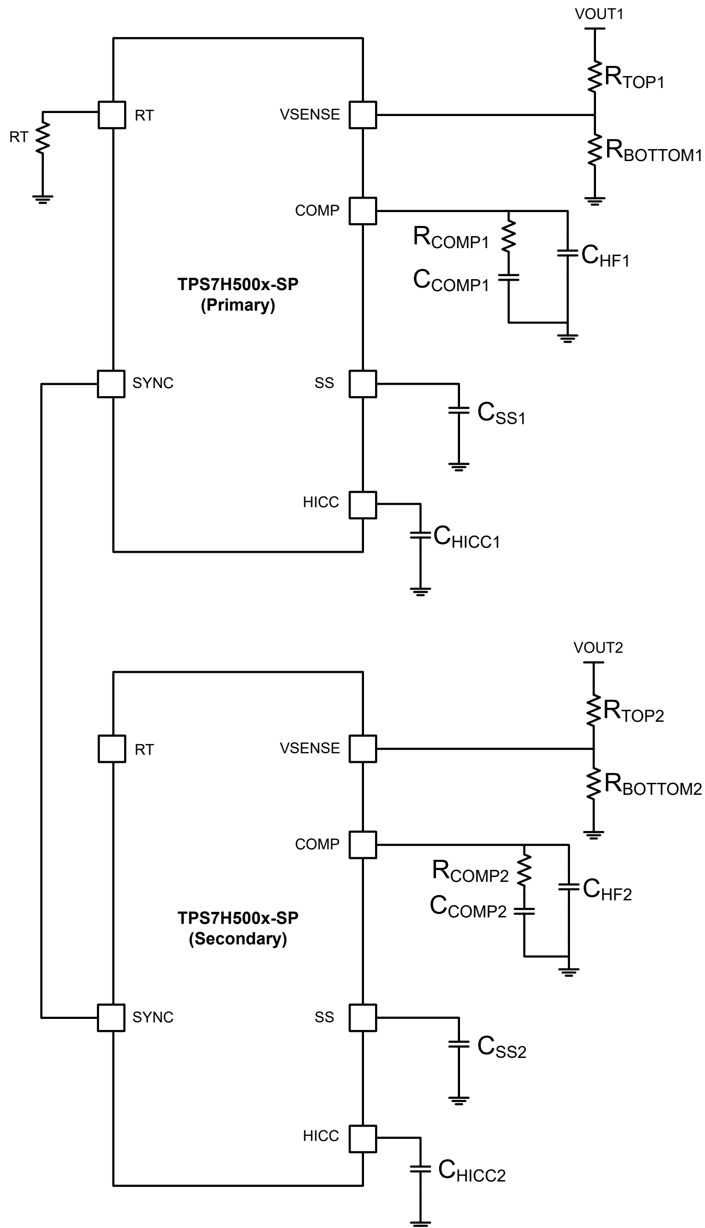


图 8-10. Primary-Secondary Mode Configuration for Two Independent Converters

In a second scenario, two controllers can be used to design a single interleaved converter with phases in parallel. In this design, the VSENSE, COMP, SS, and HICC pins would need to be connected in addition to the shared SYNC connection.

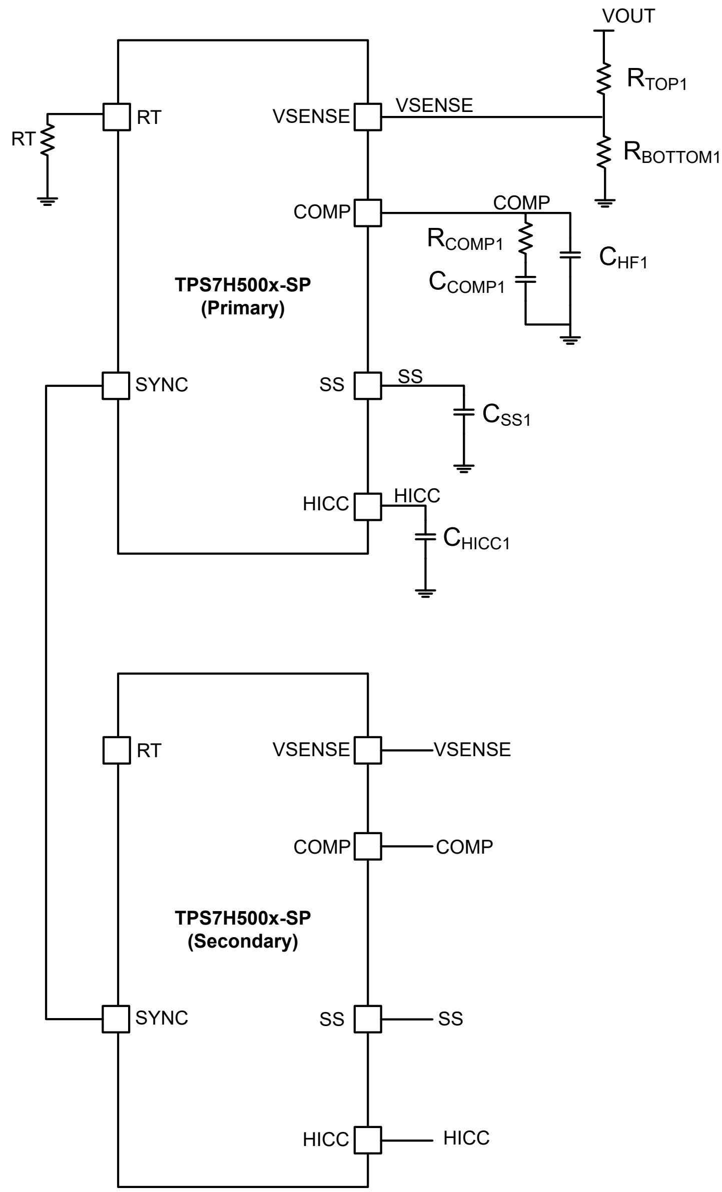


图 8-11. Primary-Secondary Mode Configuration for Parallel Operation

When using two controllers in primary-secondary mode, it is important to note that secondary controller will invert the clock signal that it receives from the primary controller. As such, there will be phase shift between the switching outputs of the primary and secondary controllers. This phase shift from an output (i.e. OUTA) on the primary controller to the corresponding output on the secondary controller will be 90° or 270°, depending on when the secondary device synchronizes to its clock input. Note that in 图 8-12, the waveforms for OUTB are only applicable for TPS7H5001-SP and TPS7H5004-SP.

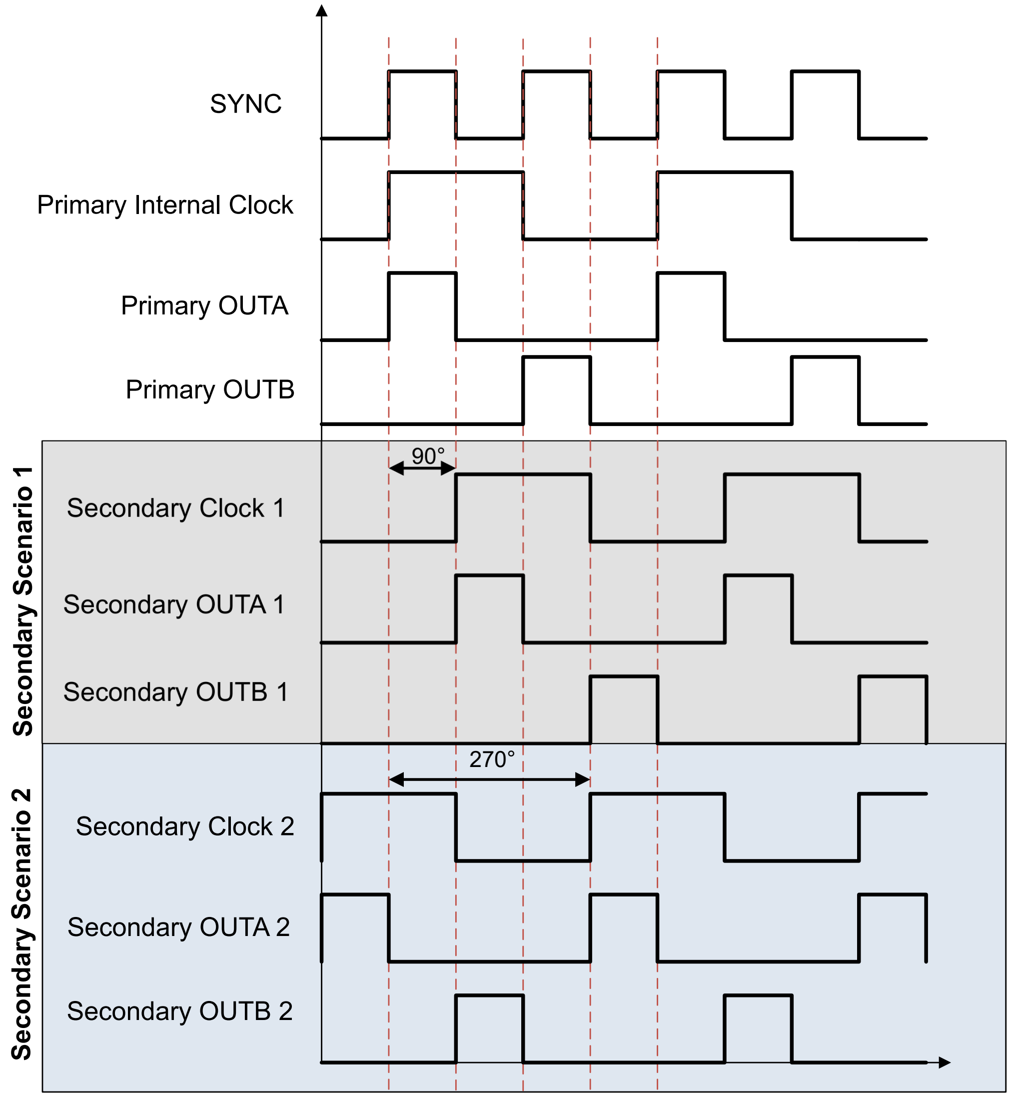


图 8-12. Switching Waveforms for Primary-Secondary Mode

The three operational modes for the controller are summarized in 表 8-1.

表 8-1. Oscillator Modes and Configurations

MODE	RT	SYNC	SWITCHING FREQUENCY
Internal oscillator	Populated with resistor to AVSS.	Configured as output. Generates in-phase clock at twice the switching frequency.	Configurable from 100 kHz to 2 MHz depending on RT value.
External synchronization	Floating.	Configured as input. Accepts 200-kHz to 4-MHz external clock that is inverted internally.	Synchronized to SYNC input clock at 1/2 of the clock frequency. Switching is out-of-phase with external clock.
Primary-secondary	Populated with resistor to AVSS on primary device. Floating on secondary device.	Configured as output on primary device. Configured as input on secondary device. The SYNC pins of primary and secondary devices are connected.	Configurable from 100 kHz to 2 MHz depending on RT value of primary device. Secondary device switching is either 90° or 270° out-of-phase with primary device.

8.3.9 Primary Switching Outputs (OUTA/OUTB)

The controllers in the TPS7H500x-SP series either have a single primary output (OUTA) or dual primary outputs (OUTA and OUTB). 表 8-2 below shows the primary switching outputs that are available for each of the devices. Due to the roughly 150-mA peak current capability of each primary switching output, an external gate drive solution is recommended. For those controllers that support buck and single ended isolated applications (TPS7H5001-SP, TPS7H5002-SP, and TPS7H5003-SP), OUTA provides the gate control signal for the main switch in the topology. For push-pull and full-bridge applications, OUTA and OUTB both provide control signals for the main primary switches. Note that OUTB is only active when the duty cycle limit is set to 50% by connecting DCL pin to AVSS, and this DCL option is only valid for TPS7H5001-SP and TPS7H5004-SP (see *Duty Cycle Programmability* for more details). For the two output controller options, OUTA and OUTB are not perfectly matched and will vary based on the COMP voltage in a given switching cycle.

表 8-2. Available Primary Output(s) for TPS7H500x-SP

DEVICE	OUTA	OUTB
TPS7H5001-SP	Yes	Yes
TPS7H5002-SP	Yes	No
TPS7H5003-SP	Yes	No
TPS7H5004-SP	Yes	Yes

8.3.10 Synchronous Rectifier Outputs (SRA and SRB)

For applications in which synchronous rectification (SR) is desired in order to increase overall converter efficiency, there are TPS7H500x-SP controllers with a single SR output (SRA) or dual SR outputs (SRA and SRB). 表 8-3 below shows the synchronous rectifier outputs that are available for each of the devices. Similar to the primary switching outputs, the peak current capability is roughly 150 mA and an external gate drive solution is recommended. The TPS7H5001-SP is the only controller in the series that contains the SRB output, and this output is only active when the duty cycle limit is set to 50% by connecting the DCL pin to AVSS. The SRA/SRB outputs will be off during the soft-start period and start switching when the voltage on SS exceeds 1 V. A small voltage transient may appear on the converter output when SRA/SRB become active.

表 8-3. Available Synchronous Rectifier Output(s) for TPS7H500x-SP

DEVICE	SRA	SRB
TPS7H5001-SP	Yes	Yes
TPS7H5002-SP	Yes	No
TPS7H5003-SP	Yes	No
TPS7H5004-SP	No	No

8.3.11 Dead Time and Leading Edge Blank Time Programmability (PS, SP, and LEB)

While the TPS7H5003-SP has a fixed dead time (50 ns typical), the TPS7H5001-SP and TPS7H5002-SP allow for the user to program two independent dead times, TD_{SP} and TD_{PS}, as shown in 图 8-13. This allows for the dead times to be optimized by the user in order to prevent shoot-though between the primary and synchronous switches while attaining the best possible converter efficiency. The dead time TD_{PS} between primary output (OUTA/OUTB) turn-off to synchronous rectifier (SRA/SRB) turn-on, can be programmed using a resistor from PS to AVSS. Likewise, the dead time TD_{SP} between synchronous rectifier turn-off and primary output turn-on is set using a resistor from SP to AVSS. The equation for determining the values of R_{PS} and R_{SP} required for a desired dead time is shown in 方程式 8.

$$R_{PS} = R_{SP} = 1.207 \times DT - 8.858 \tag{8}$$

where:

- DT is the desired dead time in ns
- R_{PS} and R_{SP} are in kΩ

If the PS and SP pins are left floating, the dead time will be set to a minimum value of 8 ns (typical). When these pins are populated, it is recommended to use a minimum resistor value of 10 kΩ for R_{PS} and R_{SP}. The maximum resistor value to be used is 300 kΩ. As mentioned in *Soft-Start (SS)* and *Synchronous Rectifier Outputs (SRA and SRB)*, the SR outputs will be disabled during soft start, so the dead time is observed only after this sequence is complete.

After OUTA or OUTB goes high, a leading edge blank time is implemented to remove any transient noise from the current sensing loop. While the leading edge blank time is fixed (50-ns typical) for TPS7H5003-SP, the leading edge blank time for all other devices in the TPS7H500x-SP series is programmable by placing an external resistor from LEB to AVSS. This pin cannot be left floating and a minimum resistor value of 10 kΩ is required from LEB to AVSS. The maximum resistor value that should be used is 300 kΩ. The equation for determining the value of R_{LEB} for a desired leading edge blank time is shown in 方程式 9.

$$R_{LEB} = 1.212 \times LEB - 9.484 \quad (9)$$

where:

- LEB is the desired leading edge blank time in ns
- R_{LEB} is in kΩ

表 8-4. Dead Time and Leading Edge Blank Time Configurations for TPS7H500x-SP

DEVICE	DEAD TIME	LEADING EDGE BLANK TIME
TPS7H5001-SP	Resistor programmable	Resistor programmable
TPS7H5002-SP	Resistor programmable	Resistor programmable
TPS7H5003-SP	Fixed (50-ns typical)	Fixed (50-ns typical)
TPS7H5004-SP	Not applicable	Resistor programmable

In 图 8-13, the dead times and leading edge blank times are shown for the switching waveforms. This figure also illustrates the minimum on-time of the device, which is comprised of the programmed blank time T_{LEB} and an internal logic delay t_d. Note that the dead-time waveforms for OUTB/SRB are only applicable for TPS7H5001-SP.

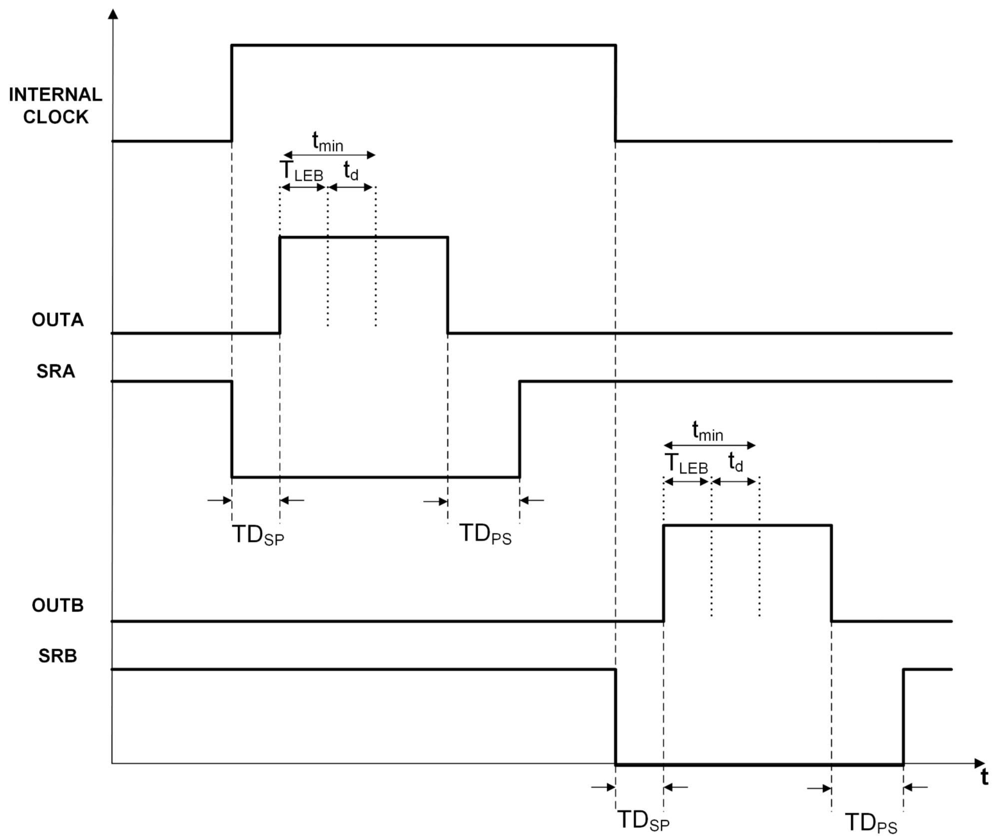


图 8-13. Outputs Timing Waveforms

8.3.12 Pulse Skipping

In order to prevent converter operational issues related to the minimum on-time of the controller, specifically during high frequency operation, a pulse skipping mode has been implemented for the TPS7H500x-SP controllers. During this mode, the primary outputs (OUTA/OUTB) will stop switching periodically. For the controllers with SR outputs, SRA/SRB remain on during pulse skipping if the soft-start period has ended. If the device enters into pulse skipping during the soft-start sequence, SRA/SRB remain off since the outputs are not yet active. Having a minimum on-time that is too long in duration during high frequency operation can lead to an issue such as inductor current runaway during the soft-start period. Pulse skipping allows for overcoming this issue by reducing the peak inductor current during the startup period. In high frequency converter designs where the V_{IN} to V_{OUT} ratio of the converter may lead to required duty cycles that are less than the minimum on-time, the controller outputs will skip pulses in order to maintain the required output voltage. Pulse skipping will occur when both of the following conditions are present:

- The voltage at the COMP pin is less than 0.3 V at the rising edge of the system clock
- The previous duty cycle was less than 25%

When the duty cycle limit of the controller is set to 50% and both OUTA and OUTB are active, the number of pulses skipped by each of the primary outputs will be equal. This will ensure the volt-second balance is maintained across the transformer and that flux-walking that leads to transformer saturation is avoided in isolated topologies such as the push-pull.

8.3.13 Duty Cycle Programmability

The TPS7H5001-SP, TPS75002-SP, and TPS7H5003-SP each have a configurable maximum duty cycle using the DCL pin. The TPS7H5004-SP only supports 50% maximum duty cycle and the DCL pin must be connected to AVSS. 表 8-5 shows the allowable maximum duty cycle limits for each device.

表 8-5. Allowable Duty Cycle Limits for TPS7H500x-SP

DEVICE	DUTY CYCLE LIMIT OPTIONS
TPS7H5001-SP	50%, 75%, 100%
TPS7H5002-SP	75%, 100%
TPS7H5003-SP	75%, 100%
TPS7H5004-SP	50%

For applications in which 100% duty cycle is needed, the user should select one of the three compatible devices and connect DCL to VLDO. For other applications which require a duty cycle limit restriction, the DCL pin could be connected to AVSS for 50% duty cycle limit or left floating for 75% maximum duty cycle. Note that only TPS7H5001-SP and TPS7H5004-SP support the 50% duty cycle limit (DCL = AVSS), and OUTB/SRB are only active in this configuration. The 50% duty cycle limit case is intended to support applications such as the push-pull that require two primary switching outputs, and in the case of the TPS7H5001-SP, two synchronous rectification outputs. If the controller is being operated in external synchronization mode, the most precise duty cycle limiting results are obtained when the applied system clock has a 50% duty cycle. Specifically, for the case when the duty cycle limit is set to 75% (DCL = floating) in the supported devices, there may be some variation of the duty cycle limit that is dependent on the duty cycle of the external clock applied at SYNC.

表 8-6. DCL Pin Configurations

MAXIMUM DUTY CYCLE (NOMINAL)	DCL CONNECTION
100%	VLDO
75%	Floating
50%	AVSS

8.3.14 Current Sense and PWM Generation (CS_ILIM)

The CS_ILIM pin is driven by a signal representative of the transformer primary-side current. The current signal has to have compatible input range of the COMP pin. As shown in 图 8-14, the COMP pin voltage is used as the reference for the peak current. Note that the OUTB waveform is only applicable for TPS7H5001-SP and TPS7H5004-SP. The primary side signals, OUTA/OUTB, are turned on by the internal clock signal and turned off when sensed peak current reaches the COMP/2 pin voltage. Note that this peak sensed current signal that is compared to COMP/2 at the PWM comparator contains an offset voltage of 150 mV. The CS_ILIM pin is also used to configure the current limit for the controller.

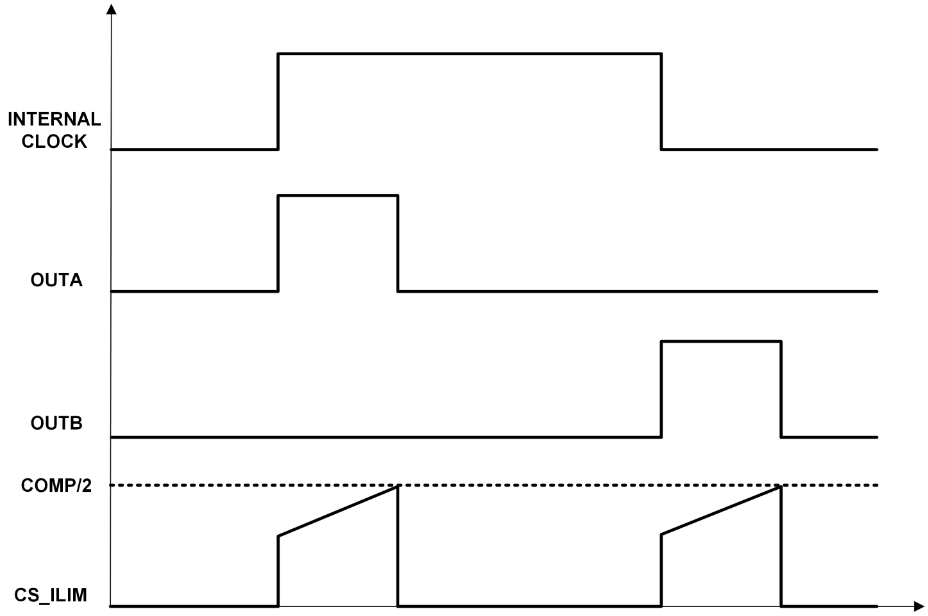


图 8-14. Peak Current Mode Control and PWM Generation

A resistor is needed from CS_ILIM to AVSS is used to detect current for both proper PWM operation and overcurrent protection. The current limit threshold V_{CS_ILIM}, is specified as 1.05 V (nominal) in the electrical specifications. This indicates that when the voltage on this pin reaches this threshold, the device will go into hiccup mode. 方程式 10 shows the calculation for determining the value of the sense resistor for a selected current limit.

$$R_{CS} = \frac{V_{CS\_ILIM}}{I_{LIM}} \tag{10}$$

Note that the value of I_{LIM} has to account for where and how the current is being sensed. For a forward converter with sense resistor between source of primary FET to AVSS, I_{LIM} will be referred to the primary side of the converter.

$$I_{LIM} = I_{L,PEAK} \times \frac{N_S}{N_P} \tag{11}$$

方程式 11 shows the calculation for determining I_{LIM} in the design of a forward converter, where:

- $I_{L,PEAK}$ is the peak output inductor current desired to activate the overcurrent protection
- N_S is the number of secondary turns for the power transformer
- N_P is the number of primary turns for the power transformer

In the design of a buck converter which senses the high side current via a current sense transformer, 方程式 12 can be used for determining I_{LIM} for this instance.

$$I_{LIM} = I_{L,PEAK} \times \frac{N_{CSP}}{N_{CSS}} \tag{12}$$

In this equation:

- $I_{L,PEAK}$ is the peak output inductor current desired to activate the overcurrent protection
- N_{CSP} is the number of primary turns of the current sense transformer

- N_{CSS} is the number of secondary turns of the current sense transformer

Regardless of the topology, the user should ensure that there is sufficient margin between the peak current during normal operation and the overcurrent trip point when determining the value of R_{CS}.

8.3.15 Hiccup Mode Operation (HICC)

Once the voltage at CS_ILIM exceeds 1.05 V, the device will execute cycle-by-cycle current limiting. The controller output is turned on at the beginning of each cycle until such point that CS_ILIM voltage reaches the current sense threshold V_{CS_ILIM}, when the output is turned off. At the same time, each time the voltage at CS_ILIM reaches 1.05 V, the capacitor at C_{HICC} is charged via a 80-μA current (hiccup delay current). This hiccup delay current is terminated at the end of the clock cycle. As long as there is still an overcurrent being detected, the cycle-by-cycle limiting will continue until the voltage on C_{HICC} reaches 0.6 V. This cycle-by-cycle limiting period is referred to as the delay mode. As such, the capacitor C_{HICC} can be chosen to dictate the amount of time that the controller will spend in delay mode.

$$C_{HICC} = \frac{t_{delay} \times 80\ \mu A}{0.6\ V} \tag{13}$$

Note that this equation is an approximation since:

- depending on the system behavior and if C_{HICC} has been charged previously, C_{HICC} may not start at 0 V as assumed by the equation
- the 80- μ A charging current is a pulsed current, the duration of which will be dictated by the nature of the overcurrent (that is,. when the current sense threshold is reached during each clock cycle)

After the voltage on HICC pin reaches 0.6 V, the SS pin of the controller is discharged and switching stops. The voltage on HICC is then quickly pulled up to 1 V with the pull-up current limited to approximately 1 mA. Once HICC voltage reaches 1 V, the 1-μA hiccup restart current begins to discharge C_{HICC}. The controller will not switch until HICC voltage falls to 0.3 V. Once the voltage falls to 0.3 V, the controller will initiate its soft-start sequence again. If the overcurrent has disappeared, normal operation will resume. The hiccup time, which is the entire non-switching period, can be calculated using 方程式 14.

$$t_{HICC} = \frac{C_{HICC} \times (1\ V - 0.3\ V)}{1\ \mu A} \tag{14}$$

In summary, the capacitor C_{HICC} on the HICC pin controls the amount of time the controller spends performing cycle-by-cycle limiting before switching stops, and also controls the amount of time switching is disabled before re-start is attempted again. It is recommended to use a minimum of 3.3 nF for C_{HICC}. 图 8-15 shows the typical behavior during hiccup mode. Note that the OUTB and corresponding CS_ILIM waveforms are only applicable for TPS7H5001-SP and TPS7H5004-SP.

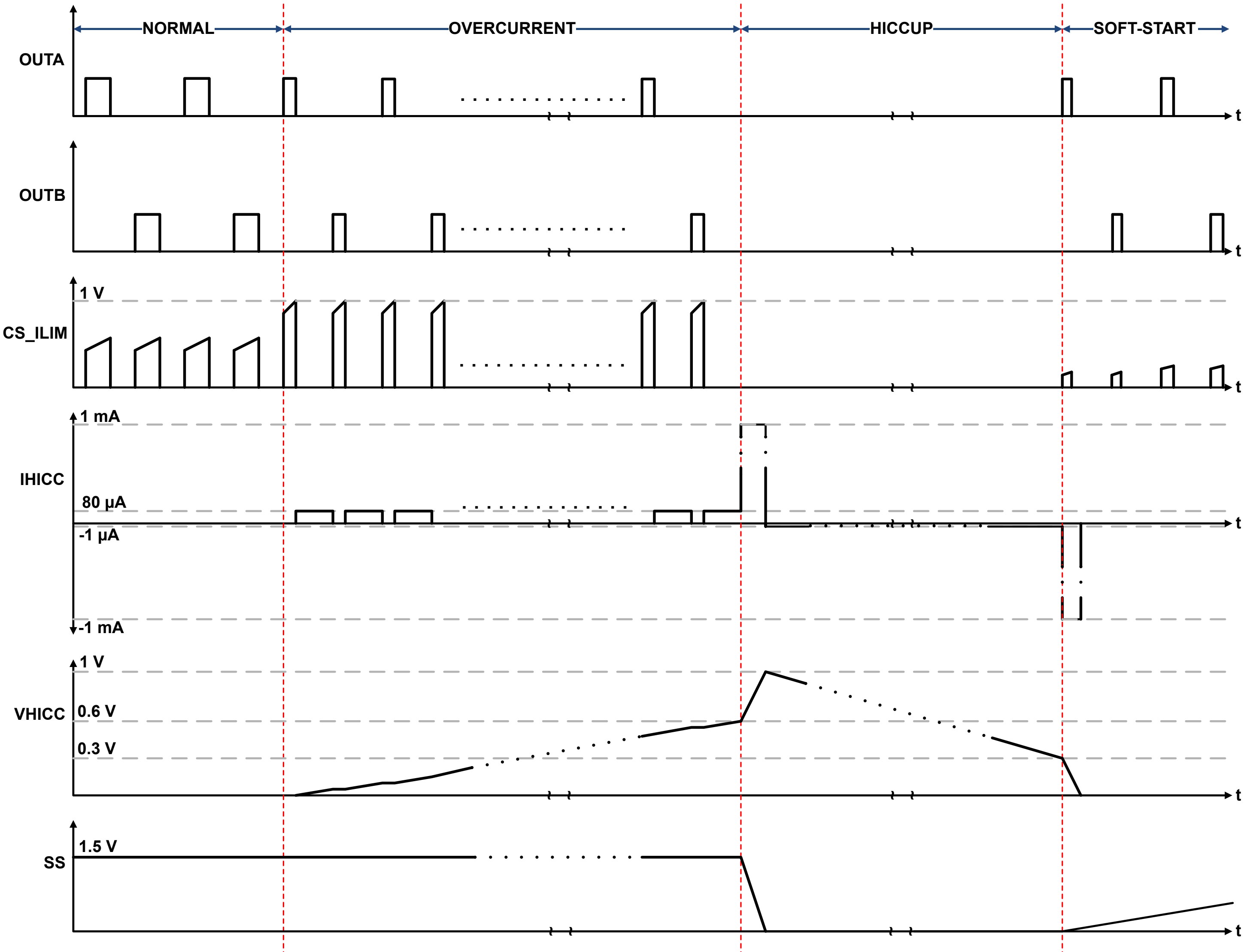


图 8-15. Cycle-by-Cycle Current Limit Delay Timer and Hiccup Restart Timer

8.3.16 External Fault Protection (FAULT)

The FAULT pin provides the user with flexibility to implement additional protections for the converter, such as input overcurrent protection or overvoltage protection, if desired. This pin can also be utilized in the event that the user desires more stringent protections than what is offered by the controller (i.e. thermal shutdown). The user can design external logic circuitry to generate the signal necessary to drive this pin based on the protection function. If the voltage on the FAULT pin exceeds 0.6 V (typical) for a duration specified by the FAULT minimum pulse width, a fault shutdown will occur. This FAULT minimum pulse width duration, which is between 0.4 µs and 1.4 µs, is intended to prevent any spurious triggering due to short-term transients. Since any short-term transient event detected on this pin that is less than 1.4 µs in duration may not activate the FAULT pin, these events should be properly evaluated by the user in order to determine the impact to the overall system. Once the fault is detected, the SS pin is discharged and the controller outputs stop switching and stay low as long as the rising threshold is exceeded on the pin. Once the fault has subsided and the voltage of FAULT falls below the falling threshold of 0.5 V (typical), the TPS7H500x-SP enters a delay period that is dependent on the switching frequency. This delay is approximately equal to 15 switching frequency cycles in addition to an internal logic delay. The soft-start sequence is again initiated after the delay period has finished. 方程式 15 can be used to determine the length of the fault delay.

$$t_{dFLT} = \frac{14700}{f_{sw}} + 2 \tag{15}$$

In this equation:

- t_{dFLT} is the fault delay duration in μs
- f_{sw} is the switching frequency in kHz

If the FAULT threshold is exceeded during the delay, the entire sequence is started again. 图 8-16 shows the switching waveforms when the fault mode has been activated in the controller. Note that the OUTB waveforms are only applicable for TPS7H5001-SP and TPS7H5004-SP.

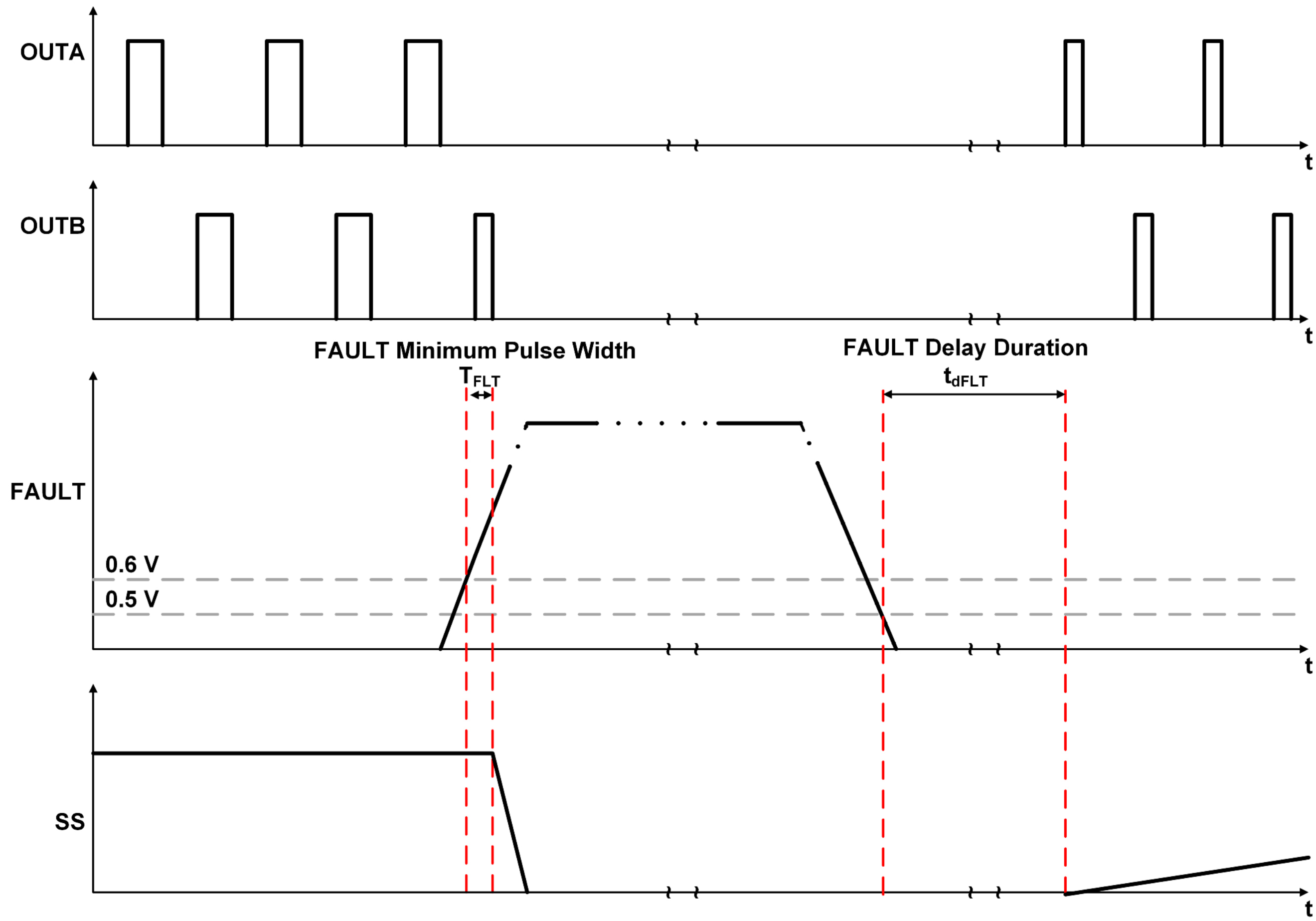


图 8-16. Switching Waveforms During Fault Mode

8.3.17 Slope Compensation (RSC)

When utilizing peak current mode control in switching power converter design, the converter can enter into an unstable state when the duty cycle for the main power switch rises above 50%. Essentially, the converter will be in a state where the error between the peak current and average current increases with each subsequent switching cycle. This instability, known as subharmonic oscillation, can be mitigated by adding slope compensation. For the TPS7H500x-SP, the slope compensation is in the form of a voltage ramp that is subtracted from the error amplifier output divided down by the parameter CCSR (COMP to CS_LIM ratio). The minimum slope compensation for stability over the entire duty cycle range is equal to 0.5 × *m*, where *m* is the inductor falling current slope. The recommended slope compensation is 1 × *m*, as any increase above this value will not improve stability.

For a typical buck converter, setting the slope compensation equal to the downward slope of the sensed current waveform yields the calculation in 方程式 16.

$$SC = \frac{V_{OUT}}{L} \times \frac{N_{CSP}}{N_{CSS}} \times R_{CS} \quad (16)$$

where:

- SC is the slope compensation value in V/μs
- L is the output inductor value in μH
- N_{CSP} is the number of primary turns of the current sense transformer
- N_{CSS} is the number of secondary turns on the current sense transformer
- R_{CS} is the value of the current sense resistor in Ω

If no current sense transformer is used, set N_{CSP} / N_{CSS} to 1.

The slope compensation for the forward converter will be similar with the note that the sensed current waveform would also need to take into account the turns ratio of the main power transformer.

$$SC = \frac{V_{OUT}}{L} \times \frac{N_S}{N_P} \times \frac{N_{CSP}}{N_{CSS}} \times R_{CS} \quad (17)$$

where:

- N_S is the number of secondary turns of the power transformer
- N_P is the number of primary turns of the power transformer

For the TPS7H500x-SP controllers, a resistor from the RSC pin to AVSS can be used to set the desired slope compensation. 方程式 18 shows the calculation for determining the proper resistor value for RSC.

$$RSC = \frac{28.3}{SC^{1.1}} \quad (18)$$

where:

- SC is the desired slope compensation is V/μs
- RSC is in kΩ

8.3.18 Frequency Compensation

Since the TPS7H500x-SP uses a transconductance error amplifier (OTA), either Type 2A or Type 2B frequency compensation can be applied. The primary difference between the two compensation schemes is that Type 2A has an additional capacitor C_{HF} in parallel with R_{COMP} and C_{COMP} in order to provide high-frequency noise attenuation. These components will be connected between the COMP pin of the controller, which is the OTA output, and AVSS.

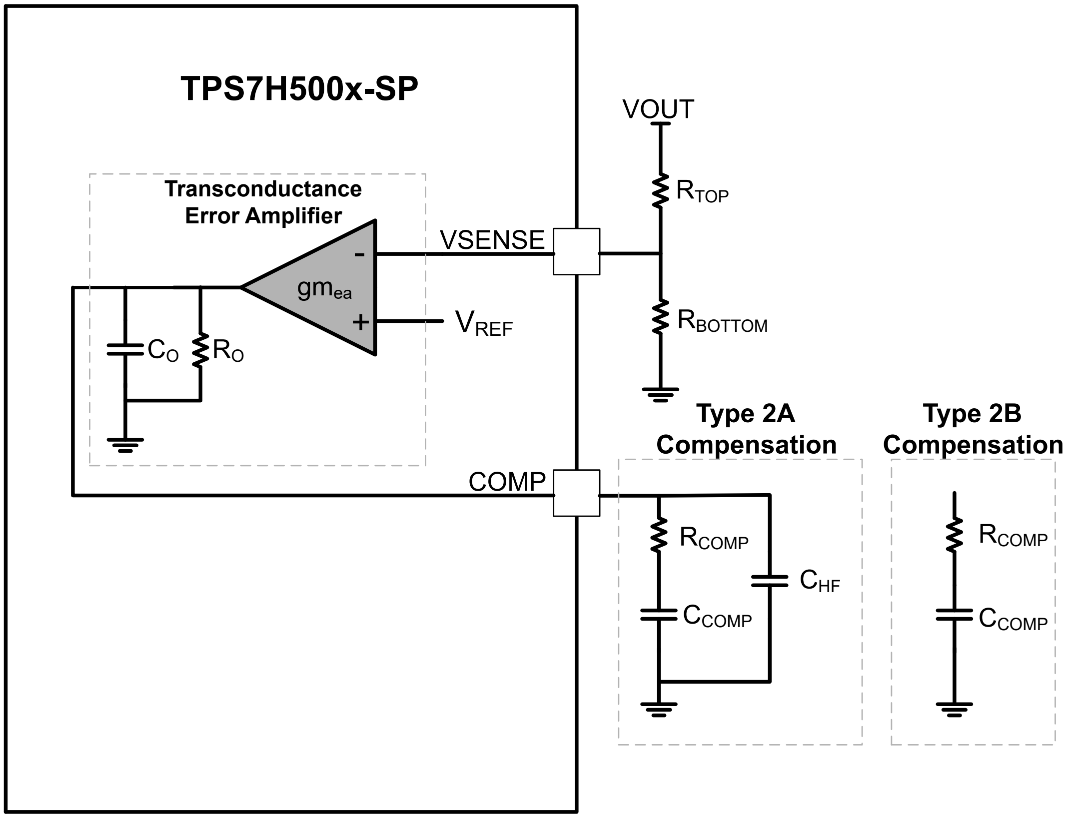


图 8-17. TPS7H500x-SP Frequency Compensation Options

For any of the topologies supported by the TPS7H500x-SP, the following procedure and equations can be used to select the compensation components. All parameters in the equations are in standard units unless otherwise indicated (that is, H for inductance, F for capacitance, Hz for frequency, and so on).

1. Select the desired crossover frequency (f_c) for the converter.
2. Calculate R_{COMP} based on the selected crossover frequency f_c.

1. $$R_{COMP} = \frac{2\pi \times f_c \times V_{OUT} \times C_{OUT}}{gm_{ea} \times V_{REF} \times gm_{PS}} \quad (19)$$

where:
- gm_{ea} is the error amplifier transconductance of 1800 × 10^{-6} A/V (typical)
- V_{REF} is the 0.613 V reference voltage (typical)
- gm_{PS} is the power stage transconductance (see 方程式 23)

2. Calculate C_{COMP} to place compensation zero at the location of the power stage dominant pole.

$$C_{COMP} = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_{COMP}} \quad (20)$$

3. Determine the output capacitor ESR zero location (optional).

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR} \quad (21)$$

4. Select the capacitor C_{HF} to provide a high frequency pole to compensate for the ESR zero (optional).

$$C_{HF} = \frac{1}{2\pi \times R_{COMP} \times f_{ESR}} \tag{22}$$

For different power converter topologies, the primary change to the compensation selection procedure will be the determination of the power stage transconductance gm_{PS}. The power stage transconductance can be calculated as shown in 方程式 23.

$$gm_{PS} = \frac{N_P \times N_{CSS}}{CCSR \times R_{CS} \times N_S \times N_{CSP}} \tag{23}$$

where:

- N_P is the number of primary turns on the main power transformer (set to 1 if no transformer is used)
- N_S is the number of secondary turns on the main power transformer (set to 1 if no transformer is used)
- N_{CSP} is the number of primary turns on the current sense transformer (set to 1 if no transformer is used)
- N_{CSS} is the number of secondary turns of the current sense transformer (set to 1 if no transformer is used)
- R_{CS} is the selected value of the current sense resistor
- CCSR is the ratio to COMP of CS_ILIM

Note that for the TPS7H500x-SP controllers, the sensed current waveform is compared to the voltage at COMP divided down by the factor CCSR at the PWM comparator, which is accounted for in the denominator of the equation. For buck converters, all turns for the main power transformer can be set equal to 1 and the equation still applies.

8.3.19 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C (typical). The device reinitiates the power-up sequence when the junction temperature drops below 160°C (typical).

8.4 Device Functional Modes

The TPS7H500x-SP series uses fixed frequency, peak current mode control. Each controller regulates the peak current and duty cycle of the converter. The internal oscillator initiates the turn-on of the primary output used as the gate driver input for the power switch. The external power switch current is sensed through an external resistor and compared via internal comparator. The voltage generated at the COMP pin is stepped down via internal resistors. When the sensed current reaches the stepped down COMP voltage, the power switch is then turned off.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TPS7H500x-SP series is a family of radiation-hardness-assured current mode PWM controllers that can be utilized for designing space-grade DC-DC converters. Each device should be paired with external gate drivers in order to provide control of the power semiconductor device(s) of the converter power stage. By allowing for switching frequencies up to 2 MHz, the controllers provide many advantages for GaN power semiconductor based designs. The TPS7H500x-SP family can be used for the design of a number of common DC-DC converter topologies, including but not limited to: buck, flyback, forward, active-clamp forward, push-pull, and full-bridge.

9.2 Typical Application

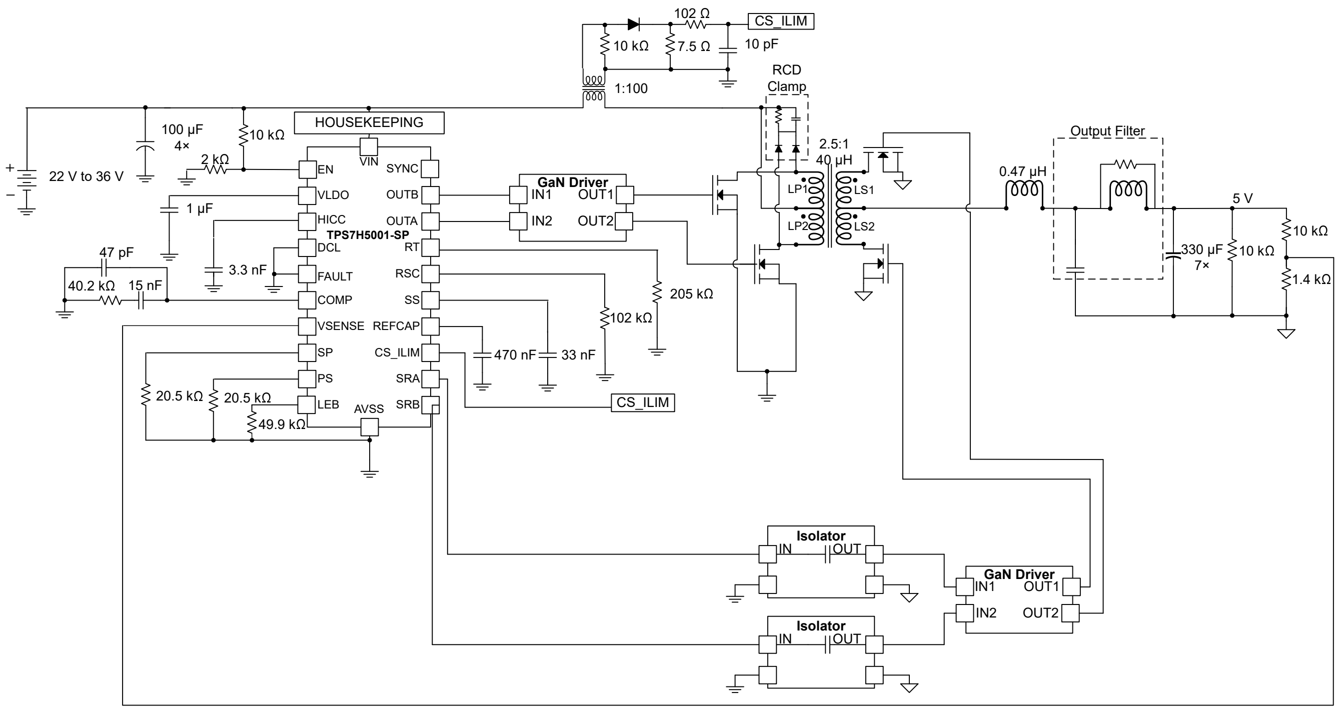


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

The example provided here is to demonstrate how to design a synchronous push-pull converter using GaN power semiconductor devices. This design example is to show how to determine the component selection for the TPS7H5001-SP as well as key components of the converter power stage.

表 9-1. Design Parameters

DESIGN PARAMETER	VALUE
Output voltage	5 V
Maximum output current	20 A
Output current pre-load	0.5 mA
Operating temperature	25°C
Switching frequency	500 kHz
Peak input current limit	14 A
Target bandwidth	~10 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Switching Frequency

The synchronous push-pull converter was designed to operate at a switching frequency of 500 kHz. For space-grade converter designs, the benefits of GaN power devices over silicon counterparts are readily apparent at this switching frequency. Using 方程式 7, the required RT resistor for the desired frequency can be determined as shown in 方程式 24.

$$\mathrm{RT} = \frac{112000}{500} - 19.7 = 204.3\ \mathrm{k\Omega} \tag{24}$$

A standard resistor value of 205 kΩ is selected for the design.

9.2.2.2 Output Voltage Programming Resistors

The converter has an output voltage of 5 V. The feedback resistor divider connected to VSENSE should be selected to correspond to the selected V_{OUT}. With a resistor of 10 kΩ selected for R_{TOP}, the value of the bottom resistor in the divider can be calculated.

$$\mathrm{R_{BOTTOM}} = \frac{\mathrm{V_{REF}}}{\mathrm{V_{OUT}} - \mathrm{V_{REF}}} \times \mathrm{R_{TOP}} \tag{25}$$

$$\mathrm{R_{BOTTOM}} = \frac{0.613\ \mathrm{V}}{5\ \mathrm{V} - 0.613\ \mathrm{V}} \times 10\ \mathrm{k\Omega} = 1.397\ \mathrm{k\Omega} \tag{26}$$

The values for R_{TOP} and R_{BOT} needed are 10 kΩ and 1.4 kΩ, respectively.

9.2.2.3 Dead Time

For GaN power semiconductor devices, a key characteristic that has to be taken into consideration is the voltage drop of the GaN FET while it is operating in reverse conduction mode. While the GaN FET does not have a body diode that is inherent in the silicon FET, it does still have the ability to conduct current in the reverse direction with behavior that is similar to a diode. When conducting in the reverse direction, the source-drain voltage of the GaN FET can be quite large. Thus, to reduce the dead-time losses and maximize efficiency, the dead time was set to a value of approximately 25 ns. Based on the selected value, 方程式 8 can be used to calculate the resistors needed to attain the desired dead time.

$$\mathrm{R_{PS}} = \mathrm{R_{SP}} = 1.207 \times 25 - 8.858 = 21.3\ \mathrm{k\Omega} \tag{27}$$

The standard resistor value of 20.5 kΩ was selected for both R_{PS} and R_{SP}.

9.2.2.4 Leading Edge Blank Time

The leading edge blank time was initially chosen to be roughly 50 ns. This value was the initial approximation based on any ringing or transient spikes that were expected to be seen on the sensed current waveform at the CS_ILIM pin. Using 方程式 9 , the value of R_{LEB} was calculated from this desired value.

$$R_{LEB} = 1.212 \times 50 - 9.484 = 51.1\ \text{k}\Omega \tag{28}$$

The value of R_{LEB} selected was 49.9 kΩ. Note that the ringing and transient spikes on the sensed current waveform will depend heavily on component placement and parastics in the PCB layout. The leading edge blank time should also account for any propagation delay that is inherent to the gate driver being used in the application. As such, the value of R_{LEB} may need to be optimized as the design is tested in accommodate for these factors. Recall that the leading edge blank time is also correlated to the minimum on-time of the device, and extending this value significantly may become a limiting factor for the maximum switching frequency that can be achieved in the design.

9.2.2.5 Soft-Start Capacitor

For this design, the soft-start time is arbitrary. The value of the soft-start capacitor selected was 33 nF. Based on this value, the soft-start time can be calculated.

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \tag{29}$$

$$t_{SS} = \frac{33\ \text{nF} \times 0.613\ \text{V}}{2.7\ \mu\text{A}} = 7.49\ \text{ms} \tag{30}$$

The soft-start time is ~7.5 ms for the design.

9.2.2.6 Transformer

The turns ratio and primary inductance of the transformer will be determined based on the target specifications of the converter. In order to calculate the maximum allowable turns ratio, a duty cycle limit must be selected for the design. Even though DCL will be connected to AVSS to impose a 50% duty cycle limit from the controller to ensure there is no overlap of the primary switching outputs, a maximum duty cycle of approximately 35% is targeted for the design in order to provide sufficient margin to the controller limit. This is due to the fact that the actual duty cycle is greater than calculated duty cycle when accounting for the converter efficiency, and to allow for duty cycle increases during load transient events. 方程式 31 provides the formulate needed to calculate the maximum turns ratio for this design.

$$N_{PS\_MAX} = \frac{2 \times V_{IN\_MIN} \times D_{LIM}}{V_{OUT} + V_{SR}} \tag{31}$$

V_{SR} is estimated to be 0.5 V for the application and D_{LIM} is 35% duty cycle limit that was selected. N_{PS_MAX} is calculated using the values in 方程式 32.

$$N_{PS\_MAX} = \frac{2 \times 22\ \text{V} \times 0.35}{5\ \text{V} + 0.5\ \text{V}} = 2.8 \tag{32}$$

A value of 2.5 is selected for the turns ratio for the design.

In order to design for the primary inductance of the transformer, the magnetizing current must be selected. The value of the magnetizing current is a trade-off between transformer size and efficiency, with larger magnetizing current leading to a smaller size due to lower required inductance, but also leading to lower efficiency. A magnetizing current equal to 6% of the output current was initially targeted for this design. With this value, the primary inductance can be calculated using 方程式 36. The minimum duty cycle expected is needed for this calculation can be determined using 方程式 34, where the estimated efficiency η for the converter used in the calculation is 85%.

$$D_{MIN} = \frac{V_{OUT} + V_{SR}}{2 \times V_{IN\_MAX} \times N_{SP} \times \eta} \tag{33}$$

$$D_{MIN} = \frac{5\ \text{V} + 0.5\ \text{V}}{2 \times 36\ \text{V} \times 0.4 \times 0.85} = 0.22 \tag{34}$$

$$L_P = \frac{N_{PS} \times V_{IN\_MAX} \times D_{MIN}}{f_{sw} \times I_{MAG}} \tag{35}$$

$$L_P = \frac{2.5 \times 36\ \text{V} \times 0.22}{500\ \text{kHz} \times 0.06 \times 20\ \text{A}} = 33\ \mu\text{H} \tag{36}$$

Though the calculated value of L_P is 33 μH, it may often be challenging to find the exact primary inductance value needed for the transformer design. As such, an inductance of 40 μH was used in the actual design.

The following equations detail the how to calculate transformer primary and secondary currents that are critical for proper design of the transformer. These equations are useful for defining the physical structure of the transformer. Note that these are ideal equations, and the final design should be optimized depending on the application.

$$I_{SEC\_MAX} = I_{OUT} + \frac{\Delta I_L}{2} \tag{37}$$

$$I_{SEC\_MAX} = 20 + \frac{8.51\ \text{A}}{2} = 24.25\ \text{A} \tag{38}$$

$$I_{PRI\_MAX} = \frac{I_{SEC\_MAX} + (0.5 \times I_{MAG})}{N_{PS}} \tag{39}$$

$$I_{PRI\_MAX} = \frac{24.25\ \text{A} + (0.5 \times 0.06 \times 20\ \text{A})}{2.5} = 9.94\ \text{A} \tag{40}$$

$$I_{SEC\_MAX\,(VIN\_MIN)} = \frac{I_{OUT} + \left(D_{MAX} \times \left(\frac{V_{IN\_MIN}}{N_{PS}} - V_{OUT} - V_{SR}\right)\right)}{2 \times f_{sw} \times L_{OUT}} \tag{41}$$

$$I_{SEC\_MAX\,(VIN\_MIN)} = \frac{20\ \text{A} + \left(0.37 \times \left(\frac{22\ \text{V}}{2.5} - 5\ \text{V} - 0.5\ \text{V}\right)\right)}{2 \times 500\ \text{kHz} \times 0.47\ \mu\text{H}} = 22.58\ \text{A} \tag{42}$$

$$I_{PRI\_MAX\,(VIN\_MIN)} = \frac{I_{SEC\_MIN\,(VIN\_MIN)} + (0.5 \times I_{MAG})}{N_{PS}} \tag{43}$$

$$I_{PRI\_MAX\,(VIN\_MIN)} = \frac{17.42\ \text{A} + (0.5 \times 0.06 \times 20\ \text{A})}{2.5} = 9.27\ \text{A} \tag{44}$$

$$I_{SEC\_MIN\,(VIN\_MIN)} = \frac{I_{OUT} - \left(D_{MAX} \times \left(\frac{V_{IN\_MIN}}{N_{PS}} - V_{OUT} - V_{SR}\right)\right)}{2 \times f_{sw} \times L_{OUT}} \tag{45}$$

$$I_{SEC\_MAX\,(VIN\_MIN)} = \frac{20\ \text{A} - \left(0.37 \times \left(\frac{22\ \text{V}}{2.5} - 5\ \text{V} - 0.5\ \text{V}\right)\right)}{2 \times 500\ \text{kHz} \times 0.47\ \mu\text{H}} = 17.42\ \text{A} \tag{46}$$

$$I_{PRI\_MIN\,(VIN\_MIN)} = \frac{I_{SEC\_MIN\,(VIN\_MIN)} - (0.5 \times I_{MAG})}{N_{PS}} \tag{47}$$

$$I_{PRI\_MIN\,(VIN\_MIN)} = \frac{17.42\ \text{A} - (0.5 \times 0.06 \times 20\ \text{A})}{2.5} = 6.73\ \text{A} \tag{48}$$

$$t_{ON\_MAX} = \frac{(V_{OUT} + V_{SR}) \times N_{PS}}{2 \times f_{sw} \times V_{IN\_MIN}} \tag{49}$$

$$t_{ON\_MAX} = \frac{(5\ \text{V} + 0.5\ \text{V}) \times 2.5}{2 \times 500\ \text{kHz} \times 22\ \text{V}} = 0.63\ \mu\text{s} \tag{50}$$

$$m_{PRI} = \frac{I_{PRI\_MAX\,(VIN\_MIN)} - I_{PRI\_MIN\,(VIN\_MIN)}}{t_{ON\_MAX}} \tag{51}$$

$$m_{PRI} = \frac{9.27\ \text{A} - 6.73\ \text{A}}{0.63\ \mu\text{s}} = 4072130.16\ \frac{\text{A}}{\text{s}} = 4.07\ \frac{\text{A}}{\mu\text{s}} \tag{52}$$

$$I_{PRI\_RMS} = \sqrt{D_{MIN} \times \left(\frac{(m_{PRI} \times t_{ON\_MAX})^2}{3} + \left(\frac{m_{PRI}}{2} \times I_{PRI\_MIN\,(VIN\_MIN)} \times t_{ON\_MAX}\right) + I_{PRI\_MIN\,(VIN\_MIN)}{}^2\right)} \tag{53}$$

$$I_{PRI\_RMS} = \sqrt{0.22 \times \left(\frac{\left(4072130.16 \frac{A}{s} \times 0.63\ \mu s\right)^2}{3} + \left(\frac{4072130.16 \frac{A}{s}}{2} \times 6.73\ A \times 0.63\ \mu s \right) + 6.73\ A^2 \right)} = 3.55\ A \tag{54}$$

9.2.2.7 Main Switching FETs

In the push-pull topology, the switching devices on the primary side will see a voltage that is equal to twice that of the input when the devices are off. As such, the GaN FETs selected should have a voltage rating that 3 times higher than the input voltage. The voltage rating for the GaN FETs was conservatively chosen for the primary side as 170 V for this application based on maximum input voltage of 36 V. This was to account for any transient spikes that were seen during operation. Also ensure that the GaN FETs are properly sized based on the primary current calculations in 节 9.2.2.6.

9.2.2.8 Synchronous Rectificier FETs

The maximum voltage stress that will be seen by the synchronous rectifier switch on the secondary side can be calculated using 方程式 55.

$$V_{SR\_STRESS} = V_{OUT} + \frac{V_{IN\_MAX}}{N_{PS}} \tag{55}$$

$$V_{SR\_STRESS} = 5\ V + \frac{36\ V}{2.5} = 19.4\ V \tag{56}$$

Note that the maximum expected voltage is approximately 20 V, but a higher rating should be selected to allow for transient spikes. For the design, an 80-V rated GaN FET was conservatively chosen for the synchronous rectifier. The current rating should be sufficient to handle the maximum secondary current as calculated in 节 9.2.2.6. In order to reduce the current through GaN FET during the soft-start period, when the controller SRA and SRB signals are off, a Schottky diode can be used in parallel with the synchronous rectifier GaN FETs. This diode would also mitigate the reverse conduction losses attributed to the GaN FET during the dead time and boost the overall efficiency of the system.

9.2.2.9 RCD Clamp

A resistor-capacitor-diode clamp circuit can be used to limit the voltage at the switch node. The equations below can be used to determine initial values for the resistor and capacitor, but the circuit will need to be optimized through testing. First, calculate the clamp voltage by determining how much overshoot is allowable at the switch node.

$$V_{CLAMP} = K_{CLAMP} \times N_{PS} \times (V_{OUT} + V_{SR}) \tag{57}$$

The parameter K_{CLAMP} defines the target overshoot value. For example, set K_{CLAMP} to 1.5 for 50% allowable overshoot.

Next, the leakage inductance L_L and peak primary current I_{PRI_MAX} of the transformer can be used to approximate the clamp resistor. The clamp capacitor value can be determined thereafter. Note that ΔV_{CLAMP} defines the allowable ripple for the clamp capacitor.

$$R_{CLAMP} = \frac{V_{CLAMP}{}^2}{0.5 \times L_L \times I_{PRI\_MAX}{}^2 \times \frac{V_{CLAMP}}{V_{CLAMP} - (N_{PS} \times (V_{OUT} + V_{SR}))} \times f_{sw}} \tag{58}$$

$$C_{CLAMP} = \frac{V_{CLAMP}}{\Delta V_{CLAMP} \times V_{CLAMP} \times R_{CLAMP} \times f_{sw}} \tag{59}$$

9.2.2.10 Output Inductor

For the output inductor, a ripple current of 40% was targeted for the design. Based on the selected ripple current, 方程式 60 can be used to determine the output inductor value. K_L is the current ripple factor, which will be set to 0.4 in this instance.

$$L_{OUT} = \frac{\left(\frac{V_{IN\_MAX}}{N_{PS}} - V_{OUT} - V_{SR}\right) \times D_{MIN}}{f_{sw} \times K_L \times I_{OUT}} \tag{60}$$

$$L_{OUT} = \frac{\left(\frac{36\text{ V}}{2.5} - 5\text{ V} - 0.5\text{ V}\right) \times 0.22}{500\text{ kHz} \times 0.4 \times 20\text{ A}} = 0.5\ \mu\text{H} \tag{61}$$

The value of the inductor selected for the design is 0.47 µH.

9.2.2.11 Output Capacitance and Filter

Generally, there are two different calculations that can be used to determine the output capacitance required for the converter. The first calculates the amount of capacitance required to meet the maximum allowable voltage deviation at the output in response to a worst-case load transient as shown in 方程式 62. The second, shown in 方程式 64, determines the amount of output capacitance that is needed to meet the output voltage ripple requirements of the design. Once the two different calculations are performed, the maximum of these should be chosen as the output capacitance for the design. The calculations are shown for target voltage ripple of 2% of the output voltage and maximum allowable voltage deviation of 2.5% of the output voltage.

$$C_{OUT} > \frac{\Delta I_{STEP}}{2\pi \times \Delta V_{OUT} \times f_c} \tag{62}$$

$$C_{OUT} > \frac{10\text{ A}}{2\pi \times 0.025 \times 5\text{ V} \times 10\text{ kHz}} = 1.27\text{ mF} \tag{63}$$

$$C_{OUT} > \frac{I_{OUT} \times 2 \times D_{MAX}}{V_{RIPPLE} \times f_{sw}} \tag{64}$$

$$C_{OUT} > \frac{I_{OUT} \times 2 \times 0.37}{0.02 \times 5\text{ V} \times 500\text{ kHz}} = 294.12\ \mu\text{F} \tag{65}$$

Based on the calculations, at least 1.3 mF of output capacitance is required. When selecting capacitors, consider any derating of capacitance that is needed to account for aging, temperature, and DC bias.

For space-grade converter designs, there is another consideration when selecting the output capacitance. This is the impact of radiation induced single event transients (SET). Single energetic particle strikes can lead to momentary variation in the PWM variation of the controller, which in turn can lead to output voltage transients in the converter. Thus, even though the value above provides a minimum value to account for voltage ripple and/or load transients, additional capacitance is likely needed to for adequate SET mitigation. For the design example, approximately 2.3 mF of total output capacitance was used.

An additional output filter can be used to further reduce the noise of the output stage if deemed necessary. This output filter consists of an additional inductor and a small amount of ceramic capacitance. This ceramic capacitance is placed immediately downstream of the main output inductor that was determined in 节 9.2.2.10. The filter inductance is then located between the added ceramic capacitance and the bulk output capacitance that was determined to be required for the design. This approach can drastically reduce the output voltage ripple without significantly increasing the size and/or number of components required. The key for the secondary filter design is to choose the resonant frequency such that it is higher than the targeted crossover frequency yet well below the switching frequency and ESR zero of the bulk output capacitance. 方程式 66, 方程式 67, and 方程式 68 can be used to determine the ESR zero as well as the resonant frequency and attenuation of the additional output filter.

$$f_{zero} = \frac{1}{2\pi \times C_{OUT\_BULK} \times ESR_{BULK}} \tag{66}$$

$$f_{resonant} = \frac{1}{2\pi \times L_f \times C_{OUT\_BULK}} \tag{67}$$

$$Att_{fsw} = 40\log_{10}\left(\frac{f_{sw}}{f_{resonant}}\right) - 20\log10\left(\frac{f_{sw}}{f_{zero}}\right) \tag{68}$$

In the event that there is peaking at high frequencies due to the output filter, a resistor can be used to dampen this peaking effect. 方程式 69 and 方程式 70 can be used to determine the frequency of the peaking and the value of the resistor needed to provide adequate damping.

$$\omega_o = \frac{2 \times \left(C_{OUT\_CER} + C_{OUT\_BULK}\right)}{L_f \times C_{OUT\_CER} \times C_{OUT\_BULK}} \tag{69}$$

$$R_f = \frac{R_{OUT} \times L_f \times \left(C_{OUT\_CER} + C_{OUT\_BULK}\right) - \frac{L_f}{\omega_o}}{\frac{R_{OUT} \times \left(C_{OUT\_CER} + C_{OUT\_BULK}\right)}{\omega_o} - \left(L_f \times C_{OUT\_CER}\right)} \tag{70}$$

9.2.2.12 Sense Resistor

The converter was designed such that the cycle-by-cycle limiting will begin once the output current reaches roughly 35 A. Given that the peak inductor current at maximum load current is 24.25 A, this provides about 45% margin before an overcurrent event is detected by the controller. The primary side current is being sensed at CS_ILIM, so the turns ratio must be accounted for when calculating the necessary value of the sense resistor. Likewise, a current sense transformer with turns ratio of 1:100 is used to step down the primary current. The following calcuations are used to arrive at the value of R_{CS} that translates to the desired output overcurrent level.

$$I_{LIM} = I_{L,PEAK} \times \frac{N_S}{N_P} \times \frac{N_{CSP}}{N_{CSS}} \tag{71}$$

$$I_{LIM} = 35\ \text{A} \times \frac{1}{2.5} \times \frac{1}{100} = 0.14\ \text{A} \tag{72}$$

$$R_{CS} = \frac{V_{CS\_ILIM}}{I_{LIM}} \tag{73}$$

$$R_{CS} = \frac{1.05\ \text{V}}{0.14\ \text{A}} = 7.73\ \Omega \tag{74}$$

Based on the calculation, a 7.5-Ω resistor was selected for R_{CS}.

9.2.2.13 Hiccup Capacitor

For the design, the value of the hiccup capacitor used is the minimum recommended value of 3.3 nF. Based on this value, the delay and hiccup times of the converter after an overcurrent are detected can be calculated.

$$t_{delay} = \frac{C_{HICC} \times 0.6\ \text{V}}{80\ \mu\text{A}} \tag{75}$$

$$t_{delay} = \frac{3.3\ \text{nF} \times 0.6\ \text{V}}{80\ \mu\text{A}} = 24.75\ \mu\text{s} \tag{76}$$

$$t_{HICC} = \frac{C_{HICC} \times (1\ \text{V} - 0.3\ \text{V})}{1\ \mu\text{A}} \tag{77}$$

$$t_{HICC} = \frac{3.3\ \text{nF} \times (1\ \text{V} - 0.3\ \text{V})}{1\ \mu\text{A}} = 2.31\ \text{ms} \tag{78}$$

Note that as mentioned in 节 8.3.15, the delay time calculation is an approximation and the actual time depends on the nature of the overcurrent.

9.2.2.14 Frequency Compensation Components

For this design, Type 2A compensation was used. With a target crossover frequency of 10 kHz, the guidelines shown in 节 8.3.18 are used here to determine the compensation values needed for the compensation network. The power stage transconductance is first needed in order to calculate the frequency compensation component values.

$$gm_{PS} = \frac{N_P \times N_{CSS}}{CCSR \times R_{CS} \times N_S \times N_{CSP}} \tag{79}$$

$$gm_{PS} = \frac{2.5 \times 100}{2.06 \times 7.5\ \Omega \times 1 \times 1} = 16.2\ \frac{\text{A}}{\text{V}} \tag{80}$$

With the power stage transconductance calculated as 16.2 A/V, the values of the external components needed at the COMP pin can be resolved.

$$R_{COMP} = \frac{2\pi \times f_c \times V_{OUT} \times C_{OUT}}{gm_{ea} \times V_{REF} \times gm_{PS}} \tag{81}$$

$$R_{COMP} = \frac{2\pi \times 10\ \text{kHz} \times 5\ \text{V} \times 2.3\ \text{mF}}{1800 \times 10^{-6} \frac{\text{A}}{\text{V}} \times 0.613\ \text{V} \times 16.2 \frac{\text{A}}{\text{V}}} = 40.4\ \text{k}\Omega \tag{82}$$

$$C_{COMP} = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_{COMP}} \tag{83}$$

$$C_{COMP} = \frac{5\ \text{V} \times 2.3\ \text{mF}}{20\ \text{A} \times 40.2\ \text{k}\Omega} = 14.3\ \text{nF} \tag{84}$$

For the output capacitance 7 × 330-μF polymer tantalum capacitors were used to meet the 2.3-mF value that was needed for the design. At the selected switching frequency and output voltage, each of these capacitors had an ESR of roughly 6 mΩ. As such, the equivalent ESR used to determine the frequency of the ESR zero in the frequency response is equivalent the parallel resistance of these seven capacitors, which is 0.86 mΩ. The ESR zero frequency is then used in the calculation of C_{HF}.

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR} \tag{85}$$

$$f_{ESR} = \frac{1}{2\pi \times 2.3\ \text{mF} \times 0.86\ \text{m}\Omega} = 80.73\ \text{kHz} \tag{86}$$

$$C_{HF} = \frac{1}{2\pi \times R_{COMP} \times f_{ESR}} \tag{87}$$

$$C_{HF} = \frac{1}{2\pi \times 40.2\ \text{k}\Omega \times 80.73\ \text{kHz}} = 49.04\ \text{pF} \tag{88}$$

The values of R_{COMP}, C_{COMP}, and C_{HF} selected were 40.2 kΩ, 15 nF, and 47 pF, respectively. Note that like many other aspects of the design, the frequency compensation is often tuned during testing in order to obtain the best possible performance.

9.2.2.15 Slope Compensation Resistor

The slope compensation for the converter should be tailored by using the RSC pin of the TPS7H5001-SP. As recommended in 节 8.3.17, the slope compensation should be set to be equal to the falling slope of the output inductor in order to optimize sub-harmonic damping. The slope compensation that is calculated is dependent on the transformer turns ratio, current sense turns ratio, output inductor and current sense resistor that have been selected for the push-pull design.

$$SC = \frac{V_{OUT}}{L} \times \frac{N_S}{N_P} \times \frac{N_{CSP}}{N_{CSS}} \times R_{CS} \tag{89}$$

$$SC = \frac{5\ \text{V}}{0.47\ \mu\text{H}} \times \frac{1}{2.5} \times \frac{1}{100} \times 7.5\ \Omega = 319148.94 \frac{\text{V}}{\text{s}} = 0.319 \frac{\text{V}}{\mu\text{s}} \tag{90}$$

$$RSC = \frac{28.3}{SC^{1.1}} \tag{91}$$

$$RSC = \frac{28.3}{0.319^{1.1}} = 99.4\ \text{k}\Omega \tag{92}$$

A resistor value of 102 kΩ is connected between RSC and AVSS for the design.

9.2.3 Application Curves

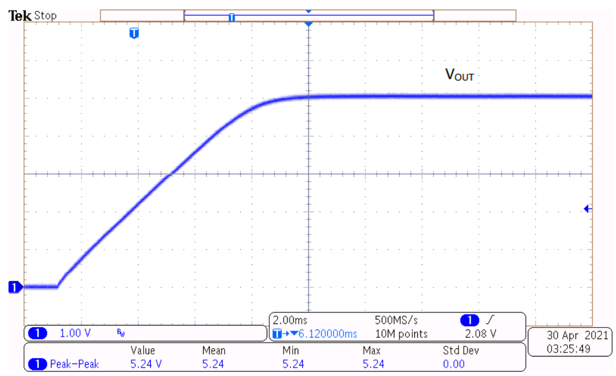


图 9-2. V_{OUT} Soft-Start of Push-Pull Converter With I_{OUT} = 10 A

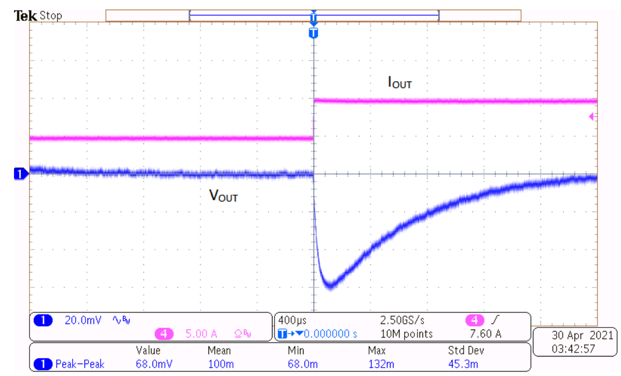


图 9-3. 5-A Load Step Response for Push Pull Converter

9.3 Power Supply Recommendations

The TPS7H500x-SP controllers are designed to operate from an input voltage supply range between 4 V and 14 V. The input voltage supply for the controller should be well regulated and properly bypassed for best electrical performance. A minimum input bypass capacitor of 0.1 µF is required from VIN to AVSS, but additional capacitance can be used to help improve the noise and radiation performance of the controller. It is recommended to use ceramic capacitors (X5R or better) for bypassing, and these capacitors should be placed as close as possible to the controller with a low impedance path to AVSS. Additional bulk capacitors should be used if the input supply is more than a few inches from TPS7H500x-SP controller.

9.4 Layout

9.4.1 Layout Guidelines

In order to increase the reliability of the converter design using the TPS7H500x-SP series, the following layout guidelines should be followed.

- Route the feedback trace as far away as possible from power magnetics components (inductor and/or power transformer) and other noise inducting traces on the printed circuit board (PCB) such as the switch node. If the feedback trace is routed beneath the power magnetic component, ensure that this trace is on another layer of the PCB with at least one ground layer separating the trace from the inductor or transformer.
- Minimize the copper area of the converter switch node for the best noise performance and reduction of parasitic capacitance to reduce switching losses. Ensure that any noise sensitive signals, such as the feedback trace, are routed away from this node as it contains a high dv/dt switching signal.
- All high di/dt and dv/dt switching loops in the power stage should have the paths minimized. This will help to reduce EMI, lower stresses on the power devices, and reduce any noise coupling into the control loop.
- Keep the analog ground of the controller (AVSS) separate from the power ground of the power stage that contains high frequency, high di/dt currents. These two grounds should be connected at a single point in the PCB layout. The sources of power semiconductor switches, the returns for bulk input capacitors of the power stage, and the ouput capacitor return should all be connected to the PCB power ground.
- All high current traces on the PCB should be short, direct, and as wide as possible. A good rule is to make the traces a minimum of 15 mils (0.381 mm) per ampere.

- Place all filtering and bypass capacitors for VIN, REFCAP, and VLDO as close as possible to the controller. Surface mount ceramic capacitors with lower ESR and ESL are recommended as these reduce the potential for noise coupling compared to through-hole capacitors. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the respective pin, and AVSS. Each bypass capacitor should have a good, low impedance connection to AVSS.
- External compensation components should be placed near the COMP pin of the controller. Surface mount components are recommended here as well.
- Attempt to keep the resistor divider used to generate the voltage at VSENSE close to the device in order to reduce noise coupling. Minimize stray capacitance to the VSENSE pin.
- OUTA, OUTB, SRA, and SRB are used to drive the inputs of a gate driver, isolator, or gate drive transformer. The PCB traces connected to these pins carry high dv/dt signals. Reduce noise coupling by routing these these PCB traces away from any traces connected to VSENSE, COMP, RT, CS_ILIM, HICC, LEB, RSC, PS, and SP.
- In addition to utilizing the leading edge blank time programmability of the controller, RC filtering may be required for the sensed current signal input to CS_ILIM. Keep the resistor and capacitor in close vicinity to CS_LIM to filter any ringing and/or spikes that may be present on the sensed current signal.
- When operating in internal oscillator mode with SYNC as an output, route the SYNC signal away from noise sensitive signals/pins such as VSENSE, COMP, RT, CS_ILIM, LEB, RSC, PS, and SP. Special care should be taken to eliminate noise from SYNC to HICC since these pins are adjacent to one another. It is recommended that the capacitor from HICC to AVSS be at least 3.3 nF to help with the reduction of the noise.
- For CFP option, connect the backside metallization of the TPS7H500x-SP to the AVSS plane of the PCB using multiple vias. It is recommended to avoid putting solder paste directly on top of the vias unless these vias are tented or filled.

9.4.2 Layout Example

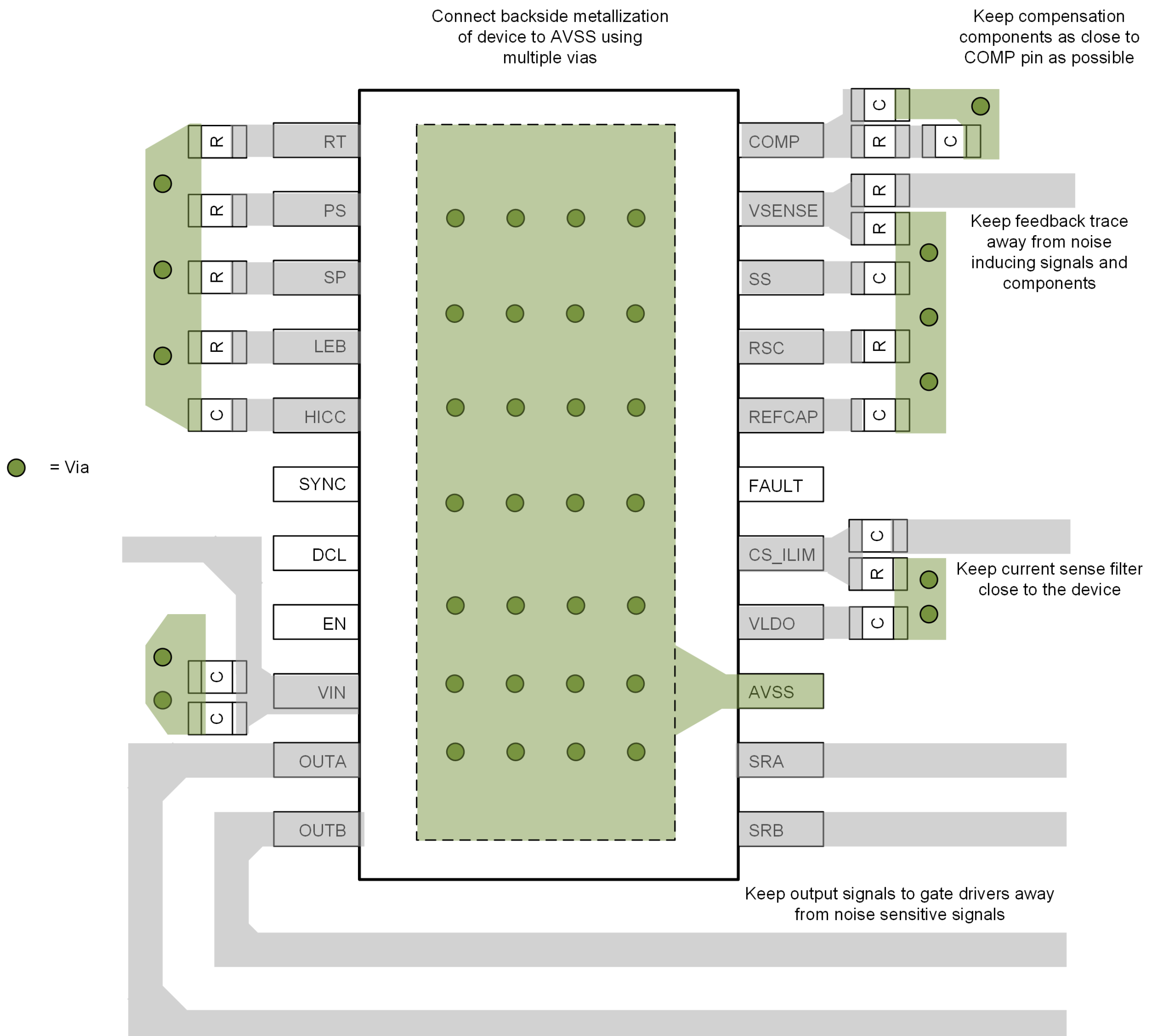


图 9-4. PCB Layout Example for CFP Package

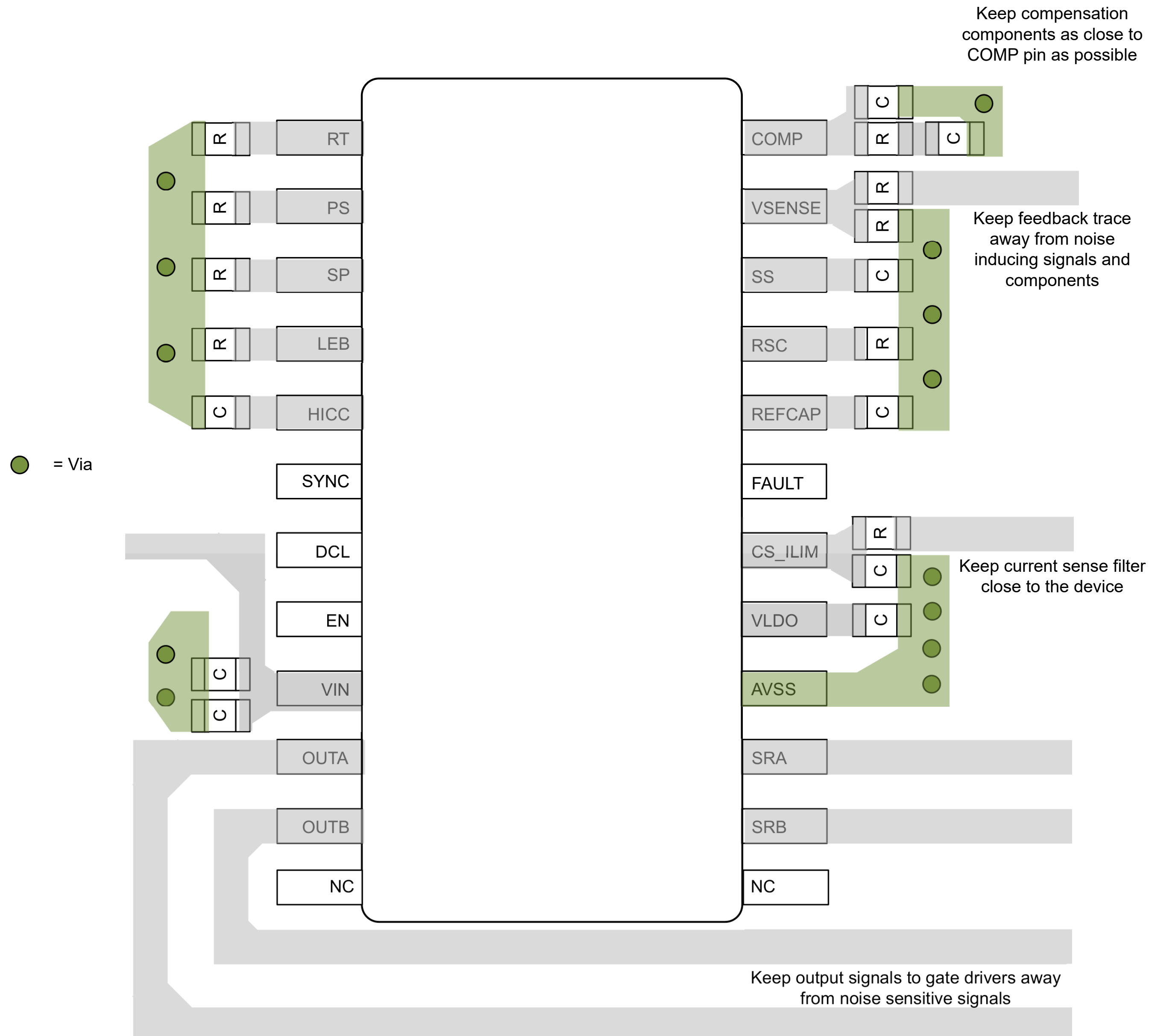


图 9-5. PCB Layout Example for TSSOP Package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H5001-SP Evaluation Module* user's guide
- Texas Instruments, *TPS7H5002/3/4-SP Evaluation Modules* user's guide
- Texas Instruments, *TPS7H5001-SP Total Ionizing Dose (TID)* radiation report
- Texas Instruments, *TPS7H5002-SP Total Ionizing Dose (TID)* radiation report
- Texas Instruments, *TPS7H5003-SP Total Ionizing Dose (TID)* radiation report
- Texas Instruments, *TPS7H5004-SP Total Ionizing Dose (TID)* radiation report
- Texas Instruments, *TPS7H500x-SP Single-Event Effects (SEE)* radiation report
- Texas Instruments, *TPS7H5001-SP Neutron Displacement Characterization* test report

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

10.4 Trademarks

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所有商标均为其各自所有者的财产。

10.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (August 2023) to Revision F (August 2024) **Page**

- 在*特性*、*说明*、*器件选项以及引脚配置和功能* 部分发布了 TPS7H5002-SP、TPS7H5003-SP 和 TPS7H5004-SP QMLP 选项，并更新了相关信息....................1
- Added orderable SN0022HFT for mechanical "no die" package to *Device Options* section....................4

Changes from Revision D (February 2023) to Revision E (August 2023) **Page**

- 发布了 TPS7H5001-SP QMLP 选项，并向*特性*、*说明*、*引脚功能*、*电气特性* 和*布局* 部分添加了相关信息.....1

- Added *Device Options* table..4
- Removed pin numbers and no connect (NC) pins from functional block diagrams in order to make these applicable for all package types in *Functional Block Diagram* section..33
- Added clarifications to *Layout Guidelines* section for guidelines that are specific to CFP package option......66

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R1822201PYE	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	R1822201P
5962R1822201V9A	Active	Production	XCEPT (KGD) | 0	10 | OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 125	
5962R1822201VXC	Active	Production	CFP (HFT) | 22	25 | TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 125	5962R1822201VXC TPS7H5001MHFTV
5962R1822202PYE	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	R1822202P
5962R1822202V9A	Active	Production	XCEPT (KGD) | 0	10 | OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 125	
5962R1822202VXC	Active	Production	CFP (HFT) | 22	25 | TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 125	5962R1822202VXC TPS7H5002MHFTV
5962R1822203PYE	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	R1822203P
5962R1822203V9A	Active	Production	XCEPT (KGD) | 0	10 | OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 125	
5962R1822203VXC	Active	Production	CFP (HFT) | 22	25 | TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 125	5962R1822203VXC TPS7H5003MHFTV
5962R1822204PYE	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	R1822204P
5962R1822204V9A	Active	Production	XCEPT (KGD) | 0	10 | OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 125	
5962R1822204VXC	Active	Production	CFP (HFT) | 22	25 | TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 125	5962R1822204VXC TPS7H5004MHFTV
TPS7H5001HFT/EM	Active	Production	CFP (HFT) | 22	25 | TUBE	Yes	NIAU	N/A for Pkg Type	25 to 25	TPS7H5001HFT EVAL ONLY
TPS7H5001Y/EM	Active	Production	XCEPT (KGD) | 0	10 | OTHER	Yes	Call TI	N/A for Pkg Type	25 to 25	
TPS7H5002HFT/EM	Active	Production	CFP (HFT) | 22	25 | TUBE	Yes	NIAU	N/A for Pkg Type	25 to 25	TPS7H5002HFT EVAL ONLY
TPS7H5002Y/EM	Active	Production	XCEPT (KGD) | 0	10 | OTHER	Yes	Call TI	N/A for Pkg Type	25 to 25	
TPS7H5003HFT/EM	Active	Production	CFP (HFT) | 22	25 | TUBE	Yes	NIAU	N/A for Pkg Type	25 to 25	TPS7H5003HFT EVAL ONLY
TPS7H5003Y/EM	Active	Production	XCEPT (KGD) | 0	10 | OTHER	Yes	Call TI	N/A for Pkg Type	25 to 25	
TPS7H5004HFT/EM	Active	Production	CFP (HFT) | 22	25 | TUBE	Yes	NIAU	N/A for Pkg Type	25 to 25	TPS7H5004HFT EVAL ONLY
TPS7H5004Y/EM	Active	Production	XCEPT (KGD) | 0	10 | OTHER	Yes	Call TI	N/A for Pkg Type	25 to 25	

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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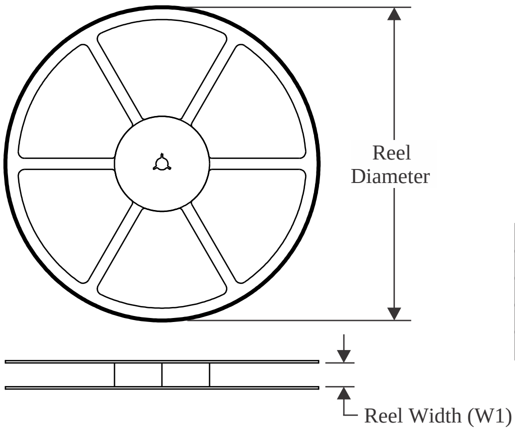
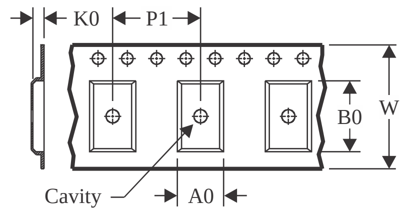
TAPE AND REEL INFORMATION

REEL DIMENSIONS

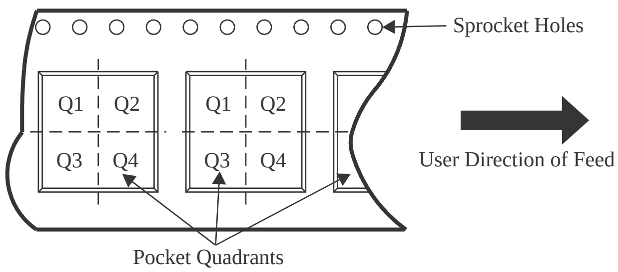


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

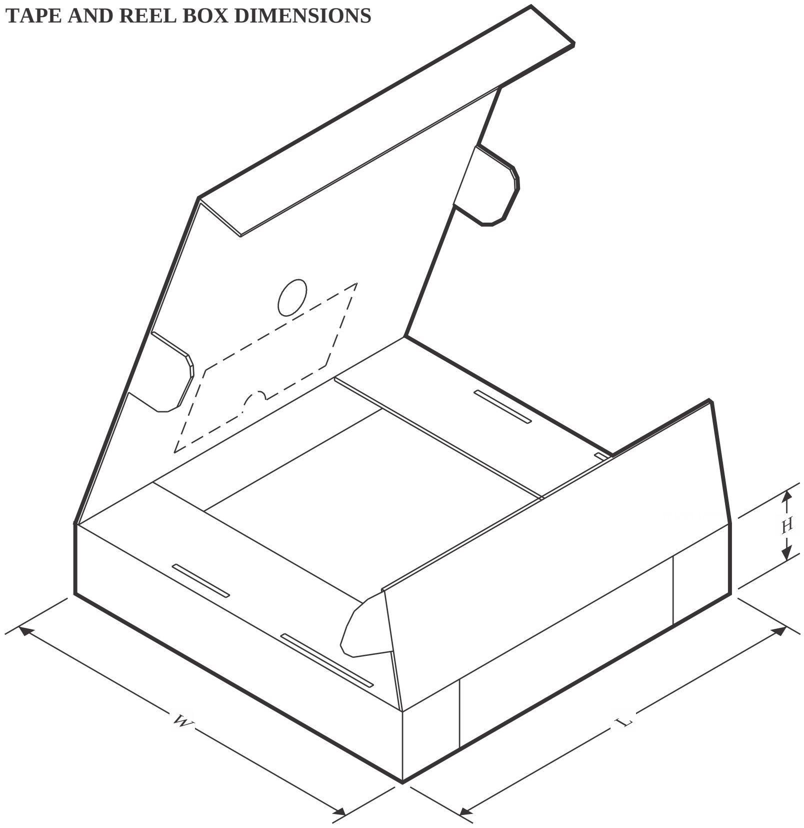
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962R1822201PYE	TSSOP	PW	24	250	178.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
5962R1822202PYE	TSSOP	PW	24	250	178.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
5962R1822203PYE	TSSOP	PW	24	250	178.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
5962R1822204PYE	TSSOP	PW	24	250	178.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

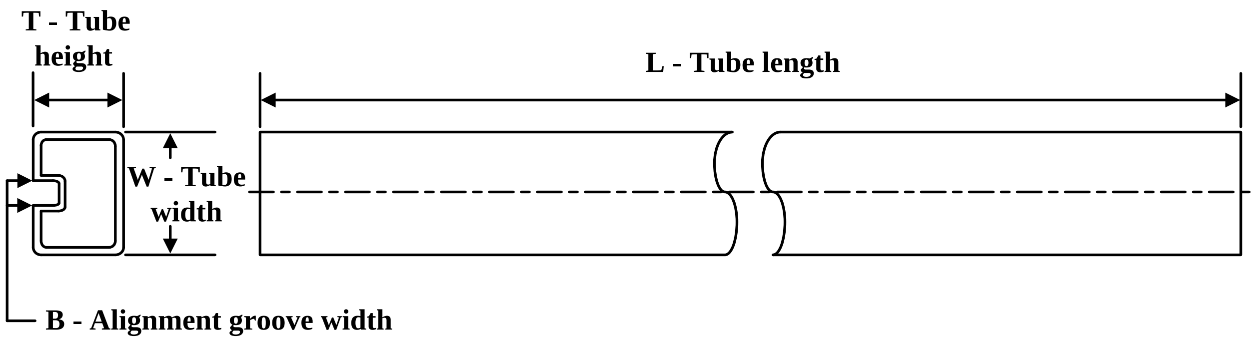
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

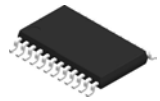
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962R1822201PYE	TSSOP	PW	24	250	210.0	185.0	35.0
5962R1822202PYE	TSSOP	PW	24	250	210.0	185.0	35.0
5962R1822203PYE	TSSOP	PW	24	250	210.0	185.0	35.0
5962R1822204PYE	TSSOP	PW	24	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R1822201VXC	HFT	CFP	22	25	506.98	32.77	9910	NA
5962R1822202VXC	HFT	CFP	22	25	506.98	32.77	9910	NA
5962R1822203VXC	HFT	CFP	22	25	506.98	32.77	9910	NA
5962R1822204VXC	HFT	CFP	22	25	506.98	32.77	9910	NA
TPS7H5001HFT/EM	HFT	CFP	22	25	506.98	32.77	9910	NA
TPS7H5002HFT/EM	HFT	CFP	22	25	506.98	32.77	9910	NA
TPS7H5003HFT/EM	HFT	CFP	22	25	506.98	32.77	9910	NA
TPS7H5004HFT/EM	HFT	CFP	22	25	506.98	32.77	9910	NA

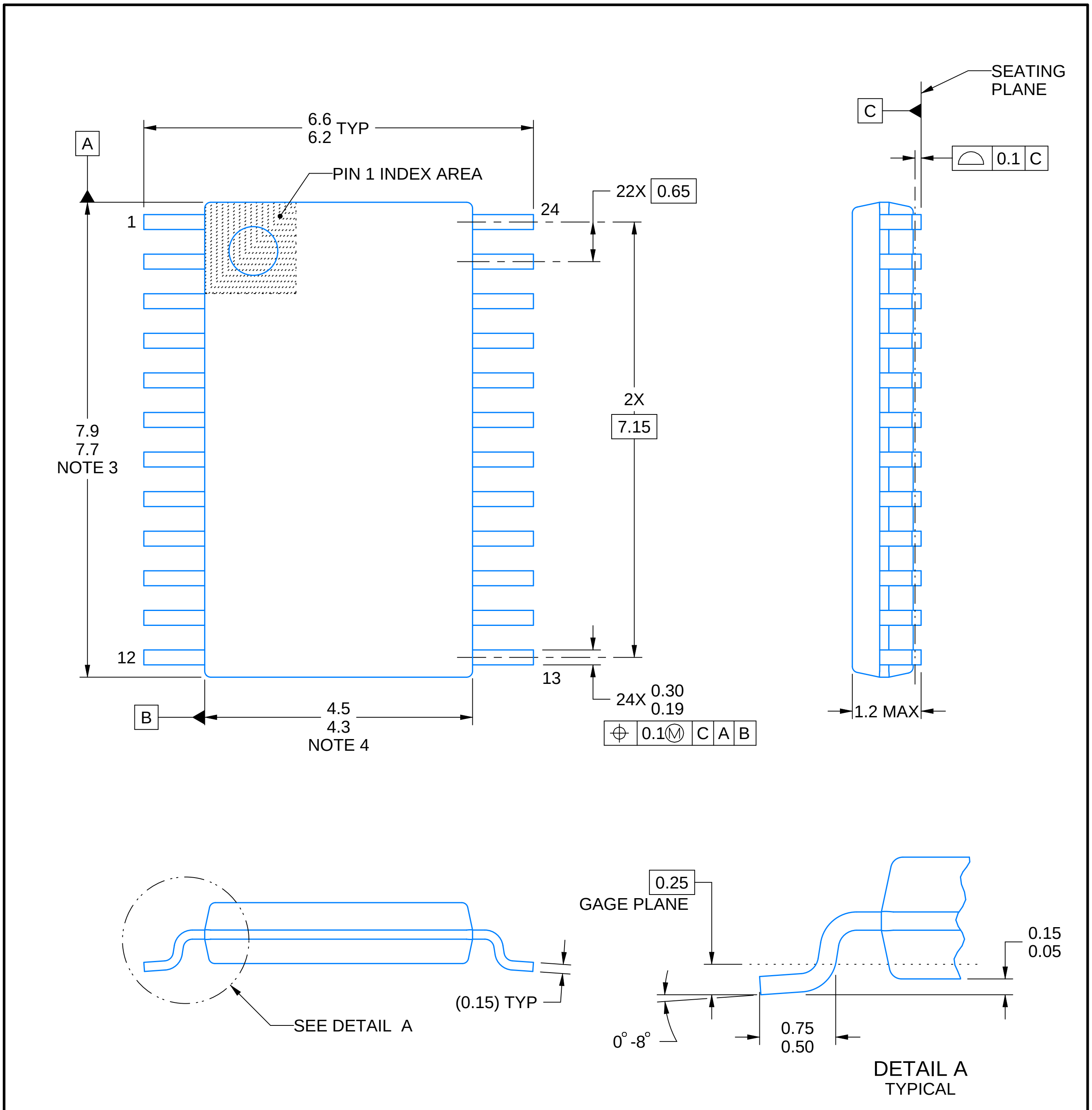


PACKAGE OUTLINE

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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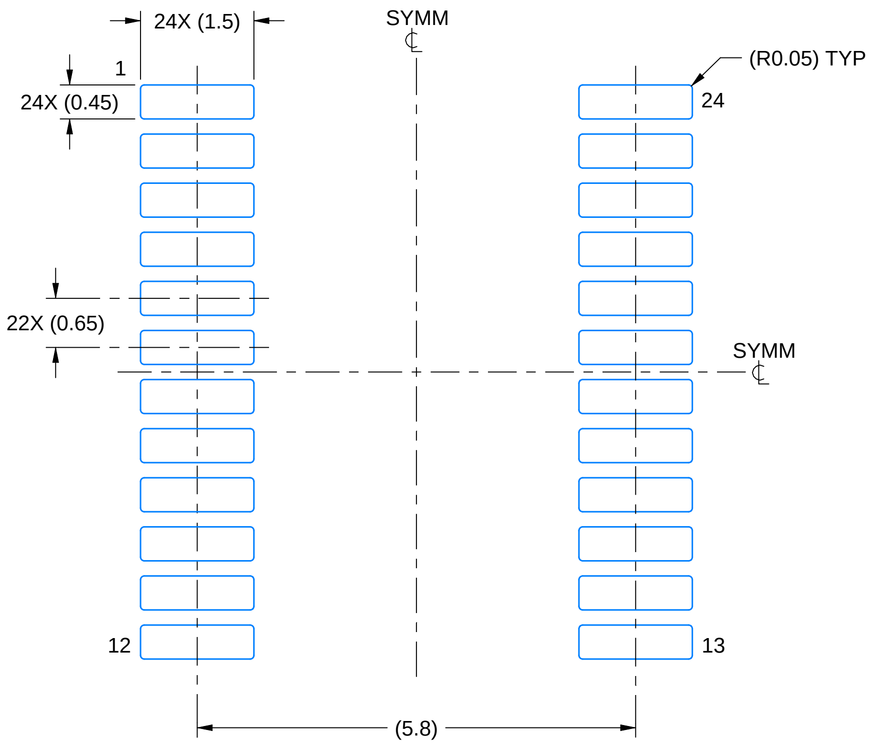
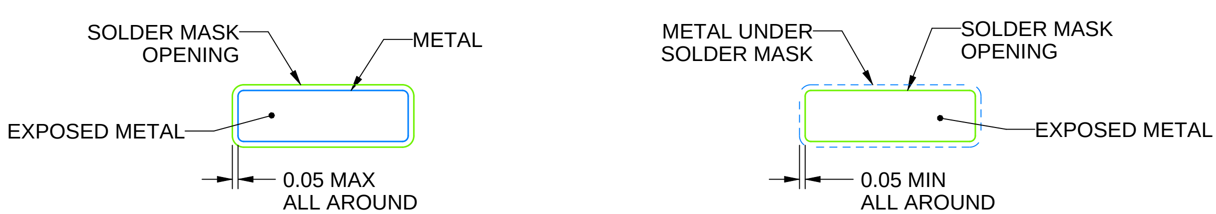
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

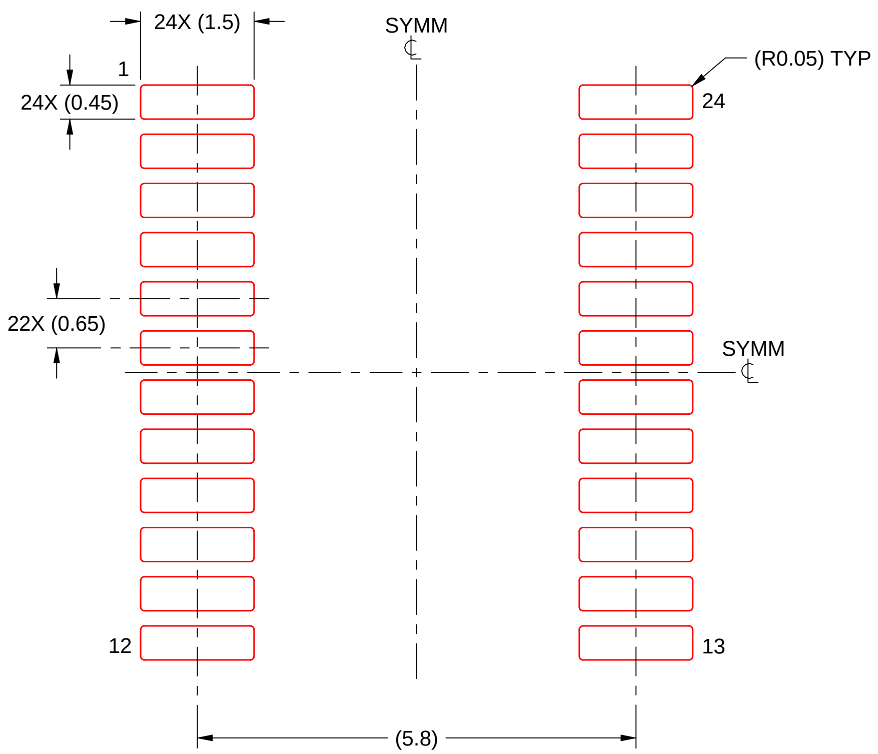


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

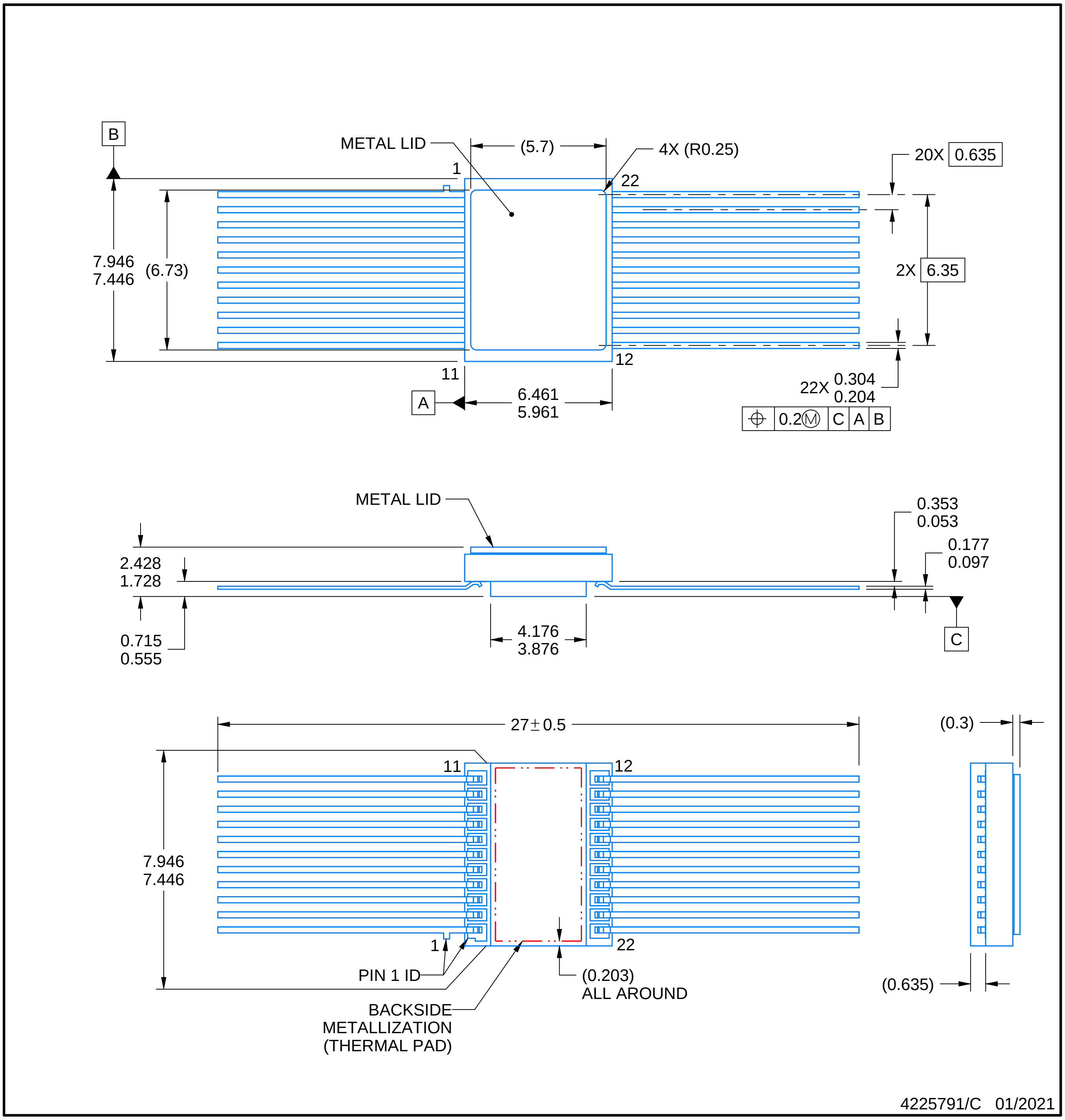


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

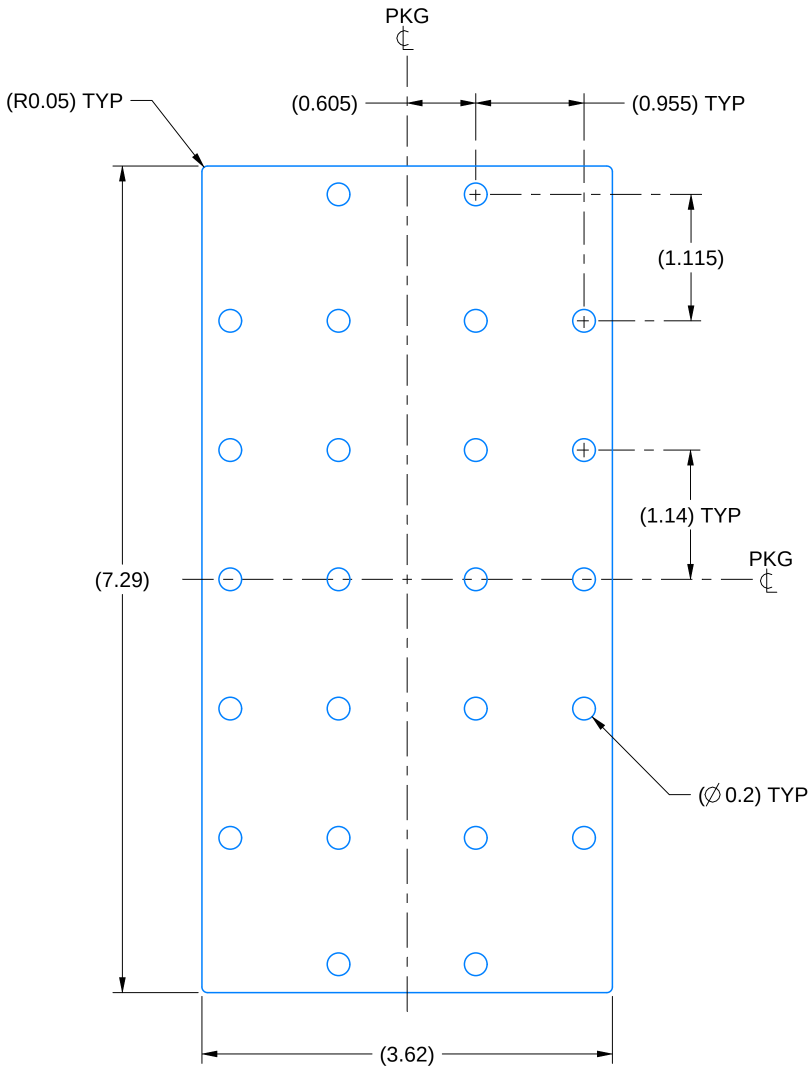
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metalization



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

4225791/C 01/2021

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2186323	03/13/2020	R. RAZAK / ANIS FAUZI
B	ADD LAND PATTERN VIEW / SHEET	2190485	10/22/2020	R. RAZAK / ANIS FAUZI
C	UPDATE TOTAL LEAD LENGTH TO 27± 0.5	2192775	01/28/2021	R. RAZAK / ANIS FAUZI

SCALE	SIZE		REV	PAGE
	A	4225791	C	4 OF 4

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