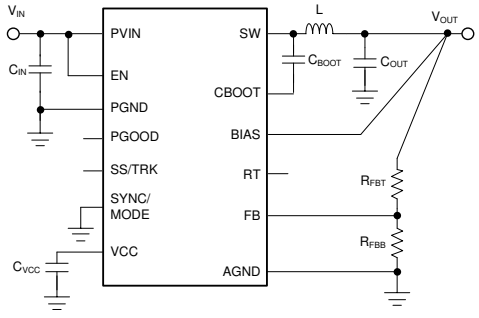
# TPS7H4010-SEP 采用增强型航天塑料的耐辐射 3.5V 至 32V、6A 同步降压转换器

## 1 特性

- 耐辐射
  - SEL、SEB 和 SEGR 对于 LET 的抗扰度高达 43MeV-cm$^2$/mg
  - SET 和 SEFI 的 LET 特征值高达 43MeV-cm$^2$/mg
  - 每个晶圆批次的保障 TID 高达 20krad(Si)
  - TID 特征值高达 30krad(Si)
- 增强型航天塑料
  - 受控基线
  - Au 键合线和 NiPdAu 铅涂层
  - 采用增强型模塑化合物实现低释气
  - 制造、组装和测试一体化基地
  - 延长了产品生命周期
  - 延长了产品变更通知
  - 产品可追溯性
- 宽电压转换范围：
  - $t_{ON-MIN}$ = 60ns（典型值）
  - $t_{OFF-MIN}$ = 70ns（典型值）
- 低 MOSFET 导通电阻：
  - $R_{DS\_ON\_HS}$ = 53mΩ（典型值）
  - $R_{DS\_ON\_LS}$ = 31mΩ（典型值）
- 可调频率范围：350 kHz 至 2.2MHz
- 可与外部时钟同步
- 内部补偿
- 电源正常状态标志
- 通过精密使能功能对系统 UVLO 进行编程
- 固定或可调的软启动时间
- 逐周期电流限制
- 具有断续模式的短路保护
- 热关断保护




简化版原理图

## 2 应用

- 用于 FPGA、微控制器、数据转换器和 ASIC 的太空卫星负载点电源
- 通信负载
- 命令和数据处理
- 光学成像有效载荷
- 雷达成像有效载荷
- 激光通信有效载荷
- 导航有效载荷
- 科学勘探有效载荷

## 3 说明

TPS7H4010-SEP 是一款易于使用的同步降压直流/直流转换器，能够驱动高达 6A 的负载电流，电源电压范围为 3.5V 至 32V。TPS7H4010-SEP 以极小的解决方案尺寸提供优异的效率和输出精度。此器件采用峰值电流模式控制。可调开关频率、与外部时钟同步、FPWM 选项、电源正常状态标志、精密使能、可调节软启动以及跟踪等其他特性可为各种应用提供灵活且简单易用的解决方案。轻负载时的自动频率折返和可选的外部偏置电源可在整个负载范围内提高效率。该器件需要超少的外部元件，引脚排列设计可简化 PCB 布局，提供出色的 EMI 和热性能。保护特性包括热关断、输入欠压锁定、逐周期电流限制和断续短路保护。

**器件信息**

| 器件型号(1) | 等级 | 封装 |
|---|---|---|
| TPS7H4010MRNPTSEP | 20krad(Si) RLAT | WQFN (30) 6.00mm × 4.00mm 质量 = 57.2mg(2) |
| TPS7H4010MRNPSEP | | |
| TPS7H4010MKGDSEP | 20krad(Si) RLAT KGD | 裸片 |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 质量误差在 ±10% 以内。

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision * (November 2020) to Revision A (December 2021) | Page |
|---|---|
| • 在*说明*部分中和整篇数据表中将封装说明从 QFN 更新为了 WQFN | 1 |
| • 向*说明*部分中的“器件信息”表添加了其他可订购器件 | 1 |
| • Added bare die information to *Pin Configuration and Functions* section | 3 |
| • Updated maximum limit for Junction temperature in *Absolute Maximum Ratings* table | 7 |
| • Added specification for Junction temperature to *Recommended Operating Conditions* table | 7 |
| • Updated *Optimize Thermal Performance* section | 40 |
| • Updated *Related Documentation* section | 42 |

# 5 Pin Configuration and Functions

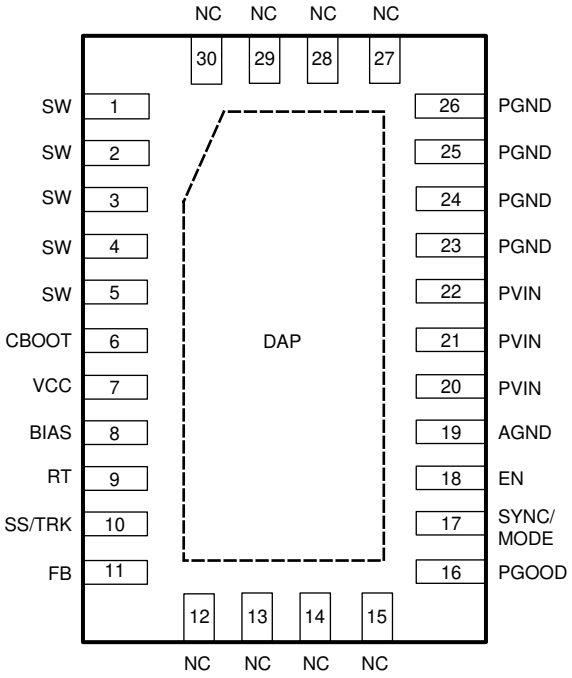



**图 5-1. RNP Package**
**30-Pin WQFN 6 mm × 4 mm × 0.8 mm**
**(Top View)**

**表 5-1. Pin Functions**

| PIN | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 – 5 | SW | P | Switching output of the regulator. Internally connected to source of the HS FET and drain of the LS FET. Connect to power inductor and bootstrap capacitor. |
| 6 | CBOOT | P | Bootstrap capacitor connection for HS FET driver. Connect a high-quality 470-nF capacitor from this pin to the SW pin. |
| 7 | VCC | P | Output of internal bias supply. Used as supply to internal control circuits and drivers. Connect a high-quality 2.2-µF capacitor from this pin to GND. TI does not recommend loading this pin by external circuitry. |
| 8 | BIAS | P | Optional BIAS LDO supply input. TI recommends tying to $V_{OUT}$ when 3.3 V ≤ $V_{OUT}$ ≤ 18 V, or tie to an external 3.3-V or 5-V rail if available, to improve efficiency. BIAS pin voltage must not be greater than $V_{IN}$. Tie to ground when not in use. |
| 9 | RT | A | Switching frequency setting pin. Place a resistor from this pin to ground to set the switching frequency. If floating, the default switching frequency is 500 kHz. Do not short to ground. |
| 10 | SS/TRK | A | Soft-start control pin. Leave this pin floating for a fixed internal soft-start ramp. An external capacitor can be connected from this pin to ground to extend the soft start time. A 2-µA current sourced from this pin charges the capacitor to provide the ramp. Connect to external ramp for tracking. Do not short to ground. |
| 11 | FB | I | Feedback input for output voltage regulation. Connect a resistor divider to set the output voltage. Never short this pin to ground during operation. |
| 12 – 15, 27 – 30 | NC | — | No internal connection. Connect to ground net and copper to improve heat sinking and board-level reliability. |
| 16 | PGOOD | O | Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = $V_{OUT}$ regulation OK, Low = $V_{OUT}$ regulation fault. PGOOD = LOW when EN = low and $V_{IN}$ > 2 V. |

表 5-1. Pin Functions (continued)

| PIN | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 17 | SYNC/MODE | I | Synchronization input and mode setting pin. Do not float. Tie to ground if not used.<br>• Tie to ground: auto mode, higher efficiency at light loads.<br>• Tie to logic high: forced PWM, constant switching frequency over load.<br>• Tie to external clock source: forced PWM, synchronize to the rising edge of the external clock. |
| 18 | EN | I | Enable input to regulator. Do not float. High = ON, Low = OFF. Can be tied to PVIN. Precision enable input allows adjustable input voltage UVLO using external resistor divider. |
| 19 | AGND | GND | Analog ground. Ground reference for internal circuitry. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB. |
| 20 – 22 | PVIN | P | Supply input to internal bias LDO and HS FET. Connect to input supply and input bypass capacitors $C_{IN}$. $C_{IN}$ must be placed right next to this pin and PGND pins on PCB, and connected with short and wide traces. |
| 23 – 26 | PGND | GND | Power ground, connected to the source of LS FET internally. Connect to system ground, DAP/EP, AGND, ground side of $C_{IN}$ and $C_{OUT}$ on PCB. Path to $C_{IN}$ must be as short as possible. |
| EP | DAP | GND | Low impedance connection to AGND. Connect to system ground on PCB. Major heat dissipation path for the device. Must be used for heat sinking by soldering to ground copper on PCB. Thermal vias are preferred to improve heat dissipation to other layers. |

(1) A = analog, I = input, O = output, P = power, GND = ground

表 5-2. Bare Die Information

| DIE THICKNESS | BACKSIDE FINISH | BACKSIDE POTENTIAL | BOND PAD METALLIZATION COMPOSITION | BOND PAD THICKNESS |
|---|---|---|---|---|
| 7.52 mils | Silicon with backgrind | GND | MetDCu | 574.5 nm |

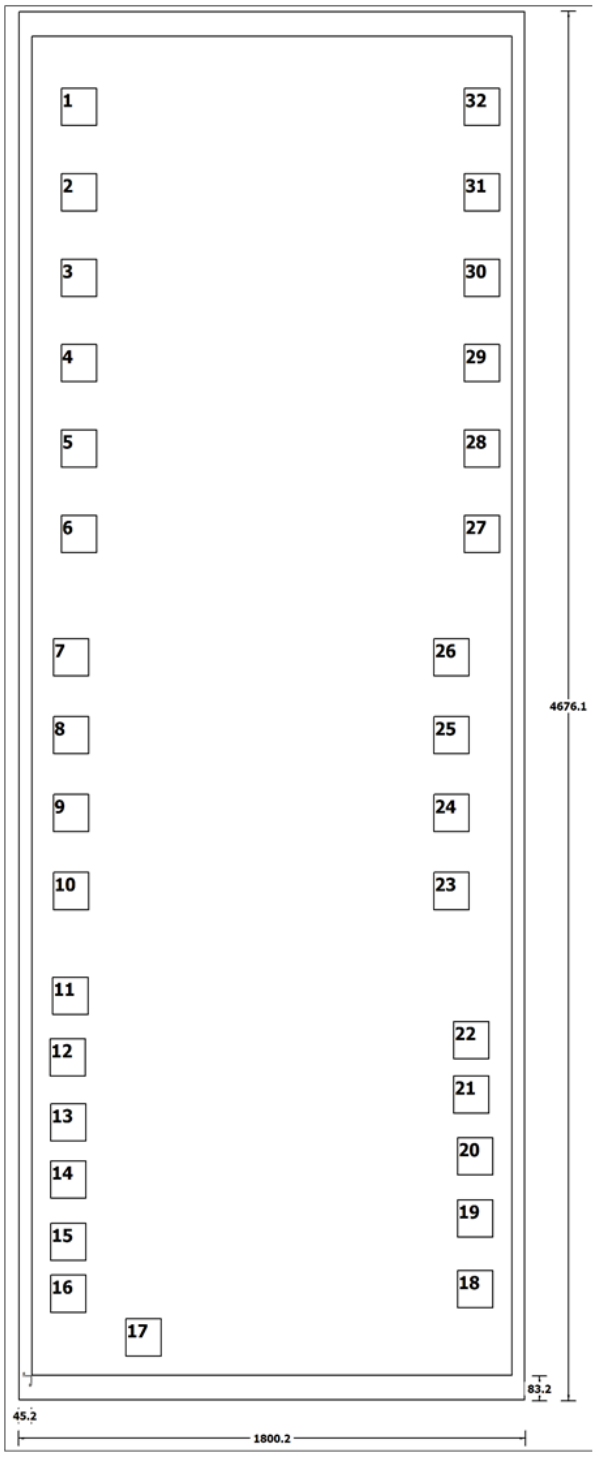



图 5-2. TPS7H4010-SEP Bare Die Diagram

表 5-3. Bond Pad Coordinates in Microns

| DESCRIPTION | PAD NUMBER | X MIN | Y MIN | X MAX | Y MAX |
|---|---|---|---|---|---|
| NC | 1 | 105.175 | 4204.585 | 235.375 | 4334.785 |
| SW | 2 | 105.175 | 3917.305 | 235.375 | 4047.505 |
| SW | 3 | 105.175 | 3630.025 | 235.375 | 3760.225 |
| SW | 4 | 105.175 | 3342.745 | 235.375 | 3472.945 |
| SW | 5 | 105.175 | 3055.465 | 235.375 | 3185.665 |
| SW | 6 | 105.175 | 2768.185 | 235.375 | 2898.385 |
| SW | 7 | 76.79 | 2352.945 | 206.99 | 2483.145 |
| SW | 8 | 76.79 | 2090.795 | 206.99 | 2220.995 |
| SW | 9 | 76.79 | 1828.645 | 206.99 | 1958.845 |
| SW | 10 | 76.79 | 1566.495 | 206.99 | 1696.695 |
| CBOOT | 11 | 74.375 | 1214.15 | 204.575 | 1344.35 |
| PVCC | 12 | 65.24 | 1006.81 | 195.44 | 1137.01 |
| VCC | 13 | 67.025 | 787.99 | 197.225 | 918.19 |
| BIAS | 14 | 67.025 | 595.56 | 197.225 | 725.76 |
| RT | 15 | 67.025 | 385.595 | 197.225 | 515.795 |
| SS | 16 | 67.025 | 211.435 | 197.225 | 341.635 |
| FB | 17 | 334.25 | 64.365 | 464.45 | 194.565 |
| PGOOD | 18 | 1511.79 | 227.185 | 1641.99 | 357.385 |
| SYNC | 19 | 1511.79 | 465.08 | 1641.99 | 595.28 |
| EN | 20 | 1511.79 | 673.54 | 1641.99 | 803.74 |
| AGND | 21 | 1497.72 | 881.895 | 1627.92 | 1012.095 |
| AVIN | 22 | 1497.72 | 1064.91 | 1627.92 | 1195.11 |
| PVIN | 23 | 1428.07 | 1566.495 | 1558.27 | 1696.695 |
| PVIN | 24 | 1428.07 | 1828.645 | 1558.27 | 1958.845 |
| PVIN | 25 | 1428.07 | 2090.795 | 1558.27 | 2220.995 |
| PVIN | 26 | 1428.07 | 2352.945 | 1558.27 | 2483.145 |
| PGND | 27 | 1535.835 | 2768.185 | 1666.035 | 2898.385 |
| PGND | 28 | 1535.835 | 3055.465 | 1666.035 | 3185.665 |
| PGND | 29 | 1535.835 | 3342.745 | 1666.035 | 3472.945 |
| PGND | 30 | 1535.835 | 3630.025 | 1666.035 | 3760.225 |
| PGND | 31 | 1535.835 | 3917.305 | 1666.035 | 4047.505 |
| PGND | 32 | 1535.835 | 4204.585 | 1666.035 | 4334.785 |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range of – 55°C to +125°C (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltages | PVIN to PGND | – 0.3 | 36 | V |
| | EN to AGND | – 0.3 | PVIN + 0.3 | |
| | FB, RT, SS/TRK to AGND | – 0.3 | 5 | |
| | PGOOD to AGND | – 0.3 | 20 | |
| | SYNC to AGND | – 0.3 | 5.5 | |
| | BIAS to AGND | – 0.3 | Lower of (PVIN + 0.3) or 20 | |
| | AGND to PGND | – 0.3 | 0.3 | |
| Output voltages | SW to PGND | – 0.3 | PVIN + 0.3 | V |
| | SW to PGND less than 10-ns transients | – 3.5 | 36 | |
| | CBOOT to SW | – 0.3 | 5 | |
| | VCC to AGND | – 0.3 | 5 | |
| $T_J$ | Junction temperature | – 55 | 150 | °C |
| $T_{stg}$ | Storage temperature | – 65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range of – 55°C to +125°C (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltages | PVIN to PGND | 3.5 | 32 | V |
| | EN | 0 | PVIN | |
| | FB | 0 | 4.5 | |
| | PGOOD | 0 | 18 | |
| | BIAS input not used | 0 | 0.3 | |
| | BIAS input used | 0 | Lower of (PVIN + 0.3) or 18 | |
| | AGND to PGND | – 0.1 | 0.1 | |
| Output voltage | VOUT | 1 | 95% of PVIN | V |
| Output current | IOUT | 0 | 6 | A |
| Junction temperature | $T_J$ | – 55 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS7H4010-SEP RNP (WQFN) 30 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 29.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 17.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 9.1 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 9.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature ($T_J$) range of –55°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated, $V_{IN}$ = 12 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE (PVIN PINS)** | | | | | | |
| PVIN | Operating input voltage | | 3.5 | | 32 | V |
| $I_{SD}$ | Shutdown quiescent current; measured at PVIN pin[1] | $V_{EN}$ = AGND, $T_J$ = 25°C | | 0.8 | 10 | µA |
| $I_{Q\_NONSW}$ | Operating quiescent current from PVIN (non-switching) | $V_{EN}$ = 2 V, $V_{FB}$ = 1.5 V, $V_{BIAS}$ = 3.3 V external | | 0.6 | 12 | µA |
| **ENABLE (EN PIN)** | | | | | | |
| $V_{EN\_VCC\_H}$ | Enable input high level for $V_{CC}$ output | $V_{EN}$ rising | | | 1.15 | V |
| $V_{EN\_VCC\_L}$ | Enable input low level for $V_{CC}$ output | $V_{EN}$ falling | 0.3 | | | V |
| $V_{EN\_VOUT\_H}$ | Enable input high level for $V_{OUT}$ | $V_{EN}$ rising | 1.14 | 1.196 | 1.25 | V |
| $V_{EN\_VOUT\_HYS}$ | Enable input hysteresis for $V_{OUT}$ | $V_{EN}$ falling hysteresis | | 100 | | mV |
| $I_{LKG\_EN}$ | Enable input leakage current | $V_{EN}$ = 2 V | | 1.4 | 200 | nA |
| **INTERNAL LDO (VCC PIN, BIAS PIN)** | | | | | | |
| $V_{CC}$ | Internal $V_{CC}$ voltage | PWM operation | | 3.27 | | V |
| | | PFM operation | | 3.1 | | |
| $V_{CC\_UVLO}$ | Internal $V_{CC}$ undervoltage lockout | $V_{CC}$ rising | 2.96 | 3.14 | 3.27 | V |
| | | $V_{CC}$ falling hysteresis | | 605 | | mV |
| $V_{BIAS\_ON}$ | Input changeover | $V_{BIAS}$ rising | | 3.09 | 3.25 | V |
| | | $V_{BIAS}$ falling hysteresis | | 63 | | mV |
| $I_{BIAS\_NONSW}$ | Operating quiescent current from external $V_{BIAS}$ (non-switching) | $V_{EN}$ = 2 V, $V_{FB}$ = 1.5 V, $V_{BIAS}$ = 3.3 V external | | 21 | 50 | µA |
| **VOLTAGE REFERENCE (FB PIN)** | | | | | | |
| $V_{FB}$ | Feedback voltage | PWM mode | 0.987 | 1.006 | 1.017 | V |
| $I_{LKG\_FB}$ | Input leakage current at FB pin | $V_{FB}$ = 1 V | | 0.2 | 60 | nA |

## 6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature ($T_J$) range of –55°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated, $V_{IN}$ = 12 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **HIGH SIDE DRIVER (CBOOT PIN)** | | | | | | |
| $V_{CBOOT\_UVLO}$ | CBOOT - SW undervoltage lockout | | 1.6 | 2.2 | 2.7 | V |
| **CURRENT LIMITS AND HICCUP** | | | | | | |
| $I_{HS\_LIMIT}$ | Short-circuit, high-side current limit(2) | | 7.4 | 8.7 | 9.85 | A |
| $I_{LS\_LIMIT}$ | Low-side current limit(2) | | 5.8 | 6.6 | 7.25 | A |
| $I_{NEG\_LIMIT}$ | Negative current limit | | | –5 | | A |
| $V_{HICCUP}$ | Hiccup threshold on FB pin | | 0.36 | 0.4 | 0.44 | V |
| $I_{L\_ZC}$ | Zero cross-current limit | | | –0.05 | | A |
| **SOFT START (SS/TRK PIN)** | | | | | | |
| $I_{SSC}$ | Soft-start charge current | | 1.8 | 2 | 2.2 | µA |
| $R_{SSD}$ | Soft-start discharge resistance | UVLO, TSD, OCP, or EN = AGND | | 1 | | kΩ |
| **POWER GOOD (PGOOD PIN) and OVERVOLTAGE PROTECTION** | | | | | | |
| $V_{PGOOD\_OV}$ | Power-good overvoltage threshold | % of FB voltage | 106% | 110% | 113% | |
| $V_{PGOOD\_UV}$ | Power-good undervoltage threshold | % of FB voltage | 86% | 90% | 93% | |
| $V_{PGOOD\_HYS}$ | Power-good hysteresis | % of FB voltage | | 1.2% | | |
| $V_{PGOOD\_VALID}$ | Minimum input voltage for proper PGOOD function | 50-µA pullup to PGOOD pin, $V_{EN}$ = AGND, $T_J$ = 25℃ | | 1.3 | 2 | V |
| $R_{PGOOD}$ | Power-good ON-resistance | $V_{EN}$ = 2.5 V | | 40 | 100 | Ω |
| | | $V_{EN}$ = AGND | | 30 | 90 | |
| **MOSFETS** | | | | | | |
| $R_{DS\_ON\_HS}$ (3) | High-side MOSFET ON-resistance | $I_{OUT}$ = 1 A, $V_{BIAS}$ = $V_{OUT}$ = 3.3 V | | 53 | 90 | mΩ |
| $R_{DS\_ON\_LS}$ (3) | Low-side MOSFET ON-resistance | $I_{OUT}$ = 1 A, $V_{BIAS}$ = $V_{OUT}$ = 3.3 V | | 31 | 55 | mΩ |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ (4) | Thermal shutdown threshold | Shutdown threshold | | 160 | | °C |
| | Recovery threshold | | | 135 | | |

(1) Shutdown current includes leakage current of the switching transistors.
(2) This current limit was measured as the internal comparator trip point. Due to inherent delays in the current limit comparator and drivers, the peak current limit measured in closed loop with faster slew rate will be larger, and valley current limit will be lower.
(3) Measured at pins.
(4) Ensured by design.

## 6.6 Timing Characteristics

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT LIMITS AND HICCUP** | | | | | | |
| $N_{OC}$ (1) | Number of switching cycles before hiccup is tripped | | | 128 | | cycles |
| $t_{OC}$ | Overcurrent hiccup retry delay time | | | 46 | | ms |
| **SOFT START (SS/TRK PIN)** | | | | | | |
| $t_{SS}$ | Internal soft-start time | CSS = OPEN, from EN rising edge to PGOOD rising edge | 3.5 | 6.3 | | ms |
| **POWER GOOD (PGOOD PIN) and OVERVOLTAGE PROTECTION** | | | | | | |
| $t_{PGOOD\_RISE}$ | PGOOD rising edge deglitch delay | | 80 | 140 | 200 | µs |
| $t_{PGOOD\_FALL}$ | PGOOD falling edge deglitch delay | | 80 | 140 | 200 | µs |

(1) Ensured by design.

## 6.7 Switching Characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PWM LIMITS (SW PINS)** | | | | | | |
| $t_{ON\text{-}MIN}$ | Minimum switch on-time | | | 60 | 82 | ns |
| $t_{OFF\text{-}MIN}$ | Minimum switch off-time | | | 70 | 120 | ns |
| $t_{ON\text{-}MAX}$ | Maximum switch on-time | HS timeout in dropout | 3 | 6 | 9 | µs |
| **OSCILLATOR (RT and SYNC PINS)** | | | | | | |
| $f_{OSC}$ | Internal oscillator frequency | RT = Open | 440 | 500 | 560 | kHz |
| $f_{ADJ}$ | Minimum adjustable frqeuency by RT or SYNC | RT = 115 kΩ, 0.1% | 315 | 350 | 385 | kHz |
| | Maximum adjustable frqeuency by RT or SYNC | RT = 17.4 kΩ, 0.1% | 1980 | 2200 | 2420 | |
| $V_{SYNC\_HIGH}$ | Sync input high-level threshold | | | | 2 | V |
| $V_{SYNC\_LOW}$ | Sync input low-level threshold | | 0.4 | | | V |
| $V_{MODE\_HIGH}$ | Mode input high-level threshold for FPWM | | | 0.42 | | V |
| $V_{MODE\_LOW}$ | Mode input low-level threshold for AUTO mode | | | 0.4 | | V |
| $t_{SYNC\_MIN}$ | Sync input minimum ON and OFF time | | | 80 | | ns |

## 6.8 Typical Characteristics

Unless otherwise specified, $V_{IN}$ = 12 V. Curves represent most likely parametric norm at specified condition.

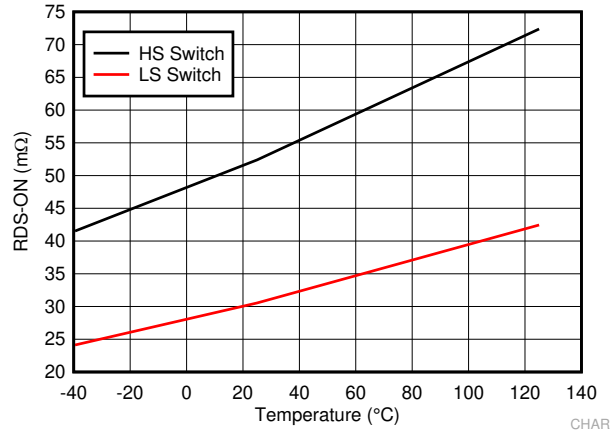



图 6-1. High-Side and Low-Side Switches $R_{DS-ON}$

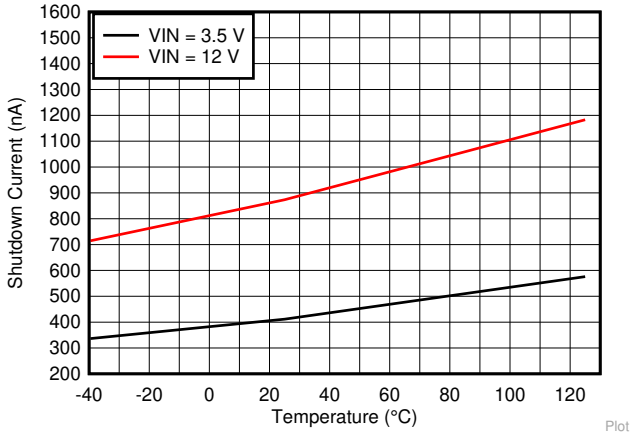



图 6-2. Shutdown Quiescent Current

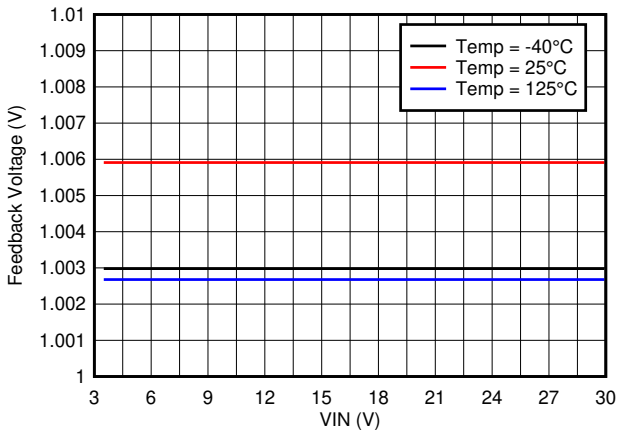



图 6-3. Feedback Voltage

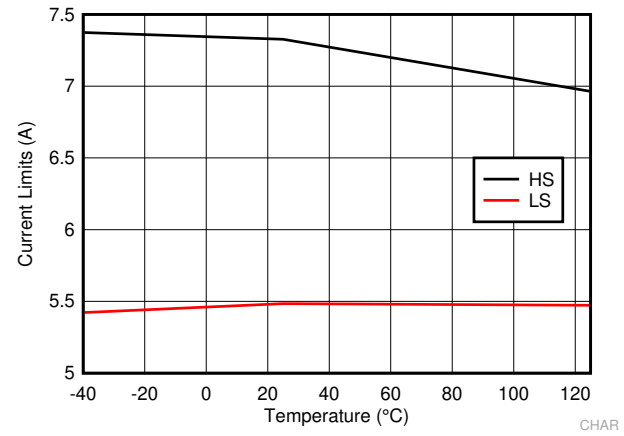



图 6-4. TPS7H4010-SEP High-Side and Low-Side Current Limits

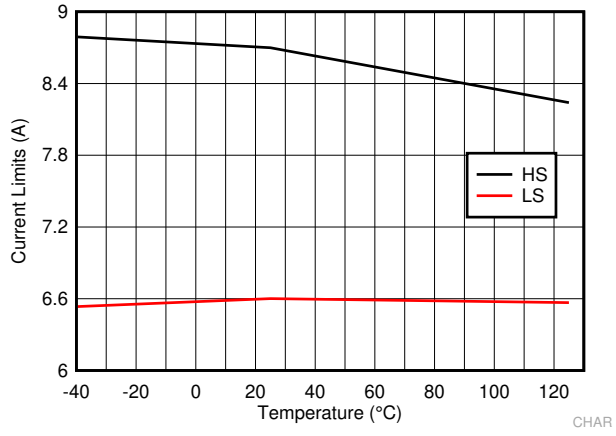



图 6-5. TPS7H4010-SEP High-Side and Low-Side Current Limit

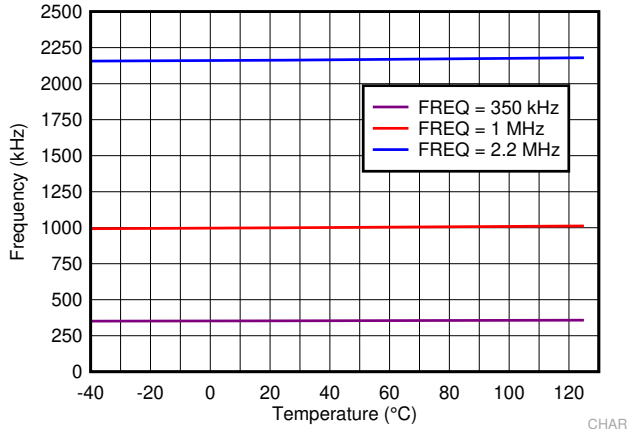



图 6-6. Switching Frequency Set by $R_T$ Resistor

## 6.8 Typical Characteristics (continued)

Unless otherwise specified, $V_{IN}$ = 12 V. Curves represent most likely parametric norm at specified condition.

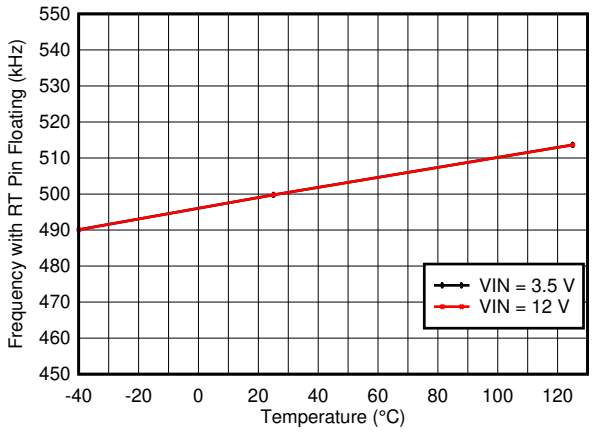



图 6-7. Switching Frequency With RT Pin Open Circuit

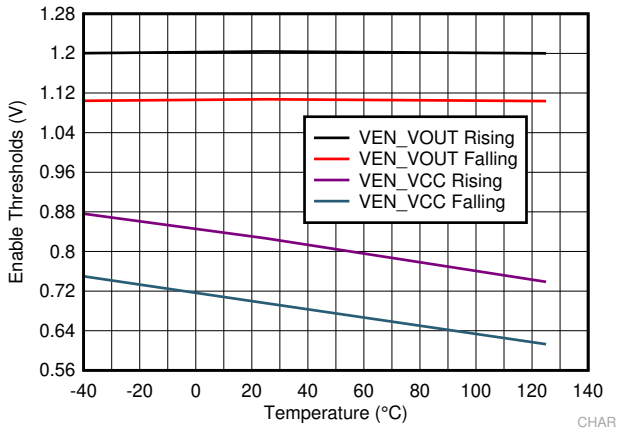



图 6-8. Enable Thresholds

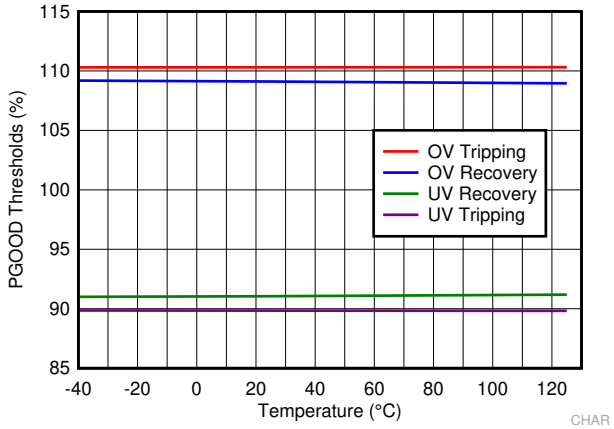



图 6-9. PGOOD Thresholds

# 7 Detailed Description

## 7.1 Overview

The TPS7H4010-SEP is an easy-to-use synchronous step-down DC/DC converter that operates from a 3.5-V to 32-V supply voltage. It is capable of delivering up to 6 A of DC load current with exceptional efficiency and thermal performance in a very small solution size.

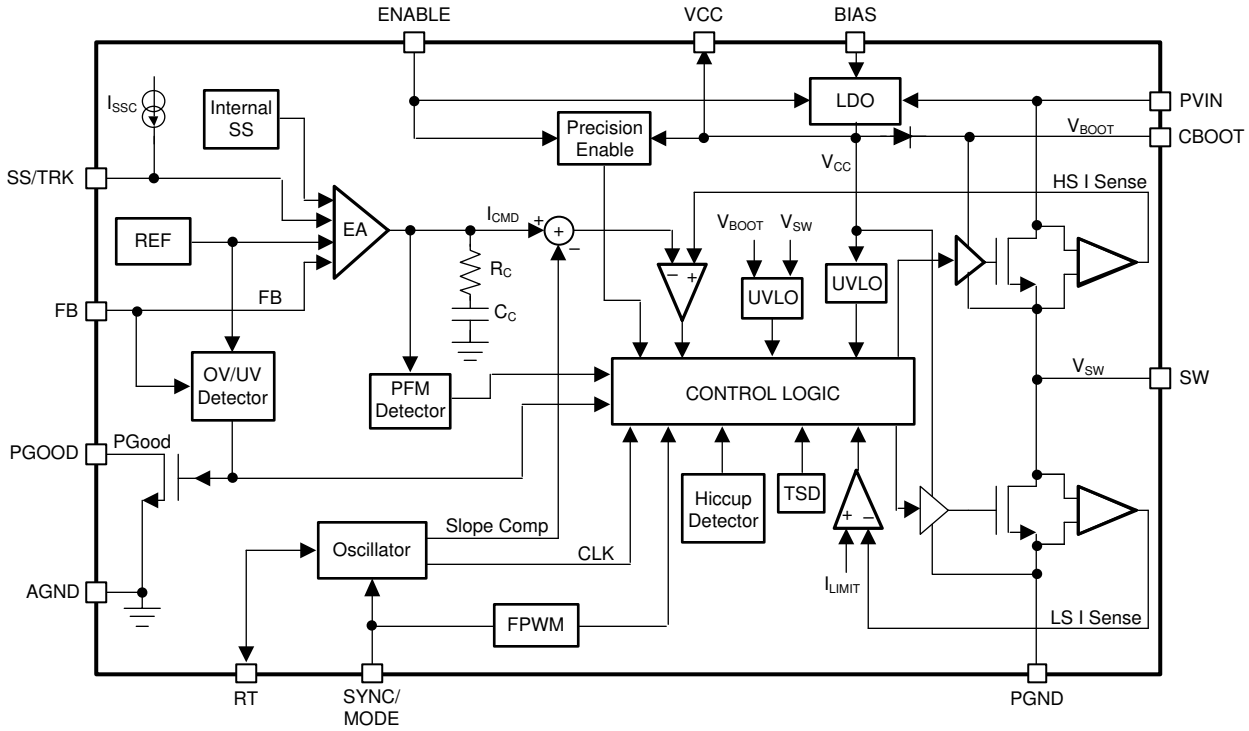
The TPS7H4010-SEP employs fixed-frequency peak current-mode control with configurable auto or FPWM operation mode. Auto mode provides very high efficiency at light loads, and FPWM mode maintains constant switching frequency over entire load range.

The device is internally compensated, which reduces design time and the number of external components. The switching frequency is programmable from 350 kHz to 2.2 MHz by an external resistor. The TPS7H4010-SEP can also synchronize to an external clock within the same frequency range. The wide switching frequency range allows the device to be optimized for a wide range of system requirements. It can be optimized for small solution size with higher frequency; or for high efficiency with lower switching frequency. The TPS7H4010-SEP has very low quiescent current, which is critical for battery operated systems. It allows for a wide range of voltage conversion ratios due to very small minimum on-time ($t_{ON-MIN}$) and minimum off-time ($t_{OFF-MIN}$). Automated frequency foldback is employed at very high or low duty cycles to further extend the operating range.

The TPS7H4010-SEP also features a power-good (PGOOD) flag, precision enable, internal or adjustable soft start, pre-biased start-up, and output voltage tracking. Protection features include thermal shutdown, undervoltage lockout (UVLO), cycle-by-cycle current limiting, and short-circuit hiccup protection. It provides flexible and easy-to-use solutions for a wide range of applications.

The device requires very few external components and has a pin out designed for simple, optimum PCB layout for enhanced EMI and thermal performance. The TPS7H4010-SEP device is available in a 30-pin WQFN leadless package.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Synchronous Step-Down Regulator

The TPS7H4010-SEP is a synchronous buck converter with both power MOSFETs integrated in the device. 图 7-1 shows a simplified schematic for synchronous and non-synchronous buck converters. The synchronous buck integrates both high-side (HS) and low-side (LS) power MOSFETs. The non-synchronous buck integrates HS MOSFET and works with a discrete power diode as LS rectifier.

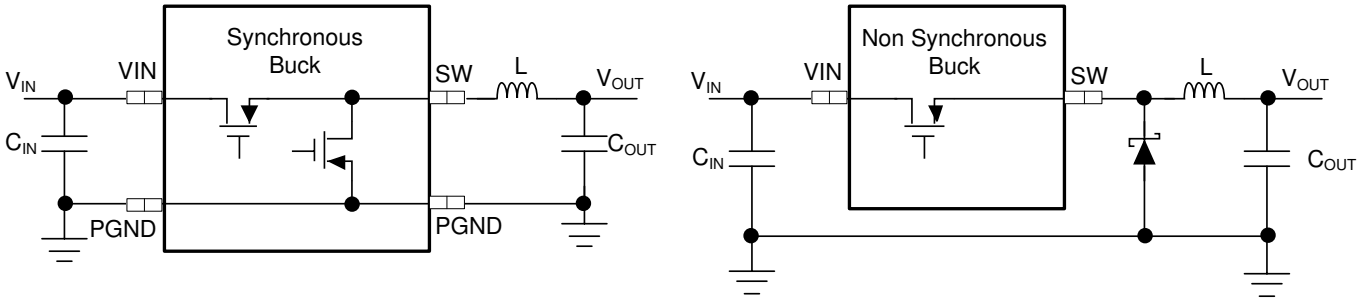



**图 7-1. Simplified Synchronous vs Non-synchronous Buck Converters**

A synchronous converter with integrated HS and LS MOSFETs offers benefits such as less design effort, lower external components count, reduced total solution size, higher efficiency at heavier load, easier PCB design, and more control flexibility.

The main advantage of a synchronous converter is that the voltage drop across the LS MOSFET is lower than the voltage drop across the power diode of a non-synchronous converter. Lower voltage drop translates into less power dissipation and higher efficiency. The TPS7H4010-SEP integrates HS and LS MOSFETs with very low on-time resistance to improve efficiency. It is especially beneficial when the output voltage is low. Because the LS MOSFET is integrated into the device, at light loads a synchronous converter has the flexibility to operate in either discontinuous or continuous conduction mode.

An integrated LS MOSFET also allows the controller to obtain inductor current information when the LS switch is on. It allows the control loop to make more complex decisions based on HS and LS currents. It allows the TPS7H4010-SEP to have peak and valley cycle-by-cycle current limiting for more robust protection.

### 7.3.2 Auto Mode and FPWM Mode

The TPS7H4010-SEP has pin configurable auto mode or FPWM options.

In auto mode, the device operates in diode emulation mode (DEM) at light loads. In DEM, inductor current stops flowing when it reaches 0 A. This is also referred to as discontinuous conduction mode (DCM). This is the same behavior as the non-synchronous regulator, with higher efficiency. At heavier load, when the inductor current valley is above 0 A, the device operates in continuous conduction mode (CCM), where the switching frequency is fixed and set by RT pin.

In auto mode, the peak inductor current has a minimum limit, $I_{PEAK\_MIN}$, in the TPS7H4010-SEP. When peak current reaches $I_{PEAK\_MIN}$, the switching frequency reduces to regulate the required load current. Switching frequency lowers when load reduces. This is when the device operates in pulse frequency modulation (PFM). PFM further improves efficiency by reducing switching losses. Light load efficiency is especially important for battery operated systems.

In forced PWM (FPWM) mode, the device operates in CCM regardless of load with the frequency set by RT pin or synchronization input. Inductor current can go negative at light loads. At light loads, the efficiency is lower than auto mode, due to higher conduction losses and switching losses. In FPWM, the device has fixed switching frequency over the entire load range, which is beneficial to noise sensitive applications.

图 7-2 shows the inductor current waveforms in each mode with heavy load, light load, and very light load. The difference between the two modes is at lighter loads where inductor current valley reaches zero.

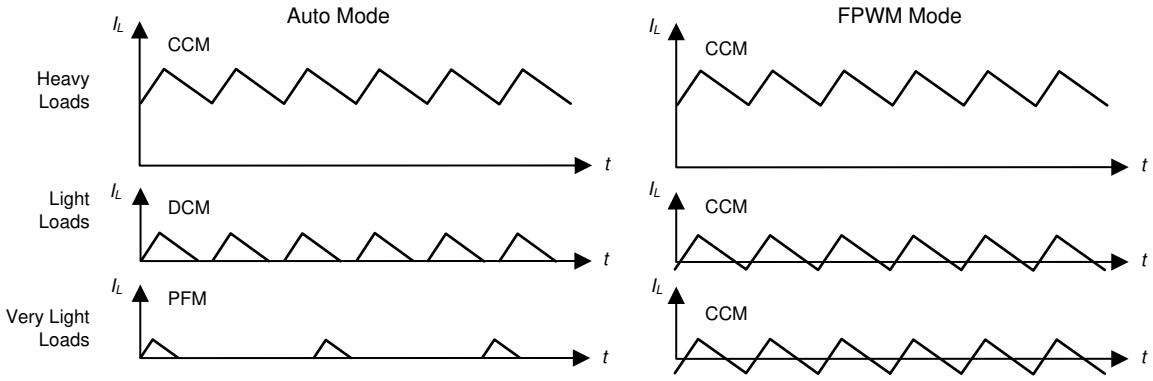



**图 7-2. Inductor Current Waveforms at Auto Mode and FPWM Mode With Different Loads**

In CCM, the inductor current peak-to-peak ripple can be estimated by 方程式 1:

$$I_{Lripple} = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

The average or DC value of the inductor current equals the load current, or output current $I_{OUT}$, in steady state. Peak inductor current can be calculated by 方程式 2:

$$I_{PEAK} = I_{OUT} + I_{Lripple} / 2 \quad (2)$$

Valley inductor current can be calculated by 方程式 3:

$$I_{VALLEY} = I_{OUT} - I_{Lripple} / 2 \quad (3)$$

In auto mode, the CCM to DCM boundary condition is when $I_{VALLEY}$ = 0 A. When $I_{Lripple} \geqslant I_{PEAK\_MIN}$, the load current at the DCM boundary condition can be found by 方程式 4. When the peak-to-peak ripple current is smaller than $I_{Lripple} \geqslant I_{PEAK\text{-}MIN}$, the PFM boundary will be reached first.

$$I_{OUT\_DCM} = I_{Lripple} / 2 \quad (4)$$

when

- $I_{Lripple} \geqslant I_{PEAK\_MIN}$

In auto mode, the PFM operation boundary condition is when $I_{PEAK} = I_{PEAK\_MIN}$. Frequency foldback occurs when peak current drops to $I_{PEAK\_MIN}$, no matter whether in CCM or DCM operation. When current ripple is small, $I_{Lripple} < I_{PEAK\_MIN}$, the peak current reaches $I_{PEAK\_MIN}$ when still in CCM. The output current at CCM PFM boundary can be found by 方程式 5:

$$I_{OUT\_CCM\_PFM} = I_{PEAK\_MIN} - I_{Lripple} / 2 \quad (5)$$

when

- $I_{Lripple} < I_{PEAK\_MIN}$

The current ripple increases with reduced frequency if load reduces. When valley current reaches zero, the frequency continues to fold back with constant peak current and discontinuous current.

In FPWM mode, there is no $I_{PEAK\text{-}MIN}$ limit. The peak current is defined by 方程式 2 at light loads and heavy loads.

Mode setting only affects operation at light loads. There is no difference if load current is above the DCM and PFM boundary conditions discussed above.

See *Frequency Synchronization and Mode Setting* section for mode setting options in TPS7H4010-SEP.

### 7.3.3 Fixed-Frequency Peak Current-Mode Control

The TPS7H4010-SEP synchronous switched mode voltage regulator employs fixed frequency peak current mode control with advanced features. The fixed switching frequency is controlled by an internal clock. To get accurate DC load regulation, a voltage feedback loop is implemented to generate peak current command. The HS switch is turned on at the rising edge of the clock. As shown in 图 7-3, during the HS switch on-time $t_{ON}$, the SW pin voltage $V_{SW}$ swings up to approximately $V_{IN}$, and the inductor current $I_L$ increases with a linear slope. The HS switch is turned off when the inductor current reaches the peak current command. During the HS switch off-time $t_{OFF}$, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the $V_{SW}$ to swing below ground by the voltage drop across the LS switch. The LS switch is turned off at the next clock cycle, before the HS switch is turned on. The regulation loop adjusts the peak current command to maintain a constant output voltage.

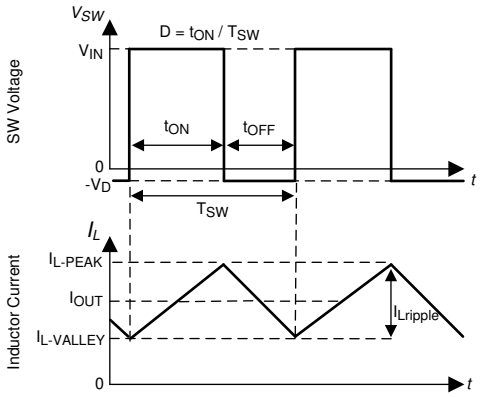



**图 7-3. SW Voltage and Inductor Current Waveforms in CCM**

Duty cycle D is defined by the on-time of the HS switch over the switching period:

$$D = t_{ON} / T_{SW} \quad (6)$$

where

- $T_{SW} = 1 / f_{SW}$ is the switching period

In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inverse proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

When the TPS7H4010-SEP is set to operate in auto mode, the LS switch is turned off when its current reaches zero ampere before the next clock cycle comes. Both HS switch and LS switch are off before the HS switch is turned on at the next clock cycle.

### 7.3.4 Adjustable Output Voltage

The voltage regulation loop in the TPS7H4010-SEP regulates the FB pin voltage to be the same as the internal reference voltage. The output voltage of the TPS7H4010-SEP is set by a resistor divider to program the ratio from $V_{OUT}$ to $V_{FB}$. The resistor divider is connected from the output to ground with the mid-point connecting to the FB pin.

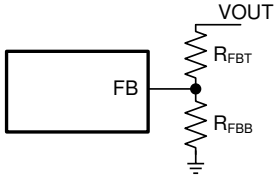



**图 7-4. Output Voltage Setting by Resistor Divider**

The internal voltage reference and feedback loop produce precise voltage regulation over temperature. TI recommends using divider resistors with 1% tolerance or better, and with temperature coefficient of 100 ppm or lower. Typically, $R_{FBT}$ = 10 kΩ to 100 kΩ is recommended. Larger $R_{FBT}$ and $R_{FBB}$ values reduce the quiescent current going through the divider, which help maintain high efficiency at very light load. But larger divider values also make the feedback path more susceptible to noise. If efficiency at very light load is critical in a certain application, $R_{FBT}$ up to 1 MΩ can be used.

$R_{FBB}$ can be calculated by 方程式 7:

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} R_{FBT} \tag{7}$$

The minimum programmable $V_{OUT}$ equals $V_{FB}$, with $R_{FBB}$ open. The maximum $V_{OUT}$ is limited by the maximum duty cycle at a given frequency:

$$D_{MAX} = 1 - (t_{OFF\text{-}MIN} / T_{SW}) \tag{8}$$

where

- $t_{OFF\text{-}MIN}$ is the minimum off time of the HS switch
- $T_{SW} = 1 / f_{SW}$ is the switching period

Ideally, without frequency foldback, $V_{OUT\_MAX} = V_{IN\_MIN} \times D_{MAX}$.

Power losses in the circuit reduces the maximum output voltage. The TPS7H4010-SEP folds back switching frequency under $t_{OFF\_MIN}$ condition to further extend $V_{OUT\_MAX}$. The device maintains output regulation with lower input voltage. The minimum fold-back frequency is limited by the maximum HS on-time, $t_{ON\_MAX}$. Maximum output voltage with frequency foldback can be estimated by:

$$V_{OUT\_MAX} = V_{IN\_MIN} \times \frac{t_{ON\text{–}MAX}}{t_{ON\text{–}MAX} + t_{OFF\text{-}MIN}} - I_{OUT} \times (R_{DS\_ON\_HS} + DCR) \tag{9}$$

The voltage drops on the HS MOSFET and inductor DCR have been taken into account in 方程式 9. The switching losses were not included.

If the resistor divider is not connected properly, the output voltage cannot be regulated because the feedback loop cannot obtain correct output voltage information. If the FB pin is shorted to ground or disconnected, the output voltage is driven close to $V_{IN}$. The load connected to the output could be damaged under this condition. Do not short FB to ground or leave it open circuit during operation.

The FB pin is a noise sensitive node. It is important to place the resistor divider as close as possible to the FB pin, and route the feedback node with a short and thin trace. The trace connecting $V_{OUT}$ to $R_{FBT}$ can be long, but it must be routed away from the noisy area of the PCB. For more layout recommendations, see *Layout* section.

### 7.3.5 Enable and UVLO

The TPS7H4010-SEP regulates output voltage when the VCC voltage is higher than the undervoltage lock out (UVLO) level, $V_{CC\_UVLO}$, and the EN voltage is higher than $V_{EN\_VOUT\_H}$.

The internal LDO output voltage VCC is turned on when the EN voltage is higher than $V_{EN\_VCC\_H}$. The precision enable circuitry is also turned on when VCC is above UVLO. Normal operation of the TPS7H4010-SEP with regulated output voltage is enabled when the EN voltage is greater than $V_{EN\_VOUT\_H}$. When the EN voltage is less than $V_{EN\_VCC\_L}$, the device is in shutdown mode. The internal dividers make sure $V_{EN\_VOUT\_H}$ is always higher than $V_{EN\_VCC\_H}$.

The EN pin cannot be left floating. The simplest way to enable the operation of the TPS7H4010-SEP is to connect the EN pin to PVIN, which allows self-start-up of the TPS7H4010-SEP when $V_{IN}$ rises. Use of a pullup resistor between PVIN and EN pins helps reduce noise coupling from PVIN pin to the EN pin.

Many applications benefit from employing an enable divider to establish a customized system UVLO. This can be used either for sequencing, system timing requirement, or to reduce the occurrence of deep discharge of a battery power source. 图 7-5 shows how to use a resistor divider to set a system UVLO level. An external logic output can also be used to drive the EN pin for system sequencing.

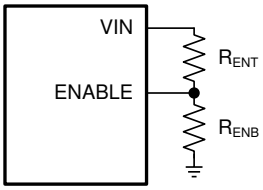



**图 7-5. System UVLO**

With a selected $R_{ENT}$, the $R_{ENB}$ can be calculated by 方程式 10:

$$R_{ENB} = \frac{V_{EN\_VOUT\_H}}{V_{IN\_ON\_H} - V_{EN\_VOUT\_H}} R_{ENT} \quad (10)$$

where

- $V_{IN\_ON\_H}$ is the desired supply voltage threshold to turn on this device

Note that the divider adds to supply quiescent current by $V_{IN}$ / ($R_{ENT}$ + $R_{ENB}$). Small $R_{ENT}$ and $R_{ENB}$ values add more quiescent current loss. However, large divider values make the node more sensitive to noise. $R_{ENT}$ in the hundreds of kΩ range is a good starting point.

### 7.3.6 Internal LDO, $V_{CC\_UVLO}$, and BIAS Input

The TPS7H4010-SEP integrates an internal LDO, generating VCC voltage for control circuitry and MOSFET drivers. The VCC pin must have a 1-µF to 4.7-µF bypass capacitor placed as close as possible to the pin and properly grounded. Do not load the VCC pin or short it to ground during operation. Shorting VCC pin to ground during operation may damage the device.

The UVLO on VCC voltage, $V_{CC\_UVLO}$, turns off the regulation when VCC voltage is too low. It prevents the TPS7H4010-SEP from operating until the VCC voltage is enough for the internal circuitry. Hysteresis on $V_{CC\_UVLO}$ prevents the part from turning off during power up if $V_{IN}$ droops due to input current demands. The LDO generates VCC voltage from one of the two inputs: the supply voltage $V_{IN}$, or the BIAS input. When BIAS is tied to ground, the LDO input is $V_{IN}$. When BIAS is tied to a voltage higher than 3.3 V, the LDO input is $V_{BIAS}$. BIAS voltage must be lower than both $V_{IN}$ and 18 V.

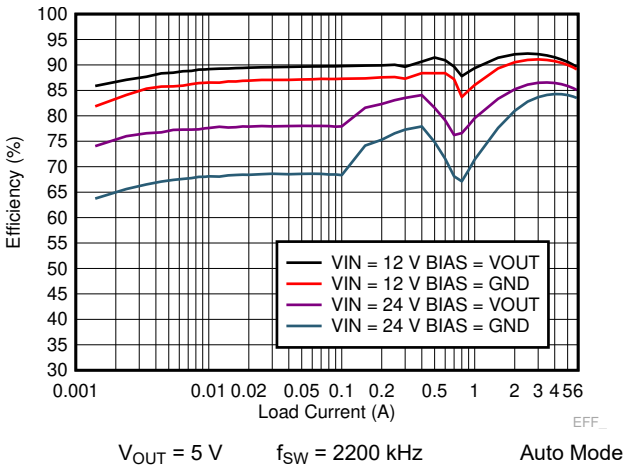
The BIAS input is designed to reduce the LDO power loss. The LDO power loss is:

$$P_{LOSS\_LDO} = I_{LDO} \times (V_{IN\_LDO} - V_{OUT\_LDO}) \quad (11)$$

The higher the difference between the input and output voltages of the LDO, the more loss occurs to supply the same LDO output current. The BIAS input provides an option to supply the LDO with a lower voltage than $V_{IN}$, to reduce the difference of the input and output voltages of the LDO and reduce power loss. For example, if the LDO current is 10 mA at a certain frequency with $V_{IN}$ = 24 V and $V_{OUT}$ = 5 V. The LDO loss with BIAS tied to ground is equal to 10 mA × (24 V – 3.27 V) = 207.3 mW, while the loss with BIAS tied to $V_{OUT}$ is equal to 10 mA × (5 – 3.27) = 17.3 mW.

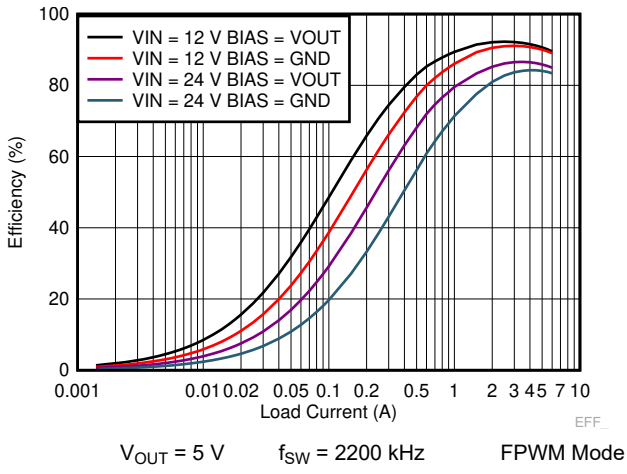
The efficiency improvement is more significant at light and mid loads because the LDO loss is a higher percentage in the total loss. The improvements is more significant with higher switching frequency because the LDO current is higher at higher switching frequency. The improvement is more significant when $V_{IN}$ » $V_{OUT}$ because the voltage difference is higher.

图 7-6 and 图 7-7 show efficiency improvement with bias tied to $V_{OUT}$ in a $V_{OUT}$ = 5 V and $f_{SW}$ = 2200 kHz application, in auto mode and FPWM mode, respectively.




$V_{OUT}$ = 5 V $f_{SW}$ = 2200 kHz Auto Mode

**图 7-6. TPS7H4010 Efficiency Comparison With Bias = $V_{OUT}$ to Bias = GND in Auto Mode**

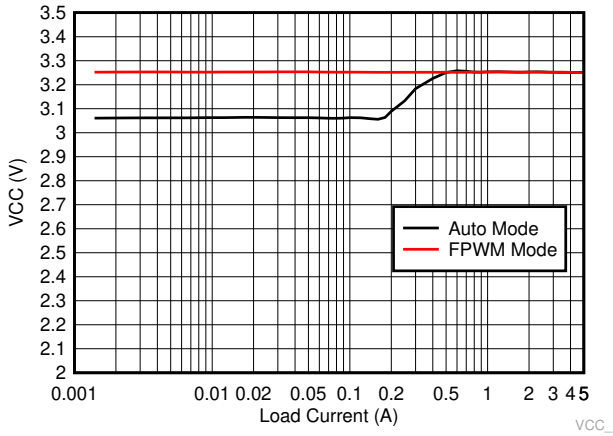



$V_{OUT}$ = 5 V $f_{SW}$ = 2200 kHz FPWM Mode

**图 7-7. TPS7H4010 Efficiency Comparison With Bias = $V_{OUT}$ to Bias = GND in FPWM Mode**

TI recommends tying the BIAS pin to $V_{OUT}$ when $V_{OUT}$ is equal to or greater than 3.3 V and no greater than 18 V. Tie the BIAS pin to ground when not in use. A ceramic capacitor, $C_{BIAS}$, can be used from the BIAS pin to ground for bypassing. If $V_{OUT}$ has high frequency noise or spikes during transients or fault conditions, a resistor (1 to 10 Ω) connected between $V_{OUT}$ to BIAS can be used together with $C_{BIAS}$ for filtering.

The VCC voltage is typically 3.27 V. When the TPS7H4010-SEP is operating in PFM mode with frequency foldback, VCC voltage is reduced to 3.1 V (typical) to further decrease the quiescent current and improve efficiency at very light loads. 图 7-8 shows an example of VCC voltage change with mode change.




$V_{OUT}$ = 5 V $f_{SW}$ = 500 kHz $V_{IN}$ = 12 V

**图 7-8. VCC Voltage vs Load Current**

VCC voltage has an internal UVLO threshold, $V_{CC\_UVLO}$. When VCC voltage is higher than $V_{CC\_UVLO}$ rising threshold, the device is active and in normal operation if $V_{EN}$ > $V_{EN\_VOUT\_H}$. If VCC voltage droops below $V_{CC\_UVLO}$ falling threshold, the $V_{OUT}$ is shut down.

### 7.3.7 Soft Start and Voltage Tracking

The TPS7H4010-SEP features controlled output voltage ramp during start-up. The soft-start feature reduces inrush current during start-up and improves system performance and reliability.

If the SS/TRK pin is floating, the TPS7H4010-SEP starts up following the fixed internal soft-start ramp.

If longer soft-start time is desired, an external capacitor can be added from SS/TRK pin to ground. There is a 2-µA (typical) internal current source, $I_{SSC}$, to charge the external capacitor. For a desired soft-start time $t_{SS}$, capacitance of $C_{SS}$ can be found by 方程式 12.

$$C_{SS} = I_{SSC} \times t_{SS} \quad (12)$$

where

- $C_{SS}$ = soft-start capacitor value (F)
- $I_{SSC}$ = soft-start charging current (A)
- $t_{SS}$ = desired soft-start time (s)

The FB voltage always follows the lower potential of the internal voltage ramp or the voltage on the SS/TRK pin. Thus, the soft-start time can only be extended longer than the internal soft-start time by connecting $C_{SS}$. Use $C_{SS}$ to extend soft-start time when there are a large amount of output capacitors, or the output voltage is high, or the output is heavily loaded during start-up.

TPS7H4010-SEP is operating in diode emulation mode during start-up regardless of mode setting. The device is capable of starting up into pre-biased output conditions. During start-up, the device sets the minimum inductor current to zero to avoid back charging the input capacitors.

TPS7H4010-SEP can track an external voltage ramp applied to the SS/TRK pin, if the ramp is slower than the internal soft-start ramp. The external ramp final voltage after start-up must be greater than 1.5 V to avoid noise interfering with the reference voltage. 图 7-9 shows how to use resistor divider to set $V_{OUT}$ to follow an external ramp.

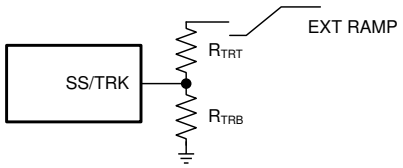



**图 7-9. Soft Start Tracking External Ramp**

$V_{OUT}$ tracking also provides the option of ramping up faster than the internal start-up ramp. The FB voltage always follows the lower potential of the internal voltage ramp and the voltage on the SS/TRK pin. 图 7-10 shows the case when $V_{OUT}$ ramps slower than the internal ramp, while 图 7-11 shows when $V_{OUT}$ ramps faster than the internal ramp. If the tracking ramp is delayed after the internal ramp is completed, $V_{FB}$ follows the tracking ramp even if it is faster than the internal ramp. Faster start-up time may result in large inductor current during start-up. Use with special care.

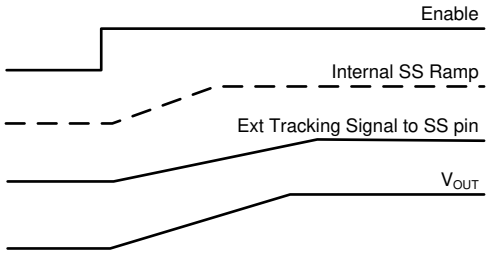



**图 7-10. Tracking With Longer Start-up Time Than the Internal Ramp**

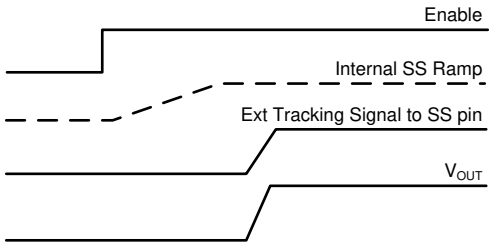



**图 7-11. Tracking With Shorter Start-up Time Than the Internal Ramp**

The SS/TRK pin is discharged to ground by an internal pulldown resistor $R_{SSD}$ when the output voltage is shutting down, such as in the event of UVLO, thermal shutdown, hiccup, or $V_{EN}$ = 0. If a large $C_{SS}$ is used, and the time when $V_{EN}$ = 0 V is very short, the $C_{SS}$ may not be fully discharged before the next soft start. Under this condition, the FB voltage follows the internal ramp slew rate until the voltage on $C_{SS}$ is reached, then follow the slew rate defined by $C_{SS}$.

### 7.3.8 Adjustable Switching Frequency

The internal oscillator frequency is controlled by the impedance on the RT pin. If the RT pin is open circuit, the TPS7H4010-SEP operates at its default switching frequency, 500 kHz. The RT pin is not designed to be connected directly to ground. To program the switching frequency by $R_T$ resistor, either 方程式 13, 图 7-12, or 表 7-1 can be used to find the resistance value.

$$R_T(k\Omega) = \frac{1}{f_{SW}(kHz) \times 2.675 \times 10^{-5} - 0.0007} \quad (13)$$

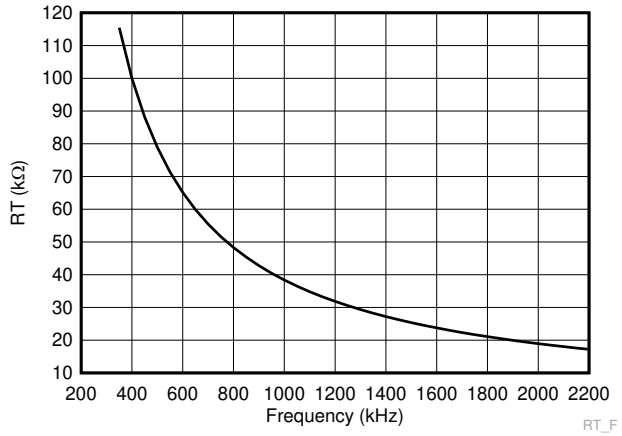



**图 7-12. $R_T$ Resistance vs Switching Frequency**

**表 7-1. Typical Frequency Setting Resistance**

| SWITCHING FREQUENCY $f_{SW}$ (kHz) | $R_T$ RESISTANCE (kΩ) |
|---|---|
| 350 | 115 |
| 400 | 100 |
| 500 | 78.7 (or open) |
| 750 | 52.3 |
| 1000 | 39.2 |
| 1500 | 26.1 |
| 2000 | 19.1 |
| 2200 | 17.4 |

The choice of switching frequency is usually a compromise between conversion efficiency and the size of the solution. Lower switching frequency has lower switching losses (including gate charge losses, switch transition losses, etc.) and usually results in higher overall efficiency. However, higher switching frequency allows the use of smaller power inductor and output capacitors, hence a more compact design. Lower inductance also helps transient response (higher large signal slew rate of inductor current), and has lower DCR. The optimal switching frequency is usually a trade-off in a given application and thus needs to be determined on a case-by-case basis. Factors that need to be taken into account include input voltage range, output voltage, most frequent load current level or levels, external component choices, solution size/cost requirements, efficiency, and thermal management requirements.

The choice of switching frequency may also be limited whether an operating condition triggers $t_{ON-MIN}$ or $t_{OFF-MIN}$. Minimum on-time, $t_{ON-MIN}$, is the smallest time that the HS switch can be on. Minimum off-time, $t_{OFF-MIN}$, is the smallest duration that the HS switch can be off.

In CCM operation, $t_{ON-MIN}$ and $t_{OFF\_MIN}$ limits the voltage conversion range given a selected switching frequency, $f_{SW}$. The minimum duty cycle allowed is:

$$D_{MIN} = t_{ON-MIN} \times f_{SW} \quad (14)$$

The maximum duty cycle allowed is:

$$D_{MAX} = 1 - t_{OFF-MIN} \times f_{SW} \quad (15)$$

Given an output voltage, the choice of the switching frequency affects the allowed input voltage range, solution size and efficiency. The maximum operational supply voltage can be found by:

$$V_{IN\_MAX} = V_{OUT} / (f_{SW} \times t_{ON-MIN}) \quad (16)$$

At lower supply voltage, the switching frequency decreases once $t_{OFF-MIN}$ is tripped. The minimum $V_{IN}$ without frequency foldback can be approximated by:

$$V_{IN\_MIN} = V_{OUT} / (1 - f_{SW} \times t_{OFF-MIN}) \quad (17)$$

With a desired $V_{OUT}$, the range of allowed $V_{IN}$ is narrower with higher switching frequency.

TPS7H4010-SEP has an advanced frequency fold-back algorithm under both $t_{ON\_MIN}$ and $t_{OFF\_MIN}$ conditions. With frequency foldback, stable output voltage regulation is extended to wider range of supply voltages.

At very high $V_{IN}$ conditions, where $t_{ON-MIN}$ limitation is met, the switching frequency reduces to allow higher $V_{IN}$ while maintaining $V_{OUT}$ regulation. Note that the peak to peak inductor current ripple will increase with higher $V_{IN}$ and lower frequency. TI does not recommend designing the circuit to operate with $t_{ON\_MIN}$ under typical conditions.

At very low $V_{IN}$ conditions, where $t_{OFF-MIN}$ limitation is met, the switching frequency decreases until $t_{ON-MAX}$ condition is met. Such frequency foldback mechanism allows the TPS7H4010-SEP to have very low dropout voltage regardless of frequency setting.

### 7.3.9 Frequency Synchronization and Mode Setting

The TPS7H4010-SEP switching action can synchronize to an external clock from 350 kHz to 2.2 MHz. TI recommends connecting the external clock to the SYNC/MODE pin with an appropriate termination resistor. Ground the SYNC/MODE pin if not used.

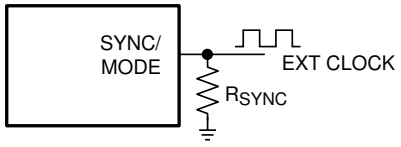



**图 7-13. Frequency Synchronization**

Recommendations for the external clock include a high level no lower than 2 V, low level no higher than 0.4 V, duty cycle between 10% and 90%, and both positive and negative pulse width no shorter than 80 ns. When the external clock fails at logic high or low, the TPS7H4010-SEP switches at the frequency programmed by the $R_T$ resistor after a time-out period. TI recommends connecting a resistor to the RT pin such that the internal oscillator frequency is the same as the external clock frequency. This allows the regulator to continue operating at approximately the same switching frequency if the external clock fails with the same control loop behavior.

The SYNC/MODE pin is also used as an operation mode control input.

- To set the operation in auto mode, connect SYNC/MODE pin to ground, or a logic signal lower than 0.3 V.
- To set the operation in FPWM mode, connect SYNC/MODE pin to a bias voltage or logic signal greater than 0.6 V.
- When the TPS7H4010-SEP is synchronized to an external clock, the operation mode is FPWM.

表 7-2 summarizes the operation mode and features according to the SYNC/MODE input signal. For more details, see *Active Mode* and *Auto Mode and FPWM Mode* sections.

**表 7-2. SYNC/MODE Pin Settings and Operation Modes**

| SYNC/MODE INPUT | SWITCHING FREQUENCY | OPERATING MODE | LIGHT LOAD BEHAVIOR |
|---|---|---|---|
| Logic low | Set by $R_T$ resistor | Auto mode | • No negative inductor current, device operates in discontinuous conduction mode (DCM) when current valley reaches 0 A<br>• Minimum peak inductor current is limited at $I_{PEAK\_MIN}$; device operates in pulse frequency modulation (PFM) mode when peak current reaches $I_{PEAK\_MIN}$<br>• Switching frequency reduces in PFM mode |
| Logic high | Set by $R_T$ resistor | FPWM mode | • Fixed frequency continuous conduction mode (CCM) regardless of load<br>• Inductor current have negative portion at light loads<br>• No $I_{PEAK\_MIN}$ |
| External clock | Set by external clock | | |

### 7.3.10 Internal Compensation and $C_{FF}$

The TPS7H4010-SEP is internally compensated. The internal compensation is designed such that the loop response is stable over a wide operating frequency and output voltage range. The internal R-C values are 500 kΩ and 30 pF, respectively.

When large resistance value (MΩ) is used for $R_{FBT}$, the pole formed by an internal parasitic capacitor and $R_{FBT}$ can be low enough to reduce the phase margin. If only low ESR output capacitors (ceramic types) are used for $C_{OUT}$, the control loop could have low phase margin. To provide a phase boost an external feed-forward capacitor ($C_{FF}$) can be added in parallel with $R_{FBT}$. Choose the $C_{FF}$ capacitor to provide most phase boost at the estimated crossover frequency $f_X$:

$$f_X = \frac{K}{V_{OUT} \times C_{OUT}} \tag{18}$$

where

- K = 24.16 with TPS7H4010-SEP

Select $C_{OUT}$ so that the $f_X$ is no higher than 1/6 of the switching frequency. Typically, $f_X$ / $f_{SW}$ = 1/10 to 1/8 provides a good combination of stability and performance.

Place the external feed-forward capacitor in parallel with the top resistor divider $R_{FBT}$ when additional phase boost is needed.

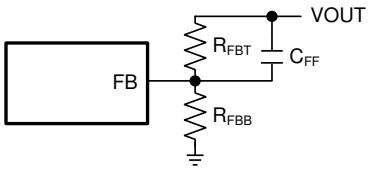



**图 7-14. Feed-Forward Capacitor for Loop Compensation**

The feed-forward capacitor $C_{FF}$ in parallel with $R_{FBT}$ places an additional zero before the crossover frequency of the control loop to boost phase margin. The zero frequency can be found by 方程式 19:

$$f_{Z\text{-}CFF} = 1 / (2 \pi \times R_{FBT} \times C_{FF}) \quad (19)$$

An additional pole is also introduced with $C_{FF}$ at the frequency of:

$$f_{P\text{-}CFF} = 1 / (2 \pi \times C_{FF} \times (R_{FBT} / R_{FBB})) \quad (20)$$

Select the $C_{FF}$ so that the bandwidth of the control loop without the $C_{FF}$ is centered between $f_{Z\text{-}CFF}$ and $f_{P\text{-}CFF}$. The zero at $f_{Z\text{-}CFF}$ adds phase boost at the crossover frequency and improves transient response. The pole at $f_{P\text{-}CFF}$ helps maintaining proper gain margin at frequency beyond the crossover.

The need of $C_{FF}$ depends on $R_{FBT}$ and $C_{OUT}$. Typically, choose $R_{FBT} \leqslant 100\ k\Omega$. $C_{FF}$ may not be required, because the internal parasitic pole is at higher frequency. If $C_{OUT}$ has larger ESR, and ESR zero $f_{Z\text{-}ESR} = 1 / (2 \pi \times ESR \times C_{OUT})$ is low enough to provide phase boost around the crossover frequency, do not use $C_{FF}$. 方程式 21 was tested for ceramic output capacitors:

$$C_{FF} = \frac{1}{2 \times \pi \times f_x} \times \frac{1}{\sqrt{R_{FBT} \times (R_{FBT} // R_{FBB})}} \quad (21)$$

The $C_{FF}$ creates a time constant with $R_{FBT}$ that couples in the attenuated output voltage ripple to the FB node. If the $C_{FF}$ value is too large, it can couple too much ripple to the FB and affect $V_{OUT}$ regulation. It could also couple too much transient voltage deviation and falsely trigger PGOOD flag.

### 7.3.11 Bootstrap Capacitor and $V_{BOOT\text{-}UVLO}$

The driver of the HS switch requires a bias voltage higher than the $V_{IN}$ voltage. The capacitor, $C_{BOOT}$ in 图 8-1, connected between CBOOT and SW pins works as a charge pump to boost voltage on the CBOOT pin to ($V_{SW}$ + $V_{CC}$). A boot diode is integrated on the die to minimize external component count. TI recommends a high-quality 0.47-µF, 6.3-V or higher voltage ceramic capacitor for $C_{BOOT}$. The $V_{BOOT\_UVLO}$ threshold is designed to maintain proper HS switch operation. If the $C_{BOOT}$ is not charged above this voltage with respect to SW, the device initiates a charging sequence using the LS switch before turning on the HS switch.

### 7.3.12 Power-Good and Overvoltage Protection

The TPS7H4010-SEP has a built-in power-good (PGOOD) flag to indicate whether the output voltage is at an appropriate level or not. The PGOOD flag can be used for start-up sequencing of multiple rails. The PGOOD pin is an open-drain output that requires a pullup resistor to an appropriate logic voltage (any voltage below 15 V). The pin can sink 5 mA of current and maintain its specified logic low level. A typical pullup resistor value is 10 kΩ to 100 kΩ. When the FB voltage is higher than $V_{PGOOD\text{-}OV}$ or lower than $V_{PGOOD\text{-}UV}$ threshold, the PGOOD internal switch is turned on, and the PGOOD pin voltage is pulled low. When the FB is within the range, the PGOOD switch is turned off, and the pin is pulled up to the voltage connected to the pullup resistor. The PGOOD function also have a deglitch timer for about 140 µs for each transition. If it is desired to pull up PGOOD pin to a voltage higher than 15 V, a resistor divider can be used to divide the voltage down.

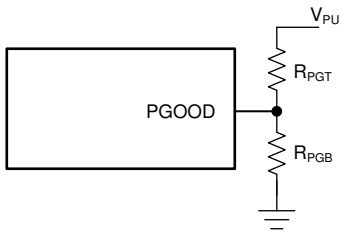



**图 7-15. Divider for PGOOD Pullup Voltage**

With a given pullup voltage $V_{PU}$, select a desired voltage on the PGOOD pin, $V_{PG}$. With a selected $R_{PGT}$, the $R_{PGB}$ can be found by:

$$R_{PGB} = \frac{V_{PG}}{V_{PU} - V_{PG}} R_{PGT} \quad (22)$$

When the device is disabled, the output voltage is low, and the PGOOD flag indicates logic low as long as $V_{IN}$ > 2 V.

### 7.3.13 Overcurrent and Short-Circuit Protection

The TPS7H4010-SEP is protected from overcurrent conditions with cycle-by-cycle current limiting on both HS and LS MOSFETs.

The HS switch is turned off when HS current goes beyond the peak current limit, $I_{HS\text{-}LIMIT}$. The LS switch can only be turned off when LS current is below LS current limit, $I_{LS\text{-}LIMIT}$. If the LS switch current is higher than $I_{LS\text{-}LIMIT}$ at the end of a switching cycle, the switching cycle is extended until the LS current reduces below the limit.

Current limiting on both HS and LS switches provides tighter control of the maximum DC inductor current, or output current. They also help prevent runaway current at extreme conditions. With TPS7H4010-SEP, the maximum output current is always limited at:

$$I_{DC\_LIMIT} = (I_{HS\_LIMIT} + I_{LS\_LIMIT}) / 2 \quad (23)$$

The TPS7H4010-SEP employs hiccup current protection at extreme overload conditions, including short-circuit condition. Hiccup is only activated when $V_{OUT}$ droops below 40% (typical) of the regulation voltage and stays below for 128 consecutive switching cycles. Under overcurrent conditions when $V_{OUT}$ has not fallen below 40% of regulation, the TPS7H4010-SEP continues operation with cycle-by-cycle HS and LS current limiting.

Hiccup is disabled during soft-start. When hiccup is triggered, the device turns off $V_{OUT}$ regulation and re-tries soft start after a retry delay time, $T_{OC}$ = 46 ms (typical). The long wait time allows the device, and the load, to cool down under such fault conditions. If the fault condition still exists when retry, hiccup shuts down the device and repeats the wait and retry cycle. If the fault condition has been removed, the device starts up normally.

If tracking was used for initial sequencing, the device restarts using the internal soft-start ramp. Hiccup mode helps to reduce the device power dissipation and die temperature under severe overcurrent conditions and short circuits. It improves system reliability and prolongs the life span of the device.

In FPWM mode, negative current protection is implemented to protect the switches from extreme negative currents. When LS switch current reaches $I_{NEG\text{-}LIMIT}$, LS switch turns off, and HS switch turns on to conduct the negative current. HS switch is turned off once its current reaches 0 A.

### 7.3.14 Thermal Shutdown

Thermal shutdown protection prevents the device from extreme junction temperature. The device is turned off when the junction temperature exceeds 160°C (typical). After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 135°C. When the junction temperature falls below 135°C, the TPS7H4010-SEP restarts.

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Mode

The EN pin provides electrical on/off control of the device. When the EN pin voltage is below $V_{EN\_VCC\_L}$, the device is in shutdown mode. The LDO output voltage $V_{CC}$ = 0 V and the output voltage $V_{OUT}$ = 0 V. In shutdown mode the quiescent current drops to a very low value.

### 7.4.2 Standby Mode

The internal LDO has a lower EN threshold than that required to start the regulator. When the EN pin voltage is above $V_{EN\_VCC\_H}$, the internal LDO regulates the VCC voltage. The precision enable circuitry is turned on once $V_{CC}$ is above $V_{CC\_UVLO}$. The device is in standby mode if EN voltage is below $V_{EN\_VOUT\_H}$. The internal MOSFETs remains in tri-state unless the voltage on EN pin goes beyond $V_{EN\_VOUT\_H}$ threshold. The TPS7H4010-SEP also employs UVLO protection. If the VCC voltage is below the $V_{CC\_UVLO}$ level, the output of the regulator is turned off.

### 7.4.3 Active Mode

The TPS7H4010-SEP is in active mode when the EN voltage is above $V_{EN\_VOUT\_H}$, and $V_{CC}$ is above $V_{CC\_UVLO}$. The simplest way to enable the operation of the TPS7H4010-SEP is to pull up the EN pin to PVIN, which allows self-start-up when the input voltage ramps up.

In active mode, depending on the load current and mode setting, the TPS7H4010-SEP is in one of four modes:

- CCM with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple;
- DCM with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation;
- PFM when switching frequency is decreased at very light load;
- Under overcurrent or overtemperature conditions, the device operates in one of the fault protection modes.

See 表 7-2 for mode-setting details.

#### *7.4.3.1 CCM Mode*

In CCM operation, inductor current has a continuous triangular waveform. The HS switch is on at the beginning of a switching cycle and the LS switch is turned off the end of each switching cycle. In auto mode, the TPS7H4010-SEP operates in CCM when the load current is higher than ½ of the peak-to-peak inductor current ($I_{Lripple}$). In FPWM mode, the TPS7H4010-SEP operates in CCM regardless of load.

In CCM operation, the switching frequency is typically constant, unless $t_{ON\text{-}MIN}$, $t_{OFF\text{-}MIN}$, or $I_{PEAK\text{-}MIN}$ conditions are met. The constant switching frequency is determined by RT pin setting, or the external synchronization clock frequency. The duty cycle is also constant in CCM: D = $V_{OUT}$ / $V_{IN}$ if loss is ignored, regardless of load. The peak-to-peak inductor ripple is constant with the same $V_{IN}$ and $V_{OUT}$, regardless of load.

With very high or very low supply voltages, when the $t_{ON\text{-}MIN}$ or $t_{OFF\text{-}MIN}$ condition is met, the frequency reduces to maintain $V_{OUT}$ regulation with even higher or lower $V_{IN}$, respectively. When the $I_{PEAK\_MIN}$ condition is met in auto mode, switching frequency will fold back to provide higher efficiency. $I_{PEAK\_MIN}$ is disabled in FPWM mode.

#### *7.4.3.2 DCM Mode*

DCM operation only happens in auto mode, when the load current is lower than half of the CCM inductor current ripple, and peak current is higher than $I_{PEAK\text{-}MIN}$. There is no DCM in FPWM mode. DCM is also known as diode emulation mode. The LS FET is turned off when the inductor current ramps to 0 A. DCM has the same switching frequency as CCM, which is set by the RT pin. Duty cycle and peak current reduces with lighter load in DCM. DCM is more efficient than FPWM under the same condition, because of lower switching losses and lower conduction losses. When the peak current reduces to $I_{PEAK\_MIN}$ at lighter load, the TPS7H4010-SEP operates in PFM mode.

#### 7.4.3.3 PFM Mode

Pulse-frequency-modulation (PFM) mode is activated when peak current is lower than $I_{PEAK-MIN}$, only in auto mode. Peak current is kept constant and $V_{OUT}$ is regulated by frequency. Efficiency is greatly improved by lowered switching losses, especially at very light loads.

In PFM operation, a small DC positive offset appears on $V_{OUT}$. The lower the frequency is folded back in PFM, the more the DC offset is on $V_{OUT}$. See $V_{OUT}$ regulation curves in *Application Curves* section. If the DC offset on $V_{OUT}$ is not acceptable, a dummy load at $V_{OUT}$, or lower $R_{FBT}$ and $R_{FBB}$ resistance values can be used to reduce the offset. Alternatively the device can be run in FPWM mode where the switching frequency is constant, and no offset is added to affect the $V_{OUT}$ accuracy unless $t_{ON\_MIN}$ is reached.

#### 7.4.3.4 Fault Protection Mode

The TPS7H4010-SEP has hiccup current protection at extreme overload and short circuit conditions. Hiccup is activated when $V_{OUT}$ droops below 40% (typical) of the regulation voltage and stays for 128 consecutive switching cycles. Hiccup is disabled during soft start. In hiccup, the device turns off $V_{OUT}$ and re-tries soft start after 46-ms wait time. Cycle repeats until overcurrent fault condition has been removed. Hiccup mode helps to reduce the device power dissipation and die temperature under severe overcurrent conditions and short circuits. It improves system reliability and prolongs the life span of the device.

Under overcurrent conditions when $V_{OUT}$ droops below regulation but above 40% of regulated voltage, the TPS7H4010-SEP stays in cycle-by-cycle HS and LS current limiting protection mode.

Thermal shutdown prevents the device from extreme junction temperature by turning off the device when the junction temperature exceeds 160°C (typical). After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 135°C. When the junction temperature falls below 135°C, the TPS7H4010-SEP restarts.

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS7H4010-SEP device is a step-down DC-DC voltage regulator. It is designed to operate with a wide supply voltage range (3.5 V to 32 V), wide switching frequency range (350 kHz to 2.2 MHz), and wide output voltage range: up to 95% $V_{IN}$. The TPS7H4010-SEP is a synchronous converter with both HS and LS MOSFETs integrated, and it is capable of delivering a maximum output current of 6 A. The following design procedure can be used to select component values for the TPS7H4010-SEP. This section presents a simplified discussion of the design process.

## 8.2 Typical Application

The TPS7H4010-SEP requires only a few external components to perform high-efficiency power conversion, as shown in 图 8-1.

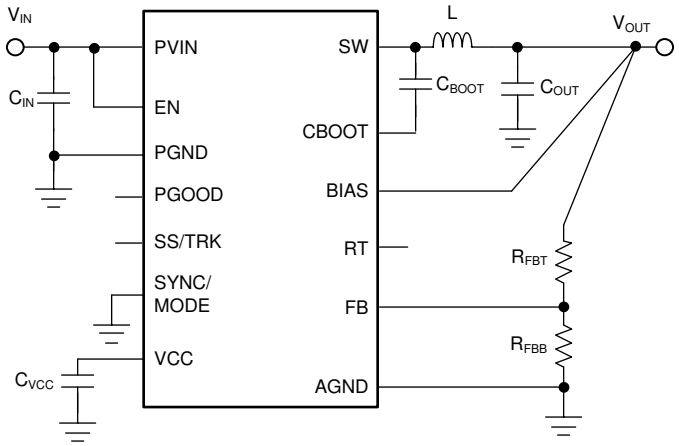



**图 8-1. TPS7H4010-SEP Basic Schematic**

The TPS7H4010-SEP also integrates many practical features to meet a wide range of system design requirements and optimization, such as UVLO, programmable soft-start time, start-up tracking, programmable switching frequency, clock synchronization and a power-good flag. Note that for ease of use, the feature pins do not require an additional component when not in use. They can be either left floating or shorted to ground. Please refer to *Pin Configuration and Functions* section for details.

A comprehensive schematic with all features utilized is shown in 图 8-2.

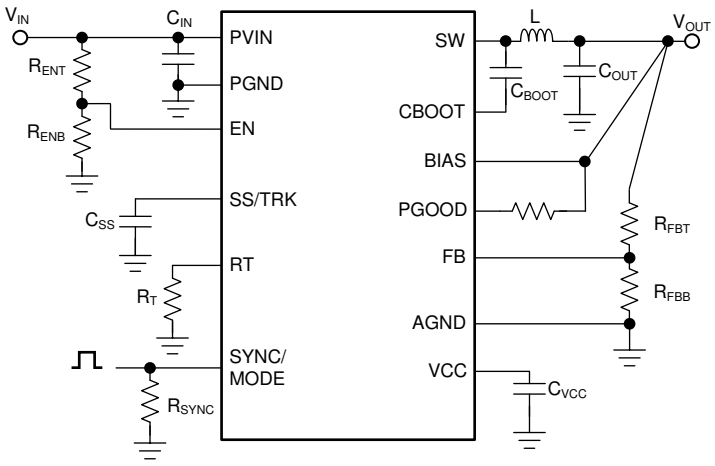





**图 8-2. TPS7H4010-SEP Comprehensive Schematic With All Features Utilized**

The external components must fulfill not only the needs of the power conversion, but also the stability criteria of the control loop. The TPS7H4010-SEP is optimized to work with a range of external components. For quick component selection, 表 8-1 can be used.

**表 8-1. Typical Component Selection**

| $f_{SW}$ (kHz) | $V_{OUT}$ (V) | L (µH) | $C_{OUT}$ (µF)(1) | $R_{FBT}$ (kΩ) | $R_{FBB}$ (kΩ) | $R_T$ (kΩ) |
|---|---|---|---|---|---|---|
| 350 | 1 | 2.2 | 500 | 100 | OPEN | 115 |
| 500 | 1 | 1.5 | 400 | 100 | OPEN | 78.7 or open |
| 1000 | 1 | 0.68 | 200 | 100 | OPEN | 39.2 |
| 2200 | 1 | 0.47 | 100 | 100 | OPEN | 17.4 |
| 350 | 3.3 | 4.7 | 200 | 100 | 43.5 | 115 |
| 500 | 3.3 | 3.3 | 150 | 100 | 43.5 | 78.7 or open |
| 1000 | 3.3 | 1.8 | 88 | 100 | 43.5 | 39.2 |
| 2200 | 3.3 | 1.2 | 44 | 100 | 43.5 | 17.4 |
| 350 | 5 | 6.8 | 120 | 100 | 25 | 115 |
| 500 | 5 | 4.7 | 88 | 100 | 25 | 78.7 or open |
| 1000 | 5 | 3.3 | 66 | 100 | 25 | 39.2 |
| 2200 | 5 | 2.2 | 44 | 100 | 25 | 17.4 |
| 350 | 12 | 15 | 66 | 100 | 9.1 | 115 |
| 500 | 12 | 10 | 44 | 100 | 9.1 | 78.7 or open |
| 1000 | 12 | 6.8 | 22 | 100 | 9.1 | 39.2 |
| 350 | 24 | 22 | 40 | 100 | 4.3 | 115 |
| 500 | 24 | 15 | 30 | 100 | 4.3 | 78.7 or open |

(1) All the $C_{OUT}$ values are after derating. Add more when using ceramics.

### 8.2.1 Design Requirements

Detailed design procedure is described based on a design example. For this design example, use the parameters listed in 表 8-2.

**表 8-2. Design Example Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Typical input voltage | 12 V |
| Output voltage | 5 V |
| Output current | 6 A |
| Operating frequency | 500 kHz |
| Soft-start time | 11 ms |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Output Voltage Setpoint*

The output voltage of the TPS7H4010-SEP device is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor $R_{FBT}$ and bottom feedback resistor $R_{FBB}$. Use 方程式 24 to determine the output voltage of the converter.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right) \tag{24}$$

Typically, $R_{FBT}$ = 10 kΩ to 100 kΩ is recommended. Larger $R_{FBT}$ and $R_{FBB}$ values reduce the quiescent current going through the divider, which help maintain high efficiency at very light loads. But larger divider values also make the feedback path more susceptible to noise. If efficiency at very light loads is critical in a certain application, $R_{FBT}$ up to 1 MΩ can be used.

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} R_{FBT} \tag{25}$$

$R_{FBT}$ = 100 kΩ is selected here. $R_{FBB}$ = 24.99 kΩ can be calculated to get 5-V output voltage.

#### *8.2.2.2 Switching Frequency*

The default switching frequency of the TPS7H4010-SEP device is set at 500 kHz. For this design, the RT pin can be floating, and the TPS7H4010-SEP switches at 500 kHz in CCM mode. An $R_T$ resistor of 78.7 kΩ, calculated using 方程式 13, 图 7-12, or 表 7-1, can be connected from RT pin to ground to obtain 500-kHz operation frequency as well.

The TPS7H4010-SEP switching action can synchronize to an external clock from 350 kHz to 2.2 MHz. TI recommends connecting an external clock to the SYNC/MODE pin with a 50-Ω to 100-Ω termination resistor. The SYNC/MODE pin must be grounded if not used.

RT pin is floating and SYNC/MODE pin is tied to ground in this design.

#### *8.2.2.3 Input Capacitors*

The TPS7H4010-SEP device requires high-frequency ceramic input decoupling capacitors. Depending on the application, a bulk input capacitor can also be added. The typical recommended ceramic decoupling capacitors include one small 0.1-µF to 1-µF capacitor, and one large 10-µF to 22-µF capacitor. TI recommends high-quality ceramic type X5R or X7R capacitors. The voltage rating must be greater than the maximum input voltage. As a general rule, to compensate the derating TI recommends a voltage rating of twice the maximum input voltage.

It is very important in buck regulator applications to place the small decoupling capacitor right next to the PVIN and PGND pins. This capacitor is used to bypass the high frequency switching noise by providing a return path

of the noise. It prevents the noise from spreading to wider area of the board. The large bypass ceramic capacitor must also be as close as possible to the PVIN and PGND pins.

Additionally, some bulk capacitance may be required, especially if the TPS7H4010-SEP circuit is not located within approximately 2 inches from the input voltage source. This capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable. The optimum value for this capacitor is four times the ceramic input capacitance with ESR close to the characteristic impedance of the LC filter formed by your input inductance and your ceramic input capacitors. It is not critical that the electrolytic filter be at the optimum value for damping, but it must be rated to handle the maximum input voltage including ripple voltage.

For this design, two 10-µF, X7R dielectric capacitors rated for 50 V are used for the input decoupling capacitance, and a capacitor with a value of 0.47 µF for high-frequency filtering.

**Note**

*DC bias effect:* High capacitance ceramic capacitors have a DC bias derating effect, which will have a strong influence on the final effective capacitance. Therefore, the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

#### *8.2.2.4 Inductor Selection*

The first criterion for selecting an output inductor is the inductance. In most buck converters, this value is based on the desired peak-to-peak ripple current in the inductor, $I_{Lripple}$. An inductance that gives a ripple current of 10% to 30% of the maximum output current (6 A) is a good starting point. The inductance can be calculated from 方程式 26:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times I_{Lripple}} \tag{26}$$

where

- $I_{Lripple}$ = (0.1 to 0.3) × $I_{L\_MAX}$
- $I_{L\_MAX}$ = 6 A for TPS7H4010-SEP
- D = $V_{OUT}$ / $V_{IN}$

Selected $I_{Lripple}$ is between 10% to 30% of the rated current of the device.

As with switching frequency, the selection of the inductor is a tradeoff between size, cost, and performance. Higher inductance gives lower ripple current and hence lower output voltage ripple. With peak current mode control, the current ripple is the input signal to the control loop. A certain amount of ripple current is needed to maintain the signal-to-noise ratio of the control loop. Within the same series (same size/height), a larger inductance will have a higher series resistance (ESR). With similar ESR, size and/or height will be greater. Larger inductance also has slower current slew rate during large load transients.

Lower inductance usually results in a smaller, less expensive component; however, the current ripple will be higher, thus more output capacitor is needed to maintain the same amount of output voltage ripple. The RMS current is higher with the same load current due to larger ripple. The switching loss is higher because the switch current, which is the peak current, is higher when the HS switch turns off and LS switch turns on. Core loss of the inductor is also larger with higher ripple. Core loss needs to be considered, especially with higher switching frequencies. Check the ripple current over $V_{IN\_MIN}$ to $V_{IN\_MAX}$ range to make sure current ripple is reasonable over entire supply voltage range.

For applications with large $V_{OUT}$ and typical $V_{OUT}$ / $V_{IN}$ > 50%, sub-harmonic oscillation can be a concern in peak current-mode-controlled buck converters. Select inductance so that

$$L \geqslant V_{OUT} / (N \times f_{SW}) \tag{27}$$

where

- N = 3.6 with TPS7H4010-SEP

The second criterion is inductor saturation current rating. Because the maximum inductor current is limited by the high-side switch current limit, it is advised to select an inductor with a saturation current higher than the $I_{LIMIT-HS}$. TI recommends selection of soft saturation inductors. A power inductor could be the major source of radiated noise. When EMI is a concern in the application, select a shielded inductor, if possible.

For this design, 20% ripple of 6 A yields 4.86-µH inductance. A 4.7-µH inductor is selected, which gives 21% ripple current.

#### *8.2.2.5 Output Capacitor Selection*

The output capacitor is responsible for filtering the inductor current, and supplying load current during transients. Capacitor selection depends on application conditions as well as ripple and transient requirements. Best performance is achieved by using ceramic capacitors or combinations of ceramic and other types of capacitors. For high output voltage conditions, such as 12 V and above, finding ceramic capacitors that are rated for an appropriate voltage becomes challenging. In such cases choose a low-ESR capacitor. It is a good idea to use a low-value ceramic capacitor in parallel with other capacitors, to bypass high frequency noise between ground and $V_{OUT}$.

For a given input and output requirement, 方程式 28 gives an approximation for a minimum output capacitor required.

$$C_{OUT} > \frac{1}{(f_{SW} \times r \times \Delta V_{OUT} / I_{OUT})} \times \left[ \left( \frac{r^2}{12} \times (1 + D') \right) + (D' \times (1 + r)) \right] \quad (28)$$

where

- r = Ripple ratio of the inductor ripple current ($I_{Lripple}$ / 6 A )
- $\Delta V_{OUT}$ = Target output voltage undershoot, for example, 5% to 10% of $V_{OUT}$
- D’ = 1 – duty cycle
- $f_{SW}$ = switching frequency
- $I_{OUT}$ = load current

Along with 方程式 28, for the same requirement calculate the maximum ESR with 方程式 29.

$$ESR < \frac{D'}{f_{SW} \times C_{OUT}} \times \left( \frac{1}{r} + 0.5 \right) \quad (29)$$

The output capacitor is also the dominating factor in the loop response of a peak-current mode controlled buck converter. A simplified estimation of the control loop crossover frequency can be found by 方程式 18.

Select $C_{OUT}$ so that the $f_X$ is no higher than 1/6 of the switching frequency. Typically, $f_X$ / $f_{SW}$ = 1/10 to 1/8 provides a good combination of stability and performance.

For this design, one 0.47-µF, 50-V X7R and four 22-µF, 16-V, X7R ceramic capacitors are used in parallel based on a target output voltage overshoot value of 10%.

#### *8.2.2.6 Feed-Forward Capacitor*

The TPS7H4010-SEP is internally compensated. Typically, select $R_{FBT} \leqslant 100\ k\Omega$, then $C_{FF}$ is not needed. When very low quiescent current is needed, $R_{FBT} = 1\ M\Omega$ may be used. If $C_{OUT}$ is mainly ceramic type low ESR capacitors, an external feed-forward capacitor $C_{FF}$ may be needed to improve the phase margin. Add $C_{FF}$ in parallel with $R_{FBT}$. $C_{FF}$ is chosen such that the phase boost is maximized at the estimated crossover frequency $f_X$. 方程式 21 was tested.

With this design, because $R_{FBT} = 100\ k\Omega$ is selected, no $C_{FF}$ is needed.

#### 8.2.2.7 Bootstrap Capacitors

Every TPS7H4010-SEP design requires a bootstrap capacitor, $C_{BOOT}$. The recommended bootstrap capacitor is 0.47 µF and rated at 6.3 V or greater. The bootstrap capacitor is located between the SW pin and the CBOOT pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

#### 8.2.2.8 VCC Capacitor

The VCC pin is the output of an internal LDO for TPS7H4010-SEP. The input for this LDO comes from either $V_{IN}$ or BIAS pin voltage. The recommended $C_{VCC}$ capacitor is 2.2 µF and rated at 6.3 V or greater. It must be a high-quality ceramic type with X7R or X5R grade to insure stability. Never short VCC pin to ground during operation.

#### 8.2.2.9 BIAS

Because $V_{OUT}$ = 5 V in this design, the BIAS pin is tied to $V_{OUT}$ to reduce LDO power loss. The output voltage is supplying the LDO current instead of the input voltage. The power saving is $I_{LDO} \times (V_{IN} - V_{OUT})$. The power saving is more significant when $V_{IN} >> V_{OUT}$ and with higher frequency operation. To prevent $V_{OUT}$ noise and transients from coupling to BIAS, a series resistor, 1 Ω to 10 Ω, may be added between $V_{OUT}$ and BIAS. A bypass capacitor with a value of 1 µF or higher can be added close to the BIAS pin to filter noise.

#### 8.2.2.10 Soft Start

The SS/TRK pin can be floating to start up following the internal soft-start ramp. In order to extend the soft-start time, an external soft-start capacitor can be used. Use 方程式 12 in order to calculate the soft-start capacitor value.

With a desired soft-start time $t_{SS}$ = 11 ms, a soft-start charging current of $I_{SSC}$ = 2 µA (typical), and $V_{FB}$ = 1.006 V (typical), 方程式 12 yields a soft-start capacitor value of 22 nF.

#### 8.2.2.11 Undervoltage Lockout Setpoint

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of $R_{ENT}$ and $R_{ENB}$. With one selected $R_{ENT}$ value, $R_{ENB}$ can be found by 方程式 10.

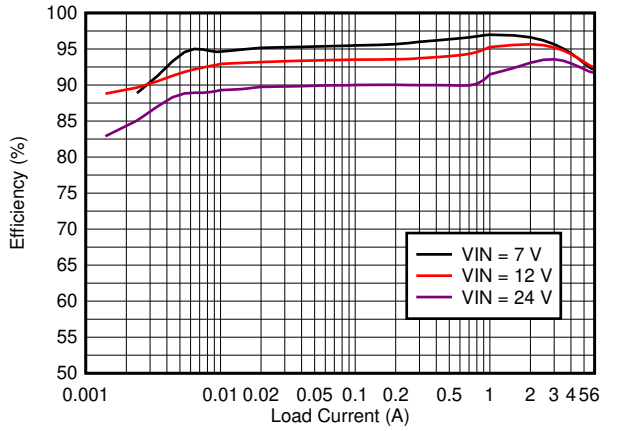
Note that the divider adds to supply quiescent current by $V_{IN}$ / ($R_{ENT}$ + $R_{ENB}$). Small $R_{ENT}$ and $R_{ENB}$ values add more quiescent current loss. However, large divider values make the node more sensitive to noise.

In this design, EN pin is tied to PVIN pin with a 100-kΩ resistor.

#### 8.2.2.12 PGOOD

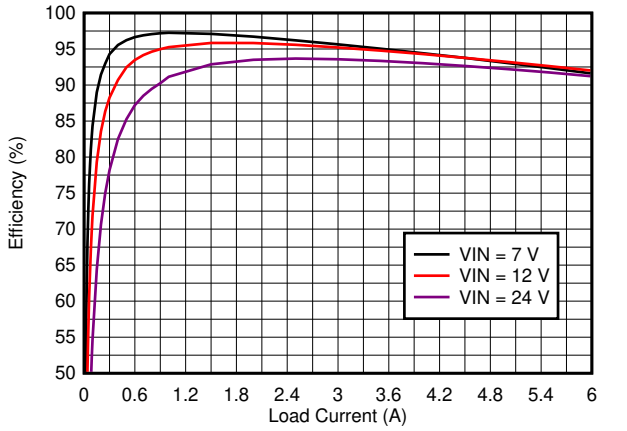
For this design, a 100-kΩ resistor is used to pull up PGOOD to $V_{OUT}$.

### 8.2.3 Application Curves



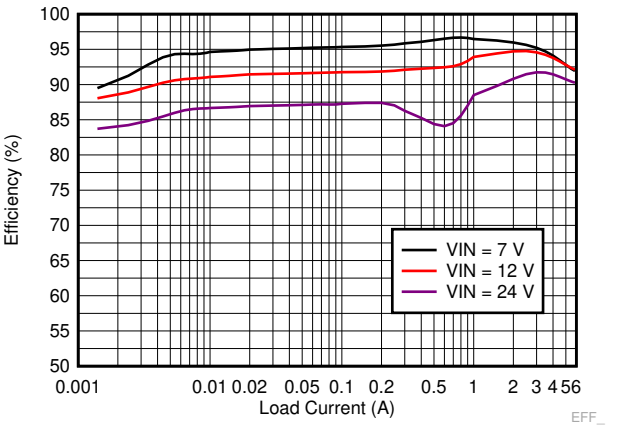

$V_{OUT}$ = 5 V $f_{SW}$ = 500 kHz Auto Mode

图 8-3. TPS7H4010-SEP Efficiency



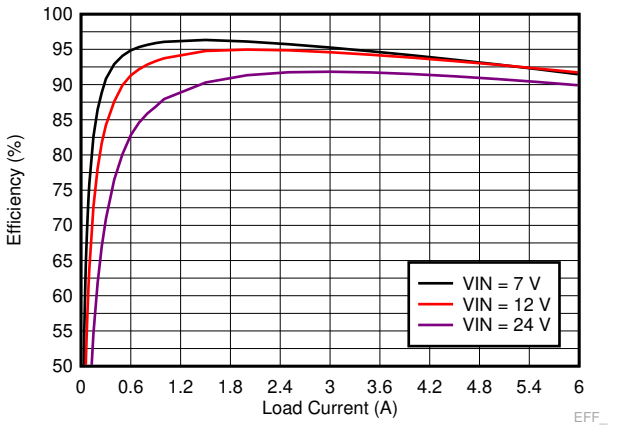

$V_{OUT}$ = 5 V $f_{SW}$ = 500 kHz FPWM Mode

图 8-4. TPS7H4010-SEP Efficiency



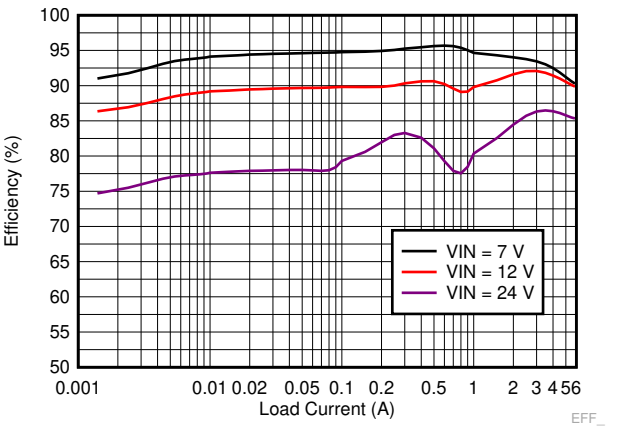

$V_{OUT}$ = 5 V $f_{SW}$ = 1000 kHz Auto Mode

图 8-5. TPS7H4010-SEP Efficiency



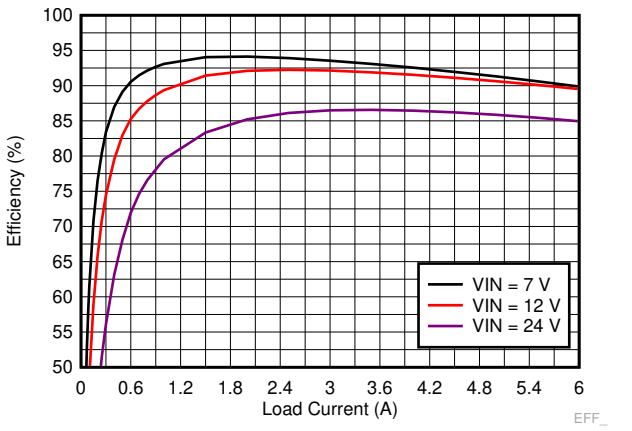

$V_{OUT}$ = 5 V $f_{SW}$ = 1000 kHz FPWM Mode

图 8-6. TPS7H4010-SEP Efficiency



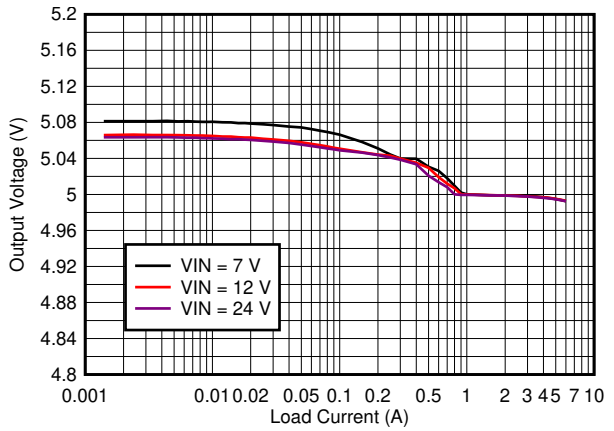

$V_{OUT}$ = 5 V $f_{SW}$ = 2200 kHz Auto Mode

图 8-7. TPS7H4010-SEP Efficiency



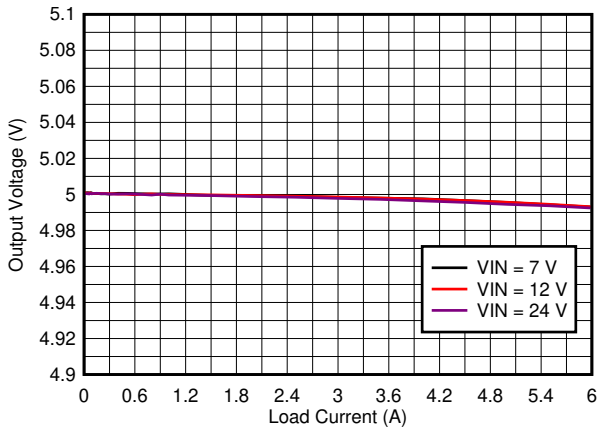

$V_{OUT}$ = 5 V $f_{SW}$ = 2200 kHz FPWM Mode

图 8-8. TPS7H4010-SEP Efficiency



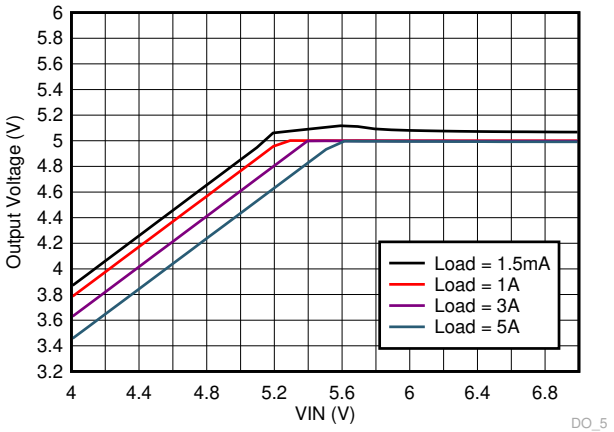

$V_{OUT}$ = 5 V $f_{SW}$ = 500 kHz Auto Mode

**图 8-9. TPS7H4010-SEP Load and Line Regulation**



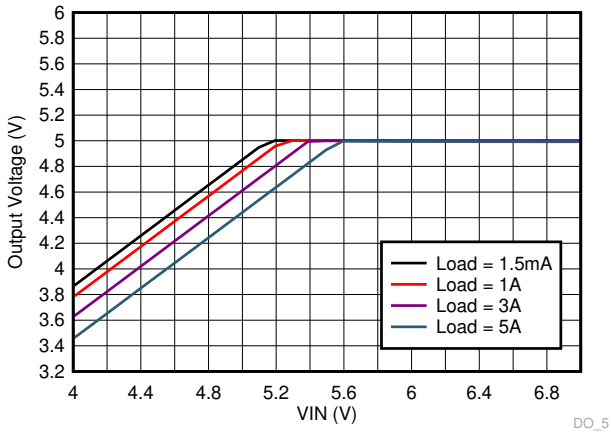

$V_{OUT}$ = 5 V $f_{SW}$ = 500 kHz FPWM Mode

**图 8-10. TPS7H4010-SEP Load and Line Regulation**



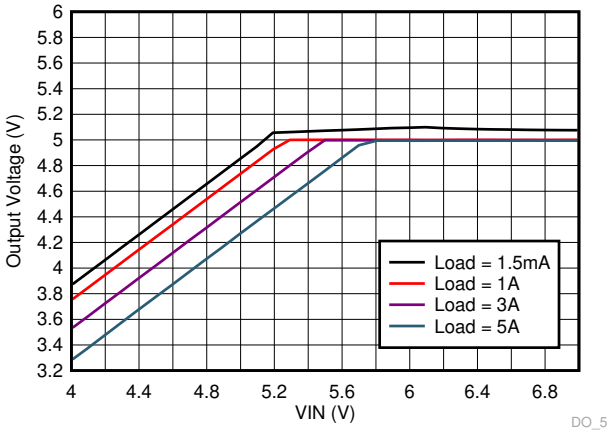

$V_{OUT}$ = 5 V $f_{SW}$ = 2200 kHz Auto Mode

**图 8-11. TPS7H4010-SEP Dropout Curve**



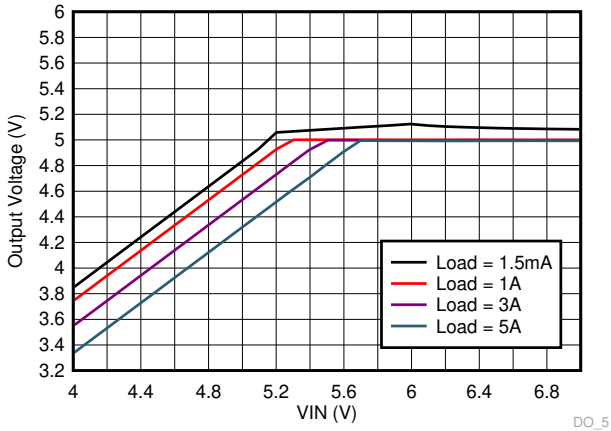

$V_{OUT}$ = 5 V $f_{SW}$ = 2200 kHz FPWM Mode

**图 8-12. TPS7H4010-SEP Dropout Curve**



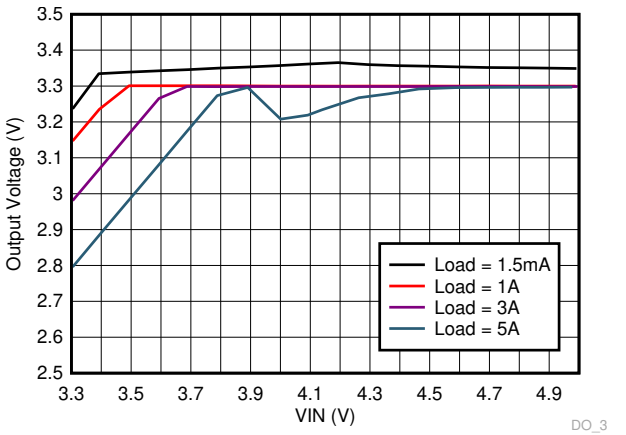

$V_{OUT}$ = 5 V $f_{SW}$ = 500 kHz Auto Mode

**图 8-13. TPS7H4010-SEP Dropout Curve**



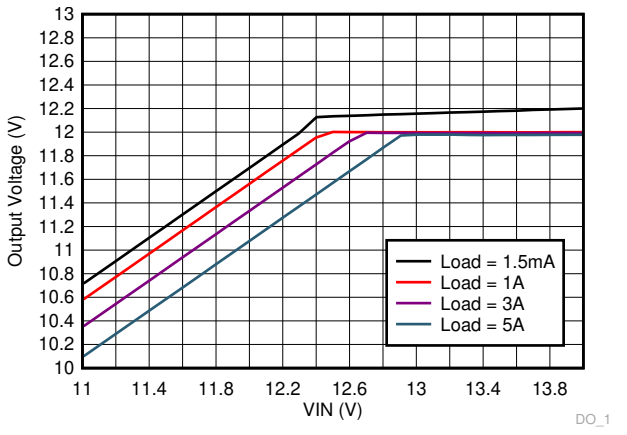

$V_{OUT}$ = 5 V $f_{SW}$ = 1000 kHz Auto Mode

**图 8-14. TPS7H4010-SEP Dropout Curve**



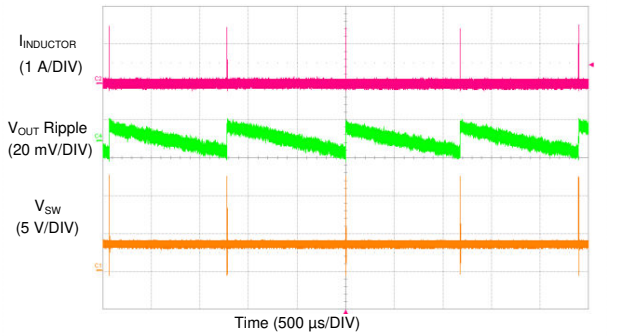

$V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz Auto Mode

**图 8-15. TPS7H4010-SEP Dropout Curve**



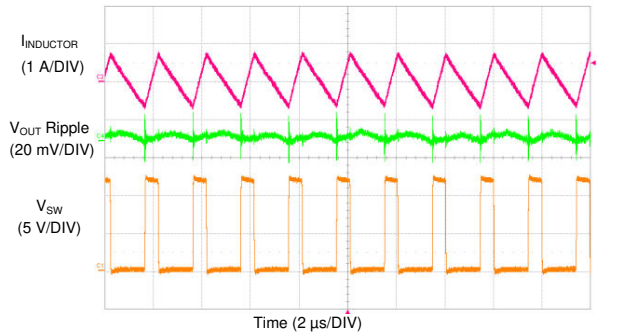

$V_{OUT}$ = 12 V $f_{SW}$ = 500 kHz Auto Mode

**图 8-16. TPS7H4010-SEP Dropout Curve**



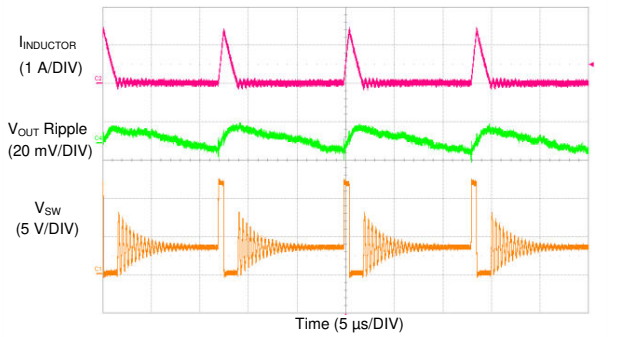

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$I_{OUT}$ = 1 mA Auto Mode

**图 8-17. TPS7H4010-SEP Switching Waveform and $V_{OUT}$ Ripple**



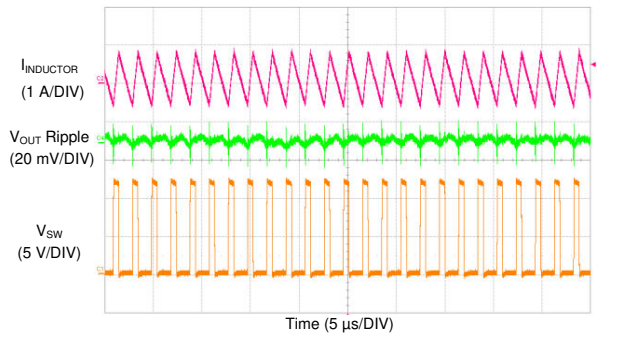

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$I_{OUT}$ = 1 mA FPWM Mode

**图 8-18. TPS7H4010-SEP Switching Waveform and $V_{OUT}$ Ripple**



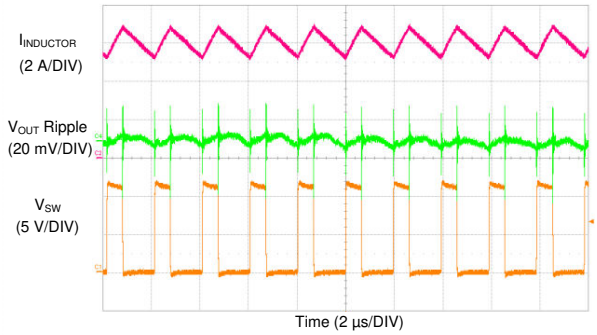

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$I_{OUT}$ = 100 mA Auto Mode

**图 8-19. TPS7H4010-SEP Switching Waveform and $V_{OUT}$ Ripple**



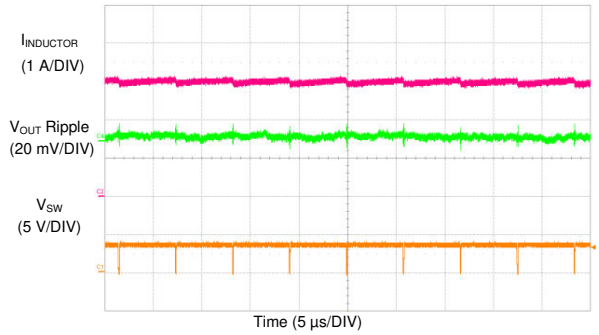

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$I_{OUT}$ = 100 mA FPWM Mode

**图 8-20. TPS7H4010-SEP Switching Waveform and $V_{OUT}$ Ripple**



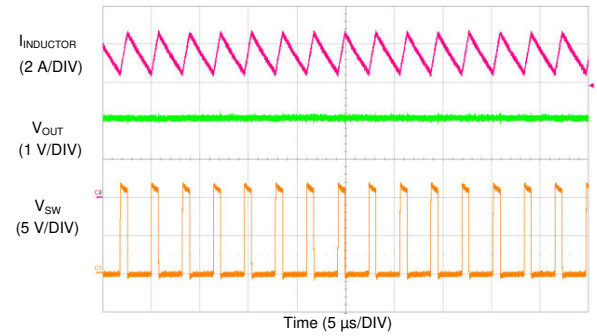

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$I_{OUT}$ = 6 A Auto Mode

**图 8-21. TPS7H4010-SEP Switching Waveform and $V_{OUT}$ Ripple**



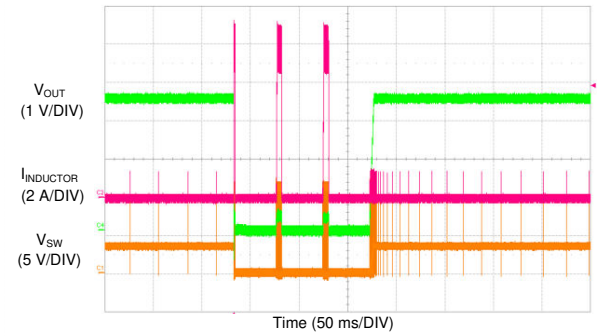

$V_{IN}$ = 3.66 V $V_{OUT}$ = 3.3 V $f_{SW}$ set at 500 kHz
$I_{OUT}$ = 3 A Auto Mode

**图 8-22. TPS7H4010-SEP Switching Waveform at Dropout**



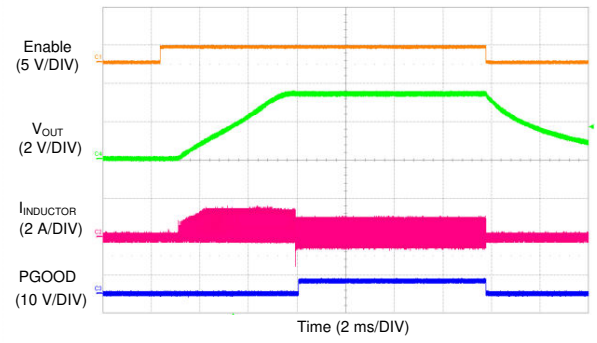

$V_{IN}$ = 12 V $V_{OUT}$ set at 3.3 V $f_{SW}$ set at 500 kHz
$I_{OUT}$ = 7.5 A $V_{OUT}$ droops to 2 V

**图 8-23. TPS7H4010-SEP Overcurrent Behavior**



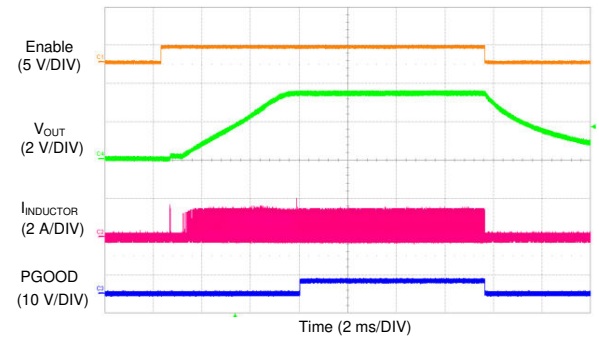

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz

**图 8-24. TPS7H4010-SEP Short-Circuit Hiccup Protection and Recovery**



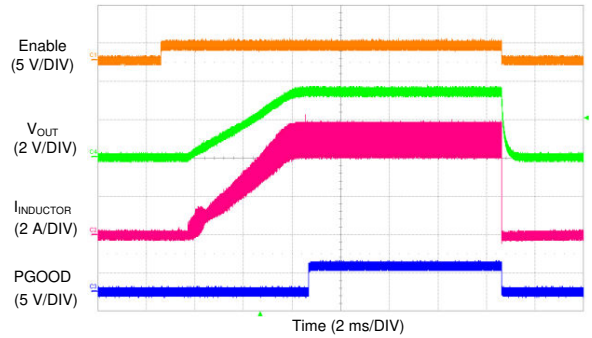

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$I_{OUT}$= 200 mA FPWM Mode

**图 8-25. TPS7H4010-SEP Soft Start With 200-mA Load in FPWM Mode**



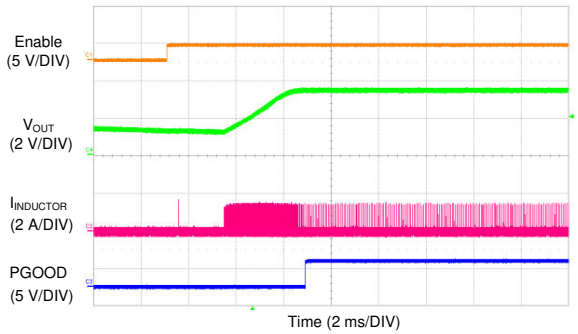

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$I_{OUT}$= 200 mA Auto Mode

**图 8-26. TPS7H4010-SEP Soft Start With 200-mA Load in Auto Mode**



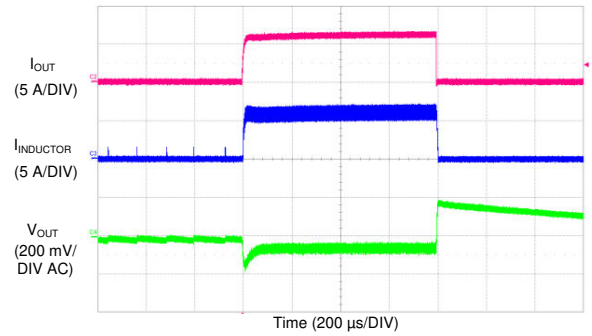

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$I_{OUT}$ = 5 A Auto Mode

**图 8-27. TPS7H4010-SEP Soft Start With 5-A Load**



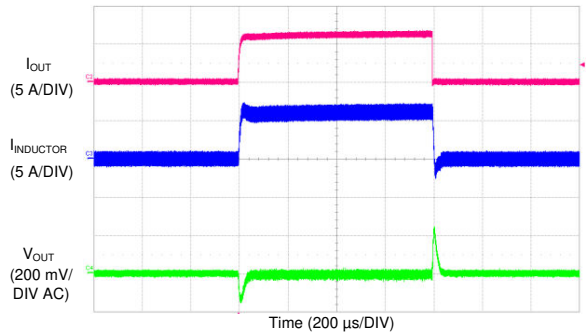

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$V_{PRE-BIAS}$= 1.5 V Auto Mode

**图 8-28. TPS7H4010-SEP Soft Start With Pre-Biased Output Voltage**



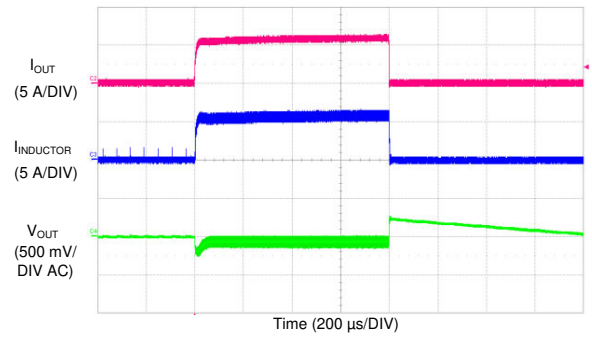

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$I_{OUT}$ = 10 mA to 6 A to 10 mA Auto Mode

**图 8-29. TPS7H4010-SEP Load Transients**



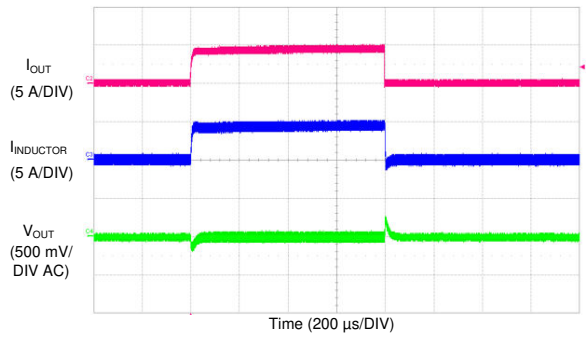

$V_{IN}$ = 12 V $V_{OUT}$ = 3.3 V $f_{SW}$ = 500 kHz
$I_{OUT}$ = 10 mA to 6 A to 10 mA FPWM Mode

**图 8-30. TPS7H4010-SEP Load Transients**




$V_{IN}$ = 12 V $V_{OUT}$ = 5 V $f_{SW}$ = 2200 kHz
$I_{OUT}$ = 10 mA to 5 A to 10 mA Auto Mode

**图 8-31. TPS7H4010-SEP Load Transients**




$V_{IN}$ = 12 V $V_{OUT}$ = 5 V $f_{SW}$ = 2200 kHz
$I_{OUT}$ = 10 mA to 5 A to 10 mA FPWM Mode

**图 8-32. TPS7H4010-SEP Load Transients**

# 9 Power Supply Recommendations

The TPS7H4010-SEP is designed to operate from an input voltage supply range from 3.5 V to 32 V. This input supply must be able to withstand the maximum input current and maintain a voltage above 3.5 V at the PVIN pin. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the TPS7H4010-SEP supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the TPS7H4010-SEP, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A 47-µF or 100-µF electrolytic capacitor is a typical choice.

# 10 Layout

## 10.1 Layout Guidelines

The performance of any switching converter depends heavily upon the layout of the PCB. Use the following guidelines to design a PCB layout with optimum power conversion performance, EMI performance, and thermal performance.

1. Place ceramic high frequency bypass capacitors as close as possible to the PVIN and PGND pins, which are right next to each other on the package. Place the small value ceramic capacitor closest to the pins. This is very important for EMI performance.
2. Use short and wide traces, or localized IC layer planes, for high current paths, such as $V_{IN}$, $V_{OUT}$, SW, and GND connections. Short and wide copper traces reduce power loss and noise due to low parasitic resistance and inductance. Wide copper traces also help reduce die temperature, because they also provide wide heat dissipation paths. Use thick copper (2 oz) on high current layer(s) if possible.
3. Confine pulsing current paths ($V_{IN}$, SW, and ground return for $V_{IN}$) on the device layer as much as possible to prevent switching noises from contaminating other layers.
4. $C_{BOOT}$ capacitor also contains pulsing current. Place $C_{BOOT}$ close to the pin and route to SW with short trace. The pinout of the device makes it easy to optimize the $C_{BOOT}$ placement and routing.
5. Use a solid ground plane at the layer right underneath the device as a noise shielding and heat dissipation path.
6. Place the VCC bypass capacitor close to the VCC pin. Tie the ground pad of the capacitor to the ground plane using a via right next to it.
7. Use via next to AGND pin to the ground plane.
8. Minimize trace length to the FB pin. Both feedback resistors must be located right next to the FB pin. Tie the ground side of $R_{FBB}$ to the ground plane with a via right next to it. Place $C_{FF}$ directly in parallel with $R_{FBT}$ if used.
9. If $V_{OUT}$ accuracy at the load is important, make sure the $V_{OUT}$ sense point is made close to the load. Route $V_{OUT}$ sense to $R_{FBT}$ through a path away from noisy nodes and preferably on a layer on the other side of the ground plane. If BIAS is connected to $V_{OUT}$, do not use the same trace to route $V_{OUT}$ to BIAS and to $R_{FBT}$. BIAS current contains pulsing driver current and it changes with operating mode. Use separated traces for BIAS and $V_{OUT}$ sense to optimize $V_{OUT}$ regulation accuracy.
10. Provide adequate device heat sinking. Use an array of heat-sinking vias to connect the exposed pad to the ground plane and the bottom PCB layer. Connect the DAP and NC pins on the short sides of the device to the GND net, so that IC layer ground copper can provide an optimal dog-bone shape heat sink. Heat generated on the die can flow directly from device junction to the DAP then to the copper and spread to the wider copper outside of the device. Try to keep copper area solid on the top and bottom layer around thermal vias on the DAP to optimize heat dissipation.

### 10.1.1 Layout For EMI Reduction

To optimize EMI performance, place the components in the high di/dt current path, as shown in 图 10-1, as close as possible to each other. When the components are close to each other, the area of the loop enclosed by these components, and the parasitic inductance of this loop, are minimized. The noises generated by the pulsing current and parasitic inductances are then minimized.

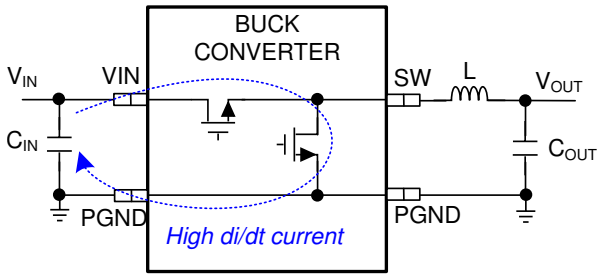



**图 10-1. Pulsing Current Path of Buck Converter**

In a buck converter, the high di/dt current path is composed of the HS and LS MOSFETs and the input capacitors. Because the two MOSFETs are integrated inside the device, they are closer to each other than in discrete solutions. PVIN and PGND pins are the connections from the MOSFETs to the input capacitors. The first step of the layout must be placing the input capacitors, especially the small value ceramic bypass one, as close as possible to PVIN and PGND pins.

The TPS7H4010-SEP pinout is optimized for low EMI layout. Multiple pins are used for PVIN and PGND to minimized bond wire resistances and inductances. The PVIN and PGND pins are right next to each other to simplify optimal layout. The CBOOT pin is placed next to SW pin for easy and compact $C_{BOOT}$ capacitor layout.

### 10.1.2 Ground Plane

The ground plane of a PCB provides the best return path for the pulsing current on the device layer. Make sure the ground plane is solid, especially the part right underneath the pulsing current paths. Solid copper under a pulsing current path provide a mirrored return path for the high frequency components and minimize voltage spikes generated by the pulsing current. It shields the layers on the other side of the plane from switching noises. Route signal traces on the other side of the ground plane as much as possible. Use multiple vias in parallel to connect the grounds on the device layer to the ground plane.

### 10.1.3 Optimize Thermal Performance

The key to thermal optimization on PCB design is to provide heat transferring paths from the device to the outer large copper area. Use thick copper (2 oz) on high current layer(s) if possible. Use thermal vias under the DAP to transfer heat to other layers. Connect NC pins to the GND net so that GND copper can run underneath the device to create dog-bone shape heat sink. Try to leave copper solid on IC side as much as possible above and below the device. Place components and route traces away from major heat transferring paths, if possible, to avoid blocking heat dissipation path. Try to leave copper solid, free of components and traces, around the thermal vias on the other side of the board as well. Solid copper behaves as heat sink to spread the heat to a larger area.

When calculating power dissipation, use the maximum input voltage and the average output current for the application. Many common operating conditions are provided in *Application Curves* section. Less common applications can be derived through interpolation. In all designs, the junction temperature must be kept below the rated maximum of 125°C.

## 10.2 Layout Example

A layout example is shown in 图 10-2. A four-layer board is used with 2-oz copper on the top and bottom layers and 1-oz copper on the inner two layers. 图 10-2 shows the relative scale of the TPS7H4010-SEP device with 0805 and 1210 input and output capacitors, 7-mm × 7-mm inductor and 0603 case size for all other passive components. The trace width of the signal connections are not to scale.

The components are placed on the top layer and the high current paths are routed on the top layer as well. The remaining space on the top layer can be filled with GND polygon. Thermal vias are used under the DAP and around the device. The GND copper was extended to the outside of the device, which serves as copper heat sink.

The mid-layer 1 is right underneath the top layer. It is a solid ground plane, which serves as noise shielding and heat dissipation path.

The $V_{OUT}$ sense trace is routed on the 3rd layer, which is mid-layer 2. Ground plane provided noise shielding for the sense trace. The $V_{OUT}$ to BIAS connection is routed by a separate trace.

The bottom layer is also a solid ground copper in this example. Solid copper provides best heat sinking for the device. If components and traces need to be on the bottom layer, leave the area around thermal vias as solid as possible. Try not to cut heat dissipation path by a trace. The board can be used for various frequencies and output voltages, with component variation. For more details, see the *TPS7H4010-SEP EVM User's Guide*.

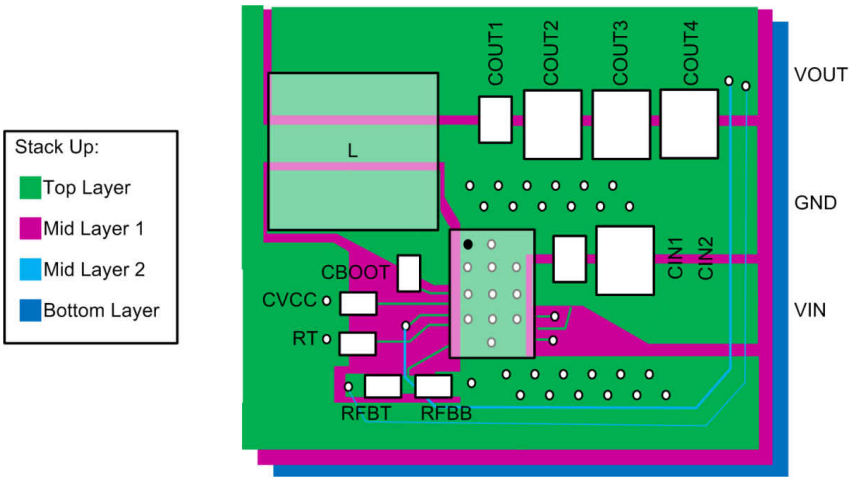



**图 10-2. TPS7H4010-SEP Layout Example**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 第三方产品免责声明

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## 11.2 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H4010EVM User's Guide* user's guide
- Texas Instruments, *TPS7H4010-SEP Total Ionizing Dose (TID)* radiation report
- Texas Instruments, *TPS7H4010-SEP Neutron Displacement Damage Characterization* radiation report
- Texas Instruments, *TPS7H4010-SEP Single-Event Effects Test Report* radiation report
- Texas Instruments, *TPS7H4010-SEP Production Flow and Reliability Report*
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report

## 11.3 接收文档更新通知

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## 11.4 支持资源

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 11.5 Trademarks

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## 11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7H4010MKGDSEP | Active | Production | XCEPT (KGD) \| 0 | 10 \| OTHER | Yes | Call TI | N/A for Pkg Type | -55 to 125 | |
| TPS7H4010MRNPSEP | Active | Production | WQFN (RNP) \| 30 | 490 \| JEDEC TRAY (10+1) | Yes | NIPDAUAG | Level-3-260C-168 HR | -55 to 125 | PS7H4010 RNPSEP |
| TPS7H4010MRNPTSEP | Active | Production | WQFN (RNP) \| 30 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -55 to 125 | PS7H4010 RNPSEP |
| V62/19623-019A | Active | Production | XCEPT (KGD) \| 0 | 10 \| OTHER | Yes | Call TI | N/A for Pkg Type | -55 to 125 | |
| V62/19623-01XE | Active | Production | WQFN (RNP) \| 30 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -55 to 125 | PS7H4010 RNPSEP |
| V62/19623-01XE-T | Active | Production | WQFN (RNP) \| 30 | 490 \| JEDEC TRAY (10+1) | Yes | NIPDAUAG | Level-3-260C-168 HR | -55 to 125 | PS7H4010 RNPSEP |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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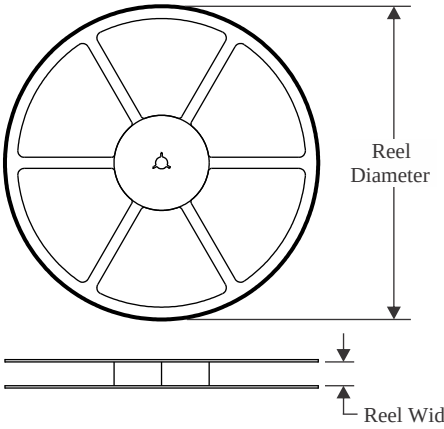
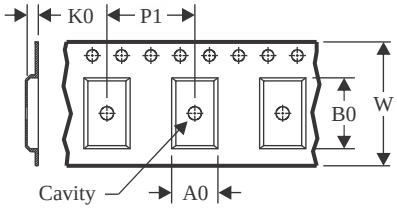
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

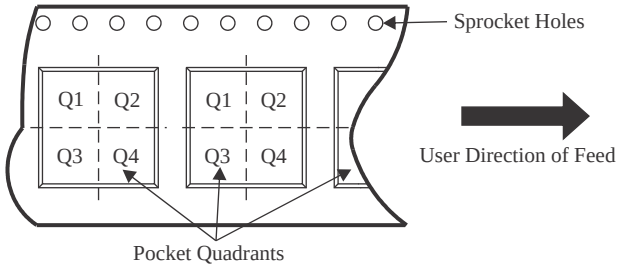



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

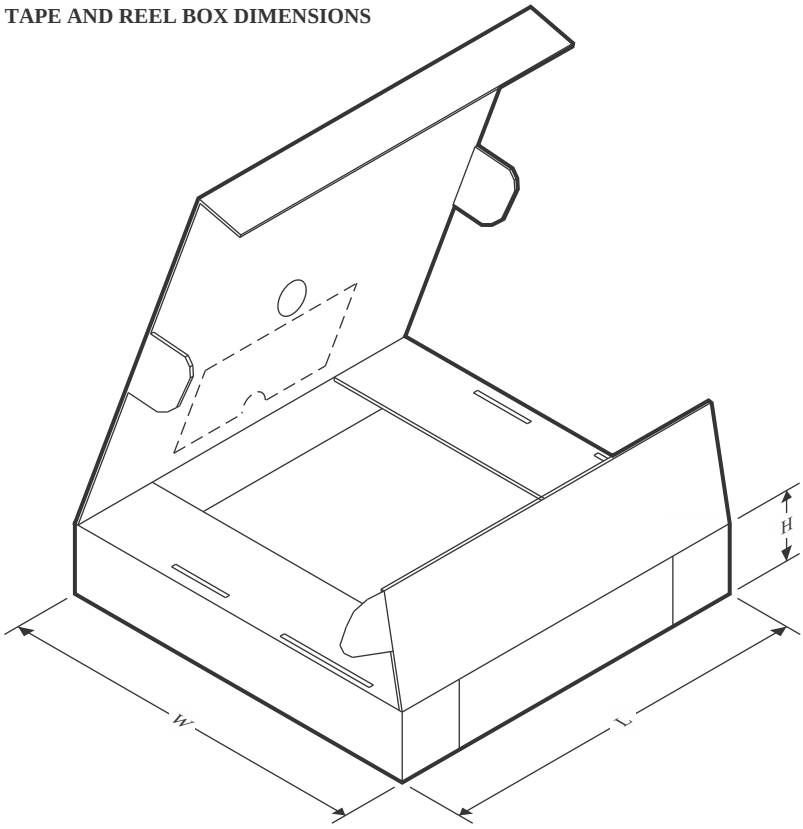
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7H4010MRNPTSEP | WQFN | RNP | 30 | 250 | 180.0 | 16.4 | 4.25 | 6.25 | 0.95 | 8.0 | 16.0 | Q1 |

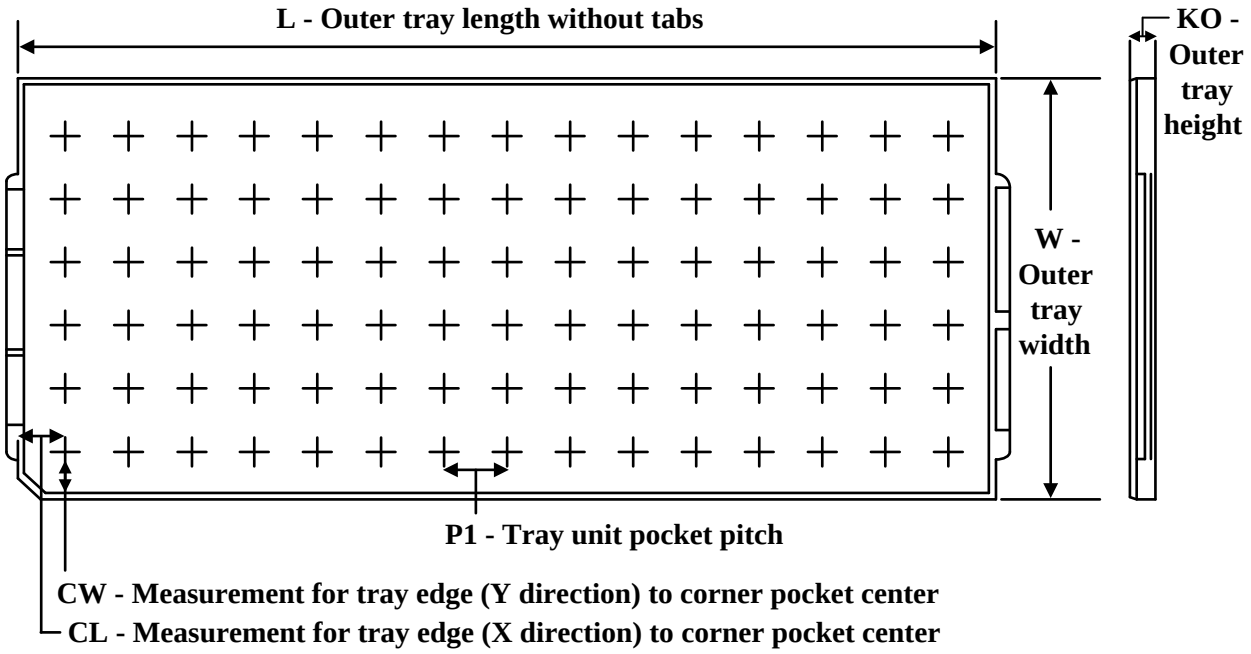
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7H4010MRNPTSEP | WQFN | RNP | 30 | 250 | 213.0 | 191.0 | 35.0 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7H4010MRNPSEP | RNP | WQFN | 30 | 490 | 35 x 14 | 150 | 315 | 135.9 | 7620 | 8.8 | 7.9 | 8.15 |
| V62/19623-01XE-T | RNP | WQFN | 30 | 490 | 35 x 14 | 150 | 315 | 135.9 | 7620 | 8.8 | 7.9 | 8.15 |

# GENERIC PACKAGE VIEW

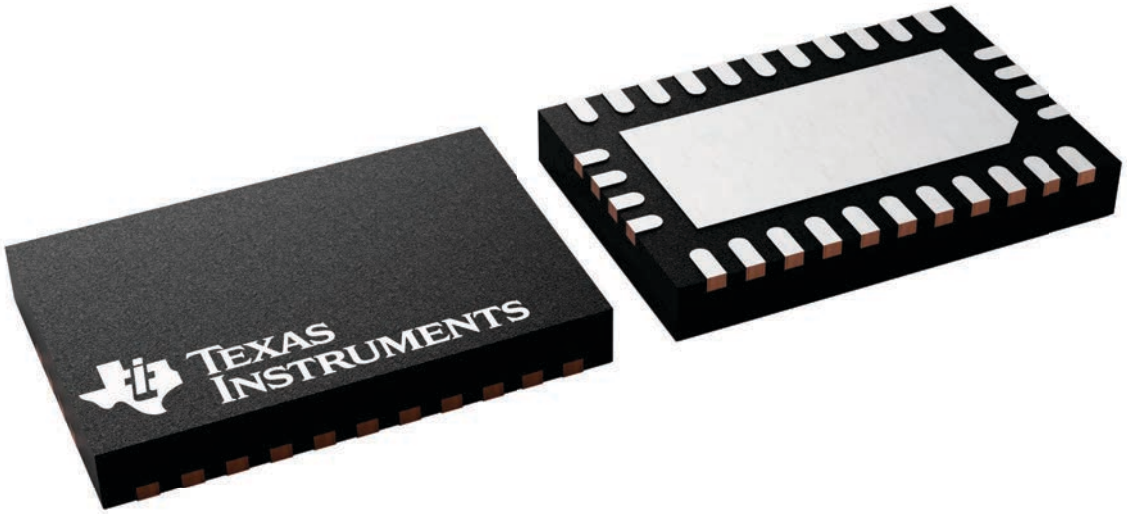
## RNP 30

## WQFN - 0.8 mm max height

**4 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



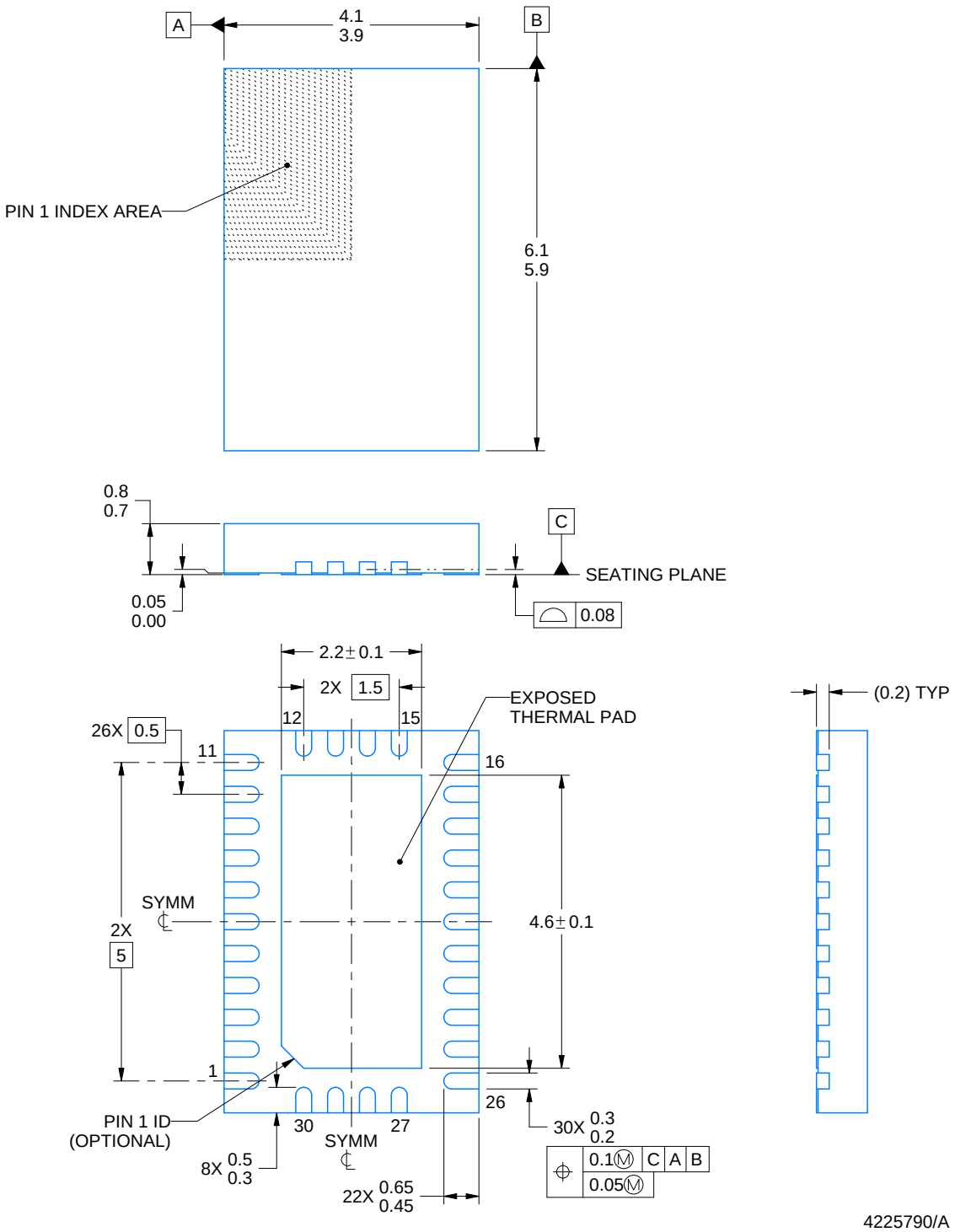

4225831/A

# RNP0030C

# PACKAGE OUTLINE

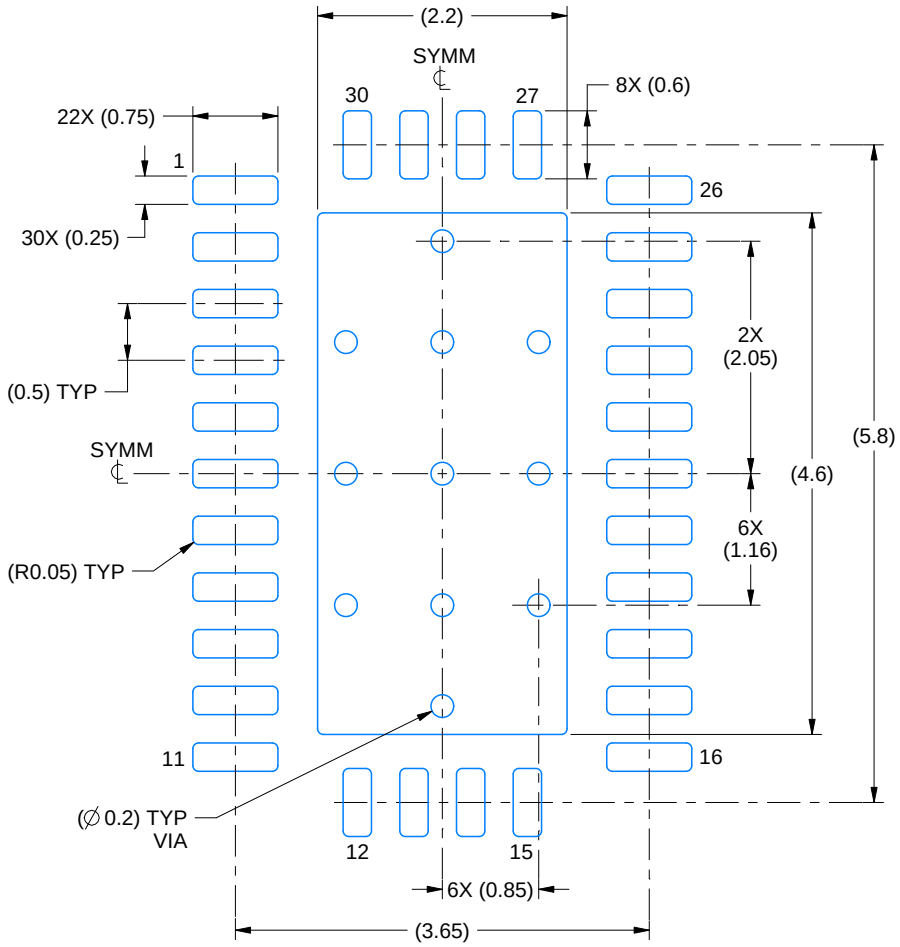
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

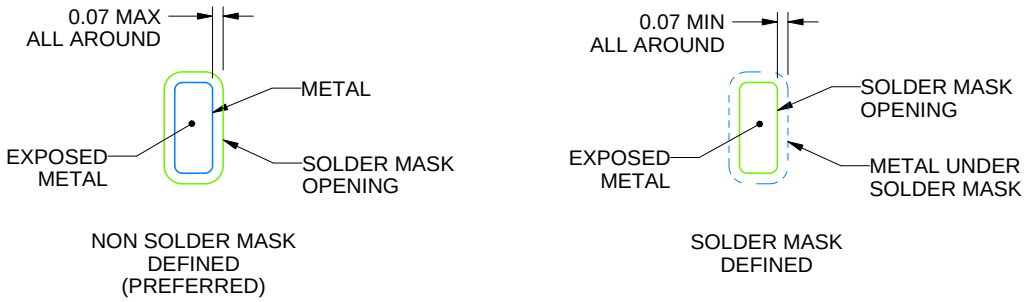



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

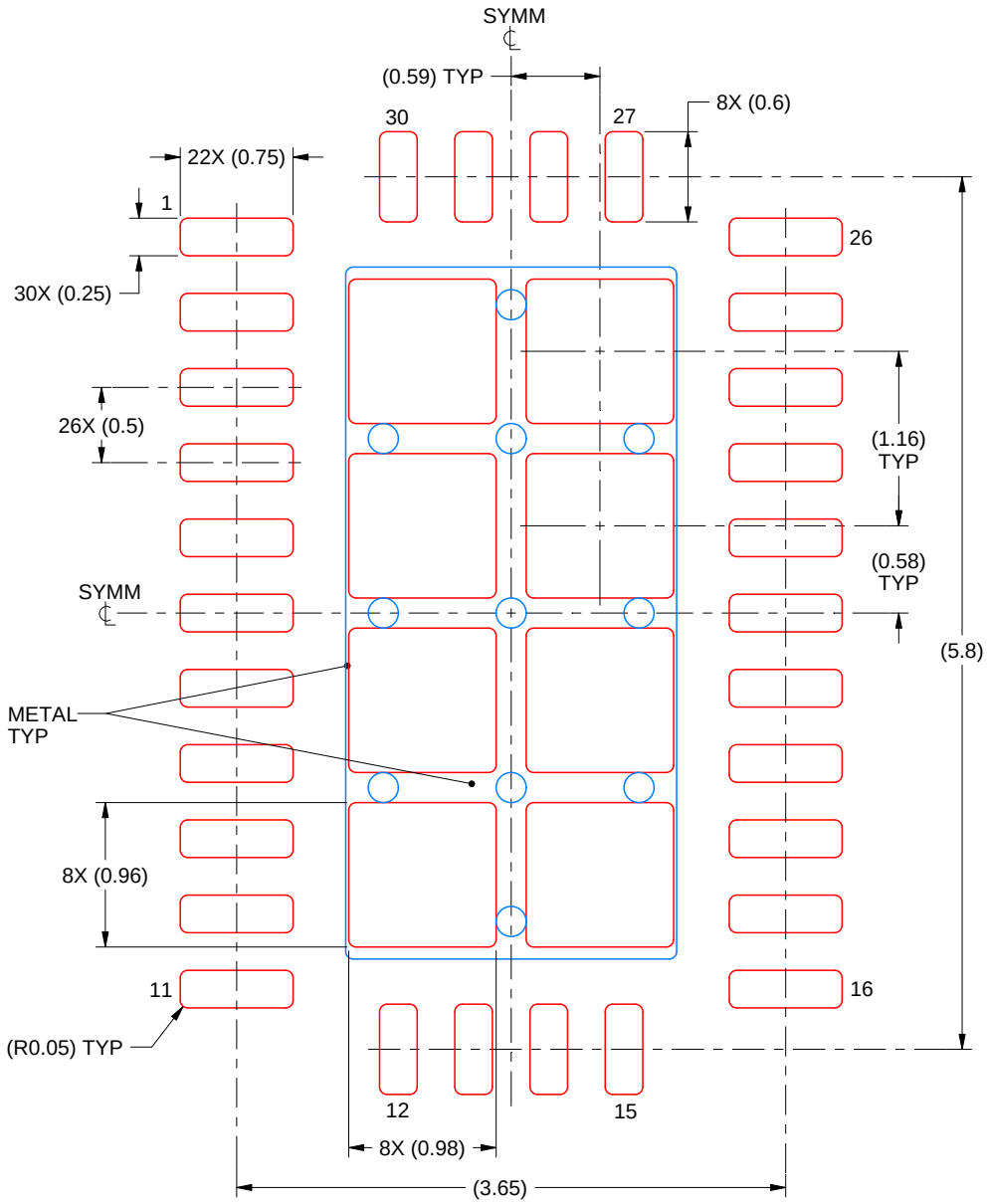



SOLDER MASK DETAILS

4225790/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
74.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225790/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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